Pericom Technology Inc.

Features

- PT8A995 works as encoder and PT8A996 work as decoders
- Supply voltage: 3.0V to 6.4V
- Internal auto-shutdown function
- Internal over-load protection to meet HD271 safety specification (996)
- Integrated RF circuit (995)
- Two analog channels, one for tachospeed and the other for steering
- 32 steps for each of two analog channels
- Fine tuning selection for two analog channels
- Few external components needed
- Closed loop adjustment for servo motor (996)
- Built-in voltage regulator (996)
- Package: 16-pin DIP (995P), 20-pin DIP (996P) and 20-pin SOIC (996S)

Applications

- Remote Controller
- Toys
- Remote Measurement

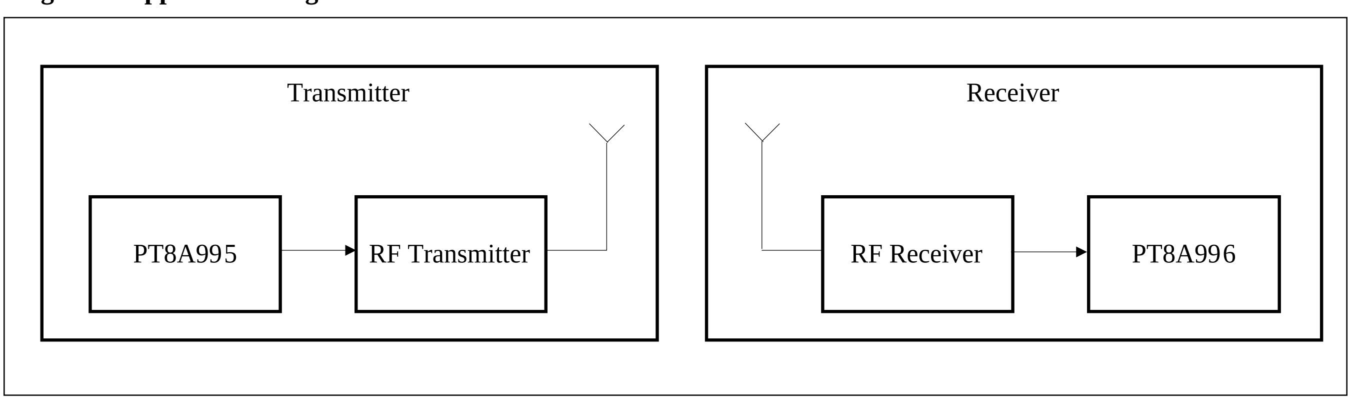
General Description:

The PT8A995 and PT8A996 provide a simple and economic solution for basic Digital Proportional R/C car toys. The chipset uses CMOS LSI Analog and Mixed Signal technology. They provide high quality encoder/decoder circuit.

PT8A995 severs as an encoder. When it is applied in R/C car, the built-in AD converter samples the external tachospeed and steering inputs and converts them into 5-bit digital signals. The internal coder assembles these signals into a multi-frame. It contains header, data and CRC value. To obtain accurate timing easily, Manchester encoding is employed. Some digital modulation scheme can be used, e.g., general ASK, OOK, FSK and QPSK. OOK is easy to implement and low cost.

PT8A996 works as a decoder. Demodulated RF signal will be amplified and filtered in 996 to get baseband signal. DPLL is adopted to generate sampling clock. The decoder logic can extract F/B, L/R and functional bits from received signal. The outputs are pulse-width-modulated. When motors are blocked, the built-in over-load protection mechanism will work to meet Toy Safety Requirement.

Figure 1: Application Diagram



Block Diagram

Figure 2. Block Diagram of PT8A995

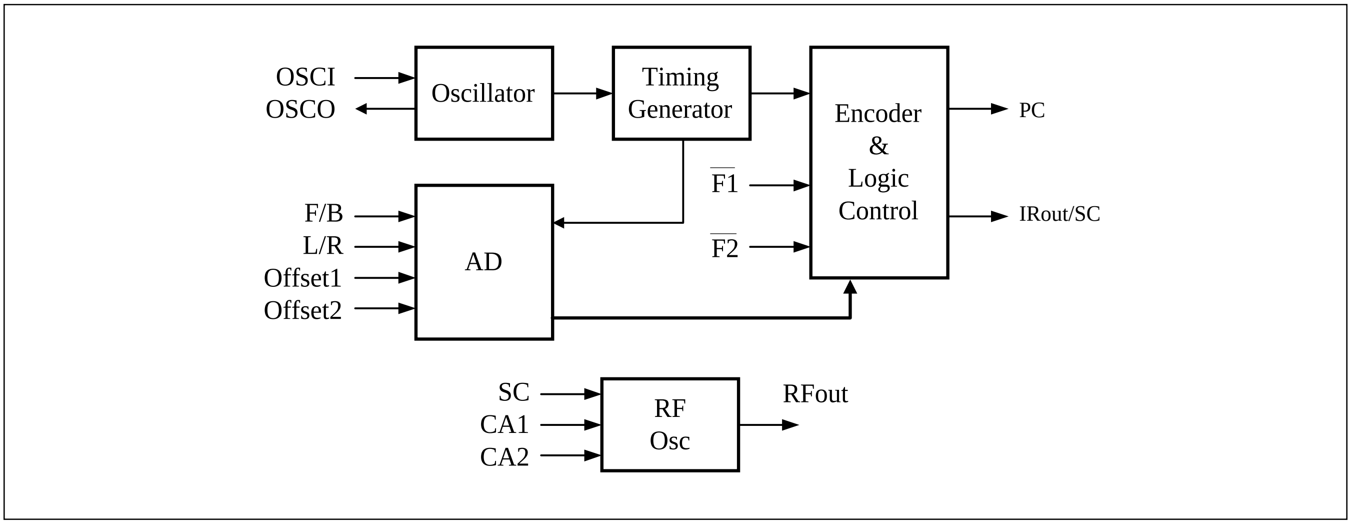
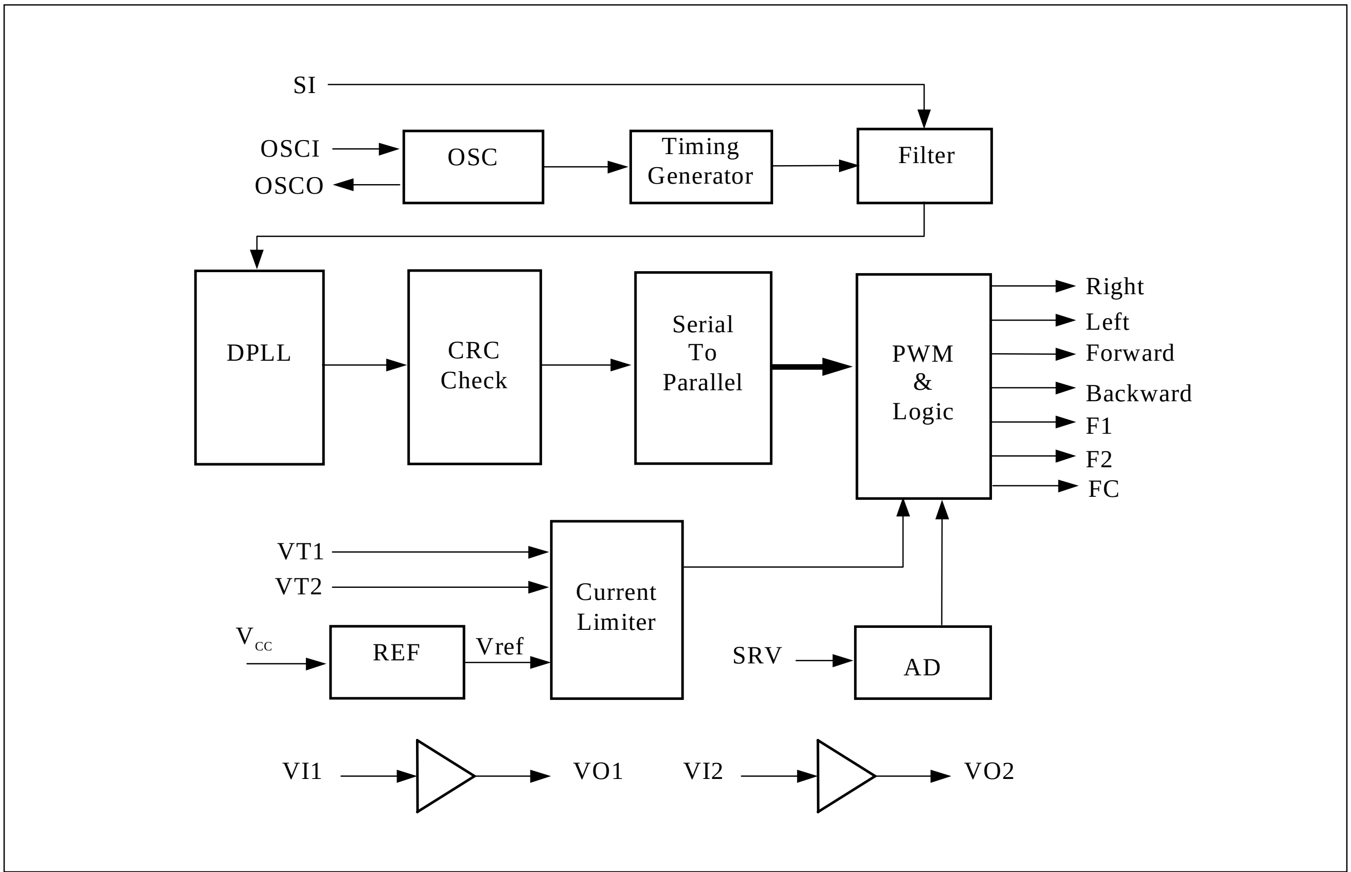
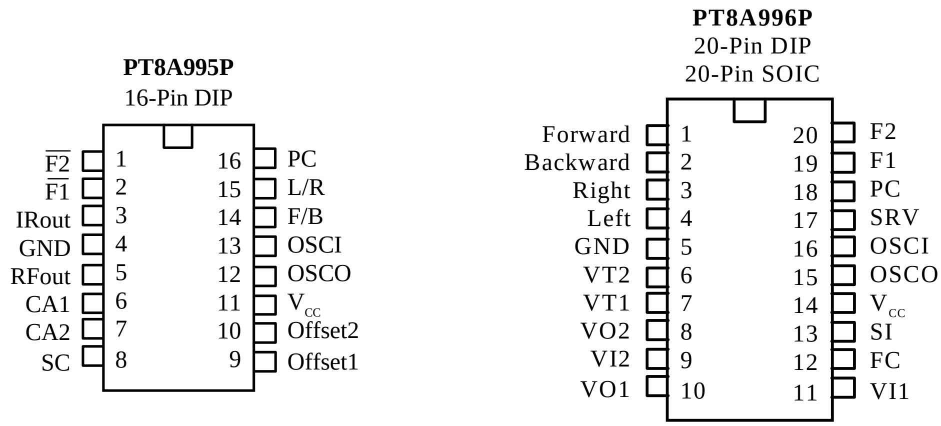


Figure 3. Block Diagram of PT8A996



Pin Configuration



Top View

Pin Description

Table 1. Pin Description of PT8A995

Pin No.	Pin name	Description
1	$\overline{F2}$	F2 function control pin
2	$\overline{F1}$	F1 function control pin
3	IRout	Output code with 38KHz carries
4	GND	Ground
5	RFout	Output code with 27M or 49MHz carries
6	CA1	27M or 49MHz crystal oscillator input
7	CA2	27M or 49MHz crystal oscillator output
8	SC	Output code
9	Offset1	Used for offset adjustment of speed input
10	Offset2	Used for offset adjustment of steering input
11	V_{CC}	power
12	OSCO	Crystal oscillator output
13	OSCI	Crystal oscillator input
14	F/B	Input for forward & backward speed
15	L/R	Input for steering angle left & right
16	PC	Power control output

Table 2. Pin Description of PT8A996

Pin No.	Pin Name	Description
1	Forward	Forward output
2	Backward	Backward output
3	Right	Right output
4	Left	Left output
5	GND	GND
6	VT2	F/B motor current limit protection input
7	VT1	L/R motor current limit protection input
8	VO2	The second stage amplify output
9	VI2	The second stage amplify input
10	VO1	The first stage amplify output
11	VI1	The first stage amplify input
12	FC	Futaba connection output
13	SI	Encode signal input
14	V_{CC}	Power
15	OSCO	Crystal oscillator output
16	OSCI	Crystal oscillator input
17	SRV	Servo motor feedback input
18	PC	Auto power off control
19	F1	Function1 control
20	F2	Function2 control

Functional Description

Functional Description of PT8A995

Oscillator Circuit

A fundamental crystal or ceramic resonator can be used as oscillator resonator. The central frequency is 455kHz. The frequency tolerance can be up to 1.5%.

Internal A/D Converter

5-bit A/D converter is built-in. It has four input channels. To get stable analog input, the level should be within 3/8 V_{CC} to 5/8 V_{CC}. The four channels are switched in turn. Refer to Fig. 3. When a 455kHz quartz is used, CLK is 1.18kHz. F/B and L/R are converted into 5-bit. OffsetX is converted into 3-bit. No external load capacitor is needed.

The analog input voltage and the corresponding digitalized values are shown in Figure 5.

When the chipset is applied in R/C car, there are gross tuning joysticks and fine tuning joysticks for SPEED and STEERING respectively. We denote them SPEEDO, speedo, STEERINGO, steeringo, corresponding to F/B, Offset1, L/R, Offset2 respectively. Offset1 and offset2 complement F/B and L/R offset respectively.

If current conversion values are Vsp, Vspo, Vst, Vsto, corresponding to SPEEDO, speedo, STEERINGO, steeringo respectively, we can describe the SPEED value to be transmitted as

$$Vspeed = Vsp + Vspo.$$

The STEERING value is

$$Vsteering = Vst + Vsto.$$

Encoder

Each time the transmitter is active, the chip will assemble SPEED value and STEERING value into a multi-frame as shown in Figure 6. The multi-frame has two sub-frames, denoted as odd frame and even frame.

After data are assembled, the bit stream is Manchester encoded. It is illustrated in Figure 7. A rising edge denotes 1, and a falling edge denotes 0.

The maximum encoding delay can be calculated by using following formula

$$Tmax = (48+5) * T_{clock} = 53/1.18kHz = 45 \text{ (ms)}$$

RF Circuit

RF circuit is integrated for easy application. A fundamental crystal or third-tune crystal is required. The RF frequency can be 27MHz or 49MHz. On-Off-Keying (OOK) scheme is adopted for low cost and easy implementation.

Auto-Shutdown Function

Auto-shutdown function is adopted to lower power consumption. Once input signal (joysticks, or F1 and F2) are silent for at least 5 minutes, the chip will enter Shutdown Operation mode, during which most circuits, including RF, are powered down. The chip will exit Shutdown Operation mode and enter Normal Operation mode when F1 and F2 are active again. For power dissipation, refer to Table 3.

When the chip enters Shutdown Operation mode, PC will output LOW level, which will switch off external circuit. If it operates normally, PC maintains HIGH level. If PC is forced to HIGH level, the chip will not be auto-shut down forever.

Figure 4. Internal A/D Converter of PT8A995

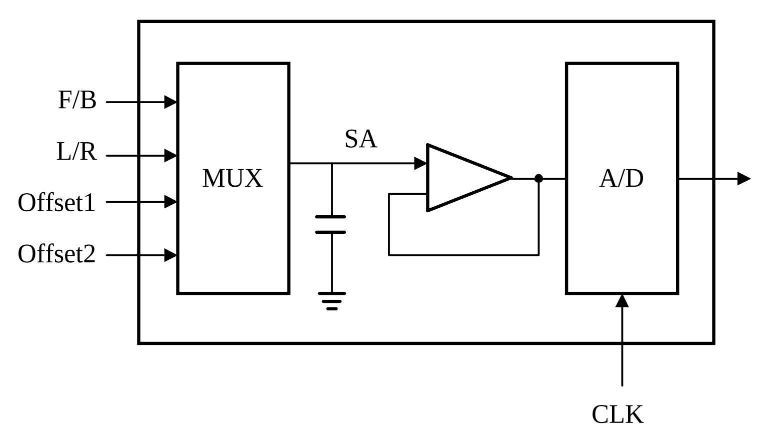


Figure 5. Analog Voltage and Digitalized Values

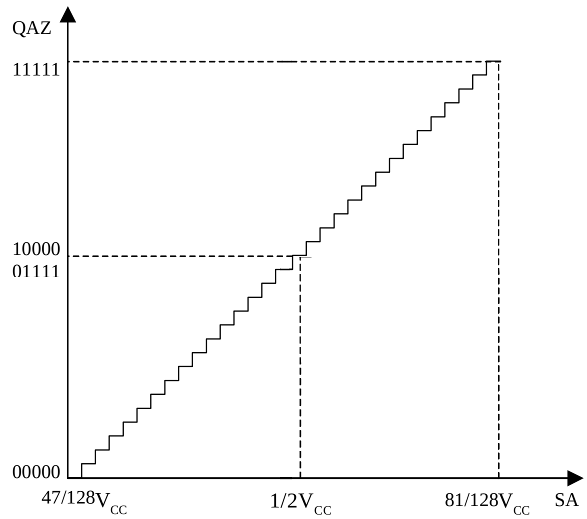


Figure 6. Multi-Frame Structure

Odd Frame (4)

0 1 1 1 1 1 1 0	1 1 1	FB4	FB3	0	FB2-FB0	F1	F3	0	CRC

Even Frame (4)

0 1 1 1 1 1 1 0	0 0 0	RL4	RL3	0	RL2-RL0	F1	F3	0	CRC

FB4-FB0: F/B values
RL4-RL0: R/L values
F4-F1: function value
F4/F3 are reserved

Figure 7. Manchester Modulation scheme

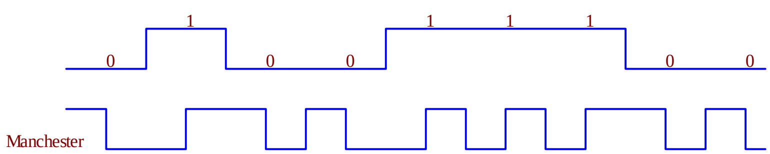


Table 3

Mode	Maximum Supply Drain Current (I_{CC})	Power Dissipation (P_d)
Normal Operation	20 mA	100 mW
Shutdown Operation	20 uA	100 uW

Functional Description of PT8A996

When a baseband signal is applied to VI1 pin, it will be amplified and then filtered by the FILTER and sent to digital phase-lock-loop (DPLL).

Once the loop is locked into input signal, HEADER in multi-frame structure is detected. Data in bit stream are converted into parallel output by Serial-to-Parallel module. If no CRC error is found, the data are valid. At final step, FB and RL will be pulse-width-modulated.

An internal A/D converter is required to make servo motor work well. The inputs are SRV and Offset.

When an R/C car is out of control, over-load protection is provided by Current Limiter. If the R/C car is blocked by some barriers, Forward and Backward are disabled. If servo motor encounters troublesome, Left and Right are disabled.

Timing Generator

Timing Generator produces frequency signals of 151kHz and 37.8kHzfrom a 455kHz master clock.

Internal Amplifier

The baseband signal is amplified in two stages. An active band-pass filter is applied externally. It can be achieved by RC filter.

DPLL

A digital PLL is built in PT8A996 to ensures 1.5 percent carrier frequency tolerance. 151kHz is used as local high frequency.

PWM Modulation Scheme

The outputs of PT8A996 are pulse-width modulated for proportional output. The duty-ratio of output is variable and adjusted by input on transmitter side. The average level is proportional to analog input.

The pulse frequency is 37.8KHz. Duty ratio ranges from 1/64 to 1. The F/B controller works as a proportional adjuster with 32 steps. The L/R controller is made up of position control loop and speed control loop to ensure high accuracy and speed.

Internal A/D Converter

5-bit A/D converter is built-in. It has two input channels. To get stable analog input, the level should be within 3/8 V_{CC} to 5/8 V_{CC}. The scale is linear. A time-division multiplexing method is used as a simple way to switch between two channels in PT8A996. When a 455kHz quartz is used, CLK is 1.18KHz. SRV is converted into 5-bit. Offset is converted into 3-bit to complement L/R offset (Offset2 on transmitter).

If current conversion values are Vsv and Vfd with regarding to SRV and Offset respectively, we can describe the servo FEEDBACK value to be transmitted as

Vsrv = Vsv + Vfd.

Servo Feedback System

For more accurate motor position, servo feedback is necessary.

Overload Protection Function

Over-load protection function is shown in Figure 9. Once VT keeps effective more than Te and ineffective less than Tm, the chip enters over-load protection mode. It will disable all output. The device will exit over-load protection mode when VT is not effective more than 200ms.

Futaba compatible connection

The PT8A996 has a FC pin, whose output signal can directly control Futaba's servo-motor or other compatible servo-motor. The signal is illustrated in Figure 10.

Figure 9. Over-Load Protection Function

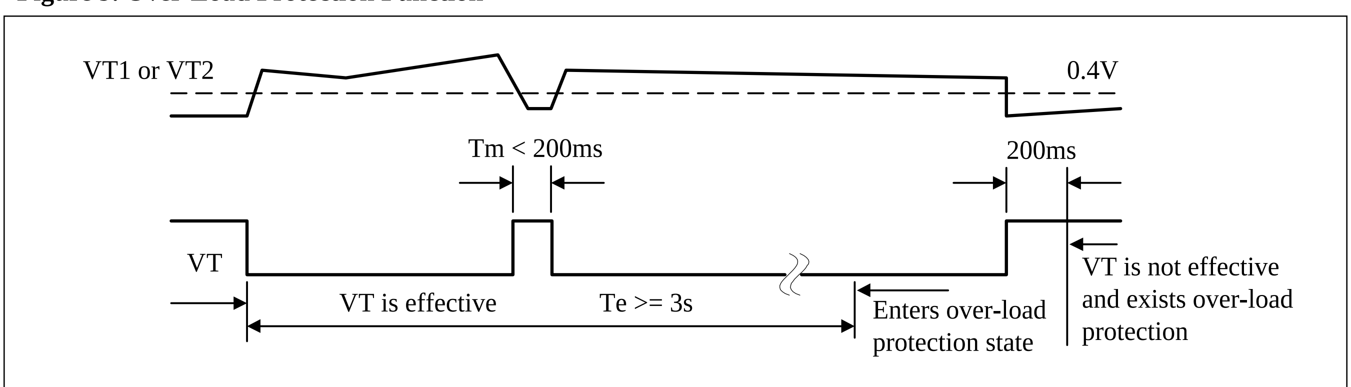
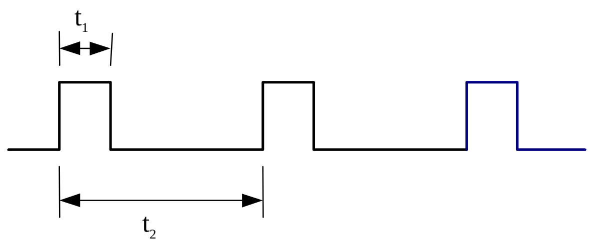
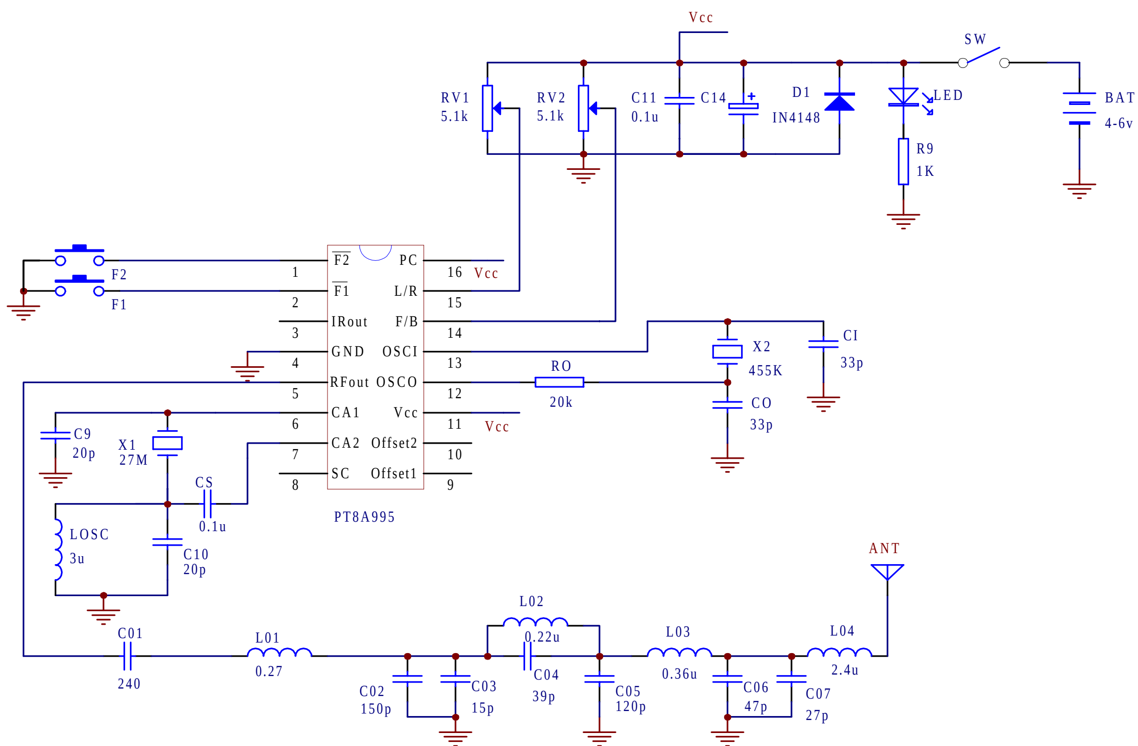


Figure 10. Output from FC Pin



t_1 =0.85ms~1.66ms (Pulsewidth Adjustment Step = 27us)
t_2 =13.5ms

Figure 11. Application of PT8A995 with Internal Modulation



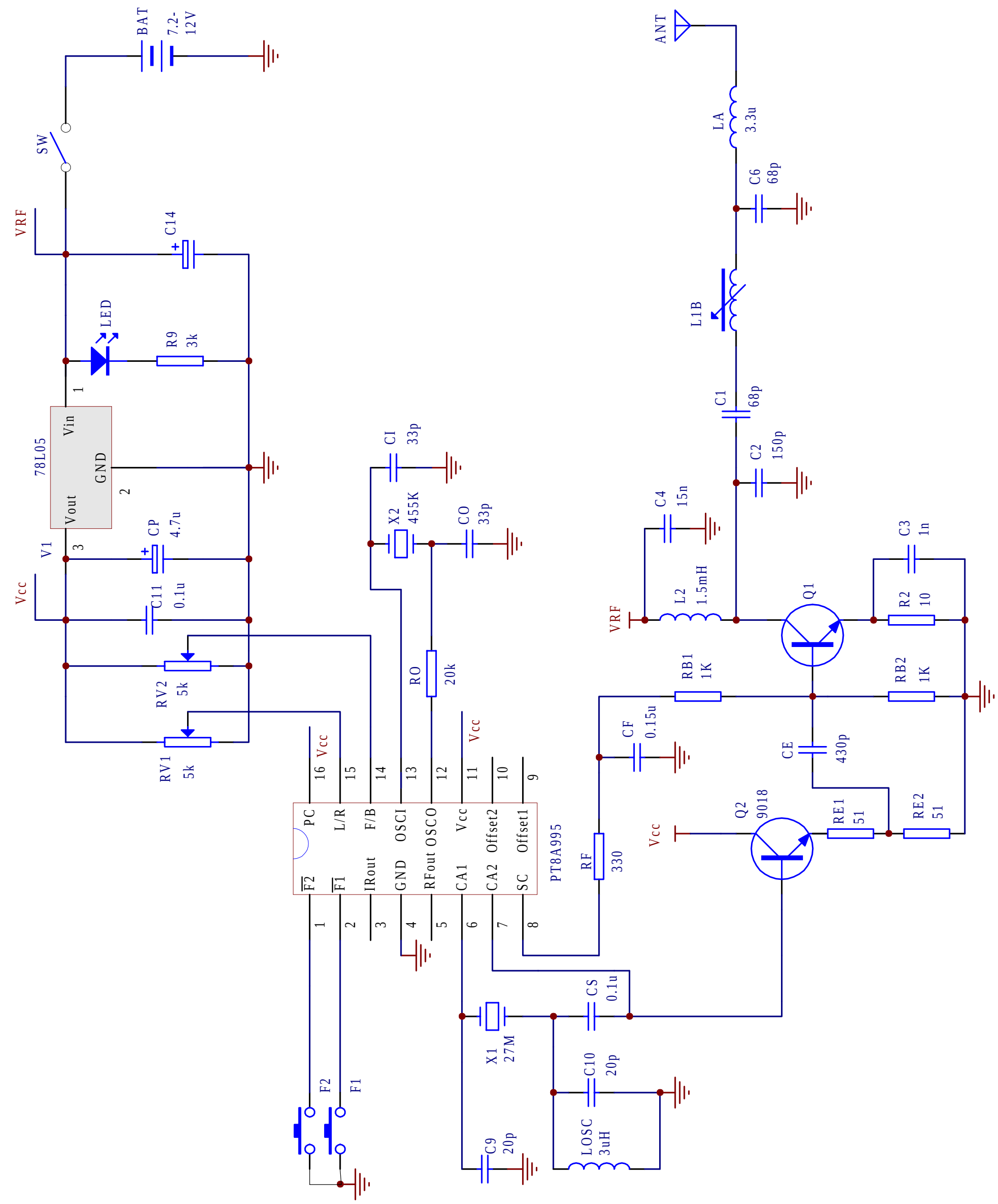


Figure 12. Application of PT8A995 with External Modulation

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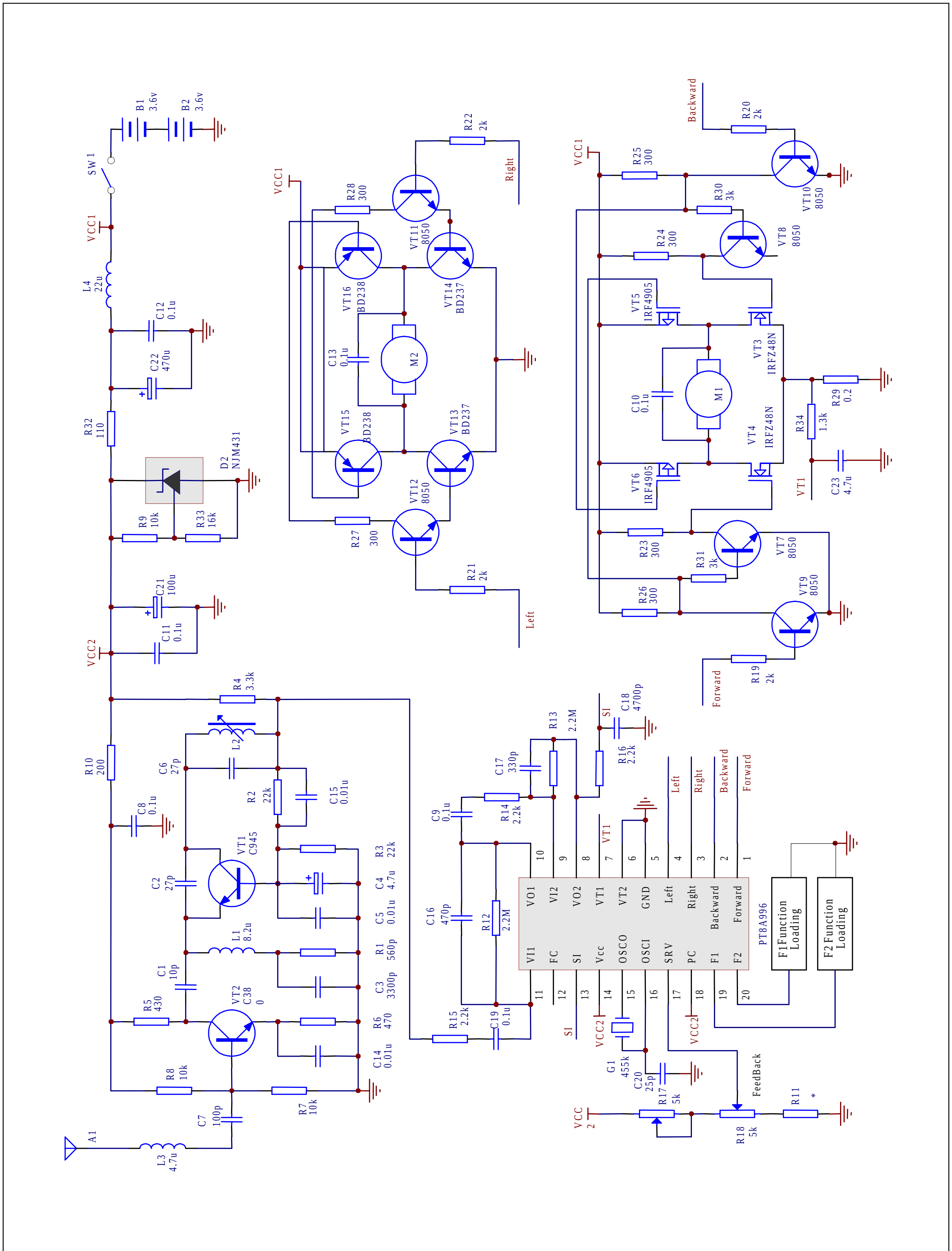


Figure 13. Supper-Regeneration Application Circuit of PT8A996

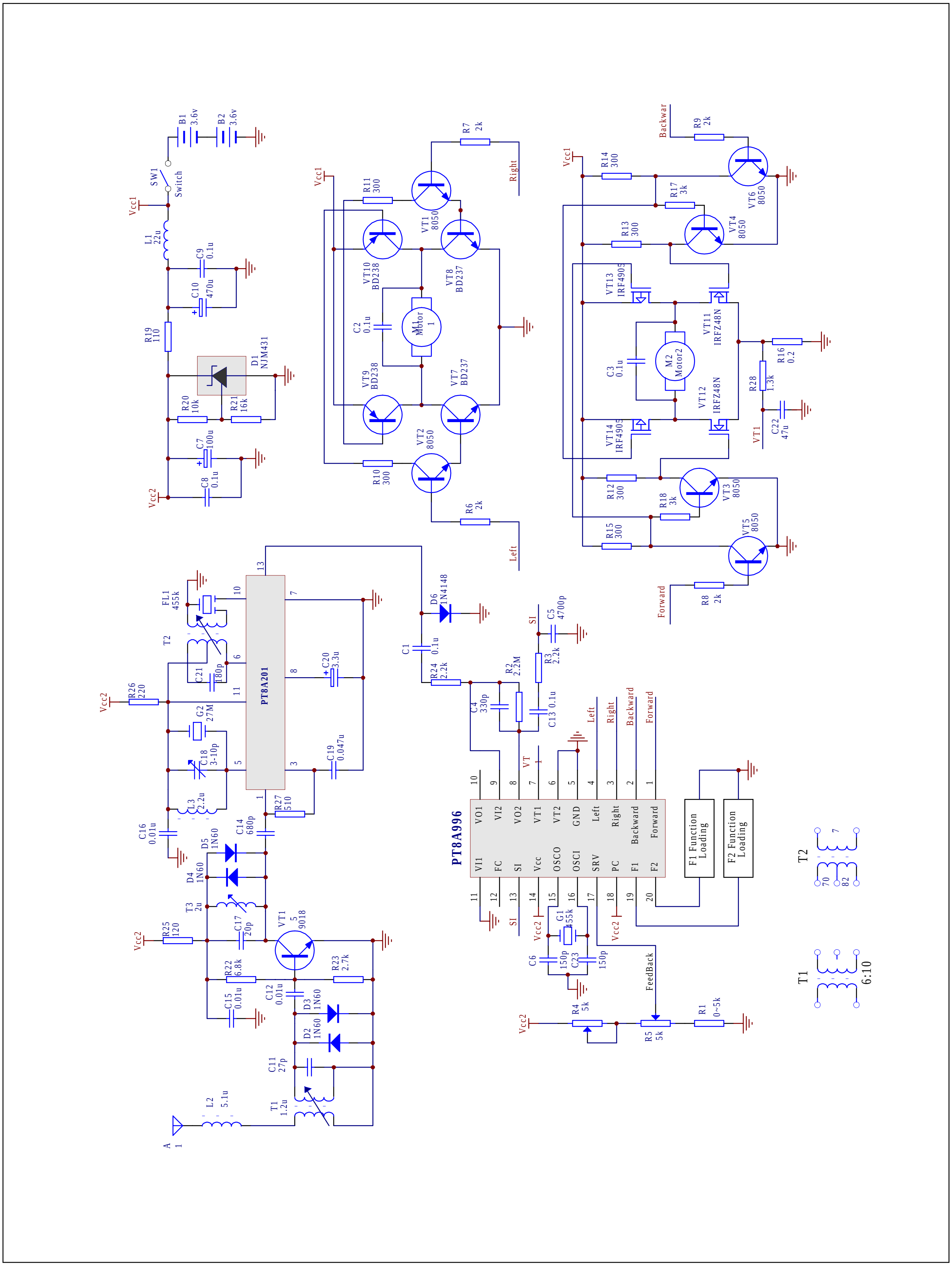


Figure 14. Supper-Heterodyne Application Circuit of PT8A996

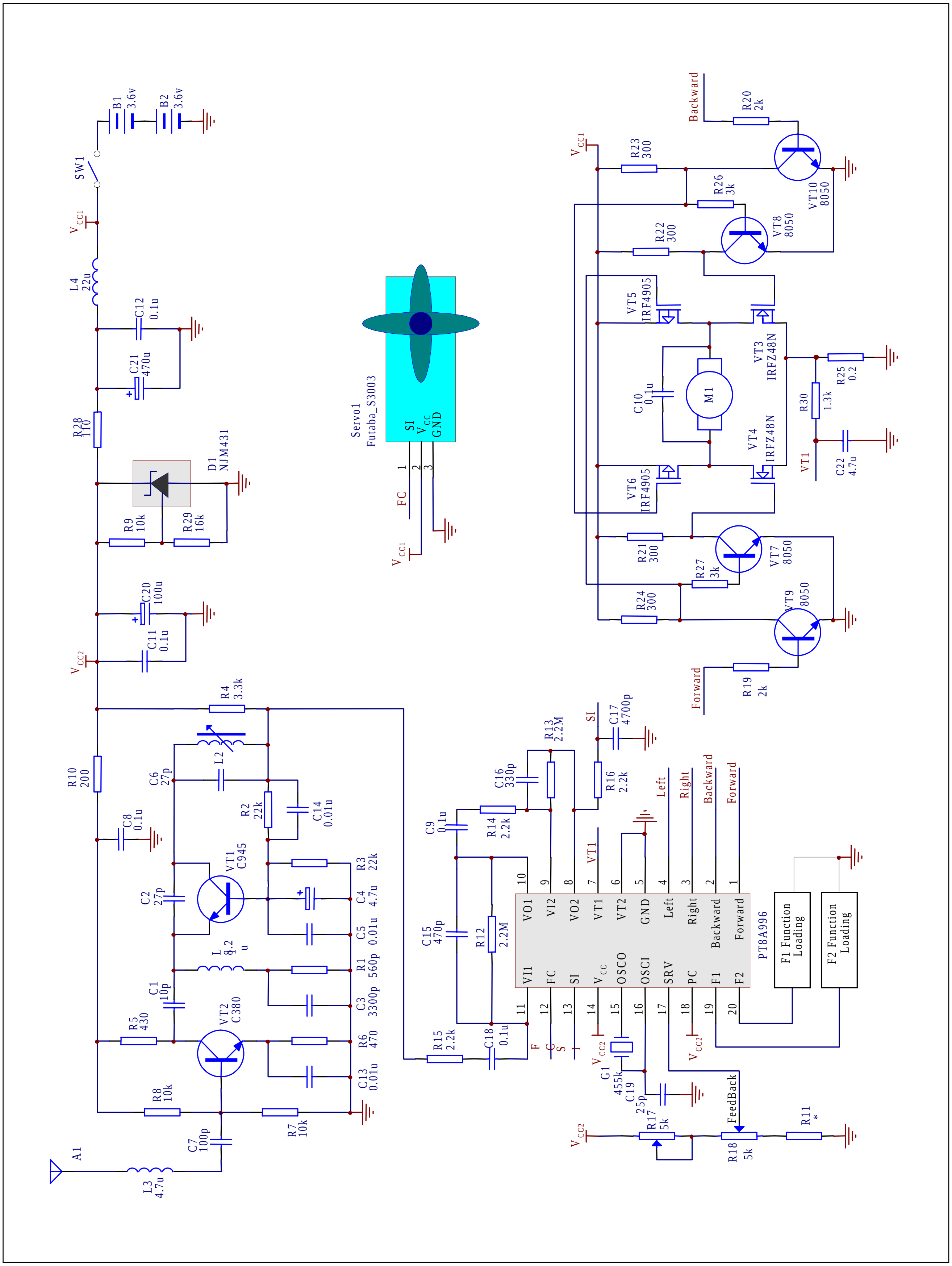
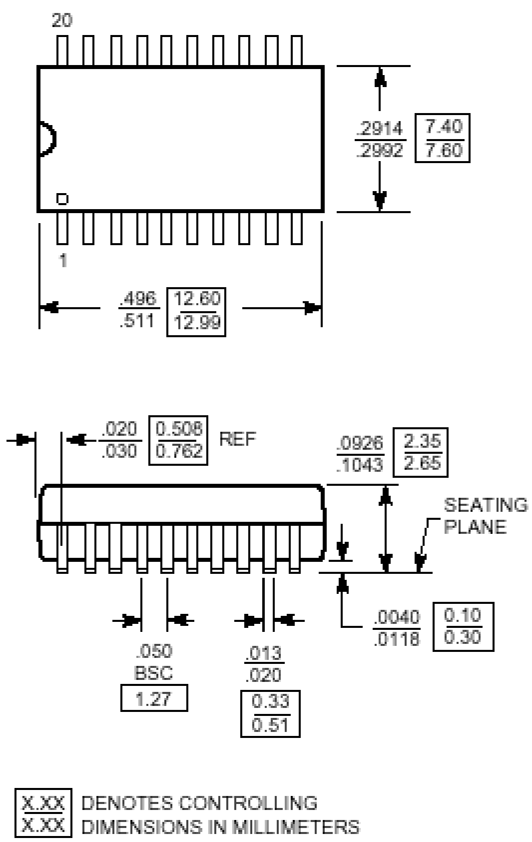


Figure 15. Futaba-S3003 Servo Application Circuit of PT8A996

Figure 16. Mechanical Diagram of 20-pin SOIC



Notes

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