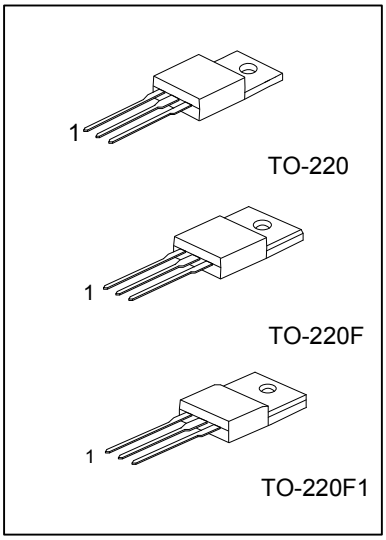
4.0 Amps, 800 Volts
N-CHANNEL POWER MOSFET



■ DESCRIPTION

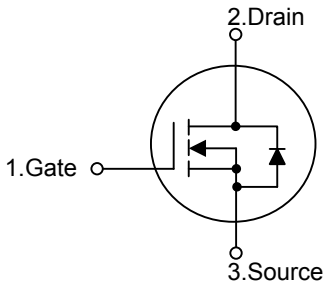
The UTC **4N80** is a N-channel mode Power FET. It uses UTC's advanced technology to provide costomers planar stripe and DMOS technology. This technology is specialized in allowing a minimum on-state resistance, and superior switching performance. It also can withstand high energy pulse in the avalanche and commutation mode.

The UTC **4N80** is universally applied in high efficiency switch mode power supply.

■ FEATURES

* 4.0A, 800V, $R_{DS(on)}$=3.6Ω @V_{GS} =10V
* High switching speed
* Improved dv/dt capability
* 100% avalanche tested

■ SYMBOL



■ ORDERING INFORMATION

Ordering Number		Package	Pin Assignment			Packing
Lead Free	Halogen Free		1	2	3	
4N80L-TA3-T	4N80G-TA3-T	TO-220	G	D	S	Tube
4N80L-TF3- T	4N80G-TF3- T	TO-220F	G	D	S	Tube
4N80L-TF1- T	4N80G-TF1- T	TO-220F1	G	D	S	Tube

Note: Pin Assignment: G: Gate D: Drain S: Source

4N80L - TA3 - T

(1) Packing Type	(1) T: Tube
(2) Package Type	(2) TA3: TO-220, TF3: TO-220F, TF1: TO-220F1
(3) Lead Free	(3) G: Halogen Free, L: Lead Free

■ ABSOLUTE MAXIMUM RATINGS (T_C=25°C, unless otherwise specified)

PARAMETER		SYMBOL	RATINGS	UNIT
Drain-Source Voltage		V_{DSS}	800	V
Gate-Source Voltage		V_{GSS}	±30	V
Drain Current	Continuous	I_D	4.0	A
	Pulsed (Note 1)	I_{DM}	15.6	A
Avalanche Energy	Single Pulsed (Note 2)	E_{AS}	460	mJ
	Repetitive (Note 1)	E_{AR}	13	mJ
Peak Diode Recovery dv/dt (Note 3)		dv/dt	4.0	V/ns
Power Dissipation	TO-220	P_D	106	W
	TO-220F/TO-220F1		36	W
Junction Temperature		T_J	+150	°C
Storage Temperature		T_{STG}	-55~+150	°C

Note: Absolute maximum ratings are those values beyond which the device could be permanently damaged. Absolute maximum ratings are stress ratings only and functional device operation is not implied.

■ THERMAL DATA

PARAMETER		SYMBOL	RATINGS	UNIT
Junction to Ambient	TO-220	θ_{JA}	62.5	°C/W
	TO-220F/TO-220F1		62.5	°C/W
Junction to Case	TO-220	θ_{JC}	1.18	°C/W
	TO-220F/TO-220F1		3.47	°C/W

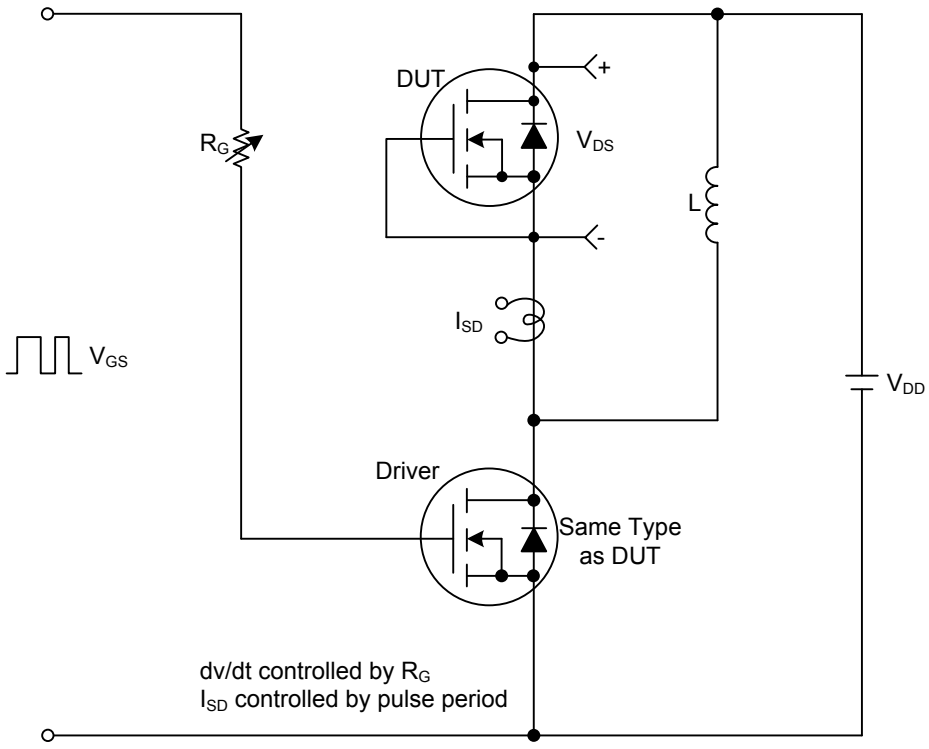
■ ELECTRICAL CHARACTERISTICS (T_C=25°C, unless otherwise specified)

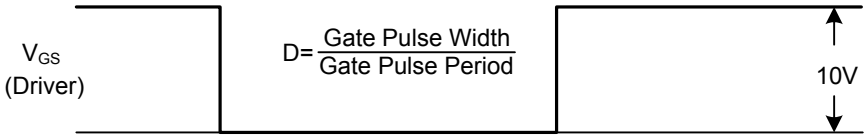
PARAMETER		SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
OFF CHARACTERISTICS							
Drain-Source Breakdown Voltage		BV_{DSS}	V_{GS}=0V, I_D=250μA	800			V
Breakdown Voltage Temperature Coefficient		$\Delta BV_{DSS}/\Delta T_J$	I_D=250μA, Referenced to 25°C		0.95		V/°C
Drain-Source Leakage Current		I_{DSS}	V_{DS}=800V, V_{GS}=0V			10	μA
			V_{DS}=640V, T_C=125°C			100	μA
Gate-Source Leakage Current	Forward	I_{GSS}	V_{DS}=0V ,V_{GS}=30V			100	nA
	Reverse		V_{DS}=0V ,V_{GS}=-30V			-100	nA
ON CHARACTERISTICS							
Gate Threshold Voltage		$V_{GS(TH)}$	V_{DS}=V_{GS}, I_D=250μA	3.0		5.0	V
Drain-Source On-State Resistance		$R_{DS(ON)}$	V_{GS}=10V, I_D=2A		2	3.6	Ω
Forward Transconductance		g_{FS}	V_{DS}=50V, I_D=2A (Note 4)		3.8		S
DYNAMIC PARAMETERS							
Input Capacitance		C_{ISS}	V_{DS}=25V,V_{GS}=0V,f=1.0MHz		680	880	pF
Output Capacitance		C_{OSS}			75	100	pF
Reverse Transfer Capacitance		C_{RSS}			8.6	12	pF
SWITCHING PARAMETERS							
Total Gate Charge		Q_G	V_{DS}=640V, V_{GS}=10V, I_D=4A (Note 4,5)		19	25	nC
Gate-Source Charge		Q_{GS}			4.2		nC
Gate-Drain Charge		Q_{GD}			9.1		nC
Turn-ON Delay Time		$t_{D(ON)}$	V_{DD}=400V, I_D=4A, R_G=25Ω (Note 4,5)		16	40	ns
Turn-ON Rise Time		t_R			45	100	ns
Turn-OFF Delay Time		$t_{D(OFF)}$			35	80	ns
Turn-OFF Fall Time		t_F			35	80	ns
SOURCE- DRAIN DIODE RATINGS AND CHARACTERISTICS							
Maximum Body-Diode Continuous Current		I_S				3.9	A
Maximum Body-Diode Pulsed Current		I_{SM}				15.6	A
Drain-Source Diode Forward Voltage		V_{SD}	I_S =4A, V_{GS}=0V			1.4	V
Body Diode Reverse Recovery Time		t_{RR}	V_{GS}=0V, I_S=4A, dI_F/dt=100A/μs (Note 4)		575		ns
Body Diode Reverse Recovery Charge		Q_{RR}			3.65		μC

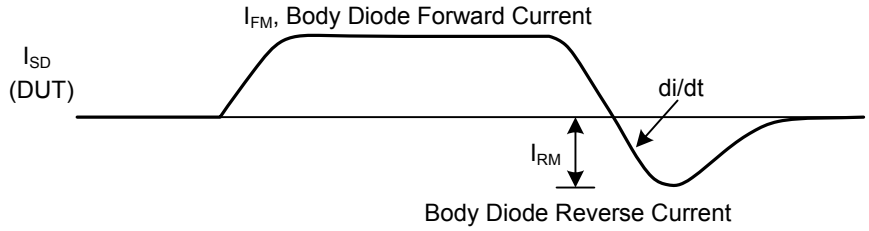
Note: 1. Repetitive Rating: Pulse width limited by maximum junction temperature
2. L=57mH, I_{AS}=4A, V_{DD}= 50V, R_G=25Ω, Starting T_J=25°C
3. I_{SD} ≤4A, di/dt ≤200A/μs, V_{DD} ≤BV_{DSS}, Starting T_J=25°C
4. Pulse Test: Pulse width ≤ 300μs, Duty cycle ≤ 2%
5. Essentially independent of operating temperature

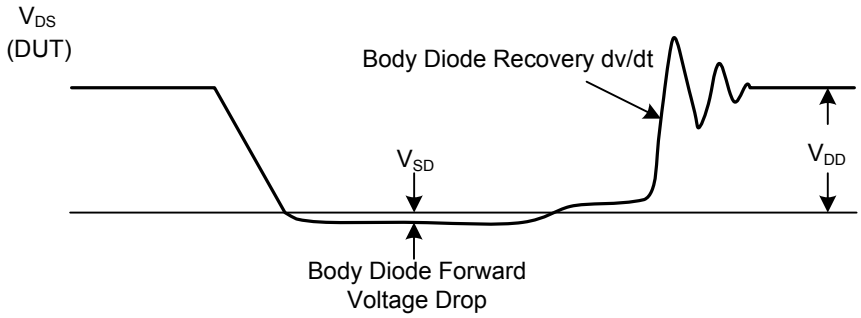
■ TEST CIRCUITS AND WAVEFORMS

Peak Diode Recovery dv/dt Test Circuit & Waveforms

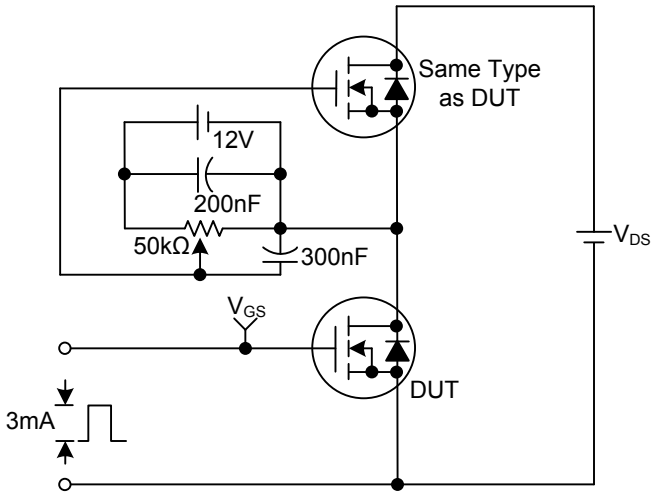




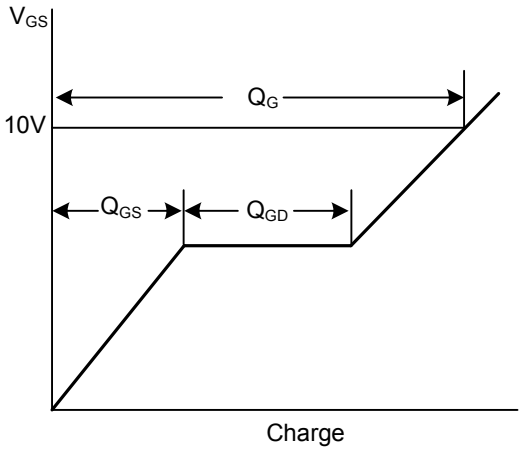




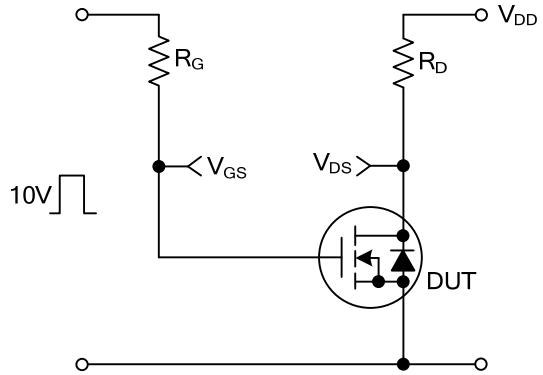
Gate Charge Test Circuit



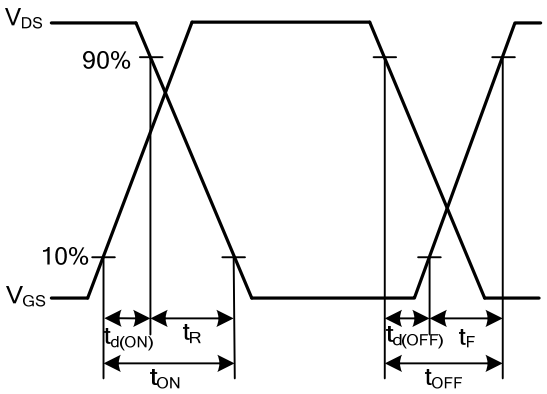
Gate Charge Waveforms



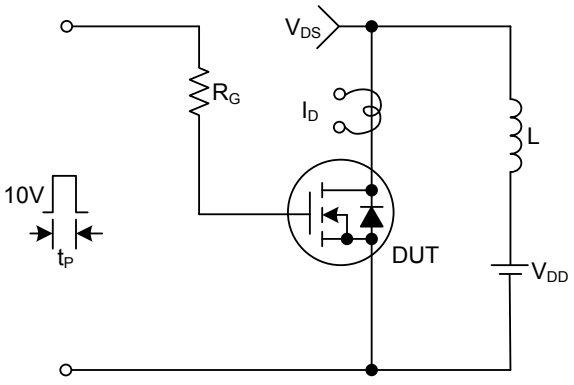
Resistive Switching Test Circuit



Resistive Switching Waveforms



Unclamped Inductive Switching Test Circuit



Unclamped Inductive Switching Waveforms

$$E_{AS}=\frac{1}{2}LI_{AS}^{2}\frac{BV_{DSS}}{BV_{DSS}-V_{DD}}$$