ANALOGIC.■

AM40016/ AM40116

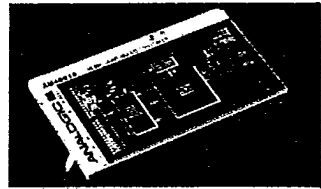**High Performance
500 kHz 16-Bit
Sampling A/D Converters**

Performance Features

The AM40016/AM40116 is a 16-bit, 500 kHz analog-to-digital converter with a built-in sample-and-hold (S/H) amplifier. With its 500 kHz sampling rate, the AM40016/AM40116 can digitize several multiplexed channels, such as in an automatic testing application. This high performance sampling A/D converter provides the user with wide flexibility; it is available in unipolar 0-10V (AM40016) or bipolar ±10V (AM40116), and module or Eurocard (the AB40416 and AB40516 are the corresponding Eurocard part numbers). Pin-for-pin compatible with Analogic's ADAM826-1, the AM40016/AM40116 can be used to upgrade existing designs to 500 kHz performance. This A/D converter is ideally suited for both single input channel or multiplexed signal sources; it is, therefore, an excellent choice for Automatic Test Equipment, and a host of other applications requiring 16-bit resolution and a 500 kHz conversion rate.

Superior performance and ease of use make the AM40016/AM40116 the ideal solution for those applications requiring a sample-and-hold amplifier directly at the input to the A/D converter. Having the S/H

amplifier integrated with the A/D converter benefits the system designer in two critical ways. First, the S/H has been designed specifically to complement the performance of the A/D converter; for example, the acquisition time, hold mode settling and droop rate have been optimized for the A/D converter, resulting in exceptional overall performance. Second, the designer achieves true 16-bit system performance, avoiding degradation due to ground loops, signal coupling and digital noise introduced when separate S/H and A/D converters are interconnected. Furthermore, the accuracy, speed, and quality of the AM40016/AM40116 are fully ensured by thorough, computer-controlled factory tests of each unit.

T-51-10-16

Features

■ 16-bit Resolution
■ 500 kHz Sampling Rate
■ High Input Impedance: $10^8\Omega$
■ Pin-for-Pin Compatible with ADAM826-1
■ Standard Eurocard Option
■ Ease of Use
■ Built-in S/H Amplifier
■ No Missing Codes
■ Differential Linearity: ±0.75 LSB
■ Integral Linearity ±0.003%
■ Binary, Offset Binary, or Two's Complement Coding Formats
■ Electromagnetic/Electrostatic Shielding

Applications

■ Automatic Test Equipment
■ Analytic Instrumentation
■ Data Acquisition Systems
■ Spectroscopy
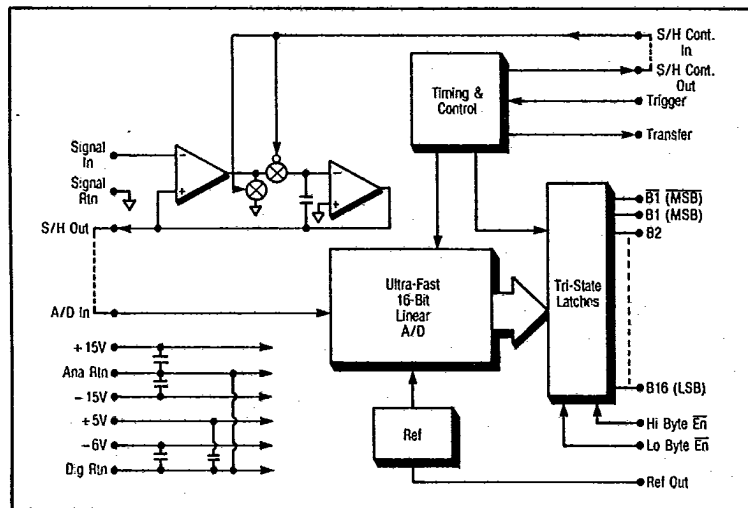■ Seismic Instrumentation
■ High Resolution Imaging

SAMPLING ANALOG-TO-DIGITAL CONVERTERS

Figure 1. AM40016/AM40116 Block Diagram.

SPECIFICATIONS(1)

ANALOG INPUT

Input Range
0V to + 10V (AM40016/AB40416)
± 10V (AM40116/AB40516)

Input Bias Current
50 nA Max.

Input Capacitance
10 pF Max.

Input Impedance
100 MΩ

DIGITAL INPUTS

Logic Levels
Trigger
Logic "0"
1.5V Max.
Logic "1"
3.5V Min.
Loading
1 HCMOS Load
Pulse Width
100 ns Min., 200 ns Max.
S/H Control
Logic "0" (Sample)
− 0.5V Min., 1.6V Max.
Logic "1" (Hold)
3.8V Min., 5.5V Max.
Loading
1 HCMOS Load
High & Low Byte Enables
Logic "0" (Enable)
1.5V Max.
Logic "1" (Disable)
3.5V Min.
Loading
1 CMOS Load

DIGITAL OUTPUTS

Fan-Out
1 LSTTL Load Max.

Output Coding
Unipolar Binary (AM40016/AB40416)
Offset Binary or
2's Complement (AM40116/AB40516)

Output Voltage
Logic "0"
0.4V Max.
Logic "1"
2.4V Min.

Transfer
Positive edge loads output data latches;
data ready after 50 ns delay

REFERENCE TEST POINT

Output Voltage
+ 10V (200 µA Max. external load)
Accuracy
±0.1%

DYNAMIC CHARACTERISTICS

Maximum Throughput Rate
500 kHz Min.

A/D Conversion Time
1.5 µs

S/H Acquisition
500 ns Max.

S/H Aperture Delay
15 ns Max.

S/H Aperture Jitter
50 ps Max.

S/H Feedthrough (2)
− 100 dB

TRANSFER CHARACTERISTICS

Resolution
16 bits

Quantization Error
± 0.5 LSB Max.

Integral Non-Linearity
± 0.003% FSR Max.

Differential Non-Linearity
± 0.75 LSB Max.

Offset Error (3)
± 5 mV Max.

Gain Error (3)
0.01% FSR

No Missing Codes
Guaranteed from 0ºC to 60ºC

A/D Converter Noise
70 µV rms (AM40016/AB40416)
90 µV rms (AM40116/AB40516)

STABILITY (0ºC to 60ºC)

Differential Non-Linearity
± 1 ppm FSR/ºC Max.

Offset Voltage
± 10 ppm FSR/ºC Max.

Gain
± 5 ppm FSR/ºC Max.

Warm-Up Time
10 minutes Max.

Supply Rejection
Offset
± 25 ppm FSR/%
Gain
± 15 ppm FSR/%

POWER REQUIREMENTS

Supply Range
± 15V Supplies
14.5V Min., 15.5V Max.

+ 5V Supply
+ 4.75V Min., + 5.25V Max.

− 6V Supply
− 5.75 Min., − 6.25V Max.

T-51-10-16

+15V Current Drain
85 mA Typ.

−15V Current Drain
95 mA Typ.

+5V Current Drain
65 mA Typ.

−6V Current Drain
140 mA Typ.

Power Consumption
4W Max.

ENVIRONMENTAL & MECHANICAL

Temperature Range
Rated Performance
0°C to 60°C

Storage
−25°C to 85°C

Relative Humidity
0 to 85% Non-condensing up to 40°C

Dimensions
3" x 5" x 0.44"
(76.2 x 127.0 x 11.18 mm)

Shielding
Electromagnetic 5 sides
Electrostatic 6 sides

Case Potential
Ground

Notes

1. Unless otherwise noted, all specifications apply at 25°C.
   Supplies are ±15V, +5V, −6V. Full-scale range is 0 to +10V for the AM40016/AB40416; full scale range is ±10V for the AM40116/AB40516.
2. Tested with full scale 250 kHz signal.
3. Adjustable to zero. Refer to "Output Coding and Trim Procedure" for field adjustable gain and offset procedures.

Coding and Trim Procedure

Figure 2 shows the output coding of the AM40016/AM40116 A/D Converter. The coding format for the AM40016/AB40416 is unipolar binary. For the AM40116/AB40516, the standard coding format is offset binary; the user can convert this coding to two's complement simply by using the available $\overline{B1}$ (MSB) instead of B1 (MSB).

To trim the offset of the AM40016/AB40416, apply 76 µV to the analog input. Adjust the offset trim potentiometer such that the 15 MSBs are "0" and the LSB alternates equally between "0" and "1". To trim the offset of the AM40116/AB40516, apply −153 µV to the analog input and adjust the offset trim potentiometer such that each of the sixteen bits alternates equally between "0" and "1".

To trim the gain of the AM40016/AB40416, apply +9.999771V to the analog input and adjust the gain trim potentiometer such that the 15 MSBs are "1" and the LSB alternates equally between "0" and "1". To trim the gain of the AM40116/AB40516, apply +9.999542V to the analog input and adjust the gain trim potentiometer such that the 15 MSBs are "1" (except $\overline{B1}$ in the case of two's complement) and the LSB alternates equally between "0" and "1".

Timing Considerations

The timing diagram in Figure 3 shows the timing characteristics of the AM40016/AM40116 A/D converter. Upon a high-to-low transition of the Trigger Input, the S/H control output goes high and the internal S/H amplifier enters the Hold mode. The S/H amplifier remains in the Hold mode for the 1.5 µs A/D conversion period. At the end of the 1.5 µs conversion period, the Transfer output goes low and remains low for 175 ns. At the end of this time, Transfer returns high, which loads the data into the tri-state output latches. After a delay of 50 ns from this rising edge, the data is valid.

Layout Considerations

Because of the extremely high resolution of the AM40016/AM40116 A/D converter, it is necessary to pay careful attention to the printed-circuit layout for the device. It is, for example, important to separate the analog and digital grounds and to return them separately to the system power supply. Digital grounds are often noisy or "glitchy", and these glitches can have adverse effects on the performance of the AM40016/AM40116 if they are introduced to the analog portions of the A/D converter's circuitry. At 16-bit resolution, the size of the voltage step between one code transition and the succeeding one is only 153 µV (305 µV for AM40116), so it is evident that any noise in the analog ground return can result in erroneous or missing codes. It is therefore important to configure a low-impedance ground-plane return on the printed-circuit board. Note that the ground-potential metal case used for the AM40016/AM40116 provides shielding against electromagnetic interference on 5 sides and against electrostatic interference on 6 sides.

SAMPLING ANALOG-TO-DIGITAL CONVERTERS

T-51-10-16

Figure 2. Output Coding for the AM40016/AM40116.

Unipolar Binary (AM40016/AB40416)

MSB	LSB	
1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1	=	+9.99985V
0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	=	0.00000V
B1,B2, ...B16	=	Pin Label

Offset Binary (AM40116/AB40516)

MSB	LSB	
1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1	=	+9.99970V
1 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	=	0.0000V
0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	=	−10.0000V
B1,B2, ...B16	=	Pin Label

2's Complement (AM40116/AB40516)

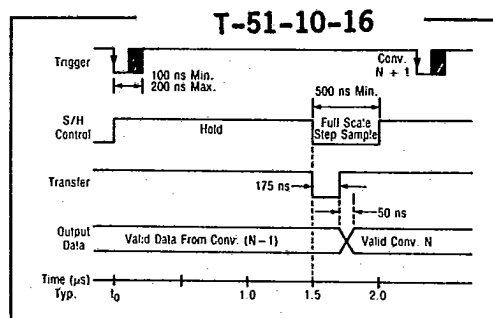| $\overline{MSB}$	LSB	
0 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1	=	+9.99970V
0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	=	0.0000V
1 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	=	−10.0000V
$\overline{B1}$,B2, ...B16	=	Pin Label

Figure 3. AM40016/AM40116 Timing Diagram.

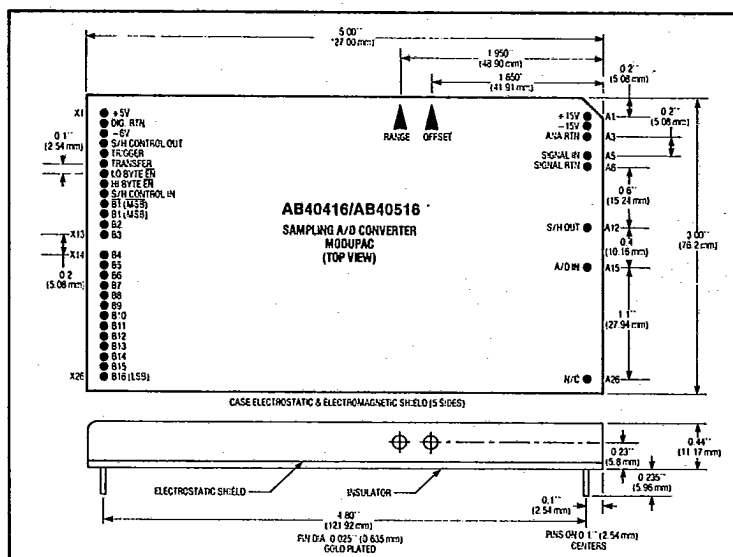### Figure 4. AM40016/AM40116 Outline Drawing and Pinouts.

Principles of Operation

To understand the operating principles of the AM40016/AM40116 A/D converter, refer to Figure 5. The simplified block diagrams in paths a, b, and c in Figure 5 illustrate the three successive passes in the sub-ranging conversion scheme of the AM40016/AM40116. For all three passes, the lines labeled "From S/H" come from the output of the internal sample-and-hold amplifier. In the first pass (a), an operational amplifier attenuates the input signal by a factor of 20, thus converting the 20V full-scale range of the input to the 1V full-scale range of the 6-bit flash A/D converter. The 6-bit A/D converter then digitizes the six MSBs of the input signal. The outputs of the A/D converter, via latches in a specialized gate array, drive the six MSBs of the 16-bit D/A converter.

In the second pass (b), a difference amplifier subtracts the D/A converter's output voltage from the input voltage then amplifies this difference by a factor of 1.6. The ±2.5 mA output range of the D/A converter, working

into the 4 kΩ resistor, matches the 20V full scale range of the input voltage. The output of the difference amplifier provides the input signal for the 6-bit flash A/D converter. The A/D converter's outputs are latched into the gate array, which supplies the next five lower-order bits of the D/A converter. The gain factor in this second pass is such that the difference signal cannot exceed half-scale in the 6-bit A/D converter. The resolution of the A/D conversion in the second pass is thus five bits (not six).

In the third pass (c), the gain-of-1.6 difference amplifier again subtracts the D/A converter's output voltage from the input voltage. In this pass, an amplifier with a gain of 32 provides additional amplification of the difference signal. The outputs of the flash A/D converter are latched into the gate array, which drives the five remaining LSBs of the 16-bit D/A converter. The effective resolution of the conversion is thus $6+5+5$, or 16 bits. Using the error signals generated by the D/A converter in the multiple passes, logic circuitry in the gate array performs an error correction on the converted output.

The AM40016/AM40116 has a 3-state output structure. Users can enable the eight MSBs, eight LSBs, or both, by using the HI BYTE EN and LO BYTE EN pins. (Both are active low). This feature makes it possible to transfer data from the AM40016/AM40116 to an 8-bit microprocessor bus. However, to prevent the coupling of high frequency noise from the microprocessor bus into the A/D converter, the output data must be buffered; see Figure 9.

The digital error-correction technique used in the AM40016/AM40116 provides an output word that is accurate and linear to within the full 16-bit resolution of the A/D converter. The method corrects for any gain and linearity errors in the amplifying circuitry, as well as in the 6-bit flash A/D converter. Without the error-correction technique, it would be necessary that all the components in the AM40016/AM40116—the difference amplifier, the switched-gain amplifier, and the 6-bit flash A/D converter—be accurate and linear to a 16-bit level. While such a design might be possible to realize on a laboratory benchtop, it would be clearly impractical to achieve on a production basis. The key to the conversion technique used in the AM40016/AM40116 is the 16-bit-accurate and 16-bit-linear D/A converter, which serves as the reference element for the conversion passes as well as for the error-correction mechanism. The use of the proprietary sub-ranging architecture in the AM40016/AM40116 results in a sampling A/D converter that offers unprecedented speed and transfer characteristics at the 16-bit level.
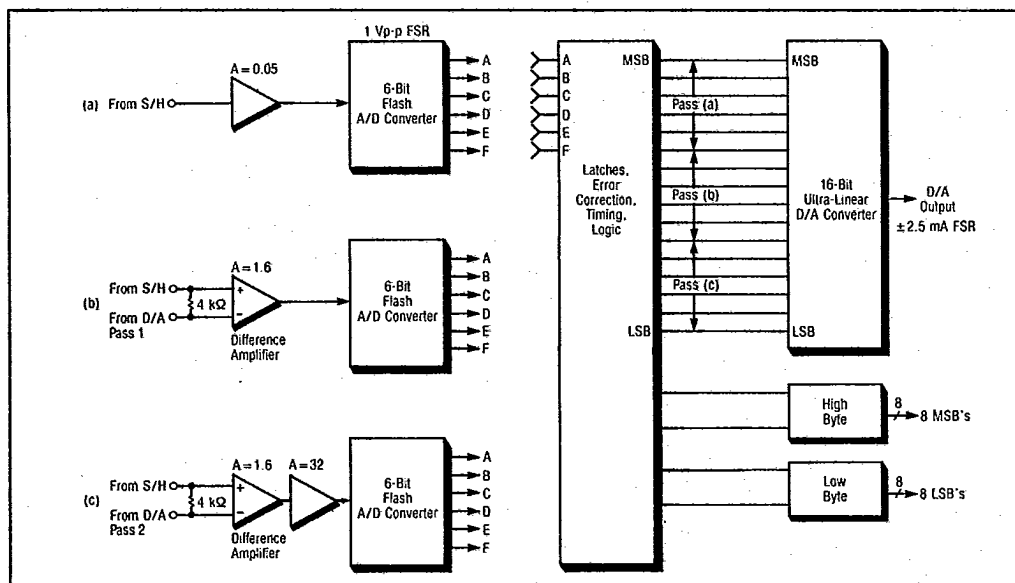

Figure 5. Operating Principle of the AM40016/AM40116.

Performance Testing T-51-10-16

Analogic provides extensive testing of each module prior to shipment to guarantee that all AM40016/AM40116's meet or exceed published specifications. Final test is performed at temperature extremes as well as room temperature. The data sheet of test results are sent to the customer as testimony of the performance results.

Amplitude Domain Testing

The Amplitude Domain Testing is performed with proprietary Automatic Test Equipment at the heart of which is a 22-bit digital-to-analog converter with a reference traceable to the National Bureau of Standards. A simplified block diagram outlining our Amplitude Domain Test System is shown in Figure 6. Using this test equipment, Analogic tests such parameters as integral linearity, differential linearity, A/D converter noise, conversion time, power supply current and power supply rejection. A typical data sheet for the AM40016 is shown in Figure 7.

These specifications may appear to be straight-forward, but Analogic is meticulous not only in testing these parameters but also in defining them so as not to mislead the customer. Following is a list of Analogic's major definitions as tested with our "Amplitude Domain" test systems:

A/D Converter Noise: Errors at the output code caused by signals present other than the signal source.

Integral Linearity: A measure of the maximum deviation (after calibration) of the output digital code transitions from the best-fit straight line through the transfer function, expressed as a percentage of the full scale range. A least squares algorithm is used to determine best fit.

Differential Linearity: A measure of the maximum deviation of any particular code width from the ideal code width, expressed as a fraction of an LSB. Refer to Figure 8.

Differential Linearity =

$$\left| \frac{V_{max} - V_{LSB}}{V_{LSB}} \right| \text{ LSB's}$$

where: V_{max} = maximum (or minimum) code width

Monotonicity: This specification ensures that the transfer function always has a single slope. For example, the transfer function of the unipolar AM40016 maintains a positive slope as the analog input increases from 0V to 10V.

Absolute Accuracy Error: A measure of the largest static difference between the actual output code and that predicted by the ideal transfer function, a worst case summation of all error sources, expressed as a percentage of full scale.

Absolute Accuracy measurements must be referenced to a standard traceable to the NBS with at least an order of magnitude more accuracy than the unit under test.
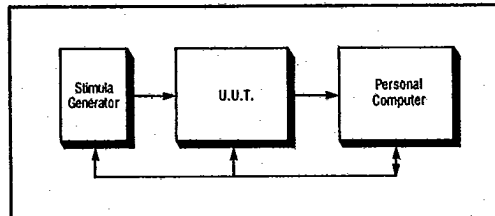
Figure 6. "Amplitude Domain" Test System.

A/D Conversion Time: Time measured from the falling edge of Trigger (the time when the T/H goes into hold) to the rising edge of Transfer, (when the data is latched into the output logic).

Power Supply Rejection: These specifications indicate how power supply voltage variations affect the offset and gain of the ADC expressed in parts per million per 1% change in supply voltage.

Frequency Domain Testing

Incorporating its own ultra-high speed Analog Array processor, Analogic's proprietary Frequency Domain Test System provides a great deal of power in gathering and formatting the frequency domain test data. For example, a Rosenfeld window is applied on a standard basis, but other types of windows, such as Hamming, Blackman, and Blackman-Harris are available for product customization. The number of samples can be varied from 512 to 8192 and the system can average up to 64 FFT's within seconds. A block diagram of the Frequency Domain Test System is shown in Figure 8.

T-51-10-16

Analogic Corporation

Audubon Road   Wakefield, Massachusetts 01880
Data Conversion Products   ------------------   Phone: (617) 246-0300
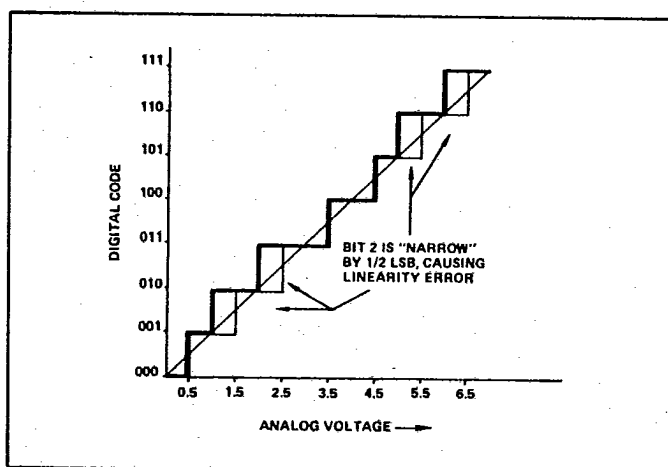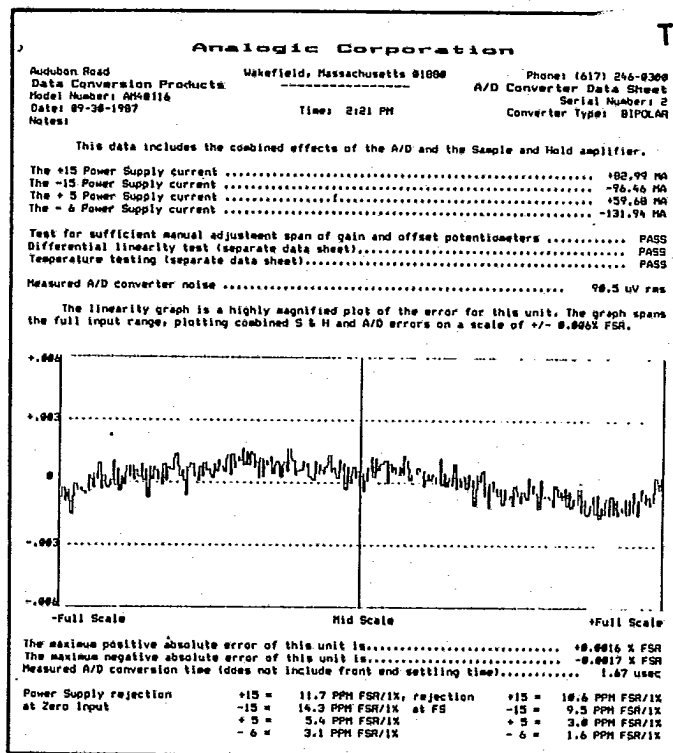Model Number: AN48116   A/D Converter Data Sheet
Date: 09-30-1987   Time: 2:21 PM   Serial Number: 2
Notes: Converter Type: BIPOLAR

         This data includes the combined effects of the A/D and the Sample and Hold amplifier.

The +15 Power Supply current .... +82.99 MA
The -15 Power Supply current .... -76.46 MA
The + 5 Power Supply current ....f............................... +59.68 MA
The - 6 Power Supply current .... -131.94 MA

Test for sufficient manual adjustment span of gain and offset potentiometers .... PASS
Differential linearity test (separate data sheet).. PASS
Temperature testing (separate data sheet)... PASS

Measured A/D converter noise .... 90.5 uV rms

     The linearity graph is a highly magnified plot of the error for this unit. The graph spans
the full input range, plotting combined S & H and A/D errors on a scale of +/- 0.006% FSR.

The maximum positive absolute error of this unit is................................... +0.0016 % FSR
The maximum negative absolute error of this unit is.................................. -0.0017 % FSR
Measured A/D conversion time (does not include front end settling time)............ 1.67 usec

Power Supply rejection   +15 =   11.7 PPM FSR/1%   rejection   +15 =   10.6 PPM FSR/1%
at Zero Input   -15 =   14.3 PPM FSR/1%   at FS   -15 =   9.5 PPM FSR/1%
                        + 5 =   5.4 PPM FSR/1%   + 5 =   3.0 PPM FSR/1%
                        - 6 =   3.1 PPM FSR/1%   - 6 =   1.6 PPM FSR/1%

Figure 8. Example of Differential Non-Linearity.

SAMPLING ANALOG-TO-DIGITAL CONVERTERS

Typical Application

Figure 9 shows a typical application circuit for the AM40016 A/D converter, a pulse amplitude digitizing system. The 500 kHz throughput rate of the AM40016 allows up to a 500 kHz repetition rate for the input signal, provided that the minimum pulse width is 600 ns and the pulse train is synchronized with the Trigger signal. In this application the minimum required sampling rate is equal to the repetition rate because the signal is known to be a pulse not an arbitrary waveform.

T-51-10-16

In some system architectures, it may be desirable to use one or more external sample-and-holds and multiplex them directly to the A/D converter. The AM40016/AM40116 provides the A/D In and S/H Control Out pins for this purpose; simply remove the jumpers between S/H Out and A/D In and between S/H Control Out and S/H Control In.
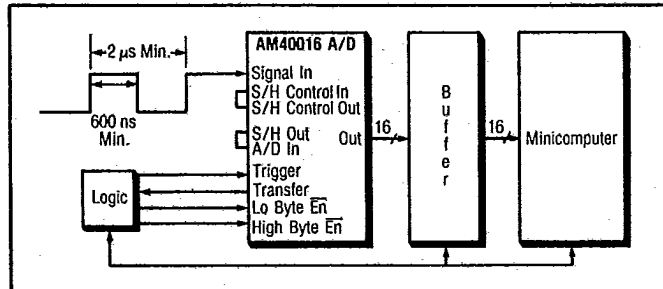

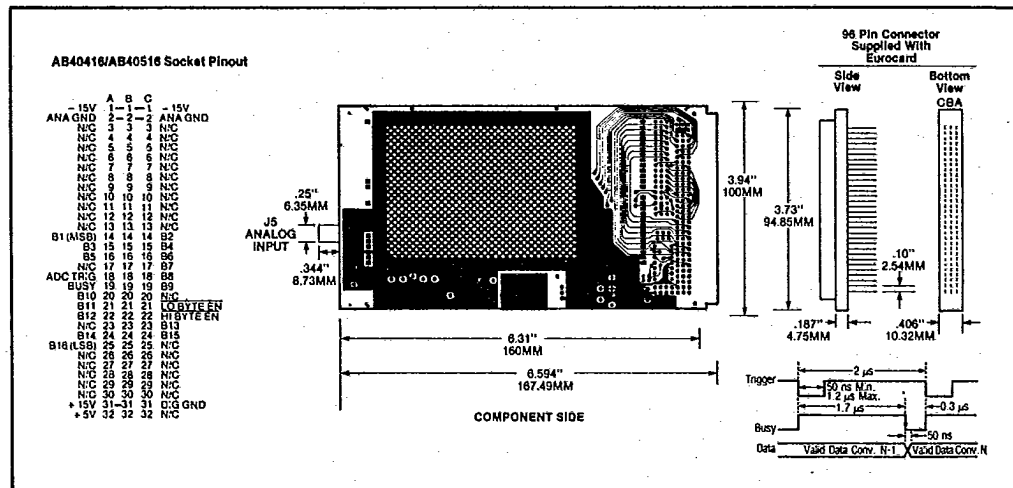**Figure 9. Typical Application Circuit for the AM40016.**

Figure 10. AB40416/AB40516 Eurocard Outline Drawing and Pinouts.

Ordering Guide

16-Bit 500 kHz Unipolar A/D Converter Module
Specify **AM40016**

16-Bit 500 kHz Unipolar A/D Converter Eurocard
Specify **AB40416**

16-Bit 500 kHz Bipolar A/D Converter Module
Specify **AM40116**

16-Bit 500 kHz Bipolar A/D Converter Eurocard
Specify **AB40516**

5-150   **SAMPLING ANALOG-TO-DIGITAL CONVERTERS**