an AMP company

140 mW Power Amplifier with T/R and Diversity Switches 2.4 - 2.5 GHz

AM55-0001

Features

- Highly Integrated PA/Attenuator and T/R Switch
- Low Current Consumption: 120 mA Typ.
- Switch and Attenuator Controls CMOS Compatible
- High Power (140 mW) and Low Power (16 mW) Transmit Power Control
- +5 V/-5 V Fixed Supply Voltages

Description

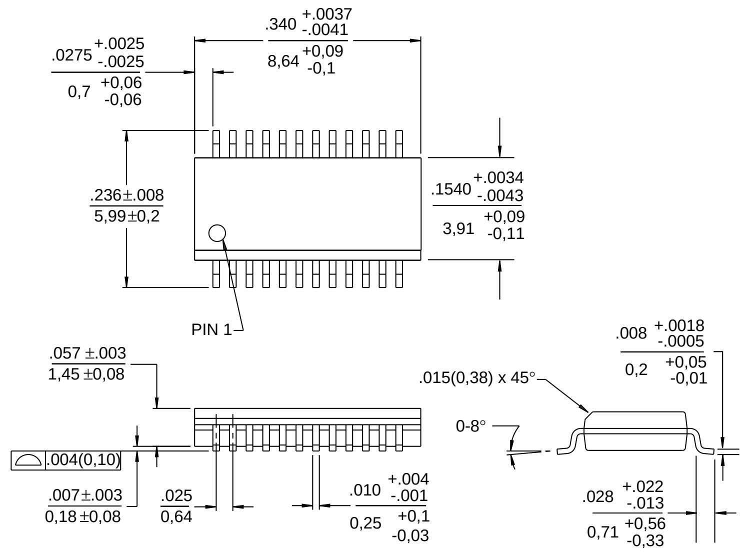
M/A-COM's AM55-0001 is a GaAs power amplifier with integrated transmit/receive and an antenna diversity switch in a low cost SSOP 24 plastic package. The AM55-0001 employs active bias circuits that eliminate the need for external bias adjustment. A 'Sleep Mode' is incorporated which turns off current draw from the positive supply of the PA during receive mode. The AM55-0001 provides a 10-dB step attenuator for use as a transmit power controller.

The AM55-0001 is designed for low power consumption and is ideally suited for FSK systems in the 2.4 - 2.5 GHz bands (North American ISM, Japanese RCR.32 and European ETSI). Typical applications include WLAN and wireless portable data collection.

This amplifier is also available without diversity switching (AM55-0007). Either power amplifier can be combined with a transceiver IC (MD58-0001) to form a complete RF front end.

M/A-COM's AM55-0001 is fabricated using a mature 0.5-micron gate length GaAs process. The process features full passivation for increased performance and reliability.

SSOP-24



Dimensions are in inches over millemeters.

Ordering Information

Part Number	Description
AM55-0001	SSOP 24-Lead Plastic Package
AM55-0001TR	Forward Tape & Reel*
AM55-0001RTR	Reverse Tape & Reel*
AM55-0001SMB	Designer's Kit

* If specific reel size is required, consult factory for part number assignment.

Typical Electrical Specifications

Test Conditions: Frequency: 2.45 GHz, V_{DD} = 5 V ±5%, V_{GG} = - 5 V ±5%, T_A= +25°C

Parameter	Test Conditions	Units	Min.	Typ.	Max.
Power Amplifier					
Linear Gain	High Power Mode	dB	22	26.5	
	Low Power Mode	dB	11	16	
VSWR In/Out	Both Modes			1.5:1	
Output Power	P_{IN} = -3 dBm High Power Mode	dBm	18	21.5	
	Low Power Mode	dBm	8	12	
Second Harmonic	P_{IN} = -3 dBm High Power Mode	dBc		-25	
Third Harmonic		dBc		-17	
I_{DD} (V_{DD1} + V_{DD2} + V_{DD} PA)		mA		120	200
T/R and Diversity Switches					
Insertion Loss		dB		1.2	
Isolation		dB	10	15	
VSWR In/Out				1.5:1	

Absolute Maximum Ratings[1]

Parameter	Absolute Maximum
Max. Input Power[2]	+23 dBm
Operating Voltages[2,3]	V_{DD} = 8 V
	V_{GG} = -8 V
Operating Temperature	-40°C to +85°C
Storage Temperature	-65°C to +150°C

1. Exceeding these limits may cause permanent damage.
2. Ambient temperature (T_A) = +25°C
3. $|V_{DD}| + |V_{GG}|$ not to exceed 12 volts.

Pin Configuration

Pin No.	Pin Name	Description
1	V_{GG}	Negative voltage to all active bias networks
2	T/R CTRL	0 V for transmit mode, +5 V for receive mode
3	Rx OUT	Output of T/R switch for receive mode
4	GND	DC and RF Ground
5	PA OUT	Output of T/R switch for transmit mode
6	V_{DD} PA	V_{DD} for output stage of PA, V_{DD} for active bias circuit of output stage
7	GND	DC and RF Ground
8	ATTN CTRL	0 V for high power mode, +5 V for low power mode
9	GND	DC and RF Ground
10	ANT COMMON	Common port of diversity switch
11	GND	DC and RF Ground
12	ANT 2	Output #2 of diversity switch
13	ANT 1	Output #1 of diversity switch
14	GND	DC and RF Ground
15	ANT CTRL	0 V for ANT Common to ANT 1, +5 V for ANT Common to ANT 2
16	GND	DC and RF Ground
17	V_{DD2}	V_{DD} for both diversity and T/R switches, V_{DD} for second stage of PA
18	GND	DC and RF Ground
19	V_{DD1}	V_{DD} for first stage of PA, V_{DD} of active bias for the first and second stage of PA
20	GND	DC and RF Ground
21	GND	DC and RF Ground
22	PA IN	RF input to PA
23	GND	DC and RF Ground
24	SLEEP CTRL	0 V PA "on" mode, -5 V PA "sleep" mode. Sleep mode shuts off active bias and "pinches off" all PA FETs.

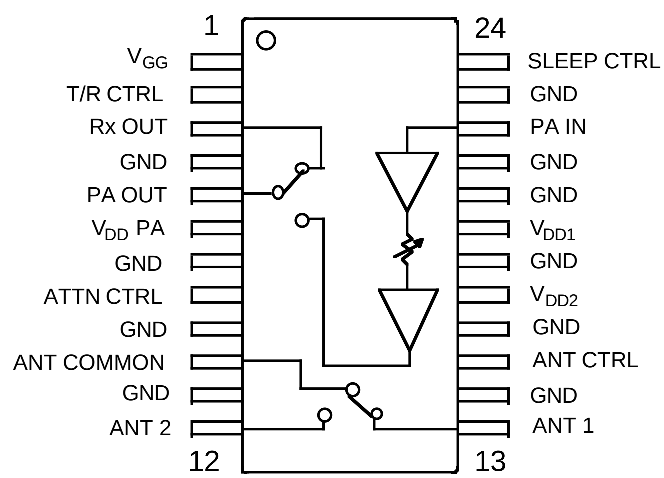
Truth Table

Control Line				Operating Mode
ANT CTRL	ATTN CTRL	T/R CTRL	SLEEP CTRL*	
X	X	1	-5 V	Receive
X	0	0	0 V	High Power
X	1	0	0 V	Low Power
X	X	1	-5 V	Sleep Mode
0	X	X	X	ANT 1
1	X	X	X	ANT 2

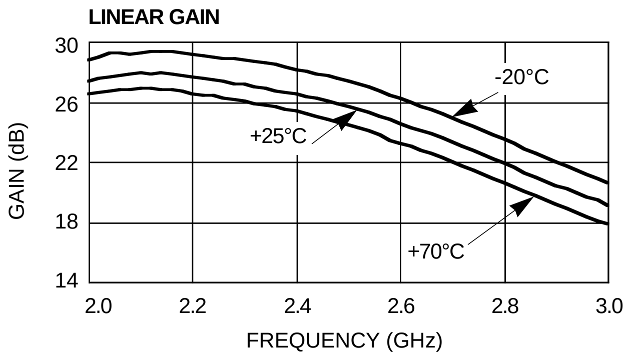
X - Don't Care
"0" = 0 V to 0.2 V @ 100 µA
"1" = V_{DD} to V_{DD} -0.2 V @ 200 µA

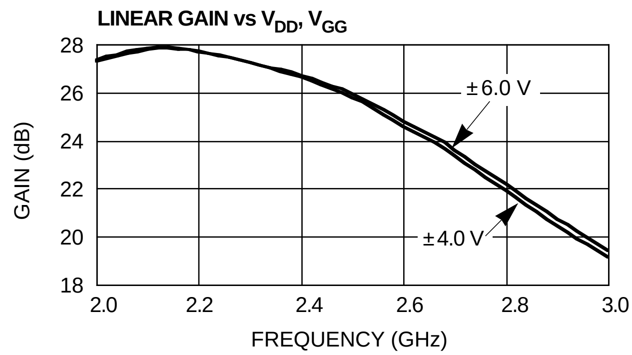
* Control voltage levels between 0 V and V_{GG} must be used on SLEEP CTRL control line. (Pin 24)

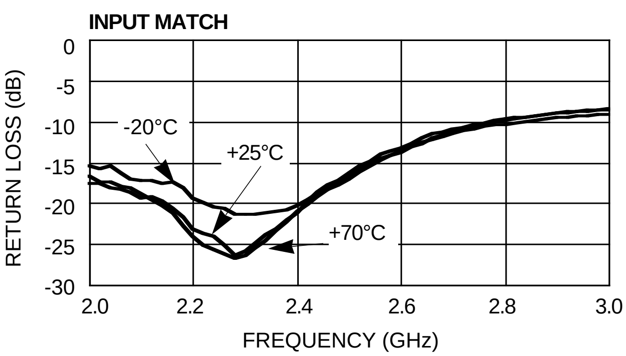
Functional Diagram and Pin Configuration

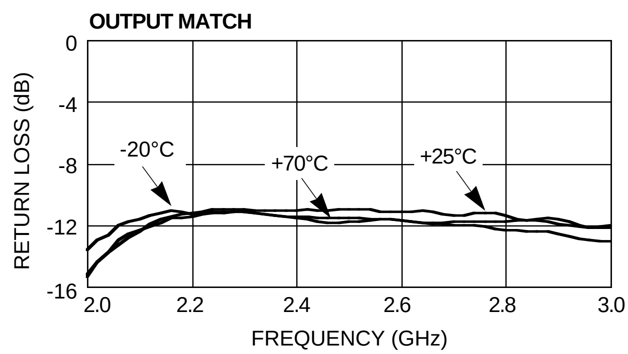


Small Signal Power Amplifier[1]

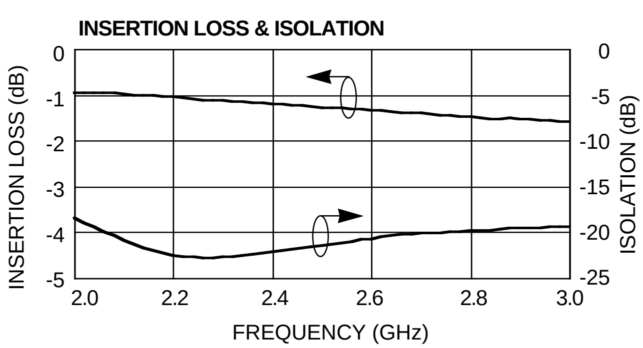


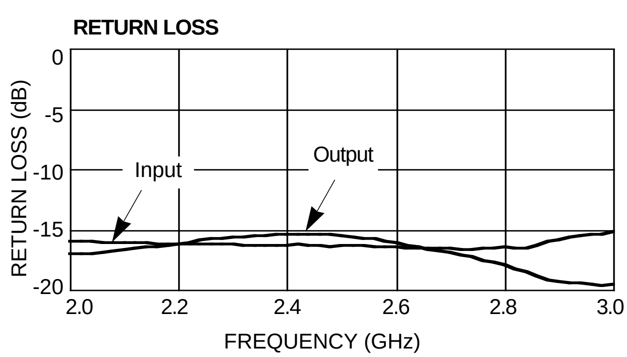






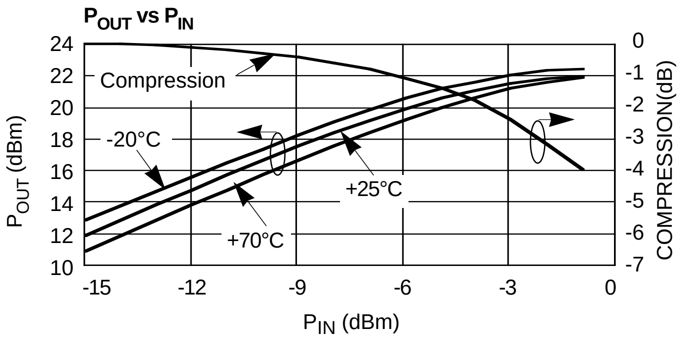
T/R Switch Small Signal Performance[1]

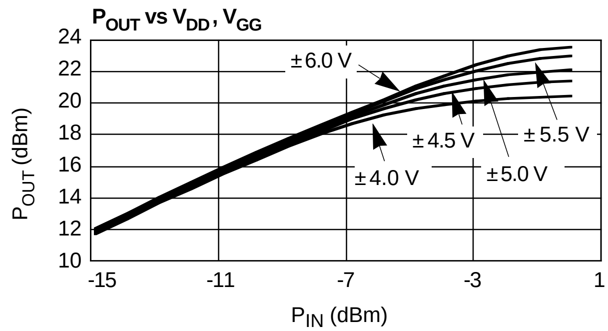


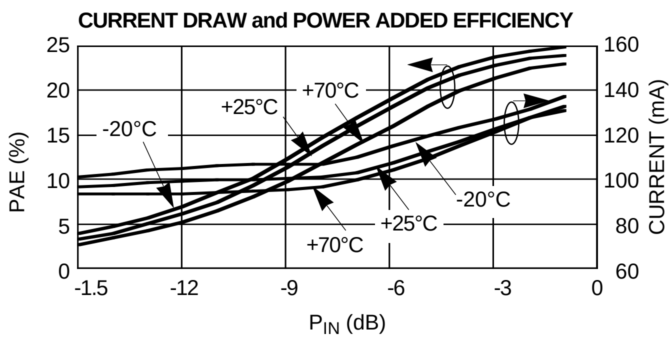


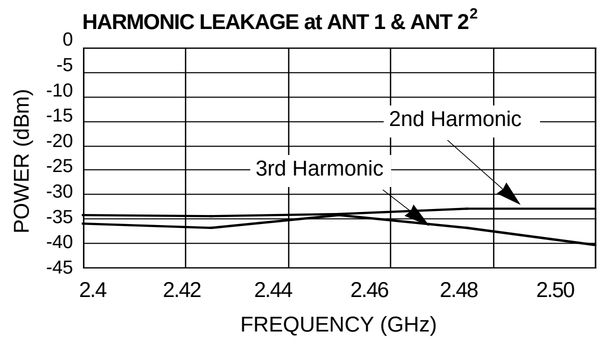
1. Unless otherwise noted, Frequency: 2.45 GHz, V_{DD} = 5 V ±5%, V_{GG} = - 5 V ±5%, T_A= +25°C

Power Amplifier Power Performance[1]



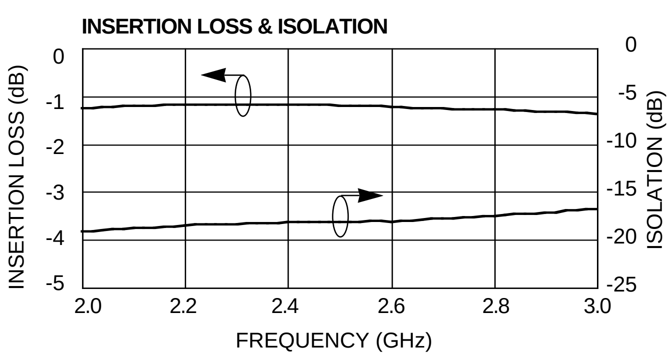


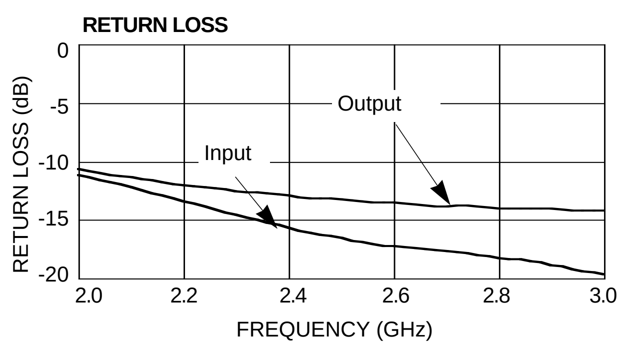




2. Measured with an RF input power of -3 dBm at PA IN. Output measured at ANT 1 and ANT 2 with PA OUT and ANT COMMON terminated in 50Ω.

Diversity Switch Small Signal Performance[1]

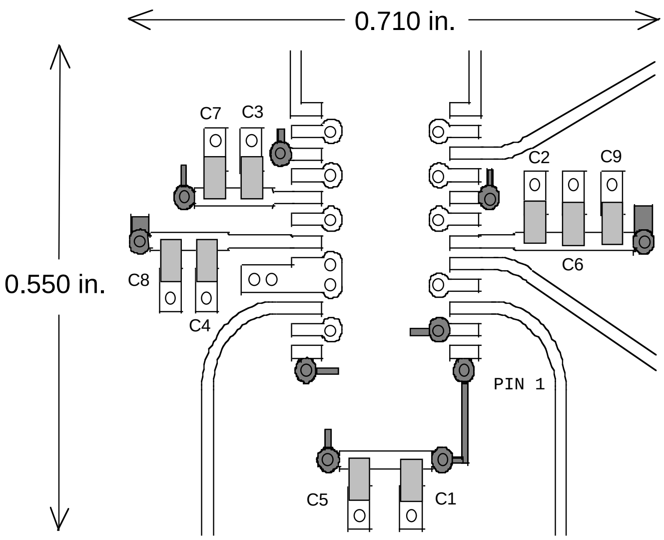




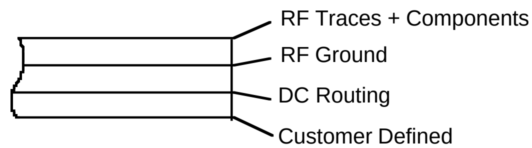
1. Unless otherwise noted, Frequency: 2.45 GHz, V_{DD} = 5 V ±5%, V_{GG} = - 5 V ±5%, T_A= +25°C

Recommended PCB Configuration

Layout View



Cross-Section View



The PCB dielectric between RF traces and RF ground layers should be chosen to reduce RF discontinuities between 50 Ω lines and package pins. M/A-COM recommends an FR-4 dielectric thickness of 0.008 in. (0.2 mm), yielding a 50 Ω line width of 0.015 in. (0.38 mm). The recommended metalization thickness is 1 oz. copper.

Shaded traces are vias to DC routing layer and traces on DC routing layer.

Biasing Procedure

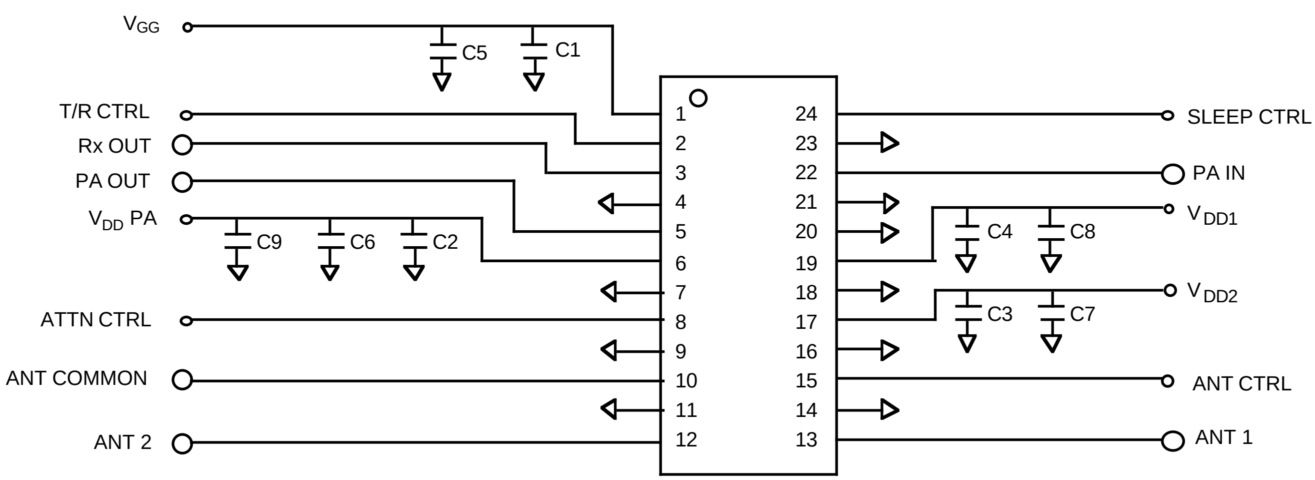
The AM55-0001 requires the V_{GG} bias be applied prior to ***any*** V_{DD} bias. Permanent damage may occur if this procedure is not followed. All FETs in the PA will draw excessive current and damage internal circuitry.

External Circuitry Parts List

Label	Value	Purpose
C1 - C4	33 pF	Bypass (GHz)
C5 - C8	1000 pF	Bypass (MHz)
C9	0.01 µF	Bypass (kHz)

All off-chip components are low-cost surface mount components obtainable from multiple sources. (0.020 in. x 0.040 in. or 0.030 in. x 0.050 in.)

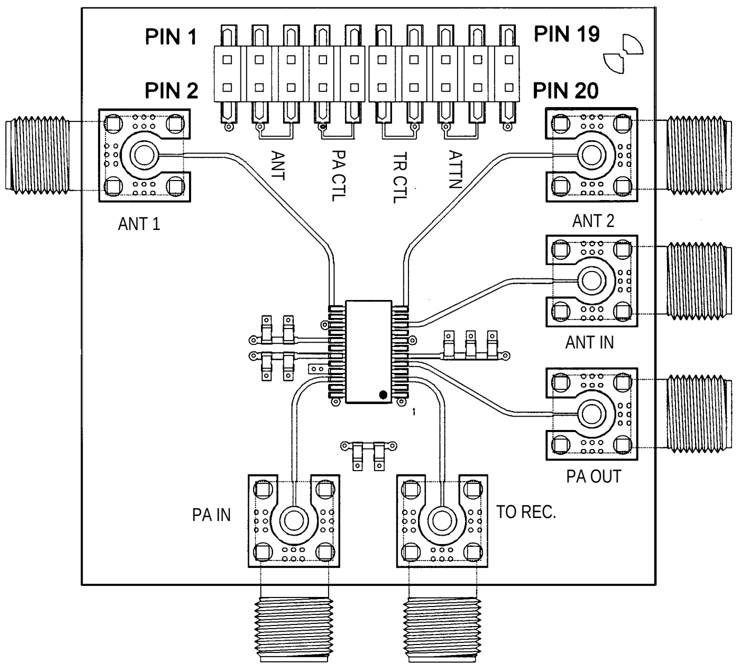
External Circuitry



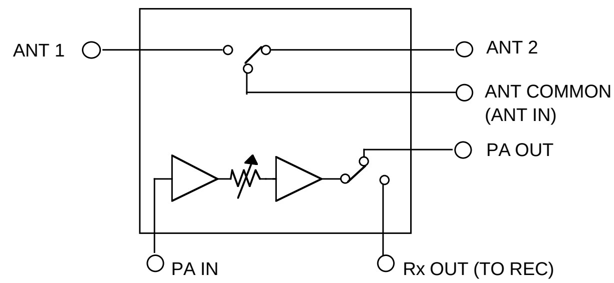
Designer's Kit (AM55-0001SMB)

The AM55-0001SMB Designer's Kit allows for immediate evaluation of M/A-COM's AM55-0001 integrated Power Amplifier with T/R and Diversity Switch. The evaluation board consists of an AM55-0001, recommended external surface mount circuitry, RF connectors and a DC multi-pin connector, all mounted to a multi-layer FR-4 PCB. Other items included in the Designer's Kit: a floppy disk (with typical performance data and a .DXF file of the recommended PCB layout) and any additional Application Notes. The AM55-0001SMB evaluation PCB and block diagram are illustrated below with all functional ports labeled.

P/A Switch Sample Board



Functional Block Diagram

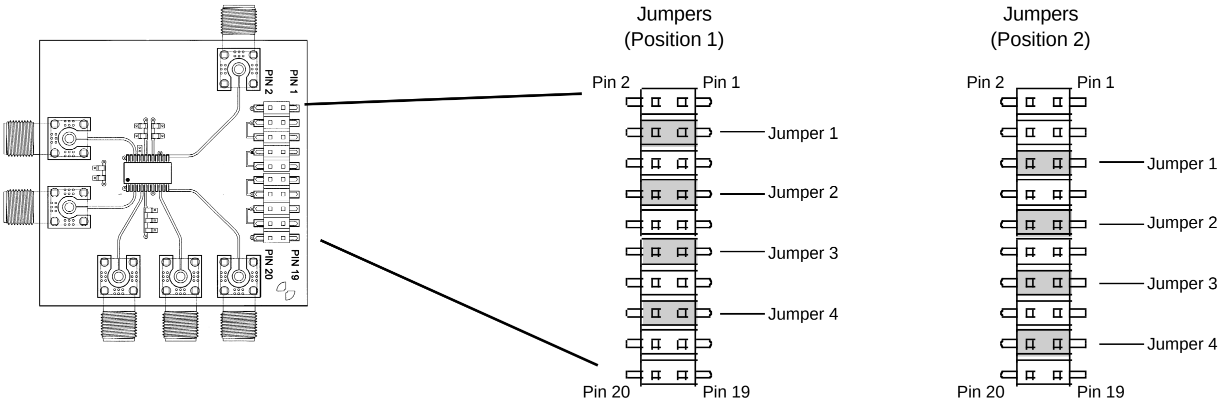


DC Connector Pinout

PCB DC Connector	Function	Device Pin Number
1	V_{DD1} (+ 5 V)	19
2	V_{DD2} (+ 5 V)	17
3	Logic Low (GND)	N/C
4	ANT Control (0 V/+5 V)	15
5	Logic High (V_{DD1})	19
6	ANT Control (0 V/+5 V)	15
7	Negative Logic High (GND)	N/C
8	PA Control (0 V/-5 V)	24
9	Negative Logic Low (V_{GG})	1
10	PA Control (0 V/-5 V)	24

PCB DC Connector	Function	Device Pin Number
11	Logic High (V_{DD1})	19
12	T/R Control (0 V/+5 V)	2
13	Logic Low (GND)	N/C
14	T/R Control (0 V/+5 V)	2
15	Logic High (V_{DD1})	19
16	ATTN Control (0 V/+5 V)	8
17	Logic Low (GND)	N/C
18	ATTN Control (0 V/+5 V)	8
19	V_{DD} PA (+5 V)	6
20	V_{GG} (- 5 V)	1

PCB DC Connector Jumper Settings



Jumper 1 (Diversity Switch Control)	Position 1 = ANT Common to ANT 2 Insertion Loss Position 2 = ANT Common to ANT 1 Insertion Loss
Jumper 2 (PA Sleep Control)	Position 1 = PA ON Position 2 = PA Sleep Mode
Jumper 3 (T/R Switch Control)	Position 1 = Receive Mode Position 2 = Transmit Mode
Jumper 4 (Attenuator Control)	Position 1 = Attenuator ON (Low Power Transmit) Position 2 = Attenuator OFF (High Power Transmit)

AM55-0001SMB Biasing Procedure

In order to prevent transients which may damage the MMIC, please adhere to the following procedure.

- Turn on all power supplies and set all voltages to 0 volts BEFORE connecting the power supplies to the DC connector.
- Set jumpers for desired test mode.
- Apply a -5.0 volt supply to DC connector pin 20 (V_{GG}).
- Apply a +5.0 volt supply to the DC connector pin 1 (V_{DD1}).
- Apply a +5.0 volt supply to the DC connector pin 2 (V_{DD2}).
- Apply a +5.0 volt supply to the DC connector pin 19 (V_{DD} PA).
- Adjust V_{GG} supply to -5 volts.
- Adjust all V_{DD} supplies to +5 volts.
- Hot switching of jumpers will not damage device.
- To power off, reverse above procedure.
  1. Set V_{DD1} & V_{DD2} & V_{DD} PA to 0 volts.
  2. Set V_{GG} to 0 volts.
  3. Disconnect bias lines from DC connector.
  4. Turn off power supplies.

Evaluation PCB and RF Connector Losses

Port Reference	Approximate Loss (dB)
PA IN	0.25
PA OUT	0.25
Rx OUT (TO REC)	0.25
ANT COMMON (ANT IN)	0.25
ANT1	0.30
ANT2	0.30

The DC connector on the Designer's Kit PCB allows selection of all the device's operating modes. It is accomplished by one or more of the following methods:

1. A mating female multi-pin connector (Newark Electronics Stock # 46F-4658, not included)
2. Wires soldered to the necessary pins (not included)
3. Clip leads (not included)
4. A combination of clip leads or wires and jumpers (jumpers included as required)