Final

Am6012/6012A

12-Bit High- and Ultra-High-Speed Multiplying D/A Converters

Advanced Micro Devices

DISTINCTIVE CHARACTERISTICS

- All grades 12-bit monotonic over temperature
- Differential nonlinearity to ±0.012% (13 bits) max over temperature (A grades)
- Fast settling output current: 250 ns typical
- Full scale current: 4 mA typical
- High output impedance and compliance: −5 to +10 V
- Differential current outputs
- Low cost
- High-speed multiplying capability
- Direct interface to TTL, CMOS, ECL, HTL, NMOS
- Low power consumption: 234 mW typical

GENERAL DESCRIPTION

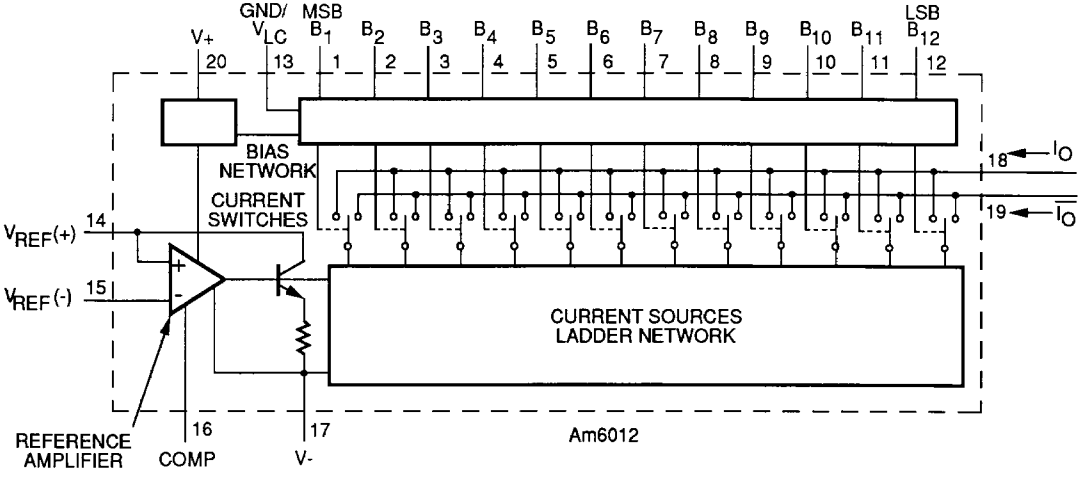
The Am6012 12-bit monolithic multiplying digital-to-analog converter represents new levels of speed, accuracy and low cost. The Am6012 is the first 12-bit DAC to be built using standard processing without the need for thin-film resistors or active trimming.

The Am6012 design guarantees a more uniform step size than is possible with standard binarily-weighted DACs. This ±1/2 LSB differential nonlinearity is desirable in many applications where local linearity is critical. The uniform step size provides for finer resolution of levels and, in most applications, is more useful than conformance to an ideal straight line from zero to full scale.

The Am6012 has high-voltage compliance, high-impedance dual complementary outputs that increase device versatility and enable differential operation to effectively double the peak-to-peak output swing. These outputs can be used directly without op amps in many applications. The dual complementary outputs can also be connected in A/D-converter applications to present a constant load current and significantly reduce switching transients and increase system throughput. Output full-scale current is specified at 4 mA, allowing use of smaller load resistors to minimize the output RC delay which usually dominates setting time at the 12-bit level.

The Am6012 guarantees full 12-bit monotonicity for all grades and differential nonlinearity as tight as 0.012% (13 bits), for the A grades and 0.025% (12 bits) for the standard grades over the entire temperature range. Device performance is essentially independent of power supply voltage, and devices work over a wide operating range from +5 and −12 V to ±18 V.

BLOCK DIAGRAM



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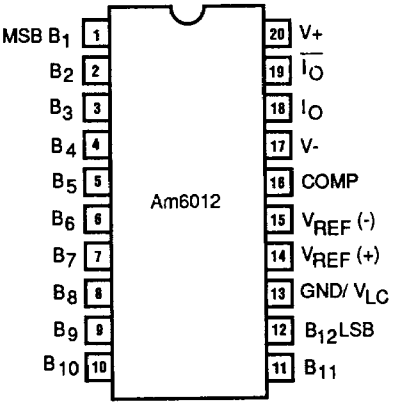
CONNECTION DIAGRAM
Top View

D-20-1, P-20-1



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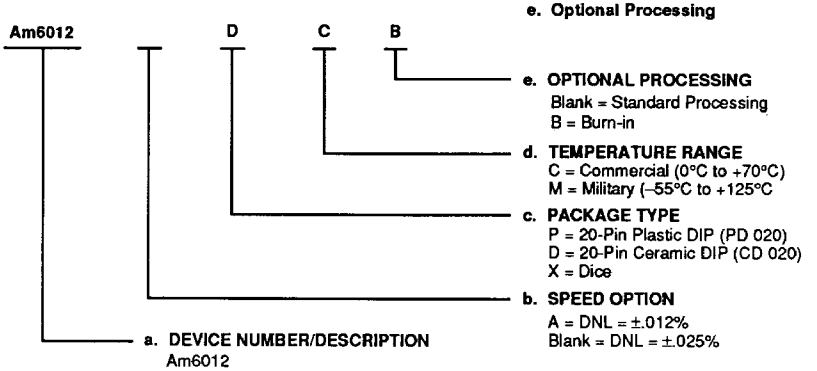
ORDERING INFORMATION

Standard Products

AMD standard products are available in several packages and operating ranges. The ordering number (Valid Combination) is formed by a combination of:

a. Device Number
b. Speed Option (if applicable)
c. Package Type
d. Temperature Range
e. Optional Processing



Valid Combinations	
Am6012	DC, PC,
Am6012A	DCB, XC, XM

Valid Combinations

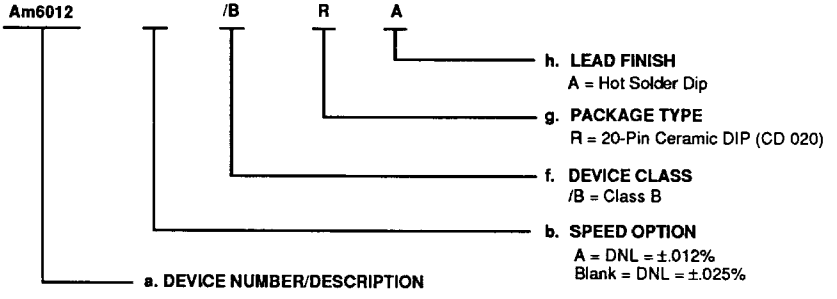
Valid Combinations list configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations, to check on newly released combinations, and to obtain additional data on AMD's standard military grade products.

MILITARY ORDERING INFORMATION

APL Products

AMD products for Aerospace and Defense applications are available in several packages and operating ranges. APL (Approved Products List) products are fully compliant with MIL-M-38510 and MIL-STD-883C requirements. The ordering number (Valid Combination) is formed by a combination of:

a. Device Number
b. Speed Option (if applicable)
f. Device Class
g. Package Type
h. Lead Finish



Valid Combinations	
Am6012	/BRA
Am6012A	

Valid Combinations

Valid Combinations list configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations to check on newly released combinations.

Group A Tests

Group A tests consist of subgroups 1, 2, and 3.

MAXIMUM RATINGS

Storage Temperature	–65 to +125°C
Lead Temperature (Soldering, 60 sec)	300°C
Power Supply Voltage	±18 V
Logic Inputs	–5 to +18 V
Analog Current Outputs	–8 to +12 V
Reference Inputs V_{14}, V_{15}	V– to V+
Reference Input Differential Voltage (V_{14} to V_{15})	±18 V
Reference Input Current (I_{14})	1.25 mA

Stresses above those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to absolute maximum ratings for extended periods may affect device reliability.

OPERATING RANGES

Am6012A, Am6012 Military	–55 to +125°C
Am6012A, Am6012 Commercial	0 to +70°C
Die Size	0.093 x 0.134 in.

Operating ranges define those limits between which the functionality of the device is guaranteed.

ELECTRICAL CHARACTERISTICS

These specifications apply for V+ = +15 V, V– = –15 V, I_{REF} = 1.0 mA, over the operating temperature range unless othewise specified. Included in Group A Subgroup. 1,2,3, unless otherwise noted.

Parameter	Description	Test Conditions	Am6012A			Am6012			Unit
			Min.	Typ.	Max.	Min.	Typ.	Max.	
	Resolution		12	12	12	12	12	12	bits
	Monotonicity		12	12	12	12	12	12	bits
DNL	Differential Nonlinearity	Deviation from ideal step size	—	—	±.012	—	—	±.025	%FS
			13	—		12	—	—	bits
NL	Nonlinearity	Deviation from ideal straight line	—	—	±.05	—	—	±0.05	%FS
I_{FS}	Full Scale Current	V_{REF} = 10.000 V $R_{14} = R_{15}$ = 10.000 kΩ T_A = 25°C	3.967	3.999	4.031	3.935	3.999	4.063	mA
TCI_{FS}	Full Scale Tempco		—	±5	—	—	±10	—	ppm/°C
			—	±.0005	—	—	±.001	—	%FS/°C
V_{OC}	Output Voltage Compliance	DNL Specification guaranteed over compliance range R_{OUT} > 10 mΩ typ	–5	—	+10	–5	—	+10	V
I_{FSS}	Full Scale Symmetry	$I_{FS} - \overline{I_{FS}}$	—	±0.2	±1.0	—	±0.4	±2.0	µA
I_{ZS}	Zero Scale Current		—	—	0.10	—	—	0.10	µA
t_S	Settling Time (Note 1)	T_O ±1/2 LSB, all bits ON or OFF, t_A = 25°C	—	250	500	—	250	500	ns
t_{PLH} t_{PHL}	Propagation Delay – All bits (Note 1)	50% to 50%	—	25	50	—	25	50	ns
C_{OUT}	Output Capacitance		—	20	—	—	20	—	pF
V_{IL}	Logic Input Levels	Logic "0"	—	—	0.8	—	—	0.8	V
V_{IH}		Logic "1"	2.0	—	—	2.0	—	—	V
I_{IN}	Logic Input Current	V_{IN} = –5 to +18 V	—	—	40	—	—	40	µA
V_{IS}	Logic Input Swing	V– = –15 V	–5	—	+18	–5	—	+18	V
I_{REF}	Reference Current Range		0.2	1.0	1.1	0.2	1.0	1.1	mA
I_{15}	Reference Bias Current		0	–0.5	–2.0	0	–0.5	–2.0	µA
dI/dt	Reference Input Slew Rate (Note 1)	$R_{14(eq)}$ = 800 Ω CC = 0 pF	4.0	8.0	—	4.0	8.0	—	mA/µs
$PSSI_{FS+}$	Power Supply Sensitivity	V+ = +13.5 V to +16.5 V, V– = –15 V	—	±.00005	±.001	—	±.0005	±.001	%FS/%
$PSSI_{FS-}$		V– = –13.5 V to –16.5 V, V+ = +15 V	—	±.00025	±.001	—	±.00025	±.001	%FS/%
V+	Power Supply Range	V_{OUT} = 0 V	4.5	—	18	4.5	—	18	V
V–			–18	—	–10.8	–18	—	–10.8	V
I+	Power Supply Current	V+ = +5 V, V– = –15 V	—	5.7	8.5	—	5.7	8.5	mA
I–			—	–13.7	–18.0	—	–13.7	–18.0	mA
I+		V+ = +15 V, V– = –15 V	—	5.7	8.5	—	5.7	8.5	mA
I–			—	–13.7	–18.0	—	–13.7	–18.0	mA
P_D	Power Dissipation	V+ = +5 V, V– = –15 V	—	234	312	—	234	312	mW
		V+ = 15 V, V– = –15 V	—	291	397	—	291	397	mW

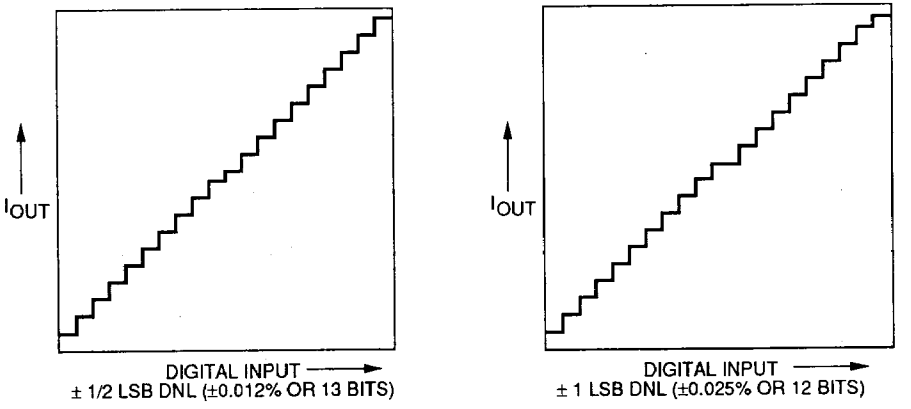
Note 1: Guaranteed by characterization. Not tested.

ACCURACY SPECIFICATIONS

The design of the Am6012 emphasizes differential linearity, which is a measure of the uniformity of each step in the transfer characteristic. The circuit design requires resistor matching and tracking tolerances of eight times lower than that of previous designs to achieve and maintain monotonicity over temperature. This advantage has been used in the Am6012A to provide 13-bit differential nonlinearity over temperature, a level of performance not generally available in previous film resistors.

The figures illustrate that ±1/2 LSB (13-bit) differential nonlinearity guarantees a converter with 4096 distinct output levels; ± 1 LSB DNL guarantees monotonicity, so that when the input code is increased the output will not decrease. Note that nonlinearity, or deviation from an ideal straight line through zero and full scale, cannot be visually determined from the figures. In most applications, 12-bit resolution and differential linearity are more important than linearity. This is especially true in video and graphics, where the human eye has difficulty discerning nonlinearity of less than 5%.

Differential Nonlinearity
Worst Case At Temperature Extreme



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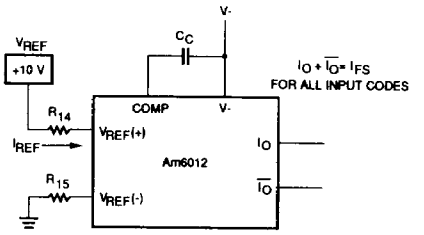
APPLICATION HINTS:

1. **Reference current and reference resistor.**
There is a 1-to-4 scale up between the reference current (I_{REF}) and the full scale output current (I_{FS}). If V_{REF} = +10V and I_{FS} = 4 mA, the value of the R_{14} is:

$$R_{14} = \frac{4 \times 10\ V}{4\ mA} = 20\ k\Omega \quad R_{14} = R_{15}$$



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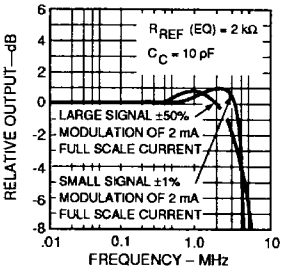
2. **Reference amplifier compensation.**
For ac reference applications, a minimum value compensation capacitor (C_C) is normally used. The value of this capacitor depends on the equivalent resistance at pin 14. The values to maximize bandwidth without oscillation are as follows:

MINIMUM SIZE COMPENSATION CAPACITOR (I_{FS} = 4 mA, I_{REF} = 1.0 mA)

$R_{14(EQ)}$ (kΩ)	C_C (pF)
10	50
5	25
2	10
1	5
.5	0

Reference Amplifier Frequency Response



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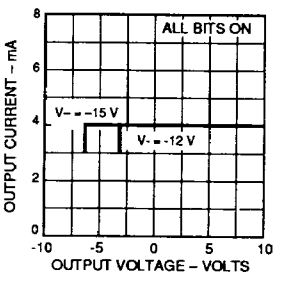
Output Voltage Compliance



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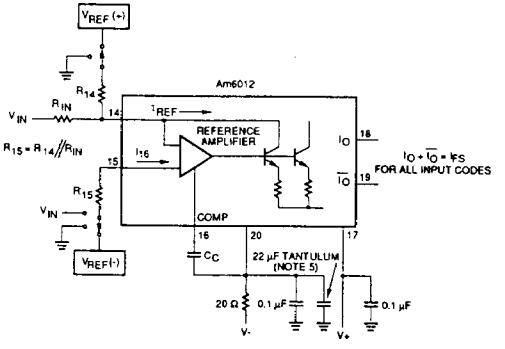
A 0.01 µF capacitor is recommended for the fixed reference operation.



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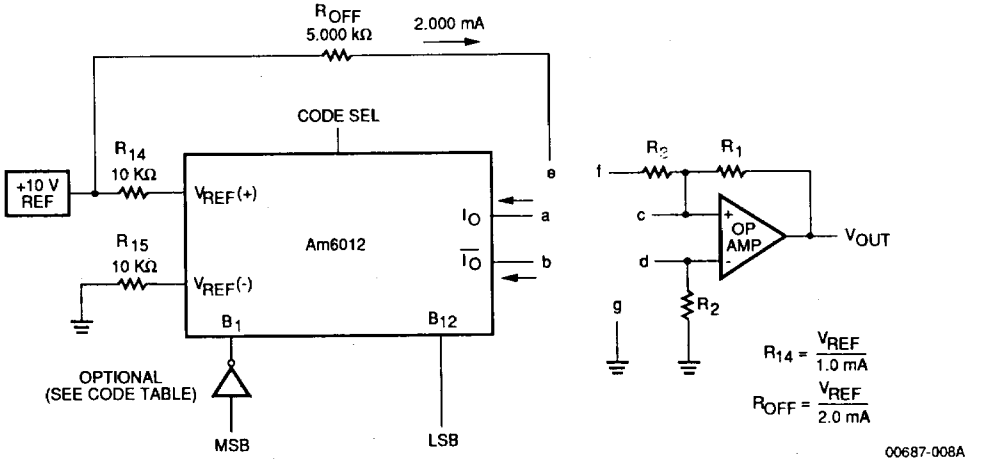
Reference Configuration	R_{14}	R_{15}	R_{IN}	C_C	I_{REF}
Positive Reference	V_{R+}	0V	N/C	.01 µF	V_{R+}/R_{14}
Negative Reference	0V	V_{R-}	N/C	.01 µF	$-V_{R-}/R_{14}$
Low Impedance Bipolar Reference	V_{R+}	0V	V_{IN}	(Note 1)	$(V_{R+}/R_{14}) + (V_{IN}/R_{IN})$ (Note 2)
High Impedance Bipolar Reference	V_{R+}	V_{IN}	N/C	(Note 1)	$(V_{R+} - V_{IN})/R_{14}$ (Note 3)
Pulsed Reference (Note 4)	V_{R+}	0V	V_{IN}	No Cap	$(V_{R+}/R_{14}) + (V_{IN}/R_{IN})$

Notes:
1. The compensation capacitor is a function of the impedance seen at the $+V_{REF}$ input and must be at least C = 5 pF x $R_{14(eq)}$ in kΩ. For R_{14} < 800 Ω no capacitor is necessary.
2. For negative values of V_{IN}, V_R+/R_{14} must be greater than $-V_{IN}$ Max/R_{IN} so that I_{REF} is always positive.
3. For positive values of V_{IN}, V_{R+} must be greater than V_{IN} Max so that the I_{REF} is always positive.
4. For pulsed operation, V_{R+} provides a dc offset and may be set to zero in some cases. The impedance at pin 14 should be 800Ω or less.
5. For optimum settling time, decouple V- with 20 Ω and bypass with 22 µF tantulum capacitor.



CODE FORMAT		CONNECTIONS	OUTPUT SCALE	MSB B1	B2	B3	B4	B5	B6	B7	B8	B9	B10	B11	LSB B12	I_O (mA)	$\overline{I_O}$ (mA)	V_{OUT}
UNIPOLAR	Straight binary; one polarity with true input code, true zero output.	a–c b–g R1 = R2 = 2.5 k	Positive full scale	1	1	1	1	1	1	1	1	1	1	1	1	3.999	.000	9.9976
			Positive full scale – LSB	1	1	1	1	1	1	1	1	1	1	1	0	3.998	.001	9.9951
			Zero scale	0	0	0	0	0	0	0	0	0	0	0	0	.000	3.999	.0000
	Complementary binary; one polarity with complementary input code, true zero output.	a–g b–d R1 = R2 = 2.5 k	Positive full scale	0	0	0	0	0	0	0	0	0	0	0	0	.000	3.999	9.9976
			Positive full scale – LSB	0	0	0	0	0	0	0	0	0	0	0	1	.001	3.998	9.9951
			Zero scale	1	1	1	1	1	1	1	1	1	1	1	1	3.999	.000	.0000
SYM-METRICAL OFFSET	Straight offset binary; offset half scale, symmetrical about zero, no true zero output.	a–c b–d f–g R1 = R3 = 2.5 k R2 = 1.25 k	Positive full scale	1	1	1	1	1	1	1	1	1	1	1	1	3.999	.000	9.9976
			Positive full scale – LSB	1	1	1	1	1	1	1	1	1	1	1	0	3.998	.001	9.9927
			(+) Zero scale	1	0	0	0	0	0	0	0	0	0	0	0	2.000	1.999	.0024
			(–) Zero scale	0	1	1	1	1	1	1	1	1	1	1	1	1.999	2.000	–.0024
			Negative full scale – LSB	0	0	0	0	0	0	0	0	0	0	0	1	.001	3.998	–9.9927
			Negative full scale	0	0	0	0	0	0	0	0	0	0	0	0	.000	3.999	–9.9976
	1's complement; offset half scale symmetrical about zero, no true zero output MSB complemented (need inverter at B1).	a–c b–d f–g R1 = R3 = 2.5 k R2 = 1.25 k	Positive full scale	0	1	1	1	1	1	1	1	1	1	1	1	3.999	.000	9.9976
			Positive full scale – LSB	0	1	1	1	1	1	1	1	1	1	1	0	3.998	.001	9.9927
			(+) Zero scale	0	0	0	0	0	0	0	0	0	0	0	0	2.000	1.999	.0024
			(–) Zero scale	1	1	1	1	1	1	1	1	1	1	1	1	1.999	2.000	–.0024
			Negative full scale – LSB	1	0	0	0	0	0	0	0	0	0	0	1	.001	3.998	–9.9927
			Negative full scale	1	0	0	0	0	0	0	0	0	0	0	0	.000	3.999	–9.9976
OFFSET WITH TRUE ZERO	Offset binary; offset half scale, true zero output.	e–a–c b–g R1 = R2 = 5 k	Positive full scale	1	1	1	1	1	1	1	1	1	1	1	1	3.999	.000	9.9951
			Positive full scale – LSB	1	1	1	1	1	1	1	1	1	1	1	0	3.998	.001	9.9902
			+ LSB	1	0	0	0	0	0	0	0	0	0	0	1	2.001	1.998	.0049
			Zero scale	1	0	0	0	0	0	0	0	0	0	0	0	2.000	1.999	.000
			– LSB	0	1	1	1	1	1	1	1	1	1	1	1	1.999	2.000	–.0049
			Negative full scale + LSB	0	0	0	0	0	0	0	0	0	0	0	1	.001	3.998	–9.9951
			Negative full scale	0	0	0	0	0	0	0	0	0	0	0	0	.000	3.999	–10.000
	2's complement; offset half scale, true zero output MSB complemented (need inverter at B1).	e–a–c b–g R1 = R2 = 5 k	Positive full scale	0	1	1	1	1	1	1	1	1	1	1	1	3.999	.006	9.9951
			Positive full scale – LSB	0	1	1	1	1	1	1	1	1	1	1	0	3.998	.001	9.9902
			+1 LSB	0	0	0	0	0	0	0	0	0	0	0	1	2.001	1.998	.0049
			Zero scale	0	0	0	0	0	0	0	0	0	0	0	0	2.000	1.999	.000
			–1 LSB	1	1	1	1	1	1	1	1	1	1	1	1	1.999	2.000	–0.049
			Negative full scale + LSB	1	0	0	0	0	0	0	0	0	0	0	1	.001	3.998	–9.9951
			Negative full scale	1	0	0	0	0	0	0	0	0	0	0	0	.000	3.999	–10.000

ADDITIONAL CODE MODIFICATIONS

1. Any of the offset binary codes may be complemented by reversing the output terminal pair.

SEGMENTED DAC DESIGN INFORMATION

The design of a 12-bit D/A converter has traditionally required precision thin-film resistors, a trimming method, and a binary-weighted ladder network. The Am6012 is a 12-bit DAC that uses diffused resistors and requires no trimming, cutting, blowing or zapping to guarantee monotonicity for all grades over the temperature range. A proprietary design technique, departing from the traditional R-2R approach used in virtually all high-speed resolution converters, provides inherent monotonicity and differential linearity as high as 13 bits. This guarantees a more uniform step size over the temperature range than available trimmed 12-bit converters. The converter performance is immune to variations in temperature, time, process, and mechanical stress. The circuit also features differential high-compliance current outputs, wide supply range, and a multiplying reference input.

In most converter applications, uniform step size is more important than conformance to an ideal straight line. Most 12-bit converters are used for high resolution rather than high linearity, since few transducers are more linear than ±0.1%. All classic binary-weighted converters require ±1/2 LSB (±.012%) linearity to guarantee monotonicity, which requires very tight resistor matching and tracking. This new circuit uses conventional bipolar processing to achieve high differential linearity, or conformance to an ideal straight line.

One design approach that provides monotonicity without requiring high linearity is the MOS switch-resistor string. This circuit is actually a full complement to a current-switched R-2R DAC, since it is slower, has a voltage output and, if implemented at the 12-bit level, would use 4096 low-tolerance resistors rather than a minimum number of high-tolerance resistors as in the R-2R network. Its lack of speed and density for 12 bits are its drawbacks.

The technique used in the Am6012 combines the advantages of both the R-2R and 2^nR approaches. It is inherently monotonic, fast, and uses untrimmed resistors which are actually fewer in number than the classic R-2R ladder.

To properly describe the new design technique, the standard R-2R ladder approach used in previous 12-bit DACs is discussed first. Figure 1 shows the 12-bit currents that are used in all possible binary combinations to generate 4096 analog output levels. The resistor-ladder tolerance is most critical for the major carry, where the 11 LSBs turn off and the MSB turns on. If the MSB is more than 1 µA low, or –05%, the converter is nonmonotonic. Table 1 shows the maximum tracking error that can be tolerated over a 100°C range to maintain monotonicity, which is ±1 LSB DNL. Achieving ±1/2 LSB differential nonlinearity is especially difficult since it requires a tracking temperature coefficient of ±1.25 ppm/°C.

Figure 2 shows the transfer characteristic for the new technique, called the segmented DAC. The Am4096 output levels are composed of eight groups of 512 steps each. Each step group is generated by a 9-bit DAC, and each of the segment slopes is determined by one of eight equal current sources, as shown in Figure 3. The resistors in the 9-bit DAC determine monotonicity. The major carry of the 9-bit DAC is repeated in each of the eight segments, and requires eight times lower initial resistor accuracy and tracking to maintain a given differential nonlinearity over temperature.

The operation of the segmented DAC may be visualized by assuming an input code of all zeroes. The first segment current I_0 is divided into 512 levels by the 9-bit multiplying DAC and fed to the output, $I_{\overline{OUT}}$. As the input code increases, a new segment current is selected for each 512 counts. The previous segment is fed to output I_{OUT} where the new step group is added to it, thus ensuring monotonicity independent of segment resistor values. All higher order segments feed $I_{\overline{OUT}}$.

At each segment endpoint, monotonicity is assured because no critical resistor tolerances are involved. For example, at the midpoint of the transfer characteristic, as shown in Figure 2, I4,0 is actually generated by the same segment resistor as $I_{3,511}$ and has been incremented by the remainder current of the 9-bit DAC.

In the segmented DAC, the precision of the eight main resistors determines linearity only. The influence of each of these resistors on linearity is four times lower than that of the MSB resistor in an R-2R DAC. Hence, assuming the same resistor tolerances for both, the linearity of the segmented approach would actually be higher than that of an R-2R design.

The step generator or 9-bit DAC is composed of a master and a slave ladder. The slave ladder generates the four LSBs from the remainder of the master ladder by active current splitting utilizing scaled emitters. This saves ladder resistors and greatly reduces the range of emitter scaling required in the 9-bit DAC. All current switches in the step generator are high-speed fully differential switches, capable of switching low currents at high speed. This allows the use of a binary-scaled network all the way to the LSB which saves power and simplifies the circuitry.

TABLE 1. RESISTOR SPECIFICATIONS

Ladder Type	No. of Resistors	Initial Matching Required for ±1 LSB DNL (%)	Tracking Required for ±1 LSB DNL (ppm/°C)		Tracking Required for ± LSB DNL (ppm/°C)
			0 Initial DNL	1/2 LSB Initial DNL	1/4 LSB Initial DNL
Straight R–2R	37	±.05	5	2.5	1.25
Segmented 3 bits – 9 bits	24	±.4	40	20	10

Diffused resistors have advantages over thin-film resistors beyond simple economy and bipolar process compatibility. The resistors are fabricated in single crystal rather than amorphous material, which gives them better long term stability and tracking and much higher moisture resistance. They are diffused at 1000°C and are, therefore, resistant to changes in value due to thermal and chemical causes. Also, no burn-in is required for stability. The contact resistance between aluminum and silicon is more predictable than between aluminum and an amorphous thin film, and no sandwich metals are required to enhance or protect the contact or limit alloying. The initial match between two diffused resistors is similar to that of thin film since both are defined by photomasks and chemical etching. Since the resistors are not trimmed or altered after fabrication, their tracking and long-term characteristics are not degraded.

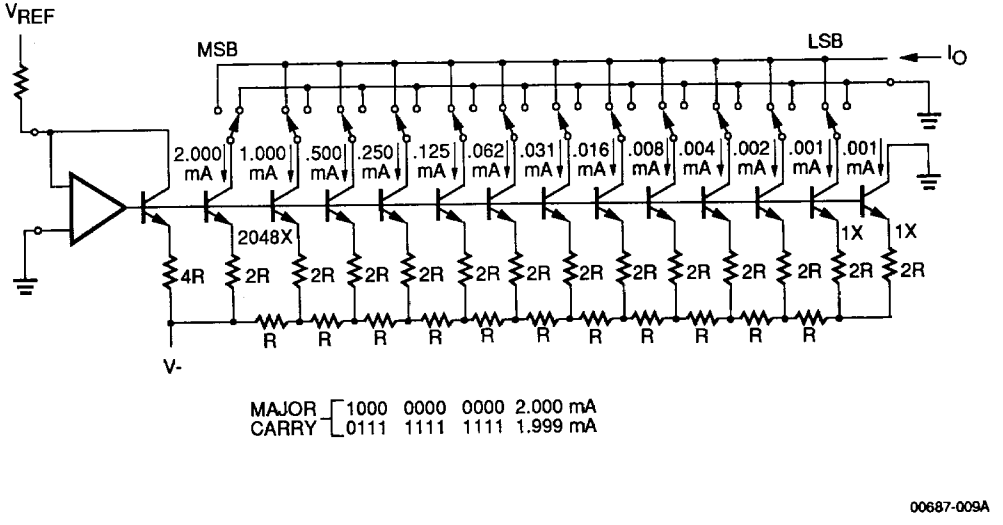


Figure 1. Traditional R-2R D/A Converter

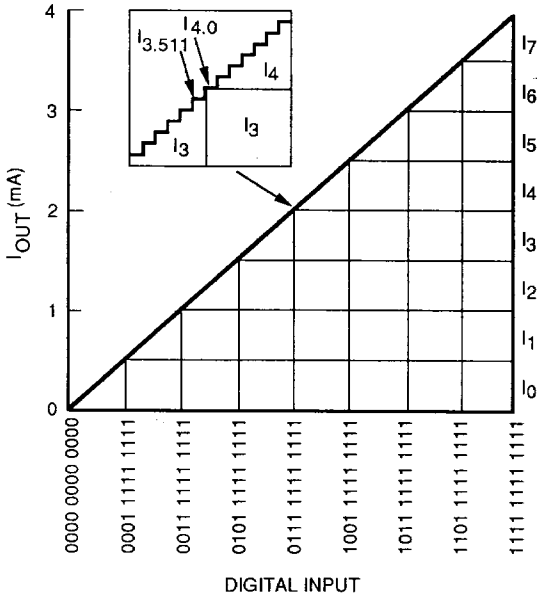


Figure 2. Transfer Characterisitc of Segmented Design

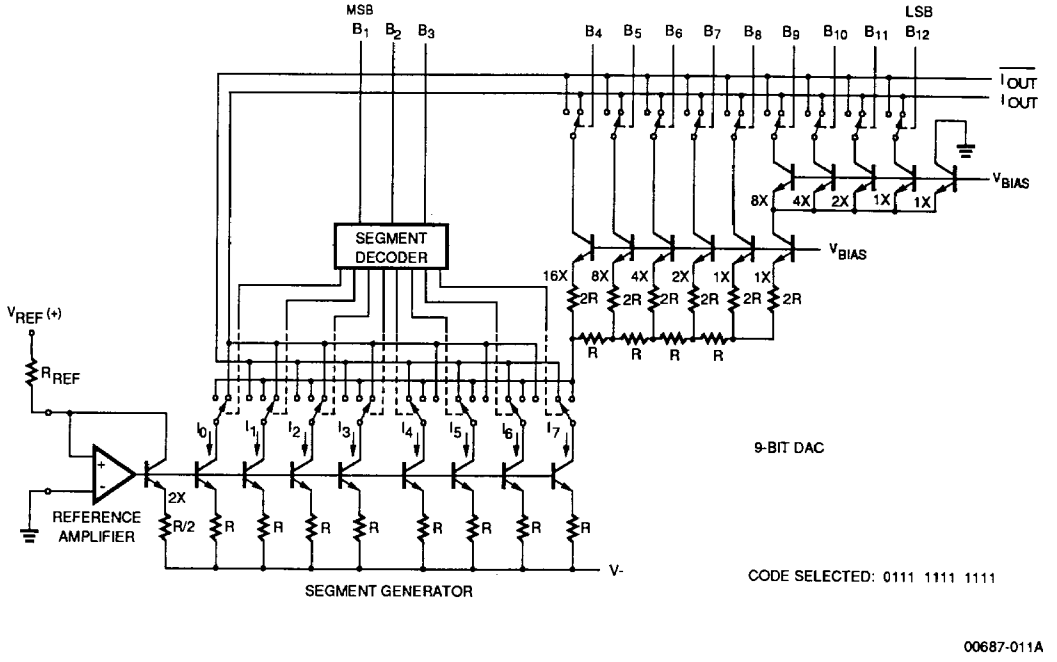


Figure 3. Segmented DAC Funcional Diagram Used in Am6012

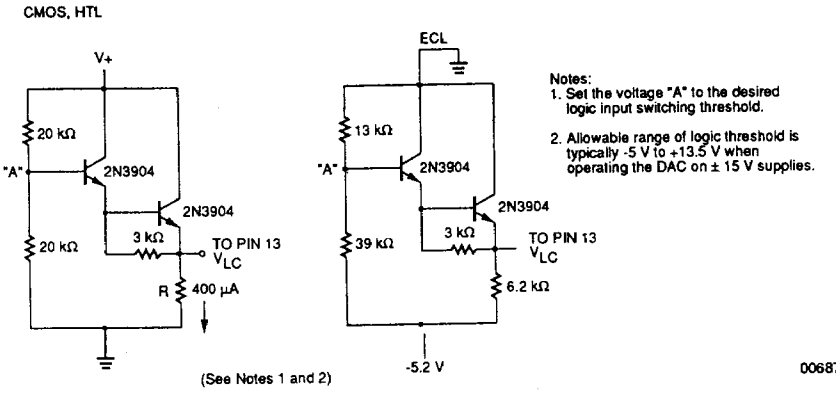
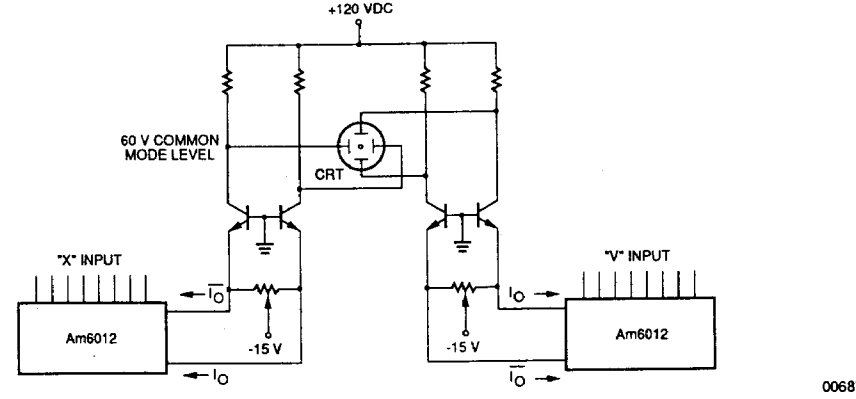


Figure 4. Interfacing Circuits for ECL, CMOS, HTL Logic Inputs



Notes:
1. Full differential drive lowers power supply voltage.
2. Eliminates inverting amplifiers and transformers.
3. Independent beam centering controls.

Figure 5. CRT Display Driver

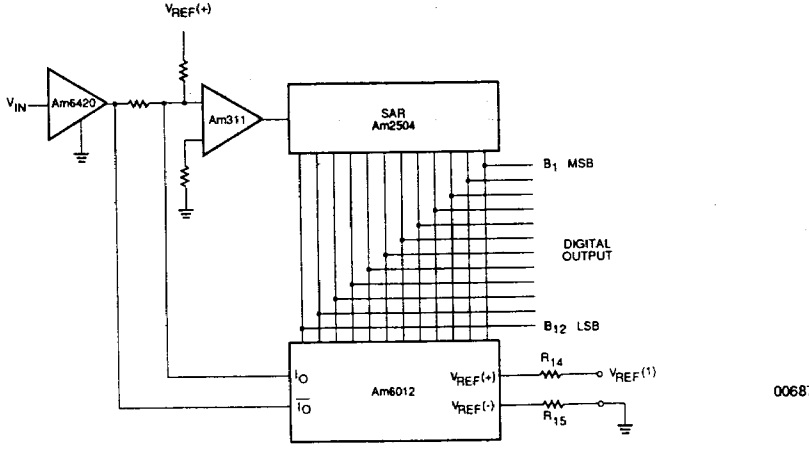
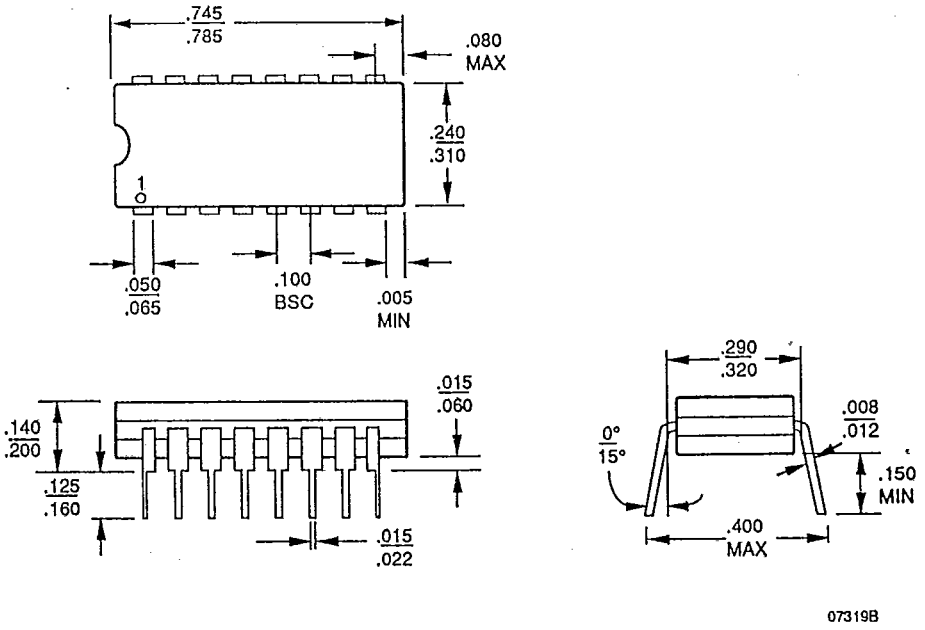


Figure 6. High-Speed 12-Bit A/D Converter

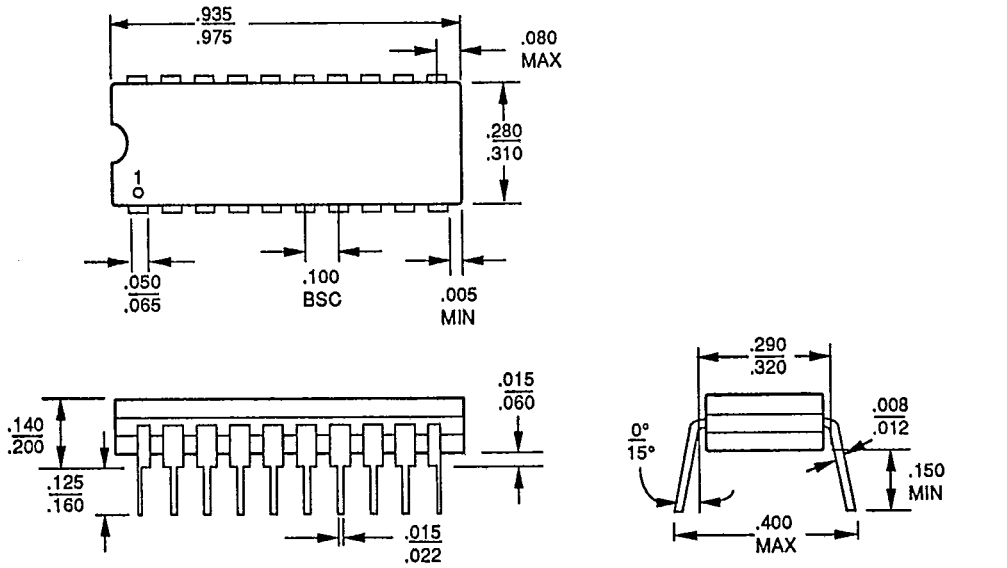
T-90-20

PHYSICAL DIMENSIONS
CD 016



07319B

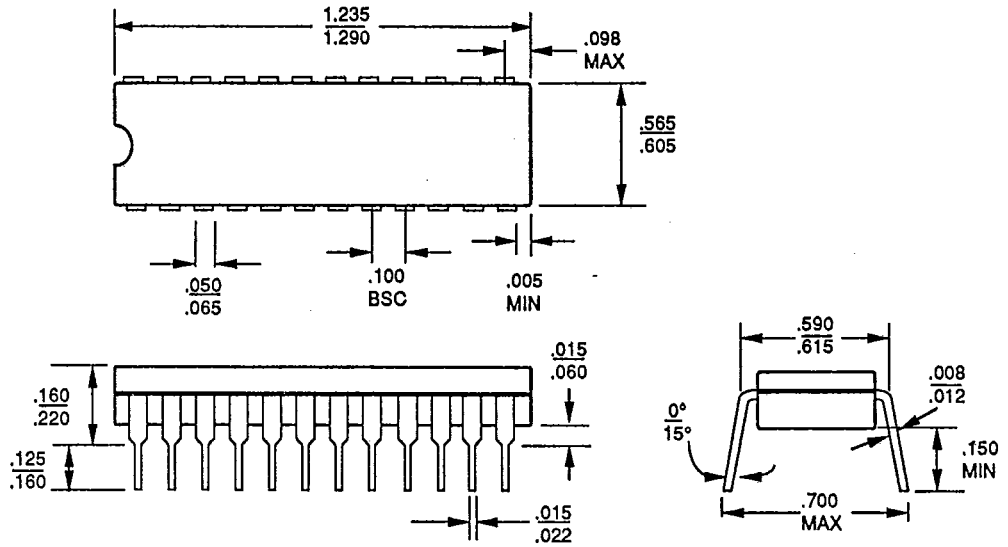
CD 020



03941-004C

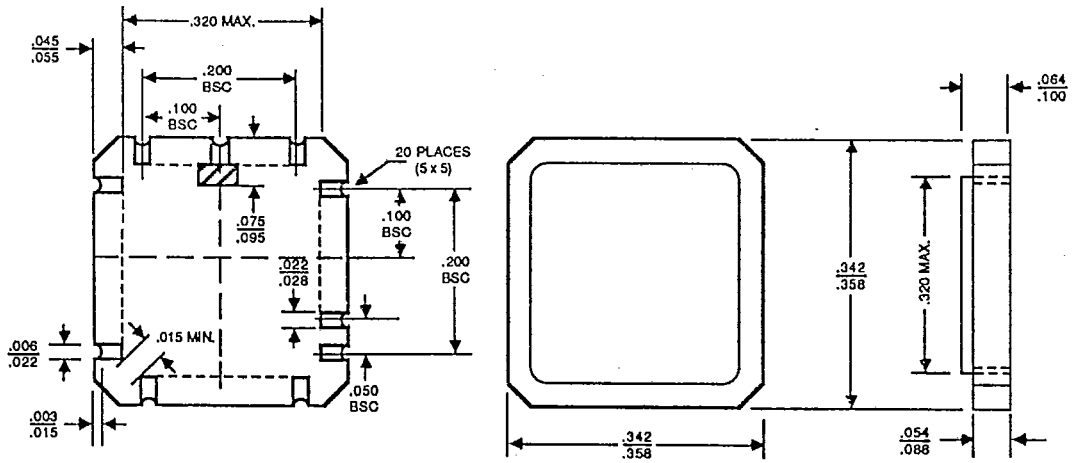
T-90-20

PHYSICAL DIMENSIONS (continued)
CD 024



03067-008A

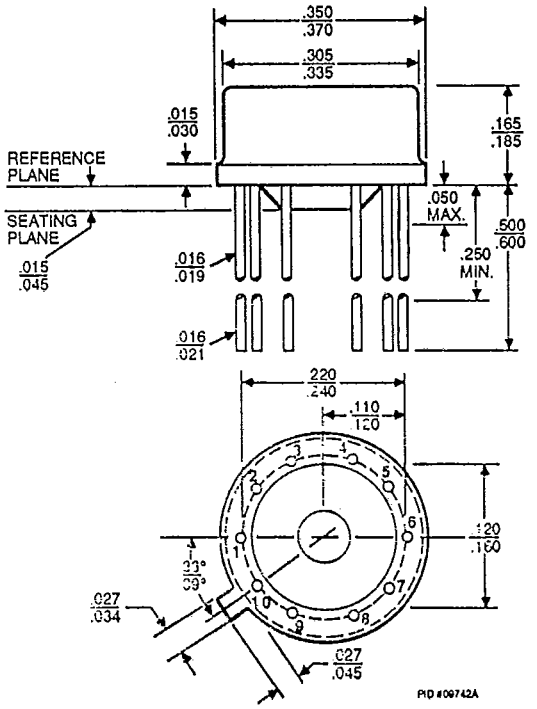
CL 020



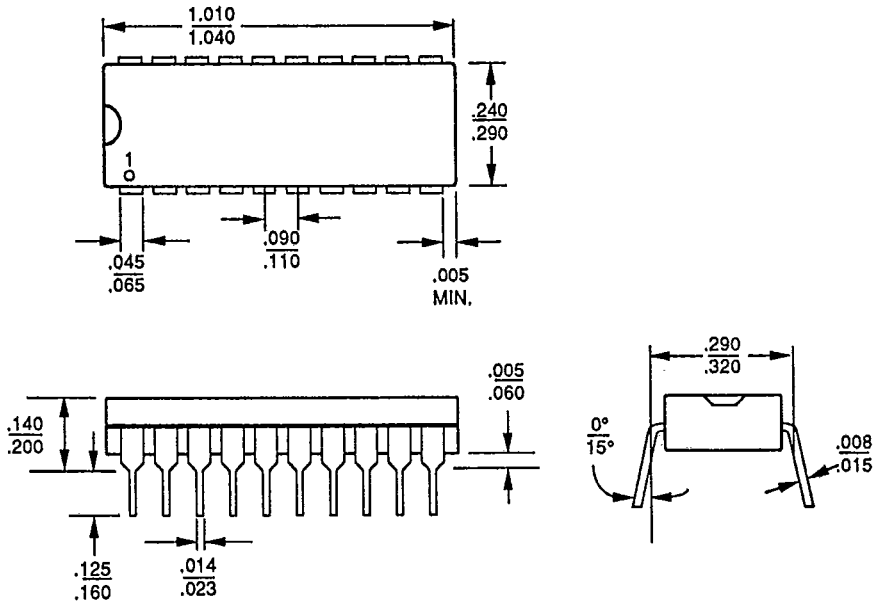
PID #07318C

PHYSICAL DIMENSIONS (continued)

MC 010



PD 020



03941-005C