Final

Am6685

Ultra-Fast Voltage Comparator

Advanced Micro Devices

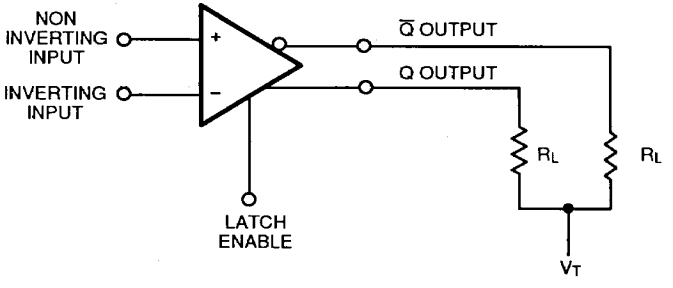
DISTINCTIVE CHARACTERISTICS

- 2.7 ns typical propagation delay
- Complementary ECL outputs
- 50-Ω line driving capability
- Built-in latch

GENERAL DESCRIPTION

The Am687 is an ultra-fast voltage comparator constructed on a single silicon chip with the advanced IMOX* process. It is pin-for-pin compatible with the Am685, and has improved speed performance. The circuit features very short propagation delays as well as excellent matching characteristics. The circuit has different analog inputs and complementary logic outputs compatible with most forms of ECL. The output current is capable of driving terminated 50-ohm transmission lines. The low-input offsets and short delays make this comparator especially suitable for high-speed precision analog-to-digital processing. A latch function is provided to allow the comparator to be used in a sample-hold mode. The latch input is intended to be driven from a standard ECL gate. If the Latch Enable input is HIGH, the comparator functions normally. When the Latch Enable is driven LOW, the comparator outputs are locked in their existing logical states. If the latch function is not used, the Latch Enable must be connected to ground.

BLOCK DIAGRAM



The outputs are open emitters, therefore external pulldown resistors are required. These resistors may be in the range of 50–200 Ω connected to –2.0 V, or 200–2000 Ω connected to –5.2 V.

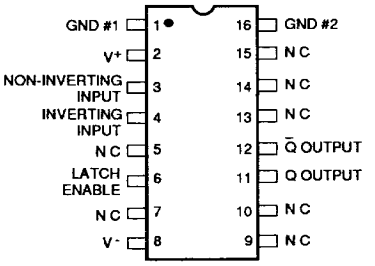
05975-001

*IMOX is a trademark of Advanced Micro Devices, Inc.

Publication # 05975 Rev. C Amendment /0
Issue Date: March 1989

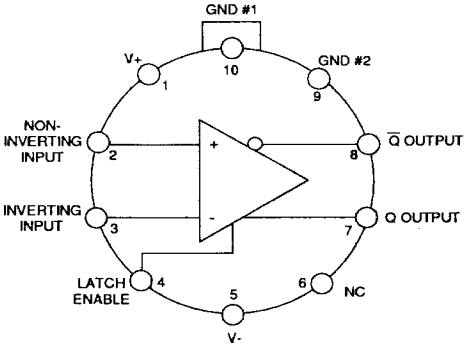
CONNECTION DIAGRAMS
Top View

DIP



05975-002

Metal Can



05975-003

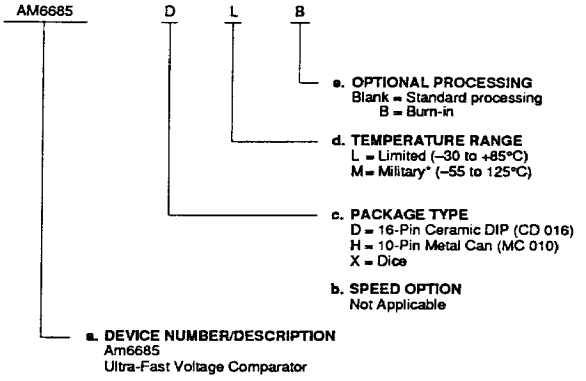
Note: Pin 1 is marked for orientation. On metal package, pin 5 is connected to case; on DIP, pin 8 is connected to case.

ORDERING INFORMATION

Standard Products

AMD standard products are available in several packages and operating ranges. The order number (Valid Combination) is formed by a combination of:

a. **Device Number**
b. **Speed Option** (if applicable)
c. **Package Type**
d. **Temperature Range**
e. **Optional Processing**



* Military or Limited Military temperature range products are "NPL" (Non-Compliant Products List) or Non-MIL-STD-883C compliant products only.

Valid Combinations

Valid Combinations	
AM6685	DL, DLB, HL, HLB, XL, XM

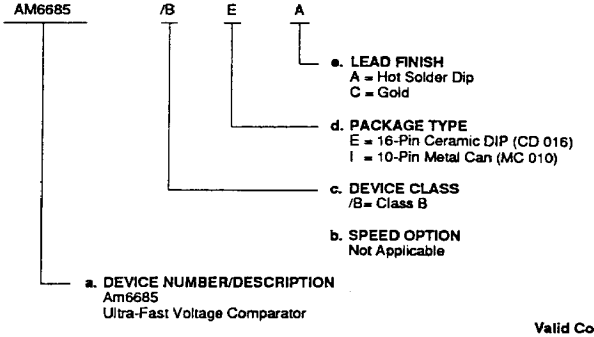
Valid Combinations list configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations, to check on newly released combinations, and to obtain additional data on AMD's standard military grade products.

MILITARY ORDERING INFORMATION

APL Products

AMD products for Aerospace and Defense applications are available in several packages and operating ranges. APL (Approved Products List) products are fully compliant with MIL-STD-883C requirements. The order number (Valid Combination) for APL products is formed by a combination of:

a. **Device Number**
b. **Speed Option** (if applicable)
c. **Device Class**
d. **Package Type**
e. **Lead Finish**



Valid Combinations

Valid Combinations	
AM6685	/BEA, /BIC

Valid Combinations list configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations or to check on newly released valid combinations.

Group A Tests

Group A tests consist of subgroups 1, 2, 3, 4, 5, 6, 9.

ABSOLUTE MAXIMUM RATINGS

Storage Temperature ..... –65 to +150°C
Positive Supply Voltage ..... +7 V
Negative Supply Voltage ..... –7 V
Input Voltage ..... ±4 V
Differential Input Voltage ..... ±6 V
Output Current ..... 30 mA
Power Dissipation (Note 1) ..... 350 mW
Lead Temperature (soldering, 60 s) ..... 300°C
Minimum Operating Voltage (V+ to V–) ..... 9.7 V

Stresses above those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to absolute maximum ratings for extended periods may affect device reliability.

OPERATING RANGES

Limited (L) Devices
Ambient Temperature (T_A) ..... –30 to +85°C

Military (M) Devices
Ambient Temperature (T_A) ..... –55 to +125°C

Operating ranges define those limits between which the functionality of the device is guaranteed.

DC CHARACTERISTICS over operating range unless otherwise specified (for APL Products, Group A, Subgroups 1, 2, 3, 4, 5, 6 are tested unless otherwise noted)

Parameter Symbol	Parameter Description	Test Conditions (Note 2)	LIMITED			MIL			Unit
			Min.	Typ.	Max.	Min.	Typ.	Max.	
V_{OS}	Input Offset Voltage	RS ≤ 100 Ω, T_A = 25°C	–2.0	0.3	+2.0	–2.0	0.3	+2.0	mV
		RS ≤ 100 Ω	–2.5		+2.5	–3.0		+3.0	
$\Delta V_{OS}/\Delta T$	Average Tempco of V_{OS} (Note 3)	RS ≤ 100 Ω	–15	3	+15	–15	3	+15	µV/°C
I_{OS}	Input Offset Current	25°C ≤ T_A ≤ T_A (Max.)	–1.5	0.2	+1.5	–1.5	0.2	+1.5	µA
		T_A = T_A (Min.)	–2.5	0.3	+2.5	–3.0	0.3	+3.0	
I_B	Input Bias Current	25°C ≤ T_A ≤ T_A (Max.)		4	15		4	15	µA
		T_A = T_A (Min.)		7	25		8	30	
V_{IN}	Input Voltage Range		–3.3		+3.3	–3.3		+3.3	V
CMRR	Common Mode Rejection Ratio	RS ≤ 100 Ω, –3.3 V ≤ V_{CM} ≤ 3.3 V	80			80			dB
SVRR	Supply Voltage Rejection Ratio	RS ≤ 100 Ω, ΔV_S = ±5%	60			60			dB
V_{OH}	Output HIGH Voltage	T_A = 25°C	–0.96	–0.885	–0.81	–0.96	–0.885	–0.81	V
		T_A = T_A (Min.)	–1.06	–0.975	–0.89	–1.1	–1.010	–0.92	
		T_A = T_A (Max.)	–0.89	–0.795	–0.70	–0.85	–0.735	–0.62	
V_{OL}	Output LOW Voltage	T_A = 25°C	–1.85	–1.750	–1.65	–1.85	–1.750	–1.65	V
		T_A = T_A (Min.)	–1.89	–1.783	–1.675	–1.91	–1.800	–1.69	
		T_A = T_A (Max.)	–1.825	–1.725	–1.625	–1.81	–1.693	–1.575	

Table continued on next page.

DC CHARACTERISTICS (Cont'd.)

Parameter Symbol	Parameter Description	Test Conditions (Note 2)	LIMITED			MIL			Unit
			Min.	Typ.	Max.	Min.	Typ.	Max.	
I+	Positive Supply Current			12	22		12	22	mA
I–	Negative Supply Current			10	18		10	18	mA
P_{DISS}	Power Dissipation (Note 1)			153	254		153	254	mW

Notes: See notes following Switching Characteristics.

DEFINITION OF TERMS

V_{OS} Input Offset Voltage
That voltage which must be applied between the two input terminals through two equal resistances to obtain zero voltage between the two outputs.

$\Delta V_{OS}/\Delta T$ Average Temperature Coefficient of Input Offset Voltage
The ratio of the change in input offset voltage over the operating temperature range to the temperature range.

I_{OS} Input Offset Current
The difference between the currents into the two input terminals when there is zero voltage between the two outputs.

I_B Input Bias Current
The average of the two input currents.

R_{IN} Input Resistance
The resistance looking into either input terminal with the other grounded.

C_{IN} Input Capacitance
The capacitance looking into either input terminal with the other grounded.

V_{CM} Input Voltage Range
The range of voltages on the input terminals for which the offset and propagation delay specifications apply.

CMRR Common Mode Rejection Ratio
The ratio of the input voltage range to the peak-to-peak change in input offset voltage over this range.

SVRR Supply Voltage Rejection Ratio
The ratio of the change in input offset voltage to the change in power supply voltages producing it.

V_{OH} Output HIGH Voltage
The logic-HIGH output voltage with an external pull-down resistor returned to a negative supply.

V_{OL} Output LOW Voltage
The logic-LOW output voltage with an external pull-down resistor returned to a negative supply.

I+ Positive Supply Current
The current required from the positive supply to operate the comparator.

I- Negative Supply Current
The current required from the negative supply to operate the comparator.

P_{DISS} Power Dissipation
The power dissipated by the comparator with both outputs terminated in 50 Ω to –2.0 V.

SWITCHING CHARACTERISTICS over operating range unless otherwise specified (for APL Products, Group A, Subgroup 9 is tested unless otherwise noted) (V_{IN} = 100 mV, $V_{OVERDRIVE}$ = 10 mV)

Parameter Symbol	Parameter Description	Test Conditions (Note 2)	LIMITED			MIL			Unit
			Min.	Typ.	Max.	Min.	Typ.	Max.	
t_{PD+}, t_{PD-}	Propagation Delay	T_A = 25°C (Note 3)	2.0	2.7	4.0	2.0	2.7	4.0	ns
t_{PD+}(E), t_{PD-}(E)	Latch Enable to Output (HIGH or LOW)	T_A = 25°C (Note 4)		2.3			2.3		ns
t_S	Min. Latch Setup Time	T_A = 25°C (Note 4)		1.0			1.0		ns
t_H	Min. Latch Hold Time	T_A = 25°C (Note 4)		–0.5			–0.5		ns

Notes:
1. For the metal can package, derate at 6.8 mW/°C for operation at ambient temperatures above +100°C; for the dual in-line package, derate at 9 mW/°C for operation at ambient temperatures above +105°C.
2. Unless otherwise specified V+ = 6.0 V, V– = –5.2 V, V_T = 2.0 V, and R_L = 50 Ω, all switching characteristics are for a 100-mV input step with 10 mV overdrive. The specification given for V_{OS}, I_{OS}, I_B, CMRR, SVRR, t_{PD+}, and t_{PD-} apply for ±5% supply voltages. The Am6685 is designed to meet the specifications given in the table after thermal equilibrium has been established with a transverse air flow of 500 linear feet per minute or greater.
3. Not 100% tested. Group A sample only.
4. Not tested in production. These tests are supported by device characterization data.

DEFINITION OF TERMS

(refer to Switching Waveforms)

t_{PD+} Input to Output HIGH Delay
The propagation delay measured from the time the input signal crosses the input offset voltage to the 50% point of an output LOW-to-HIGH transition.

t_{PD-} Input to Output LOW Delay
The propagation delay measured from the time the input signal crosses the input offset voltage to the 50% point of an output HIGH-to-LOW transition.

t_{PD+}(E) Latch Enable to Output HIGH Delay
The propagation delay measured from the 50% point of the Latch Enable signal LOW-to-HIGH transition to the 50% point of an output LOW-to-HIGH transition.

t_{PD-}(E) Latch Enable to Output LOW Delay
The propagation delay measured from the 50% point of the Latch Enable signal LOW-to-HIGH transition to the 50% point of an output HIGH-to-LOW transition.

t_S Minimum Setup Time
The minimum time before the negative transition of the Latch Enable signal that an input signal change must be present in order to be acquired and held at the outputs.

t_H Minimum Hold Time
The minimum time after the negative transition of the Latch Enable signal that the input signal must remain unchanged in order to be acquired and held at the outputs.

Other Symbols

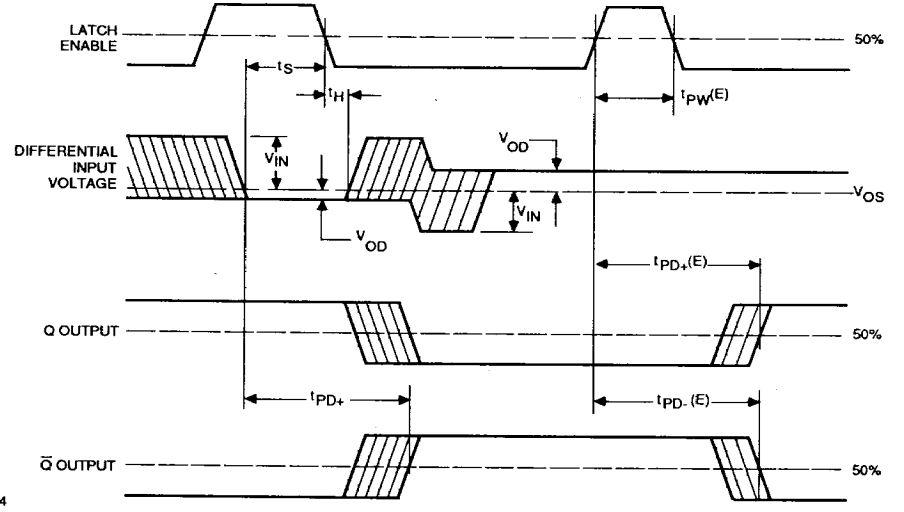
T_A = Ambient temperature
R_S = Input source resistance
V_S = Supply voltages
V+ = Positive supply voltage
V– = Negative supply voltage
V_T = Output load terminating voltage
R_L = Output load resistance
V_{IN} = Input pulse amplitude
V_{OD} = Input overdrive
f = Frequency

SWITCHING WAVEFORMS

KEY TO SWITCHING WAVEFORMS

WAVEFORM	INPUTS	OUTPUTS
	MUST BE STEADY	WILL BE STEADY
	MAY CHANGE FROM H TO L	WILL BE CHANGING FROM H TO L
	MAY CHANGE FROM L TO H	WILL BE CHANGING FROM L TO H
	DON'T CARE, ANY CHANGE PERMITTED	CHANGING, STATE UNKNOWN

KS000010

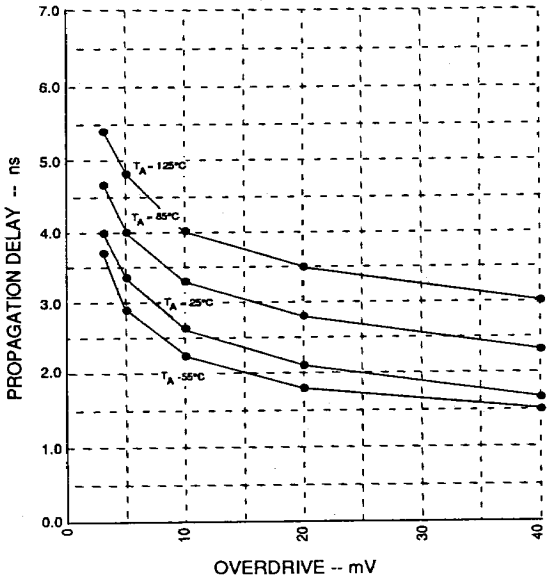


05975-004

The setup and hold times are a measure of the time required for an input signal to propagate through the first stage of the comparator to reach the latching circuitry. Input signal changes occurring before t_s will be detected and held; those occurring after t_H will not be detected. Changes between t_s and t_H may or may not be detected.

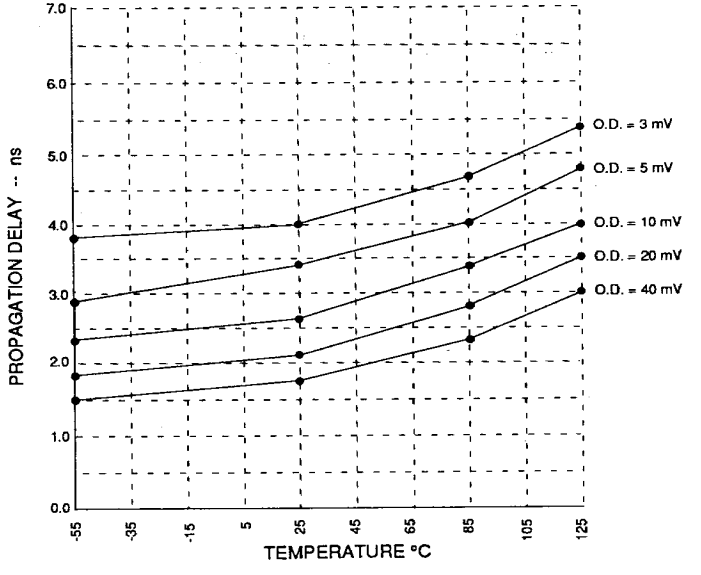
TYPICAL PERFORMANCE CURVES

Propagation Delay vs Overdrive



05975-005

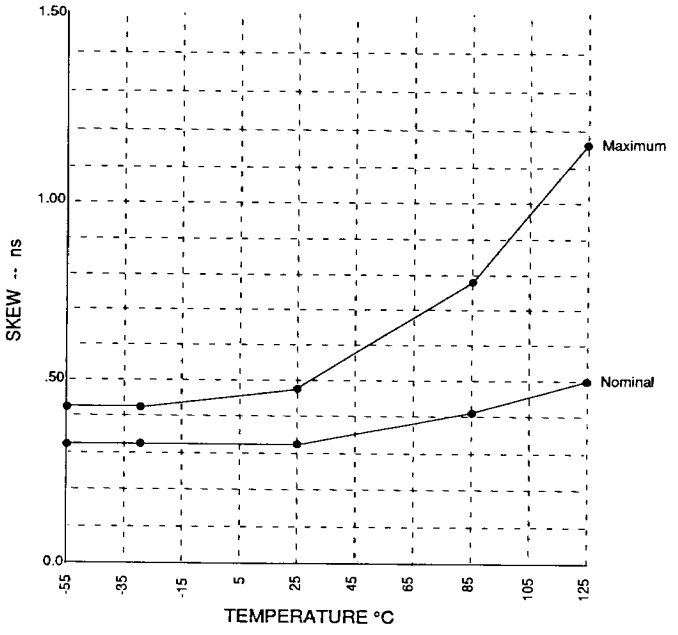
Propagation Delays vs Temperature also Overdrive



05975-006

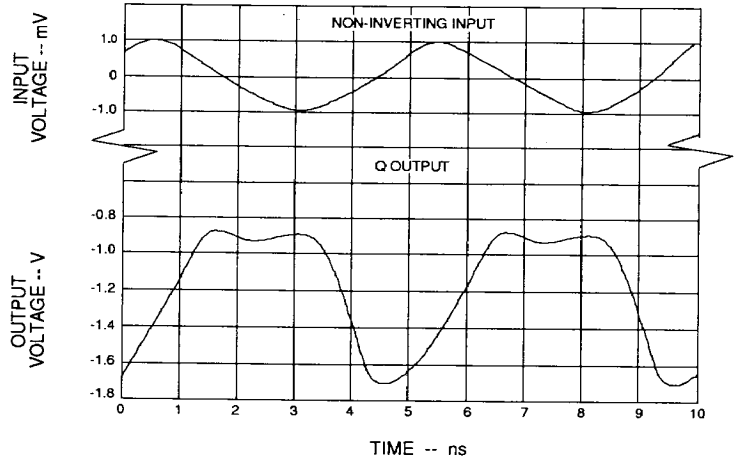
TYPICAL PERFORMANCE CURVES (Cont'd.)

Skew vs Temperature



05975-007

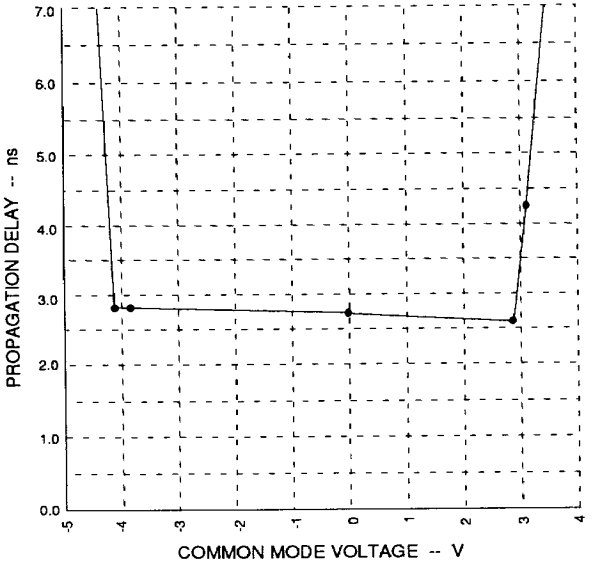
Response to 200-MHz Sine Wave



05975-008

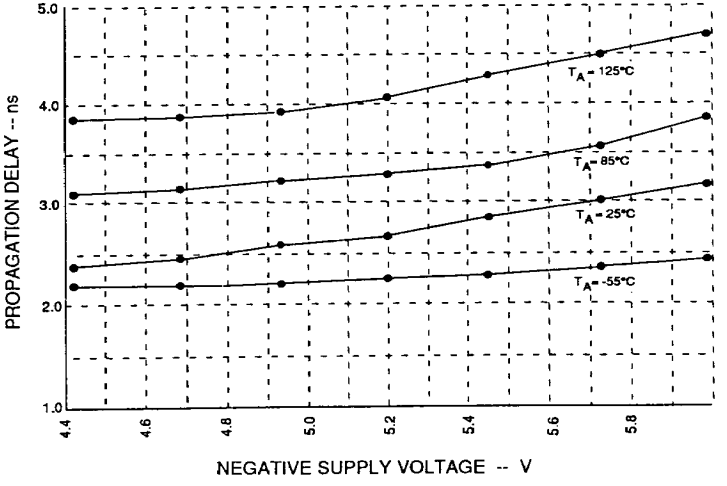
TYPICAL PERFORMANCE CURVES (Cont'd.)

Propagation Delay vs VCM



05975-009

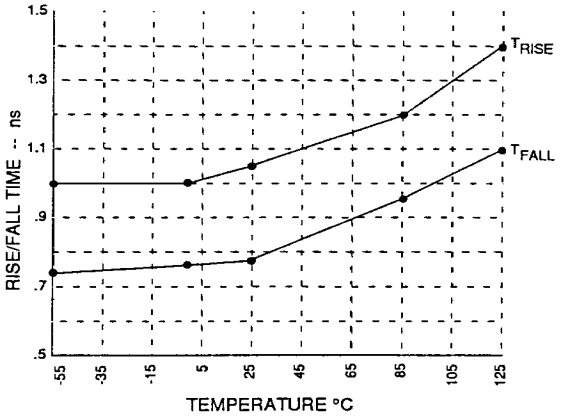
Propagation Delay vs V–



05975-010

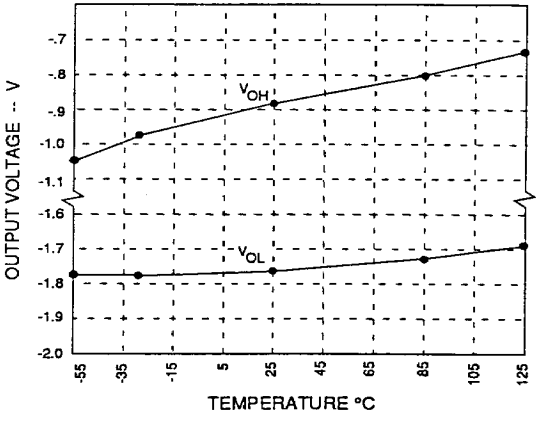
TYPICAL PERFORMANCE CURVES (Cont'd.)

Output Rise and Fall vs Temperature



05975-011

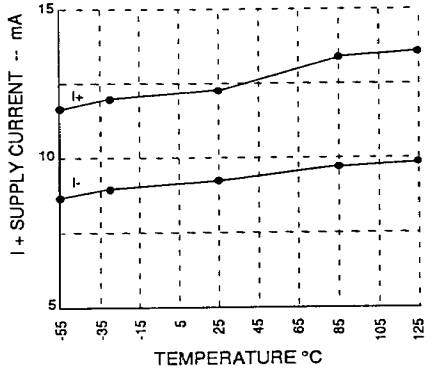
Output Voltage vs Temperature



05975-012

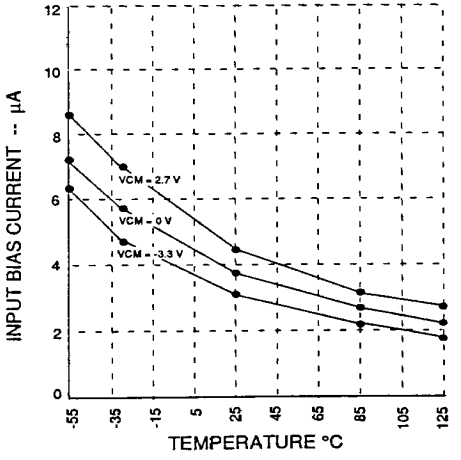
TYPICAL PERFORMANCE CURVES (Cont'd.)

Supply Currents vs Temperature



05975-013

Input Bias Current vs Temperature



05975-014