Am7901A/B

Subscriber Line Audio-Processing Circuit
WORLD-CHIP™
PRELIMINARY

DISTINCTIVE CHARACTERISTICS

- Combination CODEC and Filter
- No trimming or adjustments required
- Uses digital signal processing
- Six user-programmable digital filters
- Dynamic Time Slot assignment
- Only 2 external components (non-precision)
- Dual PCM ports
- 4.096 MHz, 64-channel expanded mode operation
- Built-in test modes
- Microprocessor-compatible Serial Interface
- Control interface to SLIC
- Low standby power
- Selectable linear, μ-law (Am7901A) or μ-law, A-law (Am7901B)

GENERAL DESCRIPTION

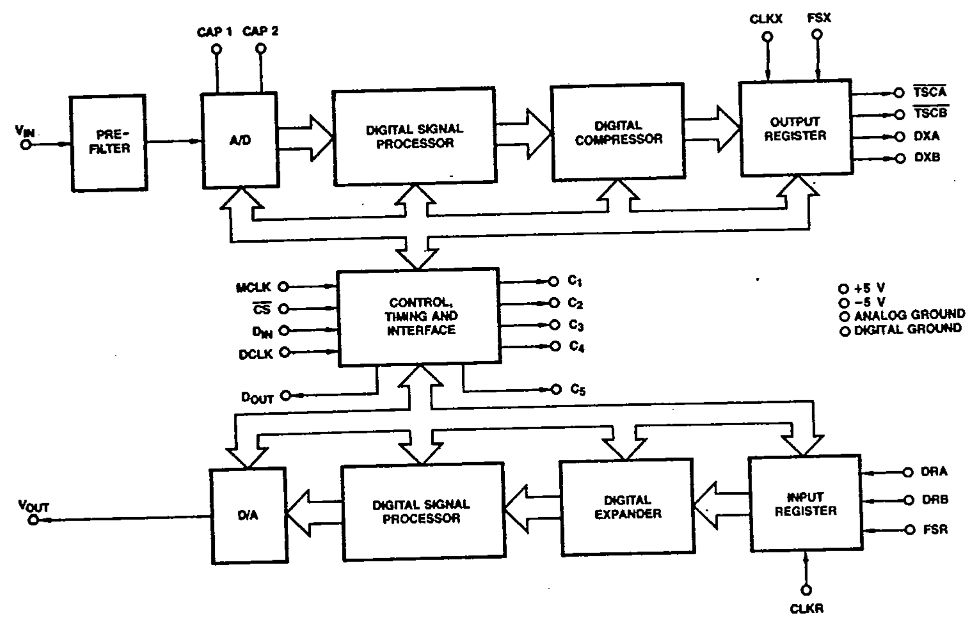
The Subscriber Line Audio-Processing Circuit (SLAC) performs the codec and filtering functions necessary in digital voice switching machines. In this application, the SLAC processes voiceband analog signals into Pulse-Code Modulated (PCM) outputs and processes PCM inputs into analog outputs. The SLAC's performance is compatible with applicable AT&T and CCITT specifications. The device consists of three main sections: transmit processor, receive processor, and control logic.

The transmit section contains an anti-aliasing filter, an interpolative A/D converter and a digital signal processor. The analog signals received are converted and digitally processed to generate either 16-bit linear or 8-bit μ-law codes (Am7901A), or 8-bit μ-law or A-law codes (Am7901B). Either one of two output ports may be selected for PCM data transmission.

The receive section contains a digital signal processor and a D/A converter. Either 16-bit linear or 8-bit μ-law codes (Am7901A), or 8-bit μ-law or A-law codes (Am7901B) are received, processed and converted to analog signals. Either one of two input ports may be selected for reception of PCM data.

The control I/O provides a microprocessor-compatible serial interface and allows the user bi-directional access to many programmable features and the capability to completely control the operation of the device via a comprehensive set of 32 commands.

BLOCK DIAGRAM



BD005161

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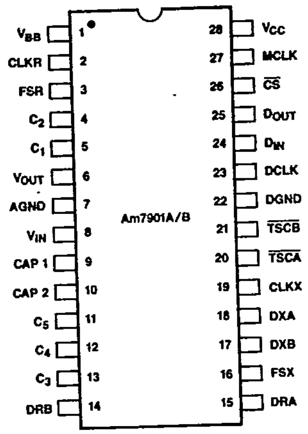
Order # 01520D

Advanced Micro Devices

September 1985

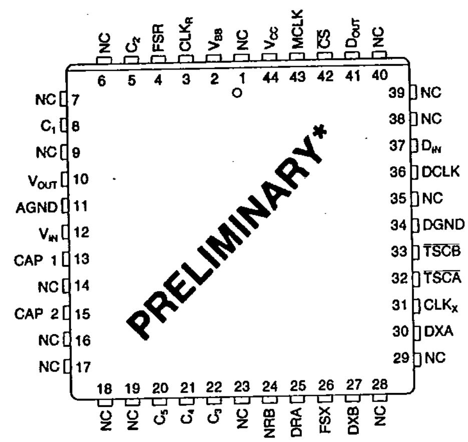
CONNECTION DIAGRAM
Top View

DIPs



CD005871

PLCC



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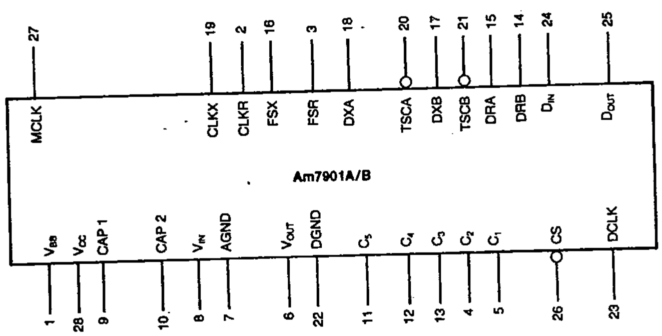
LOGIC SYMBOL
DIPs



LS001891

ORDERING INFORMATION

AMD products are available in several packages and operating ranges. The order number is formed by a combination of the following: Device number, speed option (if applicable), package type, operating range and screening option (if desired).

Am7901A D C T

- T — Optional Processing
  Blank = Standard Processing
- C — Temperature Range
  C = Commercial (0°C to +70°C)
- D — Package Type
  D = 28-Pin Ceramic DIP (CD 028)
  P = 28-Pin Plastic DIP (PD 028)
  J = 44-Pin Plastic Leaded Chip Carrier (PL 044*)
- Am7901A — AMD Device Type
  Am7901A (Linear, μ-Law)
  Am7901B (A-Law, μ-Law)
  Subscriber Line Audio-Processing Circuit (SLAC) WORLD-CHIP

Valid Combinations	
Am7901A	DC, PC*, JC*
Am7901B	DC, PC*, JC*

Valid Combinations

Consult the local AMD sales office to confirm availability of specific valid combinations, to check on newly released valid combinations, and to obtain additional data on AMD's standard military grade products.

*Preliminary. Subject to change.

PIN DESCRIPTION

V_{CC}: +5-V Power Supply

V_{BB}: −5-V Power Supply

DGND: Digital Ground

AGND: Analog Ground

Analog Input (V_{IN}) The analog input is applied to the transmit path of the SLAC. The signal is sampled, digitally processed and encoded for the PCM output.

Analog Output (V_{OUT}) The received-PCM data is digitally processed and converted to an analog signal at the V_{OUT} pin.

CAP 1, CAP 2 An external series resistor and capacitor are connected to these pins. These components are part of the integrator in the A/D converter. The recommended values of these non-precision components are 1 kΩ ±5% and 2000 pF ±20%.

Master Clock **(MCLK)** The Master Clock must be a 2.048 MHz ±100 ppm clock input. MCLK is used by the digital signal processors and is not dependent on the PCM input and output clocks.

PCM Outputs **(DXA, DXB)** The transmit-PCM data is serially fed out to either the DXA or the DXB port. The port selection is under user program control. For μ-law and A-law, 8 bits are transmitted and for linear code, 16 bits are transmitted. The output is available every 125 μs and the data is shifted out in 8/16-bit bursts at the CLKX rate. DXA and DXB are high impedance in between bursts and also in the stand-by mode.

Time Slot Control **($\overline{TSCA}$, $\overline{TSCB}$)** The Time Slot Control outputs are open drain outputs and are normally HIGH. $\overline{TSCA}$ is LOW when PCM data is present on the DXA output and $\overline{TSCB}$ is LOW when PCM data is present on the DXB output.

PCM Inputs **(DRA, DRB)** The receive-PCM data is serially received from either the DRA or the DRB port. The port selection is under user program control. For μ-law and A-law, 8 bits are received and for linear code, 16 bits are received. The data is received in 8 or 16-bit bursts every 125 μs at the CLKR rate.

Frame Sync **(FSX, FSR)** The Frame Sync pulse is an 8-kHz signal which identifies the beginning of a frame. The SLAC references individual time slots with respect to the Frame Sync pulse. FSX is the transmit-PCM Frame Sync and FSR is the receive-PCM Frame Sync. The FSX pulse must not be longer than 8 clock periods when companded code is used, and 16 clock periods when linear code is use.

PCM Clocks **(CLKX, CLKR)** The PCM Clocks determine the rate at which PCM data is serially shifted in to or out of the PCM ports. The maximum clock frequency is 4.096 MHz and the minimum clock frequency is 128 kHz. CLKX determines the rate at which PCM data is transmitted. CLKR determines the rate at which PCM data is received.

Chip Select **($\overline{CS}$)** The Chip Select input enables the device to either input or output control data.

Data Input **(D_{IN})** Control data is serially written via the Data Input port. The input rate is determined by the Data Clock.

Data Output **(D_{OUT})** Control data is serially read via the Data Output port. The output rate is determined by the Data Clock. D_{OUT} is HIGH-impedance when control data output is completed and $\overline{CS}$ is HIGH.

Data Clock **(DCLK)** The Data Clock shifts control data either in to or out of the SLAC. The maximum clock rate is 2.048 MHz.

Latched Outputs **(C_1-C_5)** The serial interface may be used to write data to a register whose outputs are brought out to C_1-C_5. These 5 lines are TTL-compatible and may be used to control the operation of a SLIC or any other device associated with the subscriber line.

FUNCTIONAL DESCRIPTION

Device Operation

General

The Am7901A/B performs the codec and filtering functions associated with the 4-wire section of the subscriber line circuitry in a digital switch. When used with the Am7950/7953 Subscriber Line Interface Circuit (SLIC), the pair provide a complete solution to the BORSCHT functions (Figure 1).

The SLAC contains auto-zeroed A/D and D/A converters. A microprocessor-compatible interface is provided to program the device into a variety of modes. These operating modes include, but are not limited to, companded or linear-code operation, dynamic time-slot assignment, and PCM-port selection..

The SLAC samples the analog signal at the V_{IN} pin and digitally processes it to produce either a linear or companded PCM code at the DXA or DXB output (Figure 2). Conversely, it receives either a linear or companded PCM code at the DRA or DRB input and digitally processes it to produce an analog output at the V_{OUT} pin. The processing is accomplished at the frame rate (8 kHz), and the digital output/input is available for transmission/reception every 125 μs.

Transmit Signal Processor

In the transmit path (Figure 3), the analog signal is converted, filtered, compressed, and made available for output.

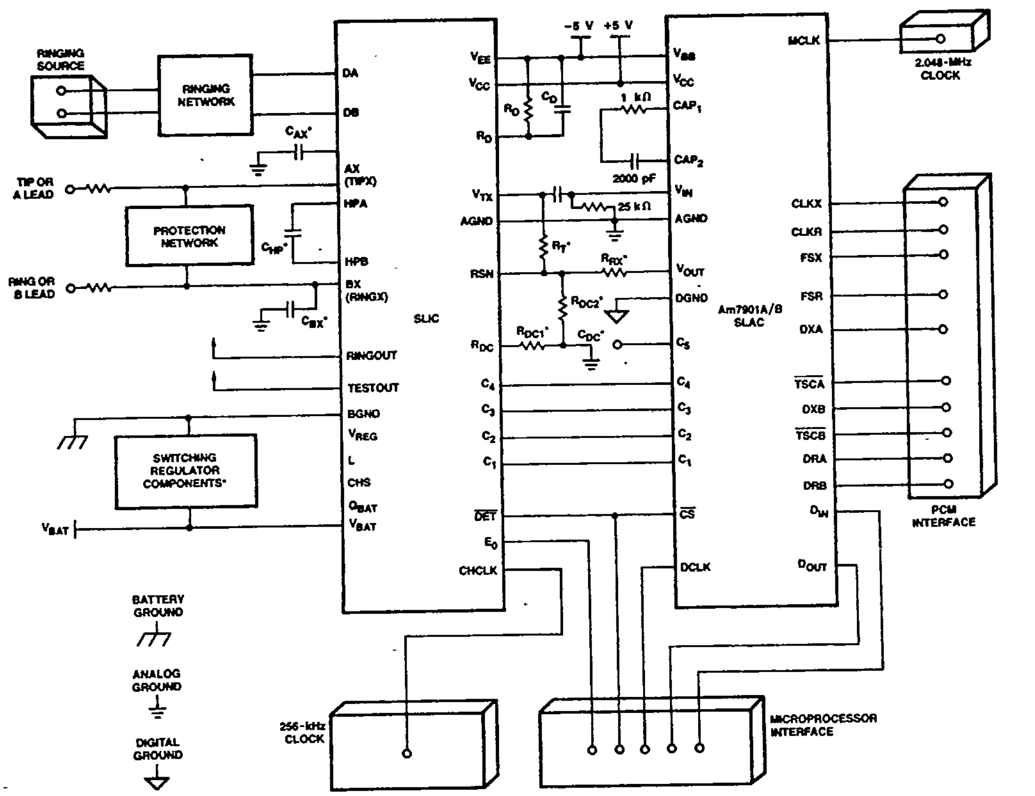
The prefilter is an integrated anti-aliasing filter which prevents signals near the sample rate from folding back into the voiceband during decimation. The A/D is designed to have a wide dynamic range and excellent signal-to-noise performance. It uses a modified sigma delta loop with a D/A converter to track the input signal at a 512-kHz sampling rate.

The Signal Processor contains an ALU, RAM, ROM and control logic to implement the filter sections. The B, X and GX blocks shown in Figure 3 are user-programmable filter sections and their coefficients are stored in the Coefficient RAM. These filters may be made transparent when not required in a system. The digital compressor may be bypassed when linear-code operation is desired.

The decimator reduces the high input sample rate. The X filter is a 4-tap Finite Impulse Response (FIR) section and is part of the frequency response correction network. The GX filter allows the user to program up to 12-dB gain in 0.1-dB steps in the transmit path. The B filter has 8 taps and operates on samples input from the Receive Signal Processor in order to provide trans-hybrid balancing in the loop. The low-pass filter limits the output bandwidth to meet the transmission requirements. The high-pass filter rejects 15-Hz and 50/60-Hz frequencies, and may be disabled during idle periods to allow low-frequency leakage testing on the 2-wire line.

Transmit PCM Interface

The Transmit PCM Interface receives either a 16-bit linear code (for linear operation) or an 8-bit compressed code (for μ-law and A-law operation) from the digital compressor. This code is loaded into the output register. The Transmit PCM Interface logic (Figure 4) controls the transmission of data onto the PCM highway through the output port-selection circuitry and the Time Slot Control block.



*Component values are user-programmable. Refer to SLIC product specification.

Figure 1. Single-Channel Subscriber Line System

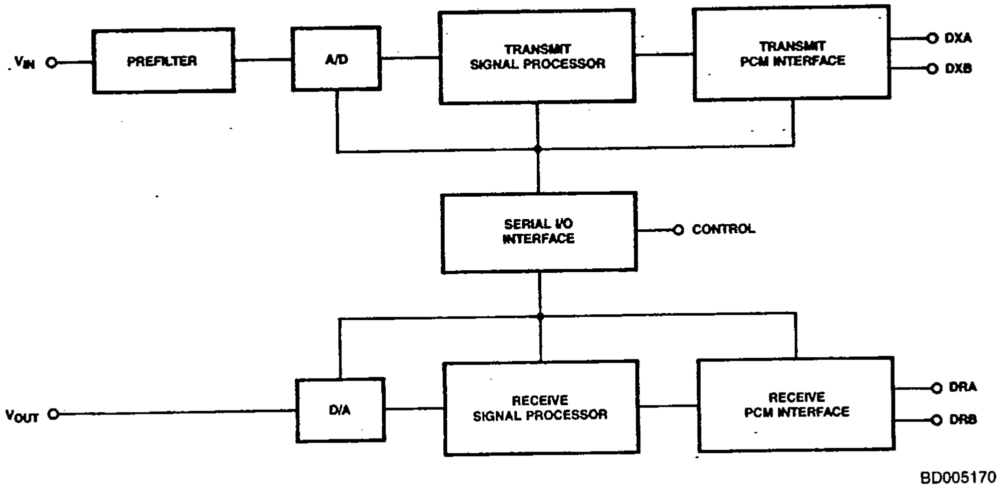
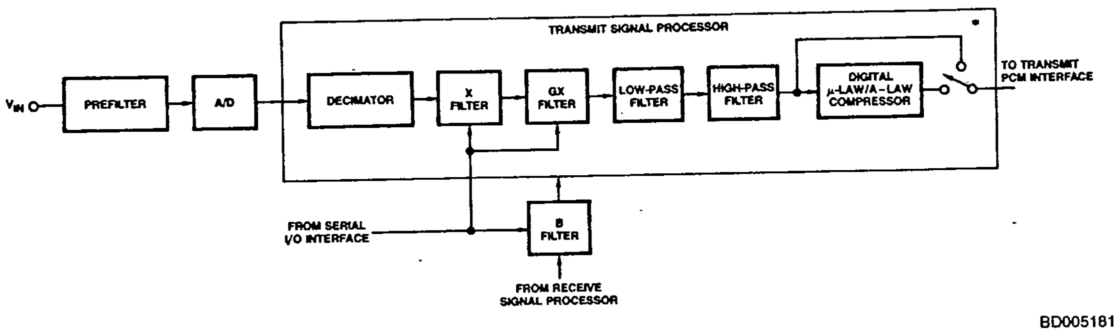


Figure 2. SLAC Block Diagram



*For Am7901B, the Digital Compressor cannot be bypassed.

Figure 3. Transmit Signal Processor

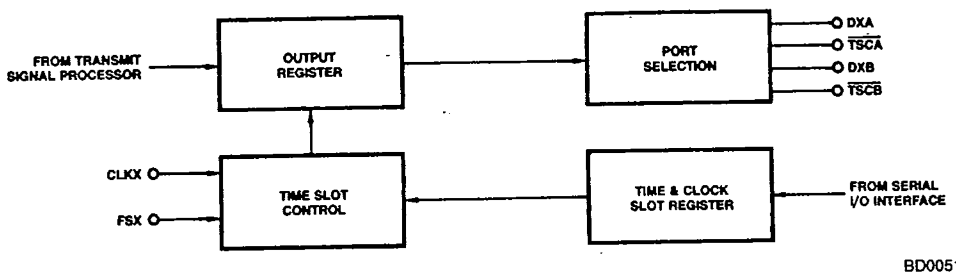


Figure 4. Transmit PCM Interface

The Frame Sync (FSX) pulse identifies the beginning of a Transmit frame and all channels (time slots) are referenced to it. The logic contains user-programmable Transmit Time Slot and Transmit Clock Slot registers. The Time Slot register is normally 5 bits wide and allows up to 32 8-bit channels or 16 16-bit channels (using CLKX = 2.048 MHz) in each frame. But in the expanded mode, 6 bits may be programmed to give 32 16-bit channels or 64 8-bit channels (using CLKX = 4.096 MHz) in each frame. The expanded mode bit becomes the sixth bit of the Time Slot register. If this bit is low, one of channels 0 to 31 is selected and if it is high, one of channels 32 to 64 is selected. This feature allows any combination of channel assignments and clock frequencies (over a range of 128 kHz to 4.096 MHz) in a system. For μ-law and A-law operation, 8 bits/channel are output and for linear code operation, 16 bits/channel are output. The data is transmitted Most Significant Bit (MSB) first. The Clock Slot register is 3 bits wide and may be programmed to offset the Time Slot assignment by 0 to 7 CLKX periods to eliminate any clock skew in the system (Figure 5).

In the Am7901A/B, the PCM data may be user-programmed to be output onto one of two ports, DXA or DXB. Correspondingly, either $\overline{TSCA}$ or $\overline{TSCB}$ is also low.

Receive PCM Interface

The Receive PCM Interface logic (Figure 7) controls the reception of data from the PCM highway and transfers it for expansion (μ-law or A-law) to the Receive Signal Processor. The operation of this interface is identical to the Transmit section.

The Frame Sync (FSR) pulse identifies the beginning of a Receive frame and all channels (time slots) are referenced to it. The logic contains user-programmable Receive Time Slot and Receive Clock Slot registers. The Time Slot register is normally 5 bits wide and allows up to 32 8-bit channels (using CLKR = 2.048 MHz) in each frame. But in the expanded mode, 6 bits may be programmed to give 32 16-bit channels or 64 8-bit channels (using CLKR = 4.096 MHz) in each frame. The expanded mode bit becomes the sixth bit of the Time Slot register. If this bit is low, one of channels 0 to 31 is selected and if it is high, one of channels 32 to 64 is selected. This feature allows any combination of clock frequencies (over a range of 128 kHz to 4.096 MHz) and channel assignments in a system. For μ-law and A-law operation, 8 bits/channel are input and for linear code, 16 bits/channel are input. The MSB of the code must be received first. The Clock Slot register is 3 bits wide and may be programmed to offset the Time Slot assignment by 0 to 7 CLKR periods to eliminate any clock skews in the system (Figure 8).

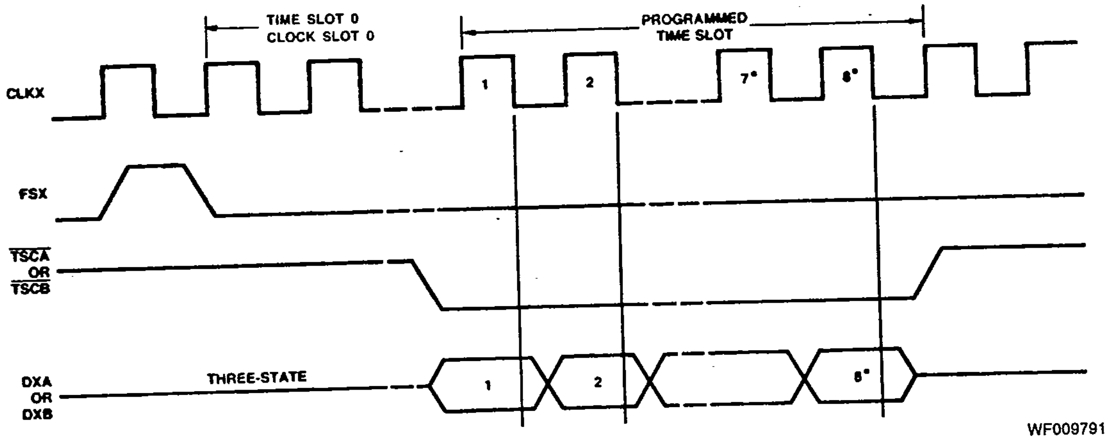
In the Am7901A/B, the PCM data may be user-programmed to be input from one of two ports, DRA or DRB.

Receive Signal Processor

In the receive path (Figure 6), the digital signal is expanded, filtered, converted to analog, and output onto the V_{OUT} pin.

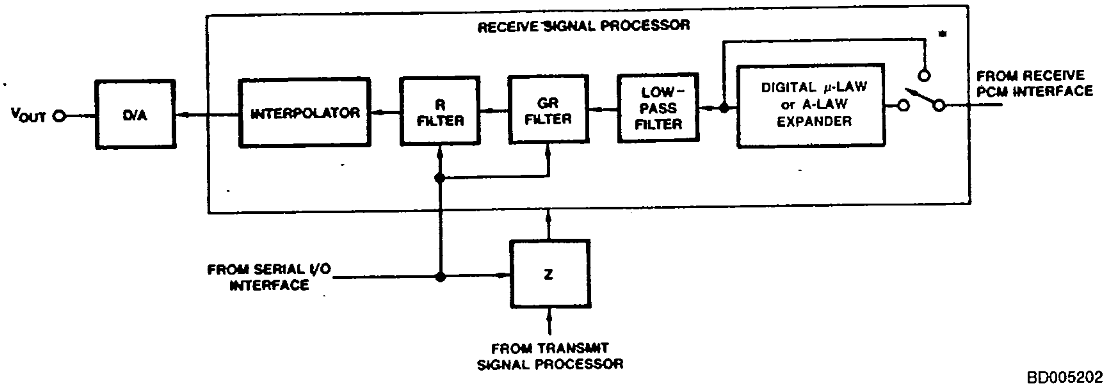
The Signal Processor contains an ALU, RAM, ROM and control logic to implement the filter sections. The Z, R and GR are user-programmable (through the Serial I/O Interface) filter sections and their coefficients are stored in the coefficient RAM. These filters may be made transparent when not required in a system.

The low-pass filter band-limits the signal. The GR filter allows the user to program a loss of up to 12 dB in 0.1-dB steps. The R filter is a 4-tap FIR section and is part of the frequency response correction network. The Z filter provides feedback from the Transmit Signal Processor to the Receive Signal Processor and is used to modify the effective input impedance to the system. The interpolator provides the higher sample rate to the D/A converter.



*For Linear Code, the 7th and 8th Clock Cycles Correspond to the 15th and 16th Clock Cycles.

Figure 5. Transmit PCM Timing Diagram



*For Am7901B, the expander cannot be bypassed.

Figure 6. Receive Signal Processor

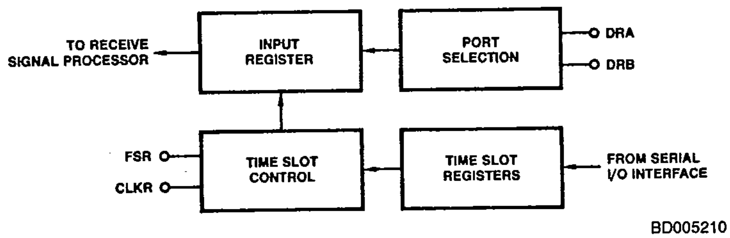
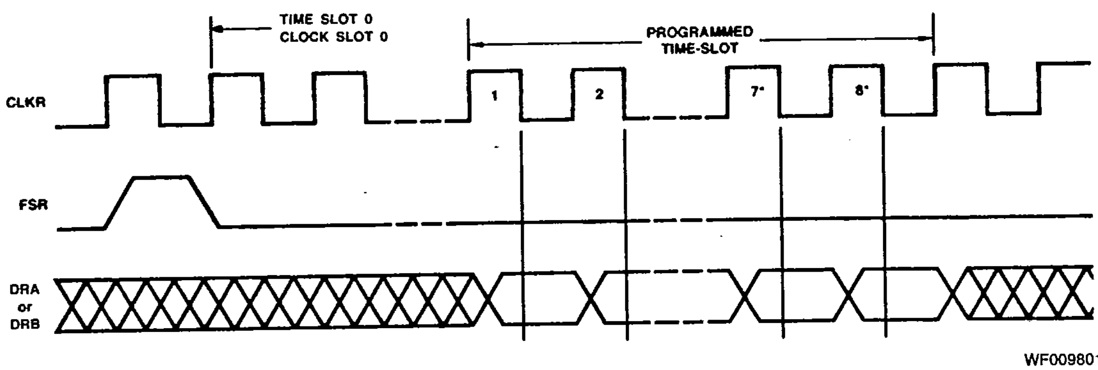


Figure 7. Receive PCM Interface



*For Linear Code, the 7th and 8th Clock Cycles Correspond to the 15th and 16th Clock Cycles.

Figure 8. Receive PCM Timing Diagram

Serial I/O Interface

A microprocessor may be used to program the SLAC and control its operation using the Serial I/O Interface (Figure 9). Additionally, data programmed previously may be read out for verification. The control word format is shown in Table 1. Commands are provided to:

- Set power-up/power-down modes
- Set up test functions
- Set up operating functions
- Program filter coefficients
- Assign time slots and port selection
- Write to the SLIC latch
- Enable/Disable each user-programmable filter

The interface consists of 4 pins, $\overline{CS}$, DCLK, D_{IN} and D_{OUT}. The device is accessed by $\overline{CS}$ and data is serially loaded-in on D_{IN}, or read-out on D_{OUT} under control of DCLK. Either commands or data words may be written to the SLAC, but only data words can be read out. All words are 8 bits wide and are written or read MSB first (Figure 10).

For both reception or transmission of words, exactly 8 Data Clock cycles must be received after $\overline{CS}$ goes LOW. $\overline{CS}$ must stay HIGH (off period) for a minimum time period before it can go LOW again (see Note 4 under Switching Characteristics). During this off-period, the logic decodes and executes the command. All reading of data must be preceded by an input command requesting the data. Once control data transmission has begun, no new input commands will be accepted until control data transmission is completed.

A Serial I/O cycle is defined by transitions of $\overline{CS}$ and DCLK. Upon proper application of power supplies and MCLK, the device expects the first word to be a command. A number of commands require additional data words to be input or output. The SLAC will not accept new commands until all this data has been transferred. But in the read mode, a data word of all zeroes is equivalent to the power-down command and the device resets to the stand-by mode and is ready to receive a new command.

There are two possible operations of DCLK and $\overline{CS}$ for the SLAC to function correctly. If the $\overline{CS}$ is held in the HIGH state between accesses, the DCLK may free run with no change to the internal control data. Using this method, the same DCLK may be run to a number of SLACs and individual $\overline{CS}$ lines will select the appropriate device to access. If the DCLK is held in the LOW state between accesses, the $\overline{CS}$ line may make multiple transitions between accesses for a particular SLAC. This allows running one $\overline{CS}$ line to all SLACs and selecting a particular device through enabling or disabling its DCLK.

It should be noted that the DCLK can stay in the LOW state indefinitely with no loss of internal control information. However, it should not be held in the HIGH state for more than 20 µs to ensure proper operation as indicated by the Switching Characteristics Table.

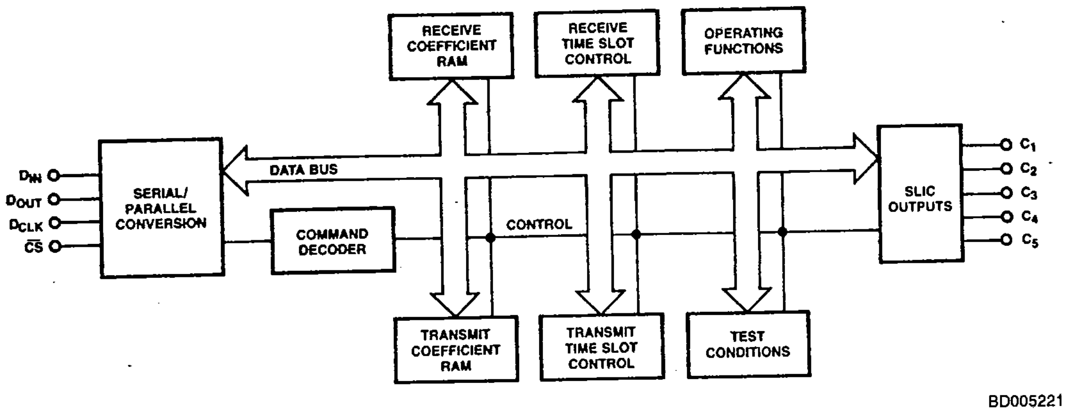
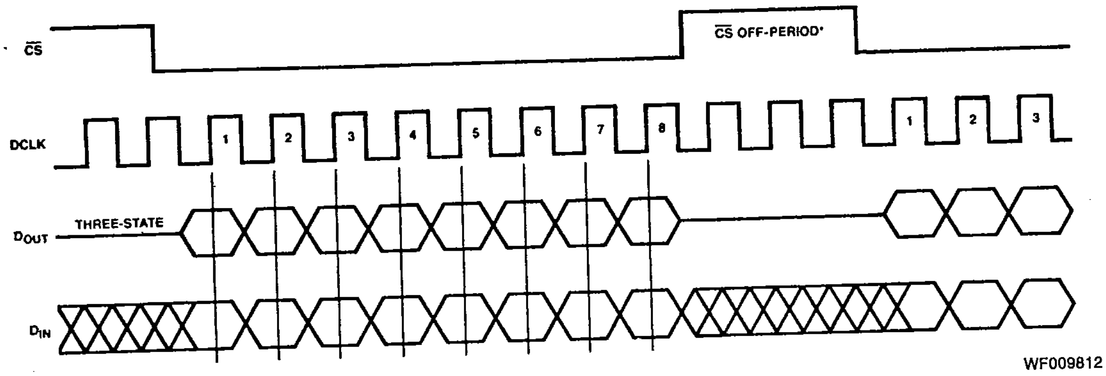


Figure 9. Serial I/O Interface



*See Note 4 under Switching Characteristics

Figure 10. Serial I/O Interface Timing Diagrams

Digital Filters

The SLAC uses digital signal processing to implement the various filters (Figure 11).

The advantages of digital filters are:

- High reliability
- No drift with time or temperature
- Unit-to-unit repeatability
- Superior transmission performance

Six of the digital filters in the signal processing sections are user-programmable. These allow the user to independently modify the gain in both the transmit and receive paths, provide trans-hybrid balancing in the system, and adjust the two-wire line termination impedance. The programming capability feature allows the user to optimize the performance of the SLAC for his system. Each programmable filter section has the following type of transfer function:

$$H_z = h_0 + h_1z^{-1} + h_2z^{-2} + \ldots\ldots + h_nz^{-n} \qquad \text{(Eq. 1)}$$

The values of the user-defined coefficients (h_n) are assigned via the Serial I/O Interface (Table 1). The number of taps (n) provided depends on the particular filter.

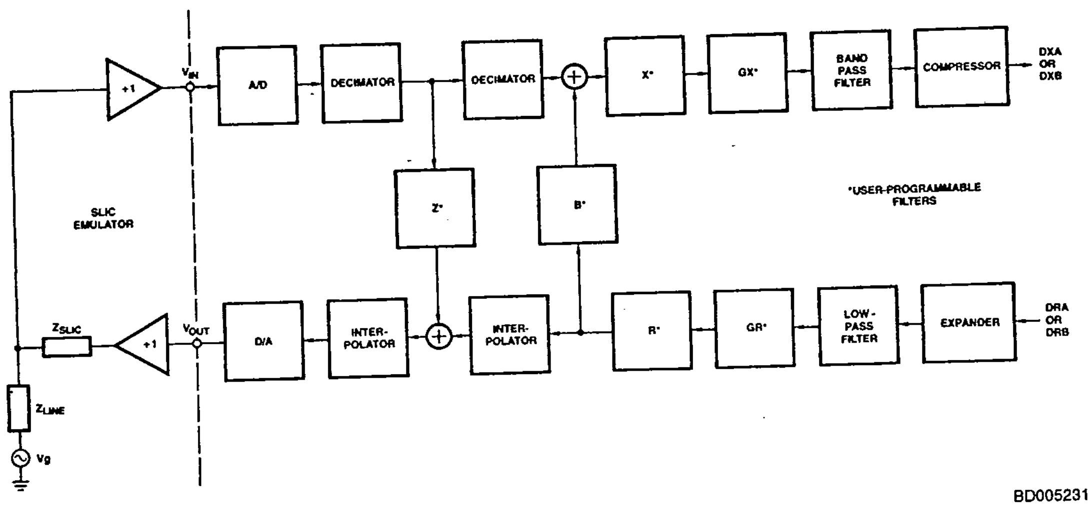


Figure 11. SLAC Signal Processing Flow

The filter function is performed by a series of multiplications and accumulations. A multiply is accomplished by shifting the multiplicand and summing the result with the previous value at that summation node. For example, a one-bit multiply is a shift of M bits where M is related to the position of the binary one in the multiplier (h_i) as expressed in the following equation:

$$h_i = B_1\, 2^{-M_1} + B_2\, 2^{-M_2} + \ldots B_N\, 2^{-M_N} \qquad \text{(Eq. 2)}$$

where: $M_i \leq M_i + 1$
$B_i = \pm 1$

The subscript N is limited to 4 for the GR, GX, R, X and Z filters, and N is 3 for the B filter. The multiply is done from the Least Significant Bit (LSB) to the Most Significant Bit (MSB). Notes 11 and 12 explain the encoding of the shift codes.

The B, X, R, Z and Gain Parameters are written in or read out as 8-bit words. The format of the parameters is shown below:

A. B Coefficients

7 — 4	3 — 0	
$C_{30}m_{30}$	$C_{20}m_{20}$	← 1st word
$C_{10}m_{10}$	$C_{31}m_{31}$	← 2nd word
$C_{21}m_{21}$	$C_{11}m_{11}$	
$C_{32}m_{32}$	$C_{22}m_{22}$	•
$C_{12}m_{12}$	•	•
•	•	•
•	•	
•	$C_{37}m_{37}$	
$C_{27}m_{27}$	$C_{17}m_{17}$	← 12th word

B. X Coefficients

7 — 4	3 — 0	
$C_{40}m_{40}$	$C_{30}m_{30}$	← 1st word
$C_{20}m_{20}$	$C_{10}m_{10}$	← 2nd word
$C_{41}m_{41}$	$C_{31}m_{31}$	
$C_{21}m_{21}$	$C_{11}m_{11}$	•
$C_{42}m_{42}$	$C_{32}m_{32}$	•
$C_{22}m_{22}$	$C_{12}m_{12}$	•
$C_{43}m_{43}$	$C_{33}m_{33}$	
$C_{23}m_{23}$	$C_{13}m_{13}$	← 8th word

C. R, Z Coefficients

7 — 4	3 — 0	
$C_{43}m_{43}$	$C_{33}m_{33}$	← 1st word
$C_{23}m_{23}$	$C_{13}m_{13}$	
$C_{42}m_{42}$	$C_{32}m_{32}$	•
$C_{22}m_{22}$	$C_{12}m_{12}$	•
$C_{41}m_{41}$	$C_{31}m_{31}$	•
$C_{21}m_{21}$	$C_{11}m_{11}$	
$C_{40}m_{40}$	$C_{30}m_{30}$	
$C_{20}m_{20}$	$C_{10}m_{10}$	← 8th word

D. Gain Coefficients

7 — 4	3 — 0	
$C_{40}m_{40}$	$C_{30}m_{30}$	← 1st word
$C_{20}m_{20}$	$C_{10}m_{10}$	← 2nd word

$C_{xy}\, m_{xy}$ = C is the sign bit and m is the 3-bit code specifying the position of the 1s.
y is the coefficient number
x specifies the relative position of the one in coefficient Y (1 = most significant one, 2 = second one, etc.).
and the coefficients in Equation 1 shown above are described by:

$$h_i = (C_{1i} \cdot 2^{-\hat{m}_{1i}}\ (1 + C_{2i} \cdot 2^{-\hat{m}_{2i}}\ (1 + C_{3i} \cdot 2^{-\hat{m}_{3i}}\ (1 + C_{4i} \cdot 2^{-m_{4i}}))))$$

except for the G_X filter where

$$h_i = 1 + (C_{1i} \cdot 2^{-\hat{m}_{1i}}\ (1 + C_{2i} \cdot 2^{-\hat{m}_{2i}}\ (1 + C_{3i} \cdot 2^{-\hat{m}_{3i}}\ (1 + C_{4i} \cdot 2^{-\hat{m}_{4i}}))))$$

where $\hat{m}_{ij} = 7 - m_{ij}$

Two-Wire Impedance Matching

A feedback path is provided from the transmit to the receive section via the Z filter. This filter may be programmed to modify the effective termination impedance (Z_{SLIC}) of a SLIC or a transformer hybrid to a desired value. The desired impedance may be complex. This feature allows the user to terminate each SLIC in a Subscriber Line System with a fixed resistor and digitally modify their impedance using the Z filter.

The X and R filters are the Transmit and Receive attenuation distortion correction filters. These filter sections are programmed to compensate the attenuation distortion caused by the Z filter.

Trans-Hybrid Balance

In a traditional line card system, a balance network is used with the SLIC to achieve trans-hybrid balancing. If the balance network perfectly matches the subscriber's line, infinite trans-hybrid balancing is achieved. But in general, the matching in traditional systems is poor and trans-hybrid balancing is not very good. Some systems have up to 2 or 3 compromise networks per line that must be selected semi-automatically or manually to provide the balance.

In the SLAC, a feedback path is provided from the receive to the transmit section via the B filter. This filter may be programmed to cancel the received signal from the transmit signal path and achieve a significantly improved level of trans-hybrid balance.

Gain Adjustment

Signal levels in the transmit and receive paths may be modified by programming the GX and GR filters. The GX filter allows the user to add up to 12 dB of gain (in 0.1-dB steps) in the transmit path. The GR filter allows the user to add up to 12 dB of loss (in 0.1-dB steps) in the receive path.

Test Features

The SLAC simplifies system testing by providing both digital and analog loop-back paths. Under program control, either the DRA or DRB input is looped to the DXA or DXB output (digital loop-back) through a path from the output of the interpolator in the receive path to the input of the decimator in the transmit path, or the V_{IN} input is looped to the V_{OUT} output (analog loop-back) through the Z filter. To allow testing of the subscriber loop cabling for leakage, the transmit high pass filter may be disabled and auto zero operation interrupted. The receive analog output may be programmed to cut off. This receive cut-off command may be used to stop oscillations in the four-wire side of the telephone network.

Stand-by Mode

The SLAC is forced into the stand-by mode either by power-on clear or by reception of the power-down code. In this mode, power is switched off from all circuitry that can be turned off. No transmission or reception of PCM data takes place. However, the circuits which contain programmed information retain their data. The Serial I/O Interface remains active to receive new commands.

Power-On Clear

Proper operation of power-on clear requires sequenced application of V_{CC}, MCLK then V_{BB}.

Stand-Alone Mode

In the stand-alone mode, the serial interface is not used. The DCLK and D_{IN} pins may be used to control the device. Applying −5 V to the DCLK pin resets the device and the D_{IN} pin can subsequently be used to power-up or power-down the SLAC.

DCLK	D_{IN}	
0	X	Normal mode
1	X	Normal mode
−5 V	0	Reset and Power-Down
−5 V	1	Reset and Power-Up

Reset State

The Reset State of the device is:

a) Both Transmit and Receive Time and Clock Slots are set to zero.
b) μ-law is selected for Am7901A. A-law is selected for Am7901B
c) B, X, R, Z filters are disabled
d) Both Transmit (GX) and Receive (RX) gains are set to unity
e) SLIC outputs are set high
f) Normal conditions are selected (see Note 9 – Command Word Format)
g) DXA/DRA ports are selected

μ-LAW: POSITIVE INPUT VALUES

1 Segment Number	2 Number of Intervals X Interval Size	3 Value at Segment End Points	4 Decision Value Number n	5 Decision Value x_n (1)	6 Character Signal (5) Bit Number 1 2 3 4 5 6 7 8	7 Value at Decoder Output y_n (3)	8 Decoder Output Value Number
		8159	(128)	(8159)			
8	16 x 256		127 ⋮ 113	7903 ⋮ 4319	1 0 0 0 0 0 0 0 ⋮ (2) 1 0 0 0 1 1 1 1	8031 ⋮ 4191	127 ⋮ 112
		4063	112	4063			
7	16 x 128		⋮ 97	⋮ 2143	⋮ (2) 1 0 0 1 1 1 1 1	⋮ 2079	⋮ 96
		2015	96	2015			
6	16 x 64		⋮ 81	⋮ 1055	⋮ (2) 1 0 1 0 1 1 1 1	⋮ 1023	⋮ 80
		991	80	991			
5	16 x 32		⋮ 65	⋮ 511	⋮ (2) 1 0 1 1 1 1 1 1	⋮ 495	⋮ 64
		479	64	479			
4	16 x 16		⋮ 49	⋮ 239	⋮ (2) 1 1 0 0 1 1 1 1	⋮ 231	⋮ 48
		223	48	223			
3	16 x 8		⋮ 33	⋮ 103	⋮ (2) 1 1 0 1 1 1 1 1	⋮ 99	⋮ 32
		95	32	95			
2	16 x 4		⋮ 17	⋮ 35	⋮ (2) 1 1 1 0 1 1 1 1	⋮ 33	⋮ 16
		31	16	31			
1	15 x 2		⋮ 2	⋮ 3	⋮ (2) 1 1 1 1 1 1 1 0	⋮ 2	⋮ 1
	1 x 1		1	1	1 1 1 1 1 1 1 1	0	0
			0	0			

Notes:
1. 8159 normalized value units correspond to $T_{MAX} = 3.17$ dBm0.
2. The character signal corresponding to positive input values between two successive decision values numbered n and n + 1 (see column 4) is (255 − n) expressed as a binary number.
3. The value at the decoder is $y_0 = x_0 = 0$ for $n = 0$, and $y_n = \frac{x_n + x_{n+1}}{2}$ for $n = 1, 2, \ldots, 127$.
4. x_{128} is a virtual decision value.
5. Bit 1 is a 0 for negative input values.

A-law, positive input values

1	2	3	4	5	6	7	8
Segment Number	Number Of Intervals X Interval Size	Value At Segment End Points	Decision Value Number n	Decision Value x_n (1)	Character Signal Before Inversion Of The Even Bits Bit Number 1 2 3 4 5 6 7 8	Value at Decoder Output y_n (3)	Decoder Output Value Number
		4096	(128)	(4096)	1 1 1 1 1 1 1 1	4032	128
7	16 x 128		127 ⋮ 113	3968 ⋮ 2176	(2)	⋮	⋮
					1 1 1 1 0 0 0 0	2112	113
		2048	112	2048			
6	16 x 64		⋮ 97	⋮ 1086	(2)	⋮	⋮
					1 1 1 0 0 0 0 0	1056	97
		1024	96	1024			
5	16 x 32		⋮ 81	⋮ 544	(2)	⋮	⋮
					1 1 0 1 0 0 0 0	528	81
		512	80	512			
4	16 x 16		⋮ 65	⋮ 272	(2)	⋮	⋮
					1 1 0 0 0 0 0 0	264	65
		256	64	256			
3	16 x 8		⋮ 49	⋮ 136	(2)	⋮	⋮
					1 0 1 1 0 0 0 0	132	49
		128	48	128			
2	16 x 4		⋮ 33	⋮ 68	(2)	⋮	⋮
					1 0 1 0 0 0 0 0	66	33
		64	32	64			
1	32 x 2		⋮ 1	⋮ 2	(2)	⋮	⋮
					1 0 0 0 0 0 0 0	1	1
↓			0	0			

Notes: 1. 4096 normalized value units correspond to $T_{max} = 3.14$ dBm0.
2. The character signals are obtained by inverting the even bits of the signals of column 6. Before this inversion, the character signal corresponding to positive input values between two successive decision values numbered n and $n+1$ (see column 4) is $(128 + n)$ expressed as a binary number.
3. The value at the decoder output is $y_n = \frac{x_{n-1} + x_n}{2}$ for $n = 1, \ldots, 127, 128$.
4. x_{128} is a virtual decision value.
5. Bit 1 is a 0 for negative input values.

TABLE I: CONTROL WORD FORMAT

The Control Interface consists of Data Input, Data Output, Data Clock and $\overline{CS}$ Input. Data is read in (read out) on the Serial Data Input (output). The Serial Input consists of 8-bit (byte) command words which may be followed with additional bytes of input data or may be followed by the SLAC outputting bytes of data. All words are input with MSB (D_7) first and LSB (D_0) last. All outputs are output with the MSB (D_7) first and the LSB (D_0) last. Words are written or read one at a time, with $\overline{CS}$ going high for at least the minimum off-period (see Note 4 under Switching Characteristics) before the next read or write operation. The first 3 bits of the command word indicate the type of command and the last 5 bits contain either data or further information about the command. The classes of command are:

D_7 D_6 D_5	
0 0 0	Power Down/No Operation
0 0 1	Transmit Time Slot Selection
0 1 0	Receive Time Slot Selection
0 1 1	Clock Slot and Gain Selection Read Slot, Gain and PCM Mode
1 0 0	Set Basic and Operating Functions and PCM Modes
1 0 1	Read/Write Coefficients, Set Test Modes, Select μ-law/A-law/linear
1 1 0	Data for SLIC Interface
1 1 1	Power Up/No Operation

MSB D_7 D_6 D_5	D_4 D_3 D_2 D_1 D_0 LSB		
0 0 0	0 0 0 0 0	Power Down[1]	
0 0 0	X X X X X	Reserved[2]	
0 0 1	Y Y Y Y Y	Transmit Time Slot Selection[3]	Choose 1 of 32 Time Slots
0 1 0	Y Y Y Y Y	Receive Time Slot Selection[3]	Choose 1 of 32 Time Slots
0 1 1	0 0 Y Y Y	Transmit Clock Slot Selection[3]	Choose 1 of 8 Clock Slots
0 1 1	0 1 Y Y Y	Receive Clock Slot Selection[3]	Choose 1 of 8 Clock Slots
0 1 1	1 0 0 1 0	Transmit Gain Selection	Followed by 2 Bytes of Data[4]
0 1 1	1 1 0 1 0	Receive Gain Selection	Followed by 2 Bytes of Data[4]
0 1 1	1 0 1 0 1	Read Transmit Time and Clock Slot[5]	Followed by 1 Byte of Data[4]
0 1 1	1 0 0 0 1	Read Transmit Gain	Followed by 2 Bytes of Data[4]
0 1 1	1 1 1 0 1	Read Receive Time and Clock Slots[5]	Followed by 1 Byte of Data[4]
0 1 1	1 1 0 0 1	Read Receive Gain	Followed by 2 Bytes of Data[4]
0 1 1	1 0 1 1 1	Read PCM Mode	Followed by 1 Byte of Data[4, 6]
1 0 0	0 A B C D	Operating & Basic Function[7]	
1 0 0	1 E F G H	PCM-Mode Selection[8]	
1 0 1	0 0 0 0 0	Write B Coefficients	Followed by 12 Bytes of Data[4, 12]
1 0 1	0 0 1 0 0	Write X Coefficients	Followed by 8 Bytes of Data[4,11]
1 0 1	0 1 0 0 0	Write R Coefficients	Followed by 8 Bytes of Data[4,11]
1 0 1	0 1 1 0 0	Write Z Coefficients	Followed by 8 Bytes of Data[4, 11]
1 0 1	0 0 0 1 1	Read B Coefficients	Followed by 12 Bytes of Data[4, 12]
1 0 1	0 0 1 1 1	Read X Coefficients	Followed by 8 Bytes of Data[4, 11]
1 0 1	0 1 0 1 1	Read R Coefficients	Followed by 8 Bytes of Data[4, 11]
1 0 1	0 1 1 1 1	Read Z Coefficients	Followed by 8 Bytes of Data[4, 11]
1 0 1	1 0 0 0 0	Reset to normal conditions[9]	
1 0 1	1 0 0 0 1	Add −6 dB to receive gain	
1 0 1	1 0 0 1 0	Cutoff receive path	
1 0 1	1 0 1 1 1	Test mode–analog loop-back	
1 0 1	1 0 1 0 0	Test mode–digital loop-back[13]	
1 0 1	1 0 0 1 1	Disable High-Pass Filter (set to 1) and freeze auto zero circuit	
1 0 1	1 1 0 0 0	Choose Linear code (Am7901A)/Choose A-law code (Am7901B)	
1 0 1	1 1 0 0 1	Choose μ-law	
1 1 0	I J K L M	Outputs to SLIC[10]	
1 1 1	X X X X X	Reserved[2]	
1 1 1	1 1 1 1 1	Power Up[1]	

NOTES:

1. During power-down the control information is not changed. The Serial I/O remains active, the SLIC control outputs remain valid, the PCM outputs are high impedance, the PCM inputs are disabled and the analog output is set to zero with a moderate series impedance to analog ground. Upon power-up, all data RAMs except the coefficient RAMs are powered up in a cleared state (set to all zeroes). No PCM data is transmitted until after the second FSX pulse is received following the execution of the power-up command.
2. These reserved codes are all codes beginning with 000 and 111 except for 00000000 (power-down) and 11111111 (power-up). These codes may be used by future members of this product family.

3. The Ys are binary codes which program the time slots for transmission and reception of PCM data. Five bits are available for time-slot selection which allow one of 32 time slots to be programmed. The three bits of the clock-slot selection allow 0 to 7 clock offsets within the time slot to be programmed.

4. All commands that are followed by additional input data to the device (transmit-gain selection, receive-gain selection, write B, Z, X or R coefficients) must have the input data as the next N words (N = 1, 2, 8, 12) written to the device (framed by the next N transitions of $\overline{CS}$). All commands that are followed by output data (read transmit time and clock slot, read transmit gain, read receive time and clock slot, read receive gain, read PCM mode, read B, Z, X or R coefficients) will cause the device to output data for the next N (N = 1, 2, 8, 12) transitions of $\overline{CS}$ going low and will not accept any input commands until all the data has been output. When in an input mode, data word of 00000000 will automatically power-down the device.

5. Time and clock slots are read out time slot first, followed by clock slot.

6. The PCM Modes are read out as the least significant 4 bits of data. The most significant 4 bits are set to 1. The least significant 4 bits contain the following data:

BIT 3: Data Receive select bit
BIT 2: Data Transmit select bit
BIT 1: Receive Expanded Mode bit
BIT 0: Transmit Expanded Mode bit

The Data Receive/Transmit select bits define which port is used to receive/transmit data. A 0 means port A has been selected. A 1 means port B has been selected.

The Receive/Transmit Expanded Mode bits allow up to 64 channels in a Receive/Transmit frame.

7. The operating function command has four 1-bit fields:
A: A = 1 enables B filter, A = 0 disables B (sets B = 0)
B: B = 1 enables X filters, B = 0 disables X (sets X = 1)
C: C = 1 enables R filter, C = 0 disables R (sets R = 1)
D: D = 1 enables Z filter, D = 0 disables Z (sets Z = 0)

8. The transmit PCM data may be output onto either the DXA or the DXB port. Either $\overline{TSCA}$ or $\overline{TSCB}$ is correspondingly output. The receive PCM data may be input onto either the DRA or the DRB port. The Transmit/Receive Expanded Mode bits allow up to 64 channels in Transmit/Receive frame.
E: E = 1 chooses DRB, E = 0 chooses DRA
F: F = 1 chooses DXB ($\overline{TSCB}$), F = 0 chooses DXA ($\overline{TSCA}$)
G: G = 1 sets Receive Expanded Mode bit
G = 0 clears Receive Expanded Mode bit
H: H = 1 sets Transmit Expanded Mode bit
H = 0 clears Transmit Expanded Mode bit

9. Normal conditions are receive gain set to value stored in the receive gain control words, the receive path and high-pass filter are enabled and the auto-zero-circuit operates, Z filter coefficients are the value set by the basic and operating function bit D and the device is not in a test mode (no loop-back). The test modes are mutually exclusive. Entering a command to set one test mode clears the other test mode (if set). "Reset to normal conditions" does reset a test mode.

10. The outputs to the SLIC are defined below:
I = C5 L = C2
J = C4 M = C1
K = C3

11. X, R, and Z coefficients are allowed to have only 1 to 4 ones. Each coefficient is encoded in a 4-bit code where the lower three bits represent the number of shifts to the next higher one in the coefficient and the first bit (MSB) defines the coefficient sign. Each one can be either positive or negative (0 = positive, 1 = negative). The maximum number of shifts allowed is six. The lower three bits are encoded for 0(111), 1(110), 2(101), 3(100), 4(011), 5(010) or 6(001) shifts. A code of 1000 implies 0 shifts and no addition and a code of 0000 is not allowed (See note 4). The four coefficients use sixteen 4-bit codes which are input as eight 8-bit words starting with coefficients 0 and ending with coefficient 3 for the X coefficients. The R and Z filter coefficient data starts with coefficient 3 and ends with coefficient 0.

12. B coefficients are allowed to have only 1 to 3 ones. Each coefficient is encoded in a 4-bit code where the lower three bits represent the number of shifts to the next higher one in the coefficient and the first bit (MSB) defines the coefficient sign. Each one can be either positive or negative (0 = positive, 1 = negative). The maximum number of shifts allowed is six. The lower three bits are encoded for 0(111), 1(110), 2(101), 3(100), 4(011), 5(010) or 6(001) shifts. A code of 1000 implies 0 shifts and no addition and a code of 0000 is not allowed (See note 4). The eight coefficients use twenty-four 4-bit codes which are input as twelve 8-bit words starting with coefficient 0 and ending with coefficient 7.

13. Digital loop-back provides 6 dB of gain.

ABSOLUTE MAXIMUM RATINGS

Storage Temperature ....-60 to 125°C
Ambient Temperature, under Bias....................0 to 70°C
V_{CC} with Respect to DGND ....-0.4 to +6.0 V
V_{BB} with Respect to DGND...................+0.4 to -6.0 V
V_{IN} with Respect to AGND........................V_{BB} to V_{CC}

Stresses above those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to absolute maximum ratings for extended periods may affect device reliability.

OPERATING RANGES

Part Number	Ambient Temperature	V_{CC}	V_{BB}	DGND	AGND
Am7901A/BDC	$0°C \leq T_A \leq 70°C$	+5.0 V±5%	-5.0 V±5%	0 V	0 V± 100 mV

Operating ranges define those limits over which the functionality of the device is guaranteed.

DC SPECIFICATIONS

ELECTRICAL CHARACTERISTICS over operating range (Note 1) unless otherwise specified

Parameters	Description	Test Conditions	Min.	Typ.	Max.	Units
Z_{IN}	Analog Input Impedance	$-3.2\ V < V_{IN} < 3.2\ V$	20			kΩ
Z_{OUT}	Analog Output Impedance	$-3.2\ V < V_{OUT} < 3.2\ V$			20	Ω
V_{IOS}	Offset Voltage Allowed on V_{IN}				±5	mV
V_{OOS}	Analog Output Offset Voltage				±200	mV
V_{IR}	Analog Input Voltage Range				±3.2 V	V
V_{OR}	Analog Output Voltage Range	$R_L \geq 10\ k\Omega$, $C_L \leq 50\ pF$			±3.2 V	V
I_{OUT}	Analog Output Current		350			μA
V_{IL}	Input Low Voltage (All Digital Inputs Except DCLK in Stand Alone Mode)		-0.5		0.8	V
V_{IH}	Input High Voltage (All Digital Inputs)		2.0		V_{CC}	V
V_{OL}	Output Low Voltage (All Digital Outputs)	$I_{OL} = 2\ mA$			0.45	V
V_{OH}	Output High Voltage (All Outputs Except TSC)	$I_{OH} = 400\ \mu A$	2.4			V
I_{OL}	Output Leakage Current				±10	μA
I_{IL}	Input Leakage Current				±1	μA
$I_{IL}\ (V_{IN})$	Input Leakage Current on V_{IN} Pin				±0.2	μA
I_{CC} (S)	V_{CC} Supply Current (Standby)	$V_{CC} = 5.25\ V$, $V_{BB} = -4.75\ V$			15	mA
I_{BB} (S)	V_{BB} Supply Current (Standby)				10	mA
I_{CC} (A)	V_{CC} Supply Current (Active)				60	mA
I_{BB} (A)	V_{BB} Supply Current (Active)				20	mA
PSRR (V_{CC})	V_{CC} Power Supply Rejection Ratio	200 mV p-p @ 1.02 kHz on the appropriate supply	35			dB
PSRR (V_{BB})	V_{BB} Power Supply Rejection Ratio		30			dB
C_I	Input Capacitance (Digital)			5		pF
C_O	Output Capacitance (Digital)			8		pF

Notes: 1. Typical values are for $T_A = 25°C$ and nominal supply voltages. Min. and max. specifications are over the temperature and supply voltage ranges shown in the above table entitled "Operating Ranges."

TRANSMISSION CHARACTERISTICS

(All measurements are made end-to-end with GX = GR = 0 dB and A-law or μ-law companded PCM unless otherwise specified.)

A 0-dBm0 signal at V_{IN} is equivalent to 1.57 V_{RMS}. A 3-dBm0 signal at V_{IN} is equivalent to 2.22 V_{RMS} which corresponds to the overload point of 3.14 volts.

A 0-dBm0 signal at V_{OUT} is equivalent to 1.6 V_{RMS}. A 3-dBm0 signal at V_{OUT} is equivalent to 2.260 V_{RMS} which corresponds to the overload point of 3.196 volts.

Description	Test Conditions	Min	Typ	Max	Units
Attenuation Distortion	800 Hz at 0 dBm0, or 1000 Hz at 0 dBm0		See Fig 12		dB
Gain[1] (either path) a) deviation from ideal value b) deviation from initial value	800 Hz at 0 dBm0, or 1000 Hz at 0 dBm0	−0.2 −0.2		+0.2 +0.2	dB dB
Group Delay Distortion (either path)	0-dBm0 signal		See Fig 13		μs
Group Delay (either path)			150		μs
Harmonic Distortion	(Note 2)			−40	dB
Intermodulation Distortion	a) (Note 3) b) (Note 4)			−35 −49	dB dBm0
Crosstalk a) Go-to-Return path b) Return-to-Go path	300-3400 Hz 0 dBm0 300-3400 Hz 0 dBm0			−70 −70	dB dB
Gain Tracking (either path)			See Fig 14		dB
Signal to Total Distortion (either path)			See Fig 15		dB
μ-Law Companded PCM					
Idle Channel Noise (weighted)	(Note 5)			19	dBrnc0
Idle Channel Noise (weighted, receive only)				15	dBrnc0
Idle Channel Noise (single frequency)				−50	dBm0
A-Law Companded PCM					
Idle Channel Noise (weighted)	(Note 5)			−71	dBm0p
Idle Channel Noise (weighted, receive only)				−75	dBm0p
Idle Channel Noise (single frequency)				−50	dBm0

Notes: 1. The device gains are adjusted during manufacture to guarantee a ±0.4 − dB maximum deviation over lifetime of device.
2. Applied signal is a 0-dBm0 sine wave within 300 to 3400 Hz. The signal measured is any frequency in the range 300 to 3400 Hz.
3. Two different frequencies f_1 and f_2 in the range 300-3400 Hz and of equal levels in the range −4 to −21 dBm0 are applied. $2f_1$-f_2 products are measured relative to the level of either f_1 or f_2.
4. Any intermodulation product due to a signal in the range 300-3400 Hz with input level −9 dBm0 and a 50-Hz signal with input level −23 dBm0.
5. Noise is measured at the analog output, with the analog input zero and the digital PCM output connected to the digital PCM input.

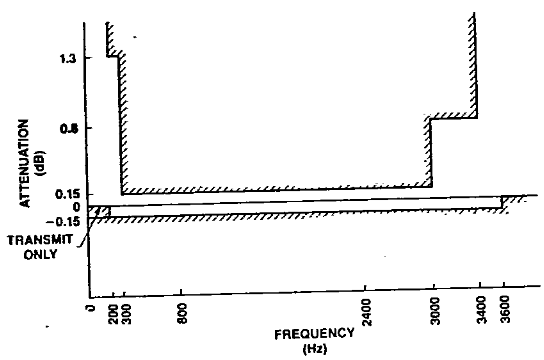


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Figure 12a. Attenuation Distortion (Single Ended)

Notes: 1. The frequency is 800/1000 Hz.
2. Input signal level is 0 dBm0.

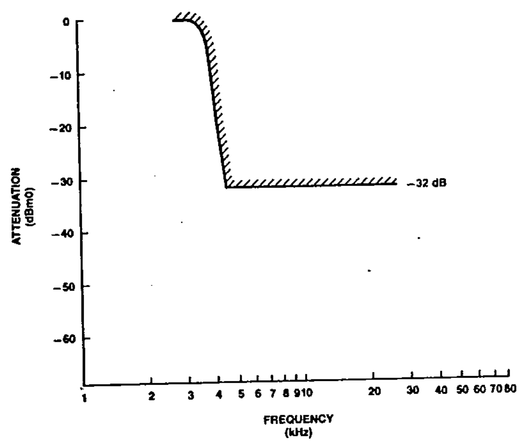

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Figure 12b. Out of Band Signals (End-to-End)

Notes: 1. The frequency is 800/1000 Hz.
2. Input signal level is 0 dBm0.

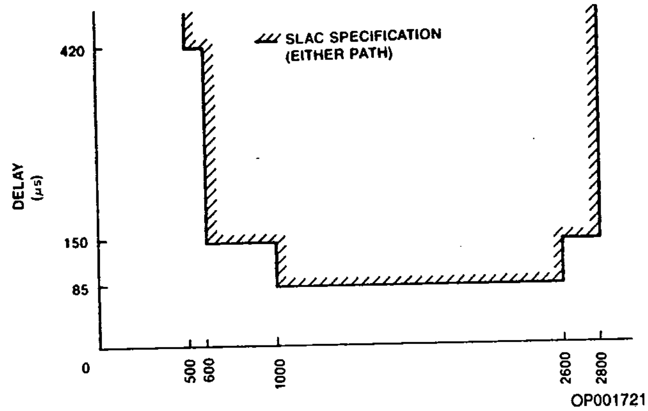


Figure 13. Group Delay Distortion (Either Path)

Notes: 1. Input signal is 0 dBm0.
2. Minimum value of group delay is taken as reference.

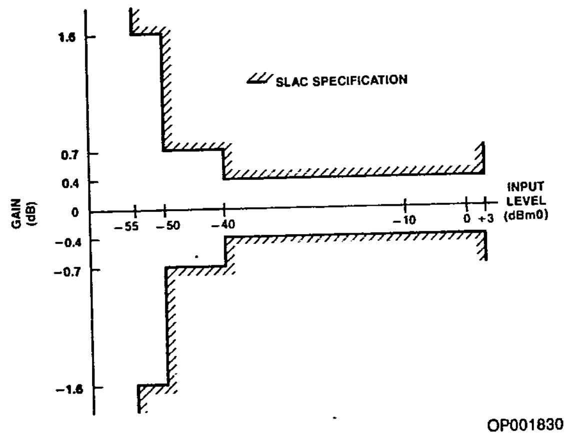


Figure 14. Gain Tracking with Tone (Either Path)

Notes: 1. The input signal is a sine wave in the range of 700 to 1100 Hz, (excluding submultiples of 8 kHz).
2. The gain variation is relative to the gain at −10 dBm0.

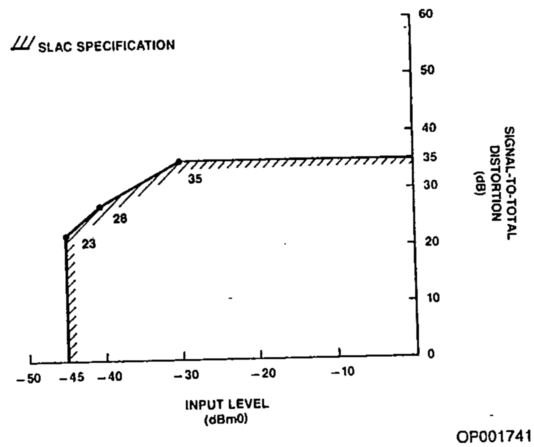


Figure 15. Signal-to-Total Distortion with Tone (Either Path)

Note: The input signal is a sine wave in the range of 700 to 1100 Hz, (excluding submultiples of 8 kHz).

SWITCHING CHARACTERISTICS over operating range unless otherwise specified
$T_A = 0$ to 70°C, $V_{CC} = +5$ V ±5%, $V_{BB} = -5$ V ±5% (See Notes 1, 7, 8)

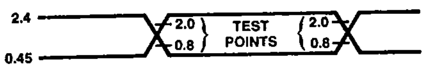
No.	Parameters	Description	Min.	Typ.	Max.	Units
Serial Interface Input Mode						
1	t_{DCH}	Data Clock High Pulse Width (Note 2)	0.220		20	µs
2	t_{DCL}	Data Clock Low Pulse Width (Note 2)	0.220			µs
3	t_{DCR}	Rise Time of Clock	5		50	ns
4	t_{DCF}	Fall Time of Clock	5		50	ns
5	t_{ICSS}	Chip Select Setup Time	150			ns
6	t_{ICSH}	Chip Select Hold Time	50			ns
7	t_{ICSL}	Chip Select Pulse Width (Notes 3 & 9)		8 t_{DCY}		ns
8	t_{ICSO}	Chip Select Off Time (Note 4)				ns
9	t_{IDS}	Input Data Setup Time	50			ns
10	t_{IDH}	Input Data Hold Time	30			ns
11	t_{OLH}	Output Latch Propagation Delay	0.75		1.9	µs
Serial Interface Output Mode						
12	t_{OCSS}	Chip Select Setup Time	150			ns
13	t_{OCSH}	Chip Select Hold Time	50			ns
14	t_{OCSL}	Chip Select Pulse Width (Notes 3 & 9)		8 t_{DCY}		ns
15	t_{OCSO}	Chip Select Off Time (Note 4)				
16	t_{ODD}	Output Data Turn on Delay			100	ns
17	t_{ODH}	Output Data Hold Time	30			ns
18	t_{ODOF}	Output Turn off Delay			100	ns
19	t_{ODC}	Output Data Valid	30		150	ns
PCM Interface						
20	t_{PCY}	PCM Clock Period (Note 5)	0.244		7.8	µs
21	t_{PCH}	PCM Clock Pulse Width (Note 5)	110			ns
22	t_{PCL}	PCM Clock Low Pulse Width (Note 5)	110			ns
23	t_{PCF}	Fall Time of Clock	5		15	ns
24	t_{PCR}	Rise Time of Clock	5		15	ns
25	t_{FSS}	Frame Sync Setup Time	50		(t_{PCY} − 30)	ns
26	t_{FSH}	Frame Sync Hold Time (Companded Mode)	30		(8 t_{PCY} − 50)	ns
		Frame Sync Hold Time (Linear Mode)	30		(16 t_{PCY} − 50)	ns
27	t_{TSD}	Delay to TSC Valid (Note 6)	(N t_{PCY} + 30)		(N t_{PCY} + 150)	ns
28	t_{TSO}	Delay to TSC Off	30			ns
29	t_{DXD}	PCM Data Output Delay	80		150	ns
30	t_{DXH}	PCM Data Output Hold Time	30		100	ns
31	t_{DXZ}	PCM Data Output Delay to High Z	40		75	ns
32	t_{DRS}	PCM Data Input Setup Time	50			ns
33	t_{DRH}	PCM Data Input Hold Time	30			ns
Master Clock						
34	t_{MCY}	Master Clock Period	488.23	488.28	488.33	ns
35	t_{MCH}	Master Clock High Pulse Width	220			ns
36	t_{MCL}	Master Clock Low Pulse Width	238			ns
37	t_{MCR}	Rise Time of Clock	5		15	ns
38	t_{MCF}	Fall Time of Clock	5		15	ns

Notes:
1. Min. and Max. values are valid on all digital outputs except C_1–C_5 with a 150-pF load. C_1–C_5 outputs are valid with a 30-pF load.
2. The Data Clock may be stopped in the Low state indefinitely without loss of information. Data will not be clocked in or out while the clock is in the low state.
3. Chip Select Pulse Width is nominally 8 Data Clock Cycles with a minimum value of 7 Data Clock Cycles + t_{ICSH} + t_{ICSS} and a maximum value of 9 Data Clock Cycles − t_{ICSH} − t_{ICSS}
4. Chip Select Off Time is defined by the type of command being executed. Commands attempting access to the coefficient RAMs, i.e., Read or Write B, Z, X, R or gain coefficients must have a minimum Chip Select Off Time of:
   7 t_{MCY} – if device is in power-down mode.
   32 t_{MCY} – if device is in power-up mode.
   For all other commands, Chip Select Off Time is defined as a minimum of:
   7 t_{MCY} – for both power-up or power-down modes.
5. The maximum allowed PCM clock frequency is 4.096 MHz. The actual PCM clock rate is dependent on the number of channels allocated within a frame. The minimum clock frequency is 128 kHz.
6. $\overline{TSC}$ is delayed from FS by a typical value of N t_{PCY}, where N is the value stored in the Time/Clock Slot register.
7. The Frame Sync pulses (FSX, FSR) repeat at an 8-kHz rate.
8. FSR, FSX, CLKR, CLKX and MCLK all must be synchronized and exactly 256 cycles of MCLK must be guaranteed between Frame Syncs. All five clocks must not be interrupted to assure proper operation.
9. t_{DCY} is 1 Data Clock Cycle.

SWITCHING WAVEFORMS

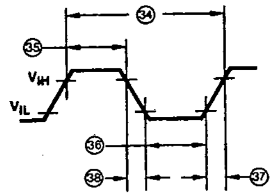
TIMING DIAGRAMS

INPUT AND OUTPUT WAVEFORMS FOR AC TESTS



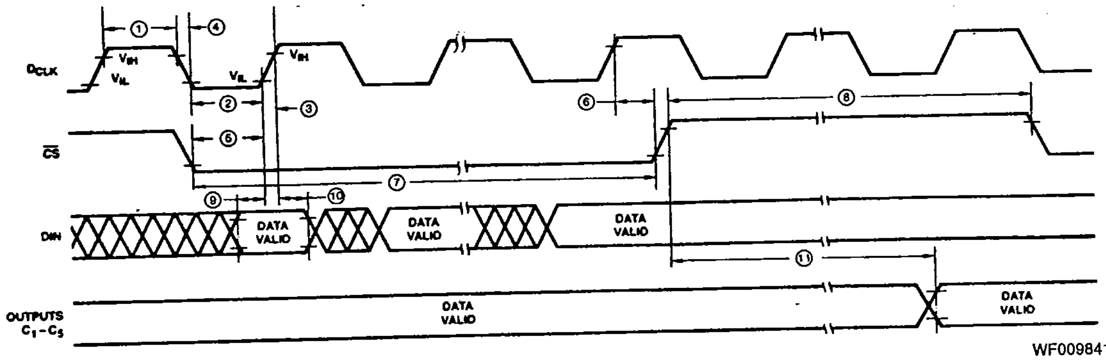
WF009820

MASTER CLOCK TIMING



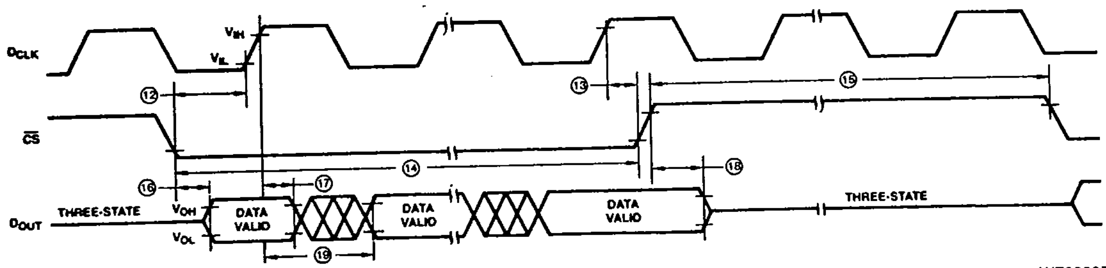
WF009832

SERIAL I/O INTERFACE (INPUT MODE)



WF009841

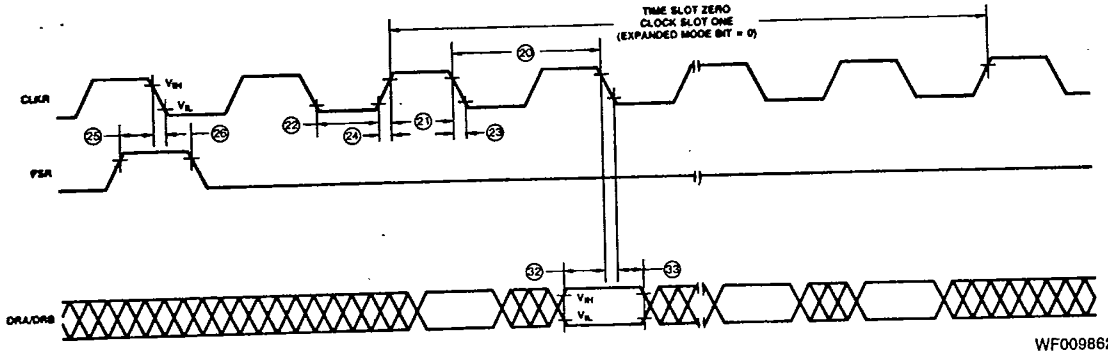
SERIAL I/O INTERFACE (OUTPUT MODE)



WF009852

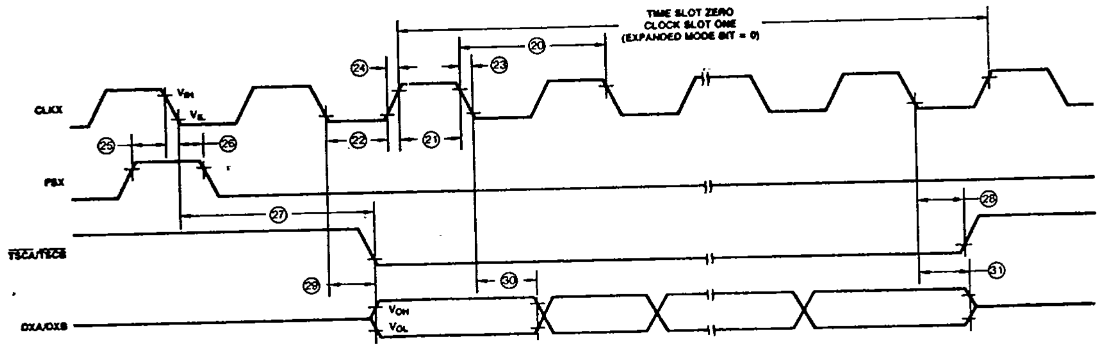
SWITCHING WAVEFORMS (Cont.)

PCM INPUT TIMING



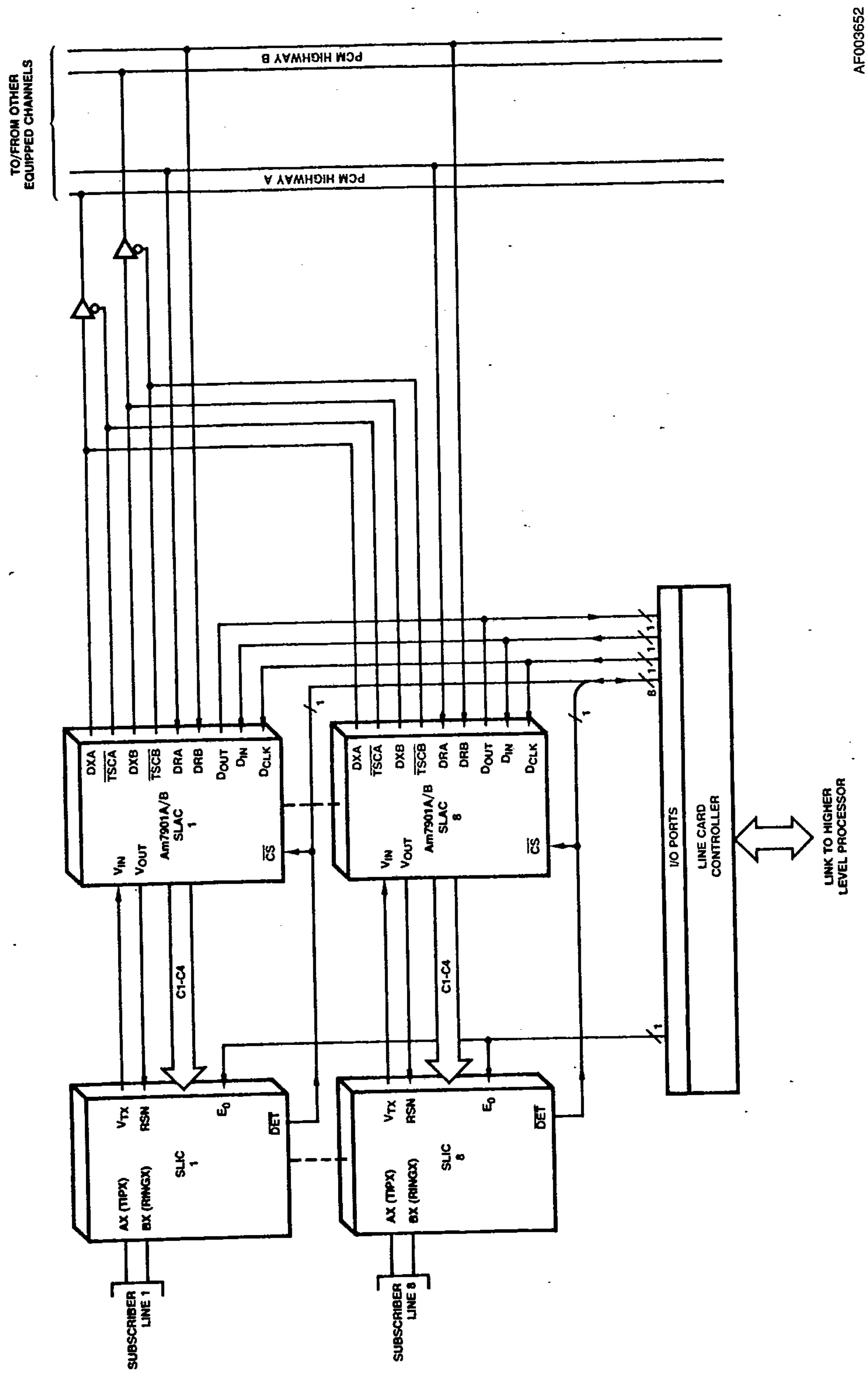
WF009862

PCM OUTPUT TIMING



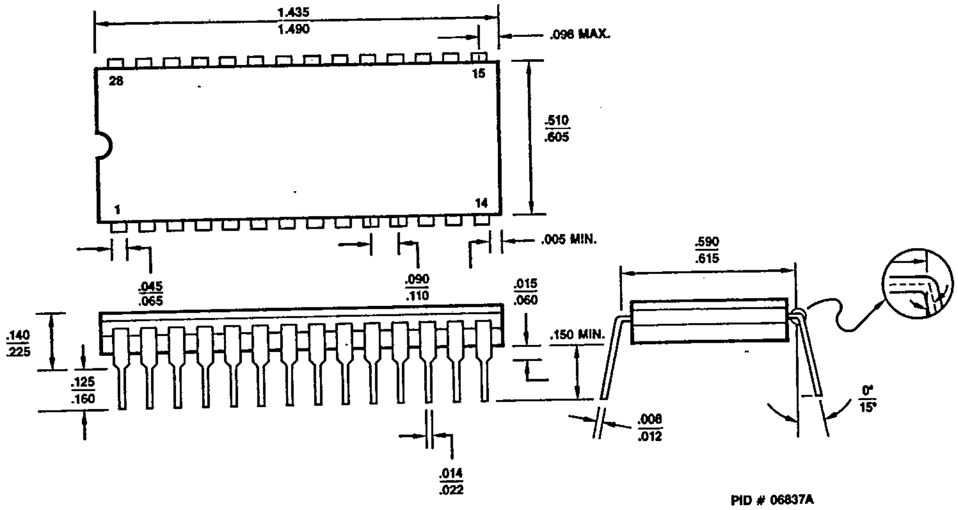
WF009872

AMD
8-CHANNEL SUBSCRIBER LINE CARD



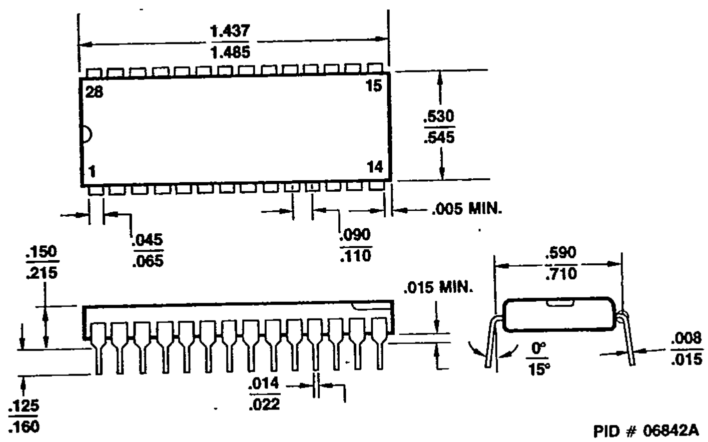
PHYSICAL DIMENSIONS

CD 028



PID # 06837A

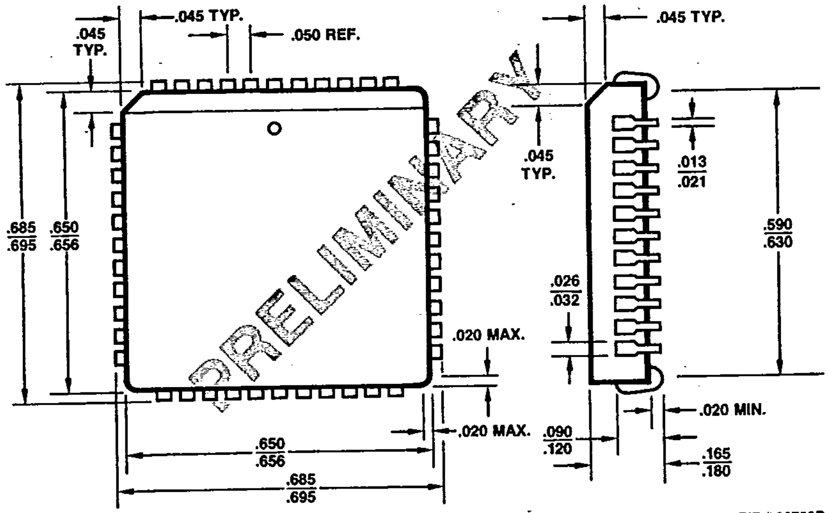
PD 028



PID # 06842A

PHYSICAL DIMENSIONS (Cont.)

PL 044



PID # 06752B