Preliminary

Am7938

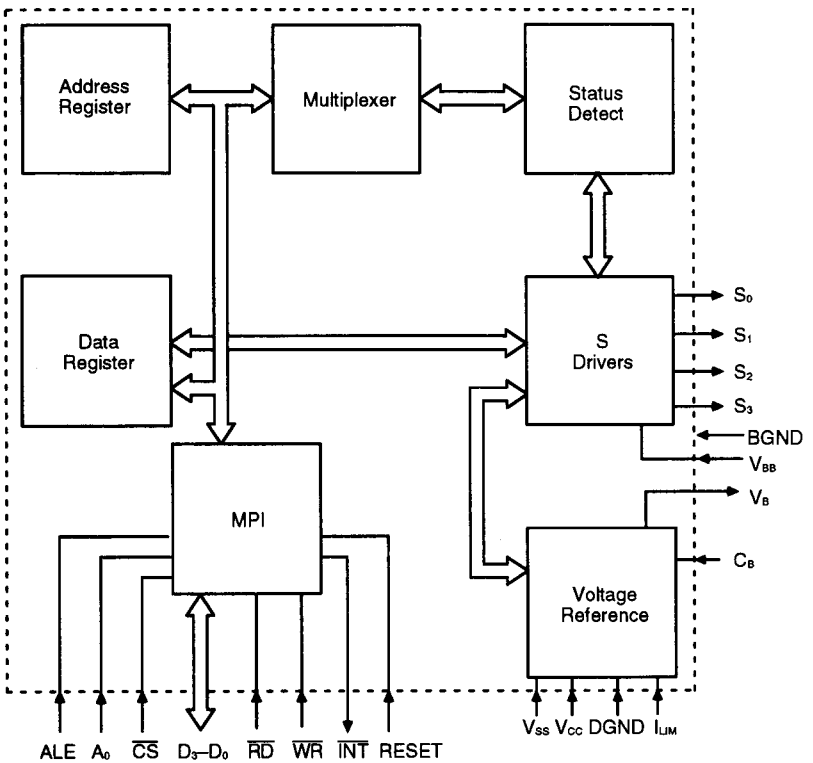
Quad Exchange Power Controller (QEPC)

Advanced Micro Devices

DISTINCTIVE CHARACTERISTICS

- Supplies power for up to four-digital telephone lines
- Conforms to the CCITT recommendations for power feed at the S or T reference point
- Applications for intelligent NTs and PABX/ Central Office line cards
- Supports point-to-point and point-to-multi-point configurations
- Built-in battery control circuit for operation at –40 V
- Each of the four lines is individually controlled
- Status detectors for each line driver; open loop, current overload, low output voltage, thermal overload
- Programmable current limiting
- Automatic shutdown of overloaded lines
- Automatic thermal shutdown
- Microprocessor-compatible interface, including interrupt on current overload
- High-voltage bipolar technology allows battery voltages up to –65 V
- Output current up to 150 mA per driver

BLOCK DIAGRAM



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GENERAL DESCRIPTION

The Am7938 Quad Exchange Power Controller (QEPC) provides a power source for up to four line interfaces. The power source to the Am7938 is a local battery or a centralized regulated power supply. The Am7938 can reside in intelligent NTs or PABX/Central Office line cards. It can operate in point-to-point and point-to-multipoint configurations. Via the Am7938's microprocessor interface, each powered line is individually controlled and monitored. The power to each line can be controlled independently. Therefore, overloads and faults are easy to detect and localize even in a large system. The status conditions detected by the Am7938 on each line that may be read by the microprocessor are: low output voltage, open loop, current overload, thermal overload, and normal line conditions.

Current limit and thermal shutdown circuits protect the Am7938 against overload conditions. However, certain applications may require additional external protection circuitry.

The Am7938 has been developed specifically for CCITT-compatible ISDN configurations. Recognize, however, that due to its versatile design, the Am7938 can be used in numerous other applications.

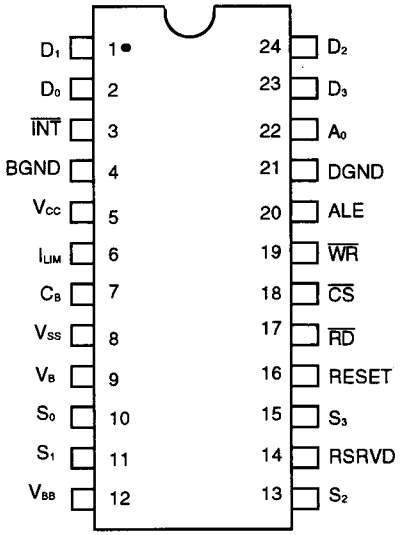
GLOSSARY OF ABBREVIATIONS

A_0	Address Bit
ALE	Address Latch Enable
BGND	Battery Ground (Battery refers to Telephone Line Supply)
C_B	Battery Compensation Capacitor
CCITT	Consultative Committee for International Telegraph and Telephone
CO	Central Office
COD	Current Overload Detector
$\overline{CS}$	Chip Select
D_3–D_0	Data Lines 3–0
DGND	Digital Ground
IAR	Indirect Address Register
I_{LIM}	Current Limit Programming
I_{SLIM}	S-Output Current Limit
$\overline{INT}$	Interrupt
ISDN	Integrated Services Digital Network
LER	Line Enable Register
LVD	Low Voltage Detector
MPI	Microprocessor Interface
NT	Network Terminator
OLD	Open Loop Detector
PABX	Private Automatic Branch Exchange
$\overline{RD}$	Read
R_{LIM}	Current Limit Programming Resistor
RSRVD	Reserved
S	S Reference Point
S_3–S_0	S Driver Lines 3–0
TE	Terminal Equipment
T/I	Thermal/Interrupt Bit
TOR	Thermal Overload Register
U	U Reference Point
V_B	Battery-control Voltage
V_{BB}	Battery Supply
V_{CC}	+5-V Power Supply
V_{SS}	Substrate Voltage
$\overline{WR}$	Write

CONNECTION DIAGRAM

Top View

24-Pin DIP

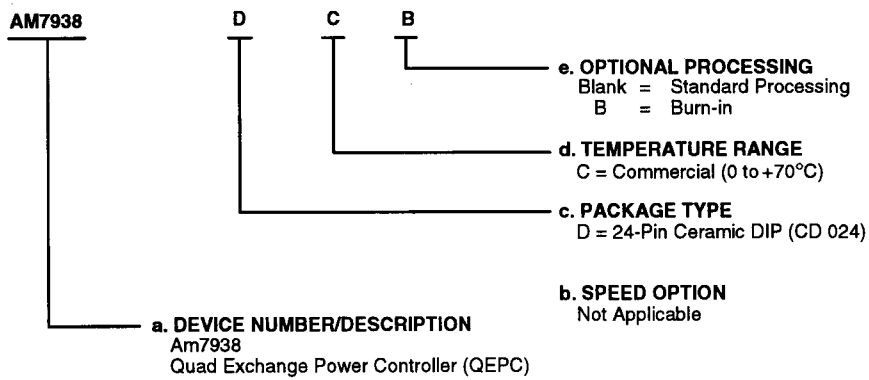


Notes: 1. Pin 1 is marked for orientation.
2. Reserved (RSRVD) pins should not be connected externally to any signal or supply.

ORDERING INFORMATION

AMD standard products are available in several packages and operating ranges. The order number (Valid Combination) is formed by a combination of:

a. Device Number
b. Speed Option (if applicable)
c. Package Type
d. Temperature Range
e. Optional Processing



Valid Combinations	
AM7938	DC, DCB

Valid Combinations

Valid Combinations list configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations, to check on newly released combinations, and to obtain additional data on AMD's standard military grade products.

PIN DESCRIPTION

A_0
Address Line (Input)

A_0 selects source and destination locations for read and write operations on the data bus. A_0 must be valid on the falling edge of ALE or during $\overline{RD}$ and $\overline{WR}$ if ALE is tied High.

ALE
Address Latch Enable (Input; Active High)

ALE is an input control pulse used to strobe the address on the A_0 line into the address latch. This signal is active High to admit the input address. The address is latched on the High–Low transition of ALE. While ALE is High, the address latch is transparent. For an unmultiplexed microprocessor bus, ALE must be tied High.

BGND
Ground Battery

Regulated output on V_B is referenced to this ground.

C_B
Battery Compensation Capacitor

C_B is intended for users who operate the QEPC with an external Darlington transistor (Figure 2) to allow users a simple way of stabilizing the QEPC/Darlington circuit over a wide range of operating conditions. If the voltage on the S-output drivers oscillates due to some instability of the Darlington, a capacitor should be connected to C_B, with the other side of the capacitor connected to V_B.

$\overline{CS}$
Chip Select (Input; Active Low)

$\overline{CS}$ must be Low to enable the read or write operations of the Am7938. Data transfer occurs over the D_3–D_0 lines. The interaction of $\overline{CS}$, $\overline{RD}$, $\overline{WR}$, and D_3–D_0 is described below.

D_3–D_0
Data Bus (Input/Output; Three State, Active High)

The four bidirectional data bus lines are to exchange information with a microprocessor. D_0 is the least significant bit and D_3 is the most significant bit. A High on the data bus corresponds to a logical 1. These lines act as inputs when $\overline{WR}$ and $\overline{CS}$ are active and as outputs when $\overline{RD}$ and $\overline{CS}$ are active. When $\overline{CS}$ is inactive, the D_3–D_0 pins are placed in a high-impedance state.

DGND
Ground Digital

Digital ground to logic.

I_{LIM}
Current Limit Programming (Input)

I_{LIM} programs the current limit of the S drivers using an external resistor connected between I_{LIM} and V_{SS}. The I_{LIM} pin is 1.25 V more positive than V_{SS}. The current limit is 5 mA plus 1000 times the current in the external resistor. The programmed current limit applies to each S driver.

$\overline{INT}$
Interrupt (Output; Open-Collector, Active Low)

$\overline{INT}$ augments the Microprocessor Interface by generating an interrupt when a Current Overload Detector (COD) occurs. $\overline{INT}$ is active whenever any bits in the COD register are active. Note that $\overline{INT}$ is not latched; when the COD register is zero, $\overline{INT}$ goes inactive (High). $\overline{INT}$ will also go inactive if the QEPC automatically disables the S-output driver that caused the interrupt (due to Thermal Overload), or if the microprocessor disables that line via the Line Enable Register (LER). COD interrupts can be masked via the Indirect Address Register (IAR); RESET always disables the $\overline{INT}$ pin.

$\overline{RD}$
Read (Input; Active Low)

The active Low read signal is conditioned by $\overline{CS}$ and transfers internal information to the data bus. If A_0 is a logical 0, logic levels of the Indirect Address Register (IAR) and Thermal Shutdown Status bit will be transferred to D_3–D_0. If A_0 is a logical 1, the data addressed by the IAR will be transferred to D_3–D_0.

RESET
Reset (Input; Active High)

RESET initializes the registers in the Am7938, leaving the S drivers switched off.

S_3–S_0
S Drivers (Output)

S_3–S_0 each supply power to one line. The outputs can sink up to 150 mA each. The voltage at the line is connected to V_{BB} through a saturated transistor switch.

V_B
Battery Reference Voltage (Output)

V_B provides an output proportional to the deviation of V_{BB} from an internal –40 V reference with respect to BGND. V_B can be used as a driver for an external PNP Darlington power transistor supplying power from the battery to V_{BB} (see Figure 2).

V_{BB}
Supply Voltage S Driver (Input)

V_{BB} supplies power to the S drivers.

V_{CC}
+5-V Power Supply (Input)

V_{SS}
Substrate Voltage (Input)

V_{SS} is the internal negative supply voltage. V_{SS} must always be connected to the most negative supply voltage. The MPI Registers will not function properly when the battery power is disconnected, that is, when V_{SS} is floating or grounded. The QEPC should also be reset if a drastic transient is applied to V_{SS}.

$\overline{WR}$
Write (Input; Active Low)

The active Low write signal is conditioned by $\overline{CS}$ and transfers information from the data bus to an internal register selected by A_0. If A_0 is a logical 1, D_3–D_0 is written into the Line Enable Register (LER). If A_0 is a logical 0, D_3–D_0 is written into the IAR. LER and IAR are the only two writable registers in the Am7938.

FUNCTIONAL DESCRIPTION

The Am7938 is divided into two sections, the Analog section and the Microprocessor Interface (MPI) section. The analog section provides power and detects the status of the S lines. This status information is available to the microprocessor via the MPI.

Initialization

The Am7938 is initialized when reset by an external signal applied to the RESET pin. In the initialized state the analog drivers are switched off, the Indirect Address Register (IAR) is cleared, and the internally latched address A_0 is cleared.

–40 V Power

The voltage at the S drivers is approximately V_{BB} (less V_{SAT}). A regulated –40V S output can be achieved by using the V_B pin to drive an external Darlington power transistor.

Analog Section

The major functions of the analog section are the four line drivers, which are saturated Darlington transistor switches capable of sinking up to 150 mA each. The power to the drivers is derived from the negative supply voltage (V_{BB}) to the Am7938. The output voltage to each line is slaved to V_{BB}, and the voltage drop in each driver is approximately 1.5 V.

Line driver protection is provided through the integration of current limit and over-temperature shut-off. The current limit is hardware-programmable via an external resistor (R_{LIM}) connected between I_{LIM} and V_{SS}. The I_{LIM} pin is 1.25 V more positive than V_{SS}. The output limit is: $5\ mA + 1000 \cdot 1.25\ V/R_{LIM}$. This $1000 \times$ gain makes the I_{LIM} pin susceptible to external noise. Care should be taken to connect R_{LIM} as close to the QEPC as possible.

The thermal shut-off is internally set at approximately 175°C. At this temperature all the drivers are unconditionally switched off. However, at approximately 140°C, only the drivers that are in the current-overload condition will be turned off.

Status detectors, associated with each of the line drivers, monitor the load conditions on each line by comparing an electrical parameter (e.g., current and voltage at the line) with a reference level. The output of each detector can be read by the microprocessor. In addition to these status detectors, the temperature of the Am7938 is monitored via integrated temperature detectors. The detectors respond at approximately 140°C and 175°C, as defined above, and the 175°C detector can be monitored by the microprocessor via the MPI. The status detectors provide the following information from each of the lines (all detectors have built-in hysteresis):

Low Output Voltage Detection

The low-output-voltage status bit becomes active when the output transistor is pulled out of saturation.

Open Loop Detection

The open-loop status bit becomes active when the current on the line drops below a minimum value.

Current Overload Detection

The current-overload status bits become active when the current on the line nears the current limit. These bits activate the $\overline{INT}$ output if COD interrupts are enabled via the IAR Register.

Thermal Overload Detection

If the Am7938 device temperature reaches 140°C, then all the line drivers in the current-overload condition will be switched off and the corresponding bits in the Thermal Overload Register will be cleared. If the device temperature increases to 175°C, all the line drivers will be turned off, and all the bits in the Thermal Overload Register will be cleared. The T-bit will also be set, and it can be read along with the Indirect Address Register (IAR) to indicate that all the drivers have been turned off. To initialize any of the bits in the Thermal Overload Register, the microprocessor must first turn off the line drivers via the Line Enable Register (LER) (see MPI definition). The line drivers must not be reactivated until the T-bit in the address register is cleared by the temperature detector in the Am7938.

MPI Section

The MPI allows the user to access the detectors defined in the analog section. The line driver's status bits are grouped by function. Bits 3–0 of the detectors correspond to lines 3–0, respectively. The status groups are:

Low Voltage Detector (LVD)
Open Loop Detector (OLD)
Current Overload Detector (COD)
Thermal Overload Register (TOR)

The data is not latched in these status groups except in the TOR. Thus, the user should filter (multiple samples) the received data to ensure its integrity. There are two other registers in the MPI: the Indirect Address Register (IAR), and Line Enable Register (LER).

The IAR contains 3 bits that address the desired status group or the LER. The IAR is read along with the T-bit defined in the analog section. The microprocessor can read the IAR to check the validity of the address. A 1-µs delay is required between a Write to the LER Register, followed by a Read of that same register. Subsequent reads of the LER do not have this constraint.

The LER is used to enable or disable the individual line drivers. The line drivers will only become active if the corresponding bit in the TOR is inactive. The LER is a read/write register. The MPI contains the interface to the following pins:

D_3–D_0	Bidirectional	Data Bus
A_0	Input	Address Line
ALE	Input	Address Latch Enable
$\overline{RD}$	Input	Read Enable
$\overline{WR}$	Input	Write Enable
$\overline{CS}$	Input	Chip Select
$\overline{INT}$	Output	COD Interrupt

The 4-bit bidirectional data bus (D_3–D_0) is used to communicate with the registers. Access to the registers is controlled by $\overline{CS}$, $\overline{RD}$, $\overline{WR}$, ALE, and A_0 as shown below. A read or write cycle must be preceded by a valid A_0. A_0 is latched internally in a transparent latch by ALE. The selection of the status group or the LER is determined by the content of the IAR.

The truth table for the MPI control is shown below:

$\overline{CS}$	$\overline{RD}$	$\overline{WR}$	A_0	
0	1	0	0	Write IAR (T bit is read only)
0	0	1	0	Read IAR and T bit
0	1	0	1	Write LER
0	0	1	1	Read status groups or LER
1	X	X	X	No access

Indirect Address Register (IAR) and T/I Bit

The IAR is 3 bits wide and accessible through the data port, D_2–D_0. The content of the Indirect Address Register (IAR_2–IAR_0) determines the selection of the status groups or the LER. The thermal overload bit T/I is read and written at the same time as IAR and occupies D_3. This register has the following format:

Bit	Symbol	
0	IAR_0	Bit 0 of the IAR
1	IAR_1	Bit 1 of the IAR
2	IAR_2	Bit 2 of the IAR
3	T/I	T bit: (Read only)
		Logical 0: temperature normal (default value)
		Logical 1: temperature above 175°C (all drivers shut off)
		I bit: (Write only)
		Logical 0: $\overline{INT}$ pin disabled
		Logical 1: COD interrupts enabled via $\overline{INT}$ pin

IAR_2–IAR_0 address the status groups and the LER as shown below:

IAR_2	IAR_1	IAR_0	Select
0	0	0	LVD
0	0	1	OLD
0	1	0	COD
0	1	1	Reserved
1	0	0	Reserved
1	0	1	Reserved
1	1	0	LER
1	1	1	TOR

The contents and format of the status groups and the LER are as follows:

LVD:

Bit	Logical 1	Logical 0 (default value)
0	S_0 low voltage	S_0 voltage normal
1	S_1 low voltage	S_1 voltage normal
2	S_2 low voltage	S_2 voltage normal
3	S_3 low voltage	S_3 voltage normal

The Low Voltage Detector (LVD) indicates the voltage level on the S lines, even when the lines are disabled. Note however, that the detection threshold is slightly different. The low-voltage condition becomes active (logical 1) if the output reaches the Low Voltage Threshold (V_{LVD}).

OLD:

Bit	Logical 1	Logical 0 (default value)
0	S_0 open loop	S_0 current normal
1	S_1 open loop	S_1 current normal
2	S_2 open loop	S_2 current normal
3	S_3 open loop	S_3 current normal

The Open Loop Detector (OLD) indicates the open-loop condition on the S lines. The open-loop condition becomes active (logical 1) if the current on the line drops below the threshold value ISOC.

COD:

Bit	Logical 1	Logical 0 (default value)
0	S_0 current overload	S_0 current normal
1	S_1 current overload	S_1 current normal
2	S_2 current overload	S_2 current normal
3	S_3 current overload	S_3 current normal

The Current Overload Detector (COD) indicates the current-overload condition on the S lines. The overload condition becomes active (logical 1) if the output current approaches the value programmed by an external resistor between I_{LIM} and V_{SS}.

TOR:

Bit	Logical 1 (default value)	Logical 0
0	S_0 operational	S_0 off
1	S_1 operational	S_1 off
2	S_2 operational	S_2 off
3	S_3 operational	S_3 off

The Thermal Overload Register (TOR) contains the overload status of the S line drivers. If the Am7938 device temperature reaches 140°C, then the S line drivers that are in the current-overload condition will be switched off. The corresponding bits in the TOR will be set to a logical 0 . To initialize any of the bits in the TOR, the microprocessor must first turn off the S line drivers via the LER. However, the TOR bits cannot be deactivated if the 175°C detector is active. The µP may reenable the S drivers via the LER after the TOR condition is removed. The TOR is a read-only register.

LER:

Bit	Logical 1	Logical 0 (default value)
0	S_0 on	S_0 off
1	S_1 on	S_1 off
2	S_2 on	S_2 off
3	S_3 on	S_3 off

The Line Enable Register (LER) is used to enable or disable the individual S line drivers. The S line will only become active if the corresponding bit in the TOR is set to a logical 1. The LER can be written directly and read indirectly.

APPLICATIONS

The Am7938 major applications are in intelligent NTs, and in PABX and Central Office line cards. The applications show the Am7938 interfaced to the CCITT S interface point; however, the Am7938 can be used to control the power feed for any transformer coupled system, that is, the CCITT U interface point.

The Am7938 Used With a Regulated Supply

Figure 1 shows the Am7938 used with a regulated supply voltage of $V_{BB} = -40\ V - V_{SAT}$. The output voltage from the S drivers (because of the voltage drop across the internal transistors) will be V_{SAT} more positive than V_{BB}. The V_B and C_B pins are unused; V_{SS} is tied to V_{BB}. Other battery voltages can be used. The Am7938 can power up to eight TEs per S line provided the total current per line does not exceed 150 mA.

Recommended Decoupling:
- ≥ 10 µF from V_{CC} to DGND
- 0.1 µF from V_{CC} to DGND
- 1.0 µF from V_{SS} to DGND
- V_{SS} shorted to V_{BB}
- DGND shorted to BGND

The Am7938 Used With an External Power Transistor

Power to the Am7938 is supplied from the local battery with an external power transistor to dissipate power from the Am7938. The Am7938 allows battery voltages up to –65 V provided the external power transistor can handle the power dissipation (see Figure 2).

Recommended Decoupling:
- ≥ 10 µF from V_{CC} to DGND
- 0.1 µF from V_{CC} to DGND
- 1.0 µF from V_{SS} to DGND
- 0.1 µF from V_{BB} to DGND
- TBD µF from C_B to V_B
- DGND shorted to BGND

The Am7938 Employing a Relay to Provide Polarity Reversal

The CCITT recommends that polarity reversal be used to resolve the power contention in a point-to-multipoint configuration when local power is lost. In Figure 3, polarity reversal is implemented using the Am7938 and one additional relay. The coil and contacts of the relay are connected so that the relay is activated when local power is available, and is deactivated when local power is lost. Hence, power consumption is minimized when local power is lost.

An alternative solution for power contention resolution is to power only a few lines when local power is lost. In the Am7938, each line is independently controlled via the microprocessor through the LER, hence, the microprocessor can turn off non-priority lines as required.

Four Am7938s Interfaced to a Microprocessor Bus

Figure 4 illustrates four Am7938s interfaced to a microprocessor. Only the lower four data lines from the microprocessor's 8-bit data bus are used. These are connected to the Am7938's D_3–D_0 pins. In a non-multiplexed microprocessor bus system ALE must be tied to a logical 1.

Protection of the QEPC Against Overvoltage

In Central Office (CO) or long-line PABX applications, the QEPC requires additional external protection against lightning and voltages induced from the power lines.

Figure 5 shows how the QEPC and the system is protected via an overvoltage-limiting device and fuse resistors.

The voltage-limiting device limits the voltage on the S line to a safe value, and the fuse resistors break the circuit if a continuous high-power source is connected to the S line. The diode in the battery line prevents the line surges from going below the substrate voltage.

General Information

$\overline{INT}$ should be connected to an edge-triggered input on the controlling microprocessor since $\overline{INT}$ is not latched. In this way, the microprocessor interrupt logic will latch the fact that $\overline{INT}$ went Low. $\overline{INT}$ is an open-collector output so that multiple QEPCs can be wire-ORed to produce a single interrupt for all QEPCs on a line card. It is impossible to read the Current Overload Interrupt mask since the interrupt mask bit is shared with the Thermal Shutdown bit (MSB of the IAR). Therefore, it is prudent to keep a RAM copy of the interrupt mask if this status is required for the application.

The microprocessor should enable one S Output Driver at a time (via the LER) to avoid undue current surges through the QEPC. This is due to the inherently inductive nature of the S Interface Lines. The user should expect the corresponding bits in the COD Register to momentarily become active when the Line has just been enabled. Because of this, it is recommended to mask the COD Interrupt (via the IAR Register) until all desired lines are enabled. In addition, for highly inductive lines, the user should connect a 0.01-µF capacitor from each S Output Driver pin to V_{SS}. Protective diodes should also be connected to S Output Drivers under these conditions (see Figure 5).

The COD Interrupt Service Routine should not blindly assume that the S Interface Line corresponding to the COD bit is shorted and immediately disable that line. A short circuit condition can be determined by the presence of a COD and a Low Voltage Detector (LVD) on the same line. This fact should be considered if the line

normally operates near the programmed current limit (set by R_{LIM}). Also, a momentary COD Interrupt may be generated by an additional load if the line was already operating near the programmed current limit. The COD Interrupt Service Routine should read the COD Register again to determine if the COD was a transient spike.

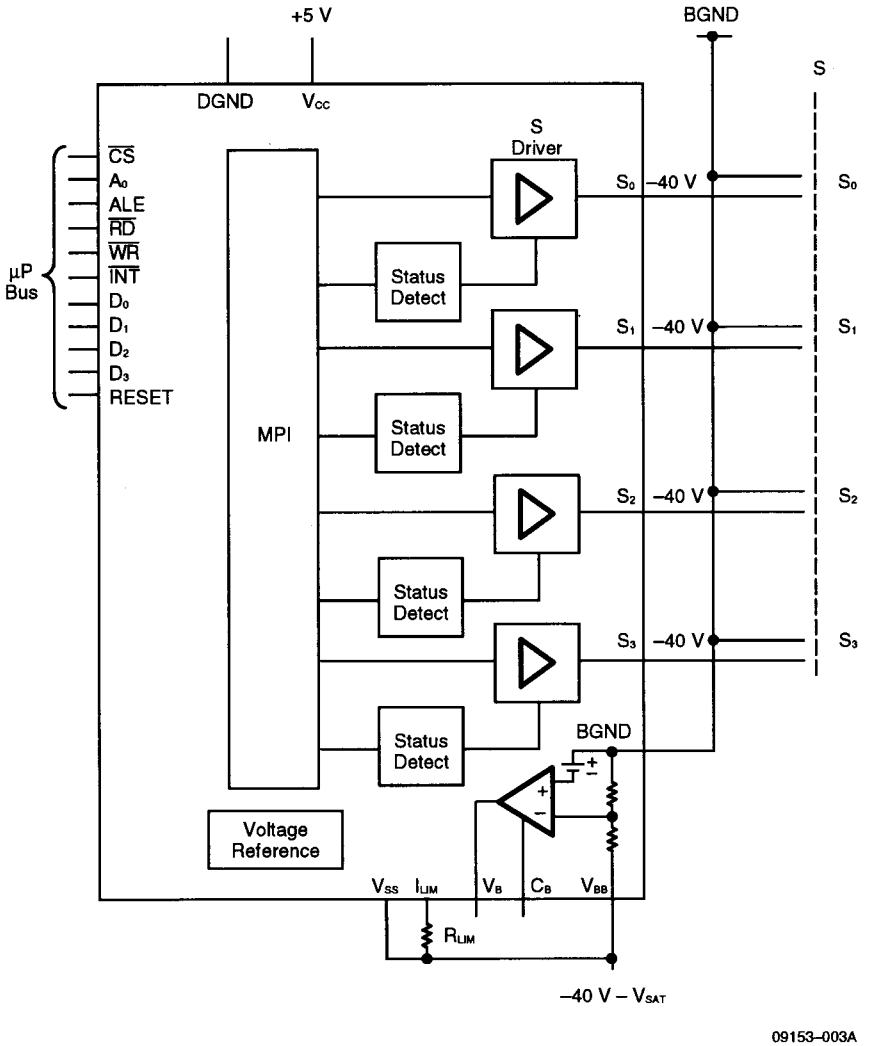


Figure 1. The Am7938 Used With a Regulated Supply
(other battery/S_{out} voltages can be used)

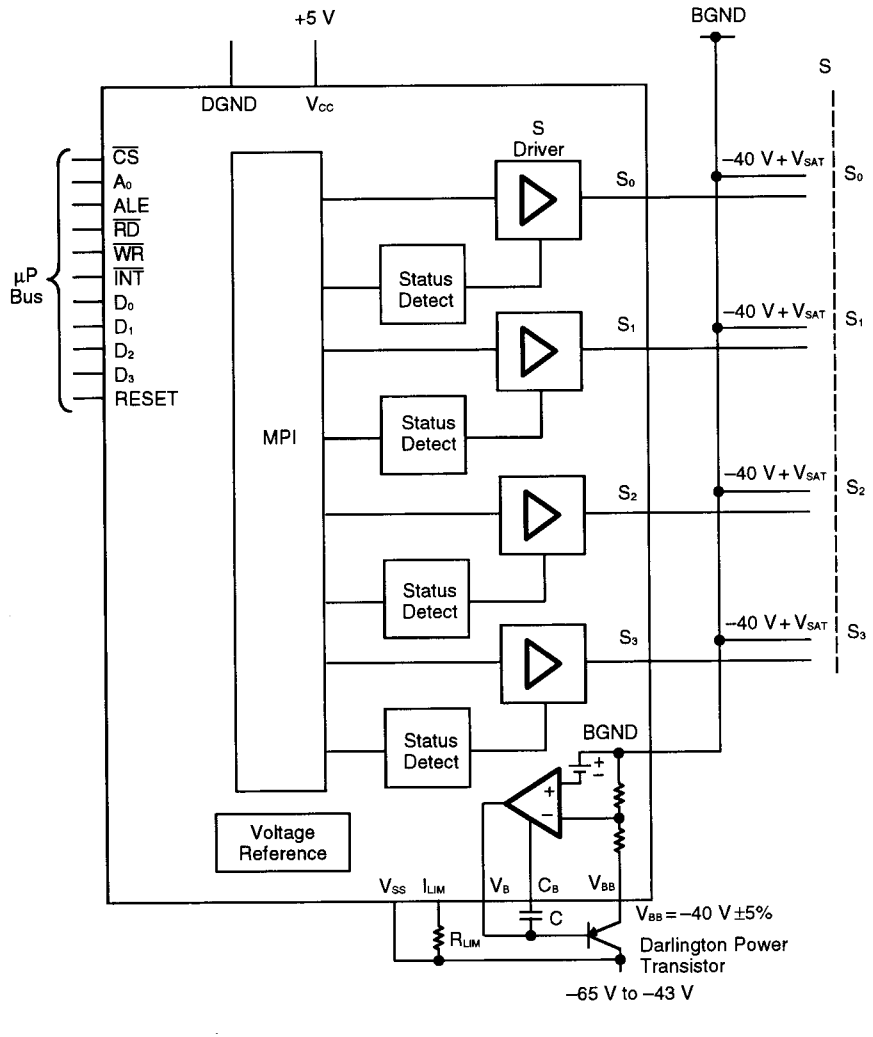


Figure 2. The Am7938 Used With an External Power Transistor

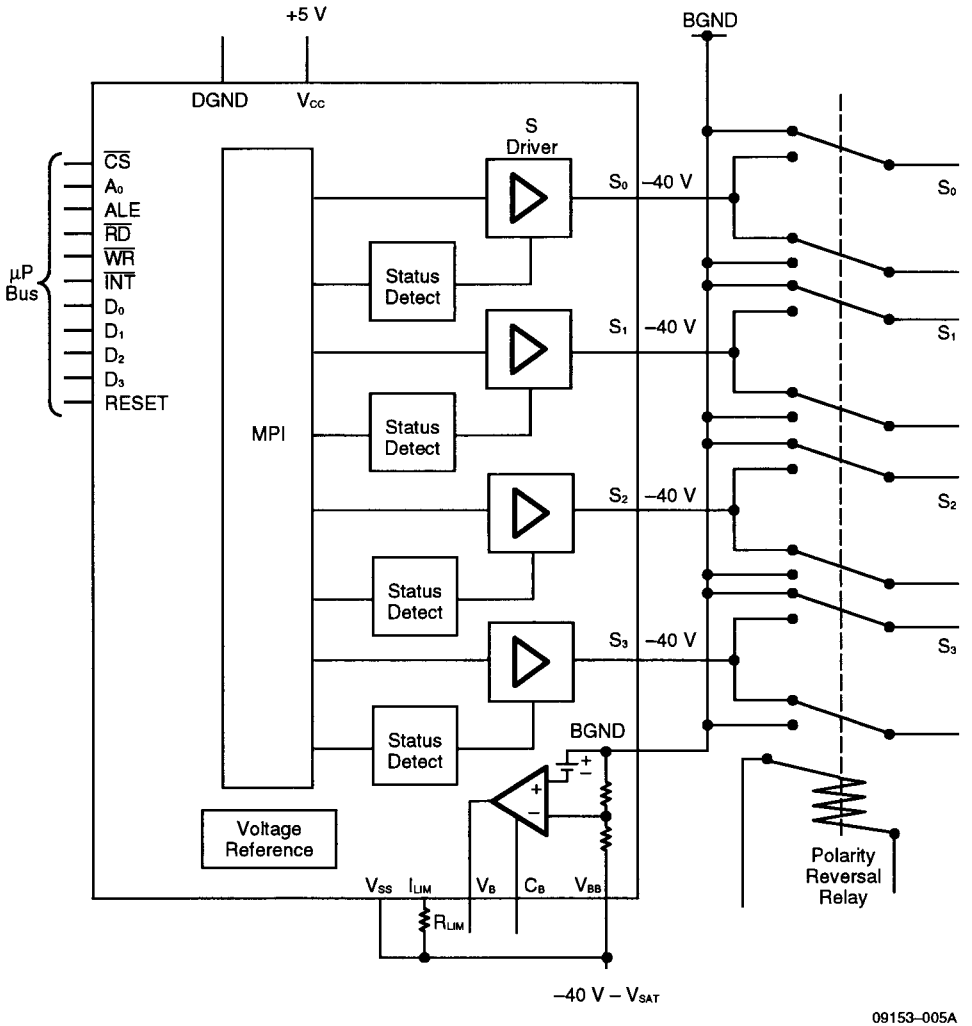


Figure 3. The Am7938 Employing a Relay to Provide Polarity Reversal

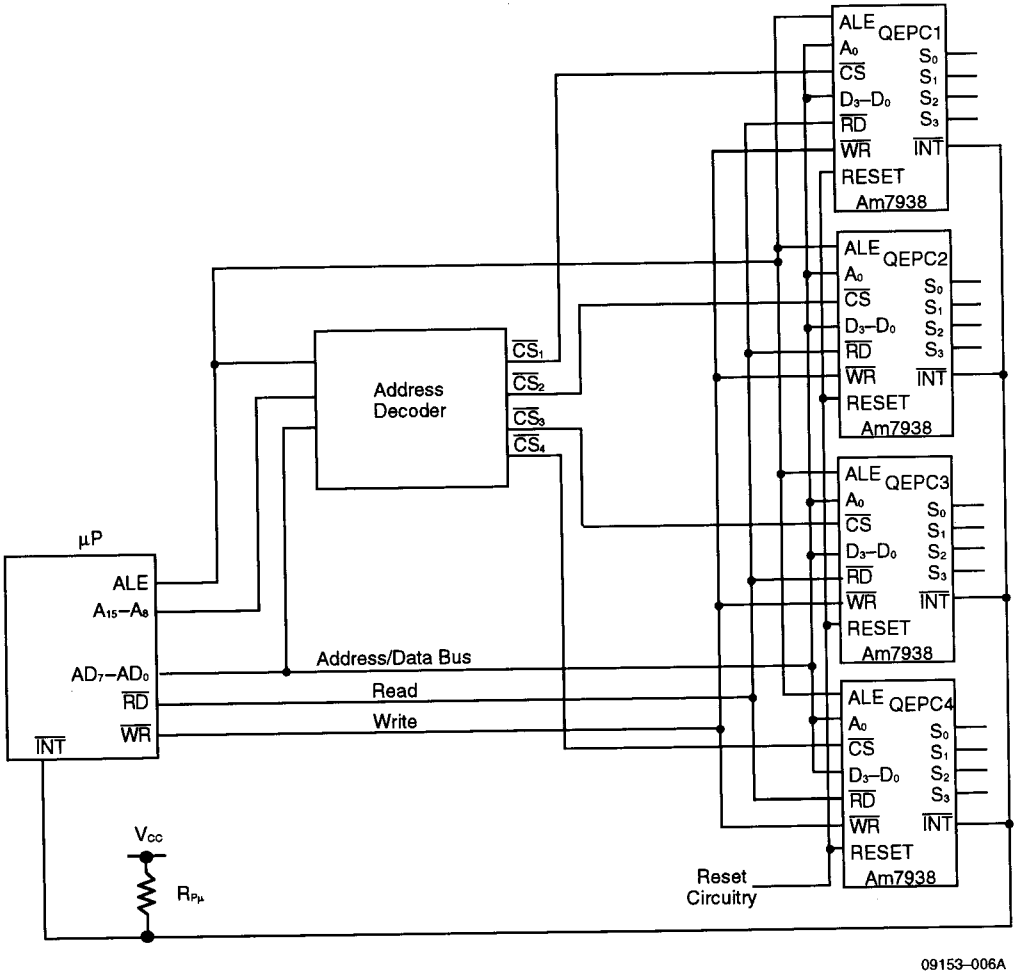


Figure 4. Four Am7938s Interfaced to a Microprocessor Bus

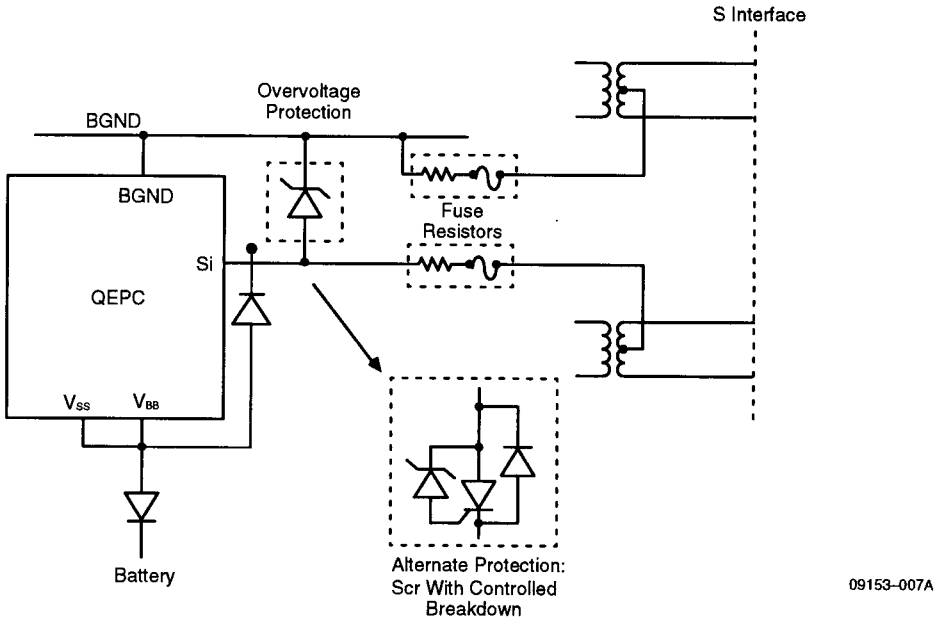
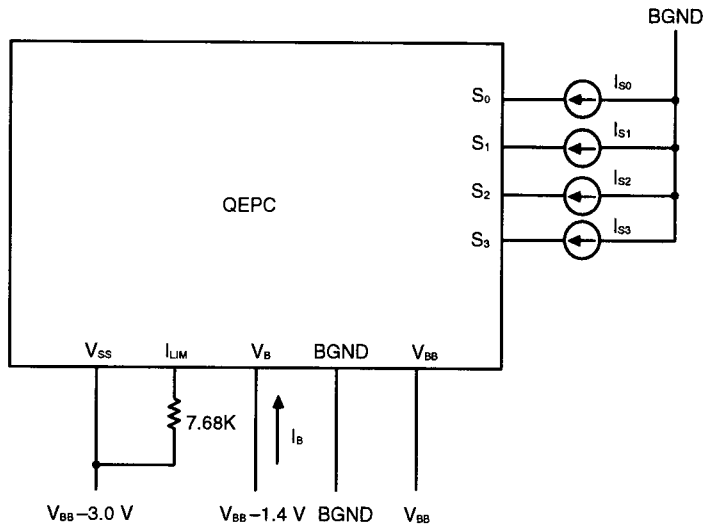


Figure 5. Protection of the QEPC Against Overvoltage



I_{Si} = Current at S Output Driver i, where i = 0–3

Figure 6. Current Into V_B

ABSOLUTE MAXIMUM RATINGS

Storage Temperature ..... –60°C to +150°C
Voltage from Digital Input
to DGND ..... –0.4 V to V_{CC}
Voltage from V_{CC}
to DGND ..... –0.4 V to 7 V
Voltage from V_{SS}
to DGND ..... –70 V to +0.4 V
Voltage from V_{BB}
to DGND ..... (V_{SS} –0.4 V) to +0.4 V
..... and (V_{CC} –70 V) to +0.4 V

100-ns Pulse Voltage from Si
to DGND (Notes 1 and 3) ..... –90 V to + 2 V
Voltage from BGND
to DGND ..... V_{SS} to V_{CC}

Stresses above those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to absolute maximum ratings for extended periods may affect device reliability.

OPERATING RANGES (Note 2)

Commercial (C) Devices
Ambient Temperature(T_A) ..... 0°C to +70°C
DGND ..... 0 V
BGND Voltage ..... –2 V to + 0.5 V
V_{CC} Voltage ..... +5 V ± 5%
V_{BB} Voltage ..... –65 V to –38 V
V_{SS} Voltage, V_B Unused ..... V_{BB}
V_{SS} Voltage, V_B Used ..... –65 V to –43 V

Operating ranges define those limits between which the functionality of the device is guaranteed.

Notes:
1. Si stands for S_0, S_1, S_2, or S_3 outputs.

2. Operation at smaller V_{BB} magnitudes is possible, but parameters are not guaranteed. V_{BB} must be at least –15 V with respect to BGND.

3. The test condition is specified with a diode in series with V_{SS} as shown in Figure 5.

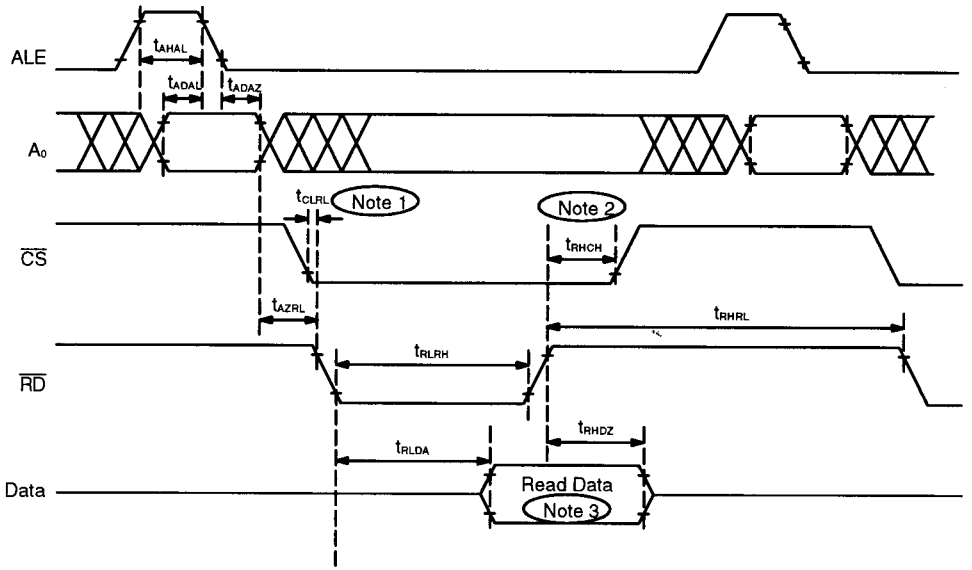
DC CHARACTERISTICS over commercial operating range

Parameter Symbol	Parameter Description	Test Conditions	Min	Typ	Max	Unit
V_{IH}	Logic Input High Level		2.0			V
V_{IL}	Logic Input Low Level				0.8	V
I_{OH}	Logic Output High Current	(V_{OH} = 2.4 V)	400			µA
I_{OL}	Logic Output Low Current	(V_{OL} = 0.4 V)	2.0			mA
I_{IH}	Logic Input High Current	(V_{IH} = 2.0 V)			10	µA
I_{IL}	Logic Input Low Current	(V_{IL} = 0.8 V)			60	µA
I_{OZH}	Output Hi-Z Current High	(2.4 V < V_{OZ} < V_{CC})			10	µA
I_{OZL}	Output Hi-Z Current Low	(0 V < V_{OZ} < 0.4 V)			10	µA
I_{CC}	V_{CC} Supply Current			17	TBD	mA
C_L	Logic Input/Output Capacitance			10		pF
V_{SAT}	Saturation Voltage	($V_{Si} - V_{BB}$), I_{Si} = 150 mA			2.0	V
I_B	Current Into V_B (see Figure 6)	V_{BB} = –42 V			80	µA
		V_{BB} = –38 V	1200			µA
I_{SS}	V_{SS} Supply Current	V_{SS} = –65 V, V_{BB} = –40 V		1.5	TBD	mA
I_{BB}	V_{BB} Supply Current, V_{BB} = –42 V	(Outputs Disabled)		2.6	TBD	mA
I_{SLIM}	Limit Current	R_{LIM} = 8.62K	TBD	150	TBD	mA
		R_{LIM} = 27.8K	TBD	50	TBD	mA
V_{LVD}	Low Voltage Detector	Si off		1.7	TBD	V
	Relative to V_{BB}	Si on		3	TBD	V
I_{SOL}	Current Overload Detector(I_{SLIM})		TBD	85	TBD	%
I_{SOC}	Current at Open Circuit Detector		TBD	5	TBD	mA
I_{SZ}	S_i Current to Ground, S_i Disabled	S_i is i-th output		50	TBD	µA
H_{LVD}	Low Voltage Detector Hysteresis			60		mV
H_{OLD}	Open Loop Detector Hysteresis			1		mA
H_{COD}	Current Overload Detector Hysteresis			2.6		mA
H_{140}	Thermal Detector (140°C) Hysteresis			15		°C
H_{175}	Thermal Detector (175°C) Hysteresis			15		°C

SWITCHING CHARACTERISTICS over operating range

Parameter Number	Parameter Symbol	Parameter Description	Min	Max	Unit
Microprocessor Read/Write Timing					
1	t_{RLRH}	$\overline{RD}$, $\overline{CS}$ Pulse Width	220		ns
2	t_{RHRL}	$\overline{RD}$ Recovery Time	200		ns
3	t_{RLDA}	$\overline{RD}$, $\overline{CS}$ Low to Data Available		220	ns
4	t_{RHDZ}	$\overline{RD}$ or $\overline{CS}$ High to Data Hi Z		110	ns
5	t_{AHAL}	ALE Pulse Width	60		ns
6	t_{ADAL}	Address Setup Time	30		ns
7	t_{ADAZ}	Address Hold Time	30		ns
8	t_{AZRL}	Address Hi Z to $\overline{RD}$ Low	0		ns
9	t_{WLWH}	$\overline{WR}$ or $\overline{CS}$ Pulse Width	200		ns
10	t_{WHWL}	Write Recovery Time	200		ns
11	t_{DAWH}	Data Setup Time	100		ns
12	t_{WHDZ}	Data Hold Time	30		ns
Reset Timing					
13	t_{RES}	Reset Pulse Width	200		ns
14	t_{PHRL}	Power Stable to Reset Low	1		µs
15	t_{ACC}	Reset Recovery Time to Access	700		ns
Si Timing			**Typ**		
16	t_{EN}	Si Output Enable Time (from LER)	1		µs
17	t_{DIS}	Si Output Disable Time (from LER or RESET)	2		µs

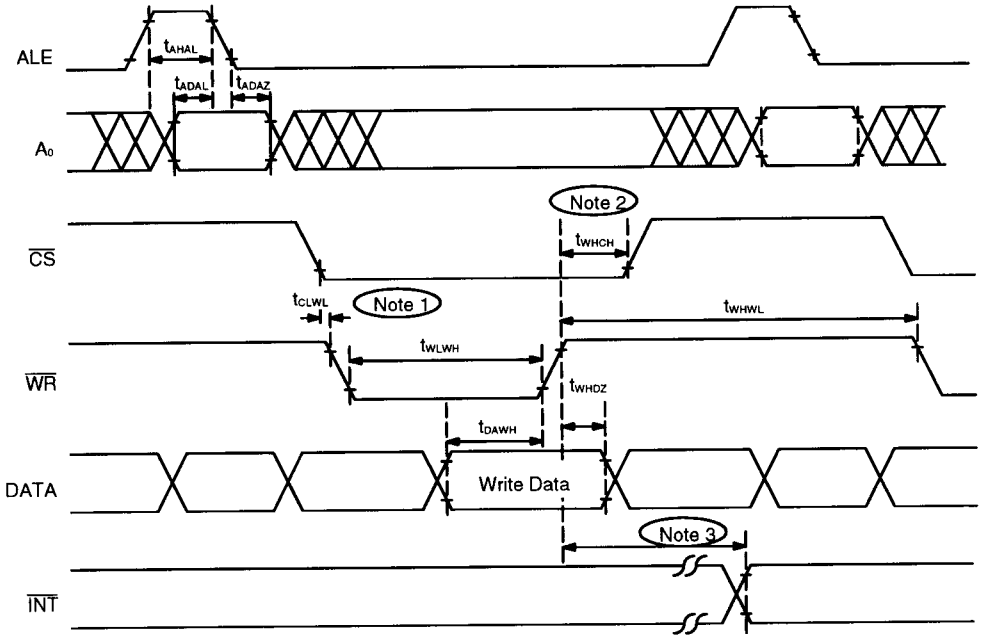
Note: All switching characteristics tests are performed with a 100-pF test load, and TTL-compatible voltage levels.



Notes:

1. If t_{CLRL} is negative, t_{RHRL}, t_{RLRH}, t_{AZRL}, and t_{RLDA} are measured from $\overline{CS}$ rathar than $\overline{RD}$.
2. If t_{RHCH} is negative, t_{RHRL}, t_{RLRH}, and t_{RHDZ} are measured from $\overline{CS}$ rather than $\overline{RD}$.
3. When a read from the LER immediately follows a write to the LER, a minimum of 1 µs is required between these operations. This is to allow the internal buffers in the Am7938 to settle. Subsequent reads from the status group or the LER do not have this restriction.

Figure 7. Microprocessor Read Timing



Notes:
1. If t_{CLWL} is negative, t_{WHWL} and t_{WLWH} are measured from $\overline{CS}$ rather than $\overline{WR}$.
2. If t_{WHCH} is negative, t_{WHWL}, t_{WLWH}, t_{DAWH}, and t_{WHDZ} are measured from $\overline{CS}$ rather than $\overline{WR}$.
3. The propagation delay from the writing of the T/I bit to the effect on the $\overline{INT}$ pin is approximately 1.3 µs for both mask and enable operations.

Figure 8. Microprocessor Write Timing

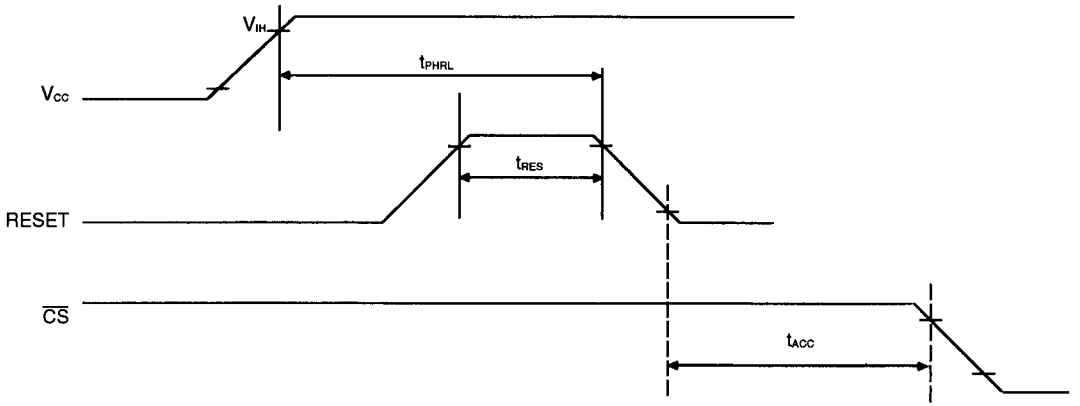


Figure 9. Reset Timing

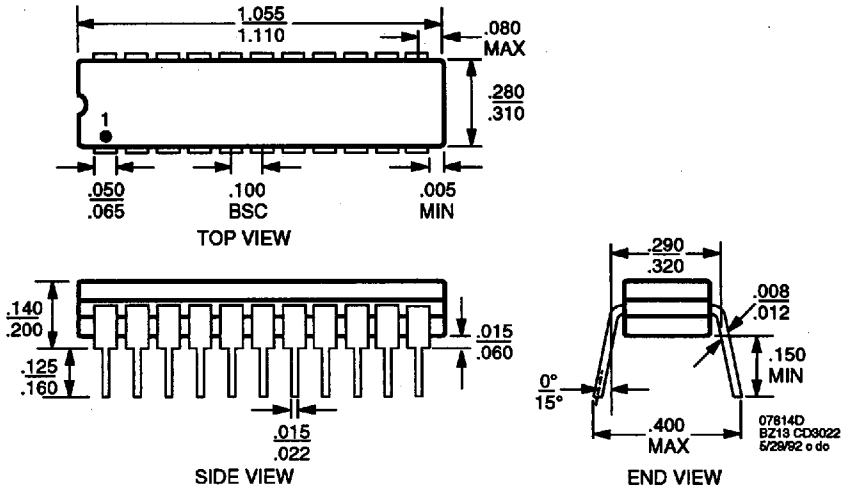
09153–010A

PHYSICAL DIMENSIONS

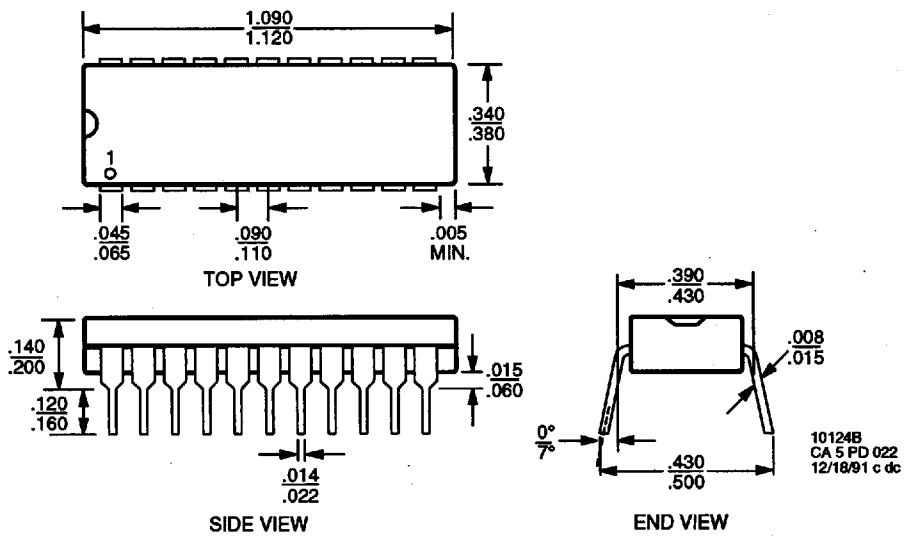
Preliminary; package in development. BSC is an ANSI standard for Basic Space Centering. Dimensions are measured in inches or millimeters.

T-90-20

CD022



PD022



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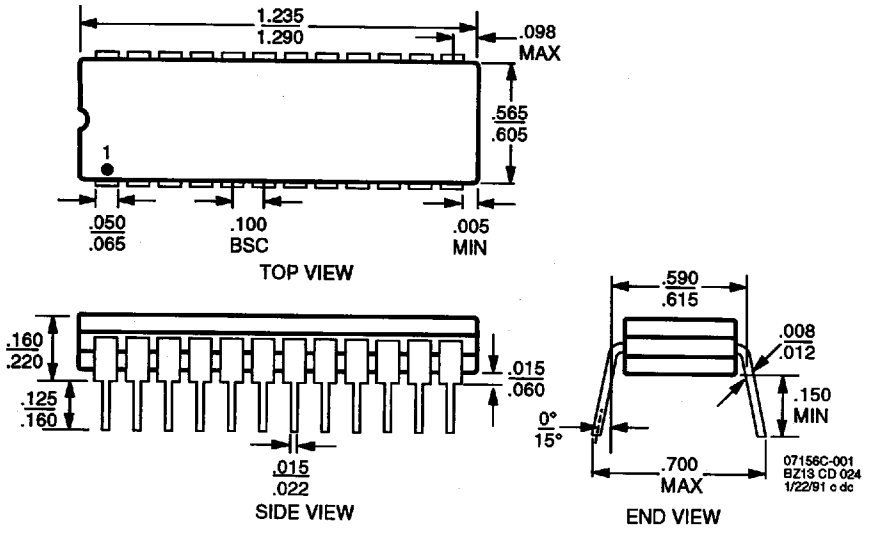

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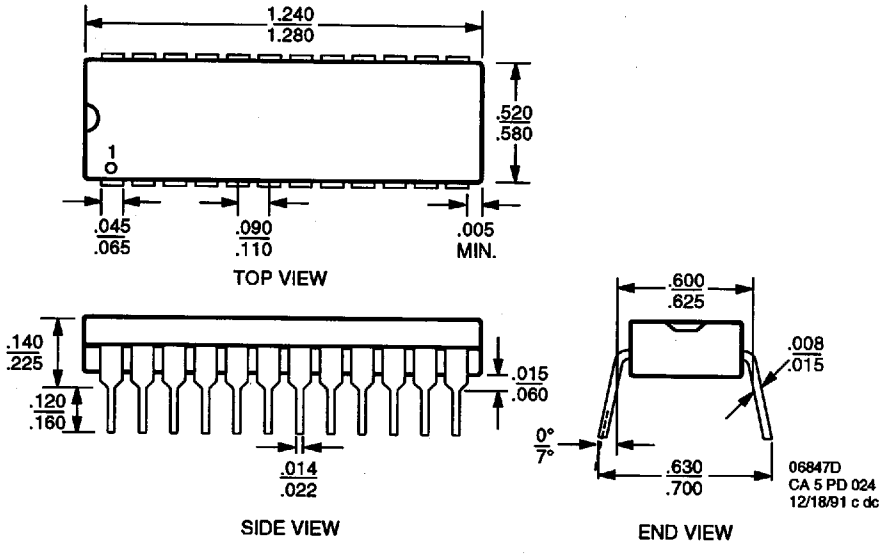
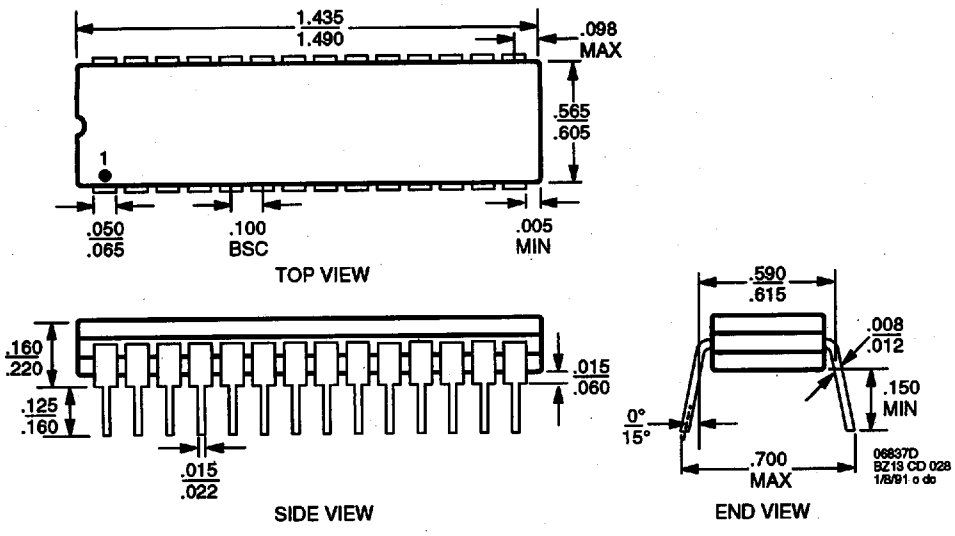


CD028



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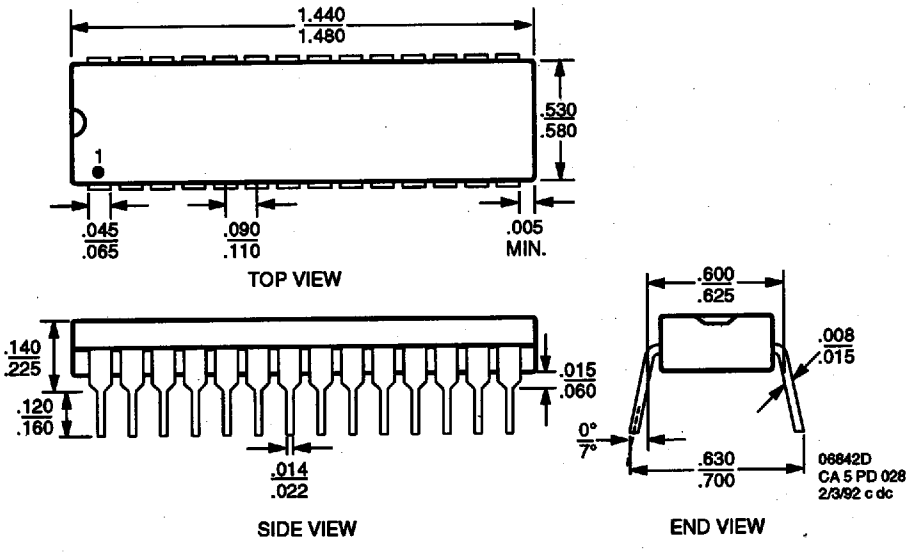
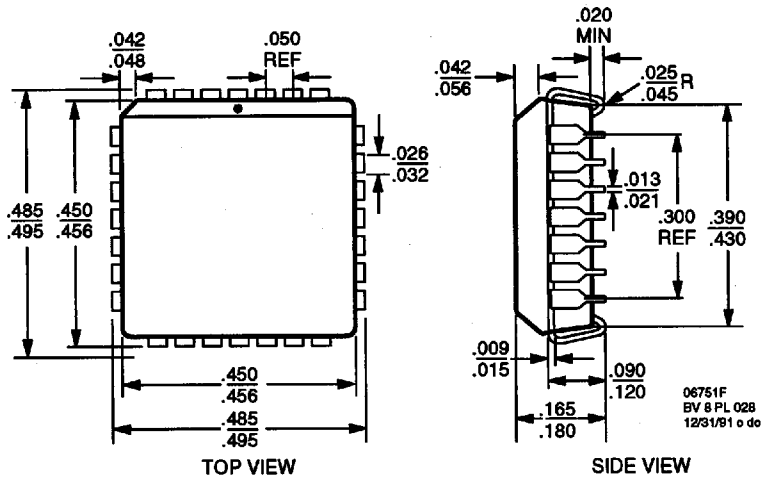
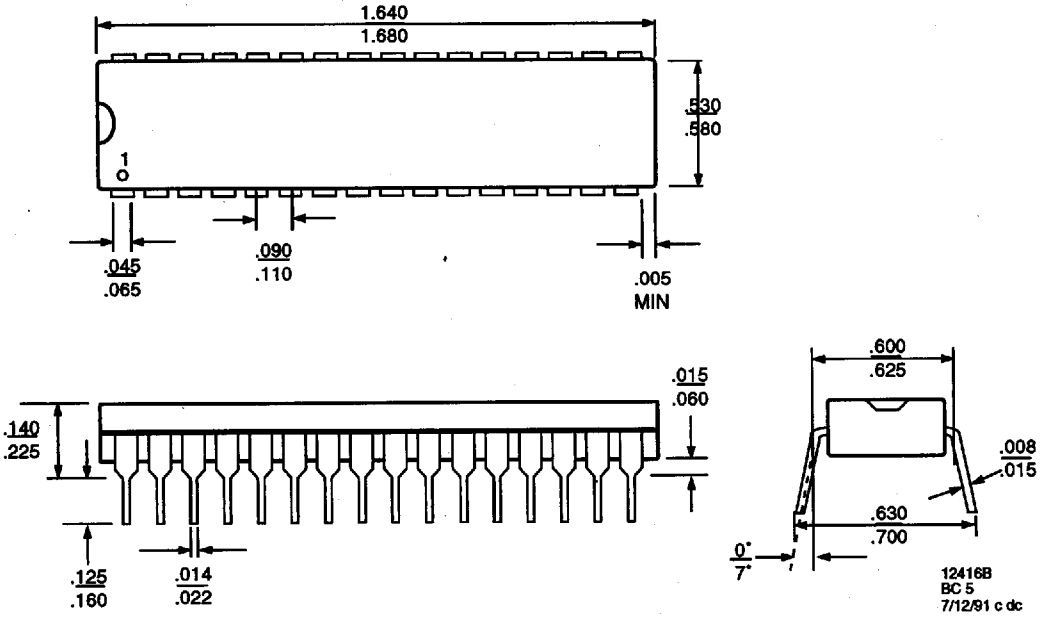


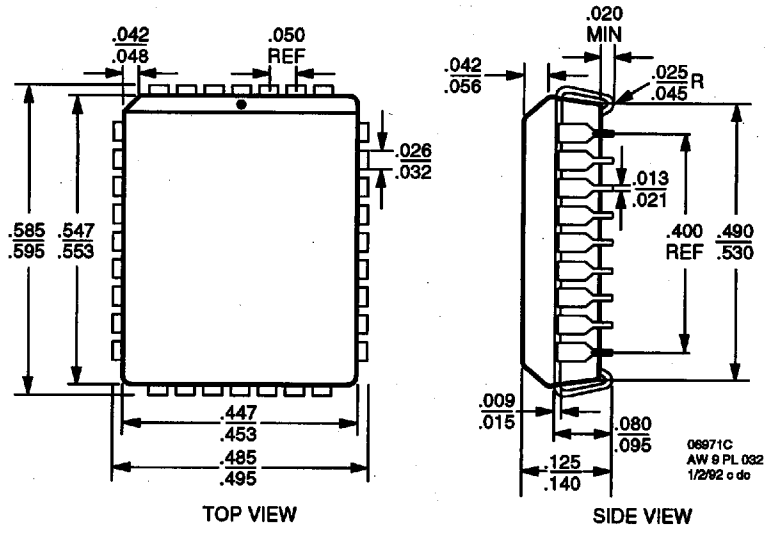
PL028



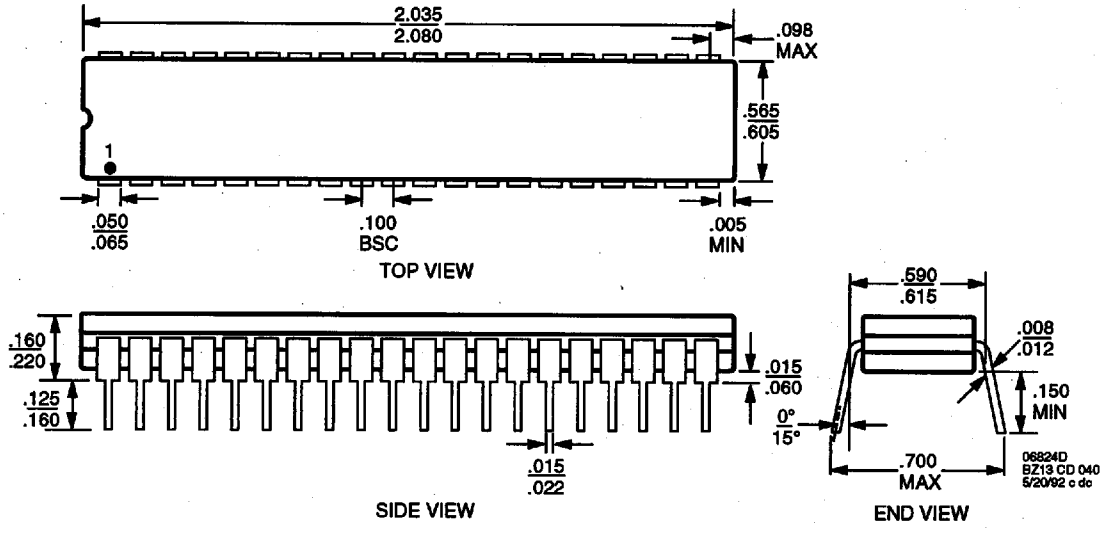
PD 032



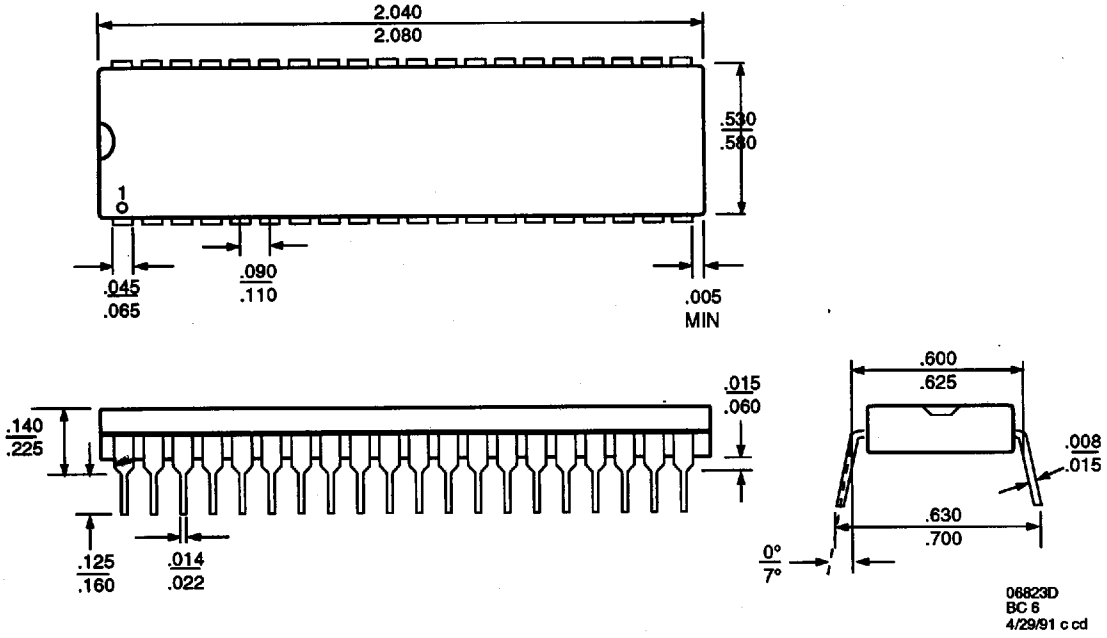
PL032



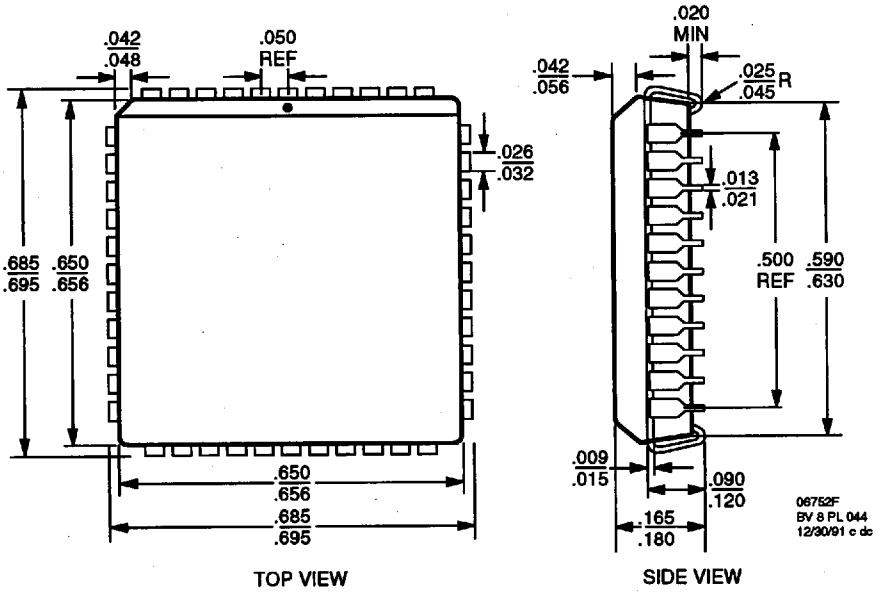
CD040



PD 040



PL044



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