

# Am7943

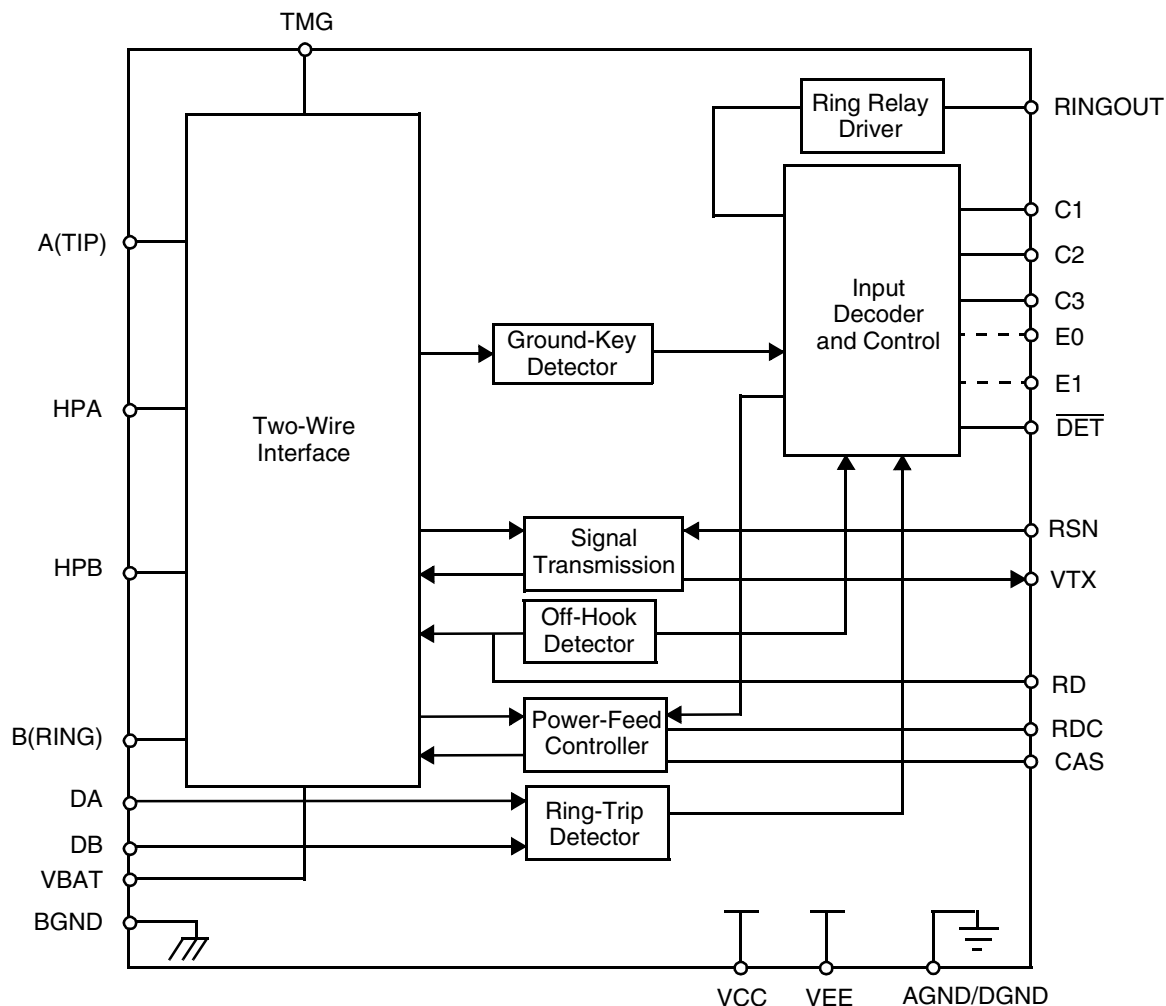
## Subscriber Line Interface Circuit



### DISTINCTIVE CHARACTERISTICS

- Programmable constant-current feed
- Current gain = 200
- Programmable loop-detect threshold
- Low power Standby state
- Performs polarity reversal
- Ground-key detector
- Tip Open state for ground-start lines
- -19 V to -58 V battery operation
- Two-wire impedance set by single external impedance
- On-hook transmission
- On-chip ring relay driver and relay snubber circuit
- On-chip Thermal Management (TMG) feature
- Ideal for DLC and PABX applications

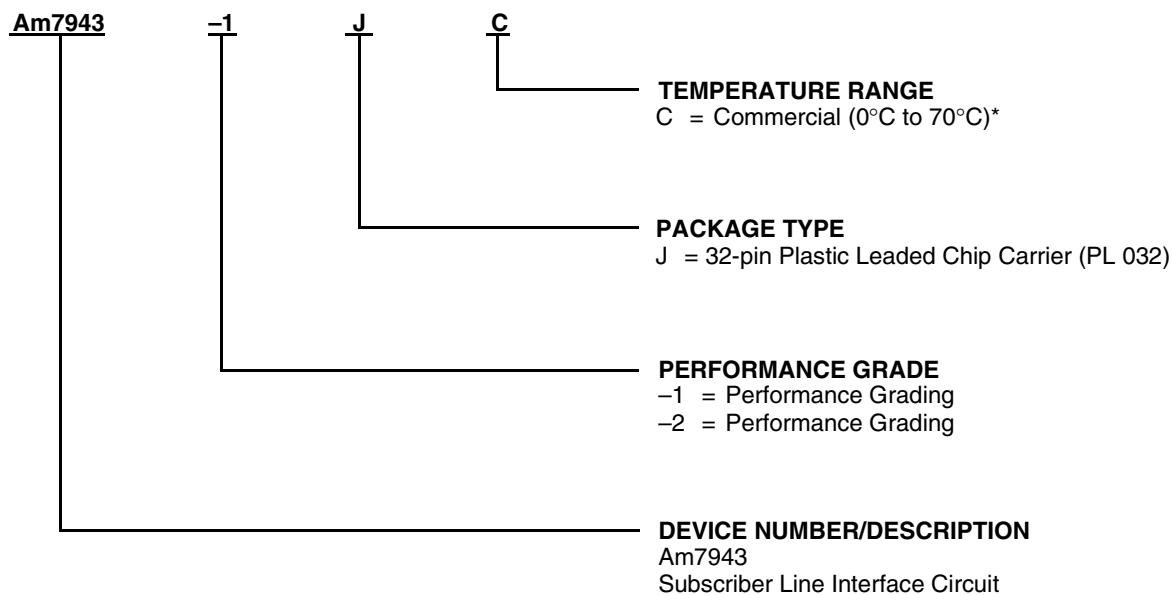
### BLOCK DIAGRAM



## ORDERING INFORMATION

### Standard Products

Legerity standard products are available in several packages and operating ranges. The order number (Valid Combination) is formed by a combination of the elements below.



Valid Combinations		
Am7943	-1	JC
	-2	

#### Valid Combinations

Valid Combinations list configurations planned to be supported in volume for this device. Consult the local Legerity sales office to confirm availability of specific valid combinations, to check on newly released combinations, and to obtain additional data on Legerity's standard military-grade products.

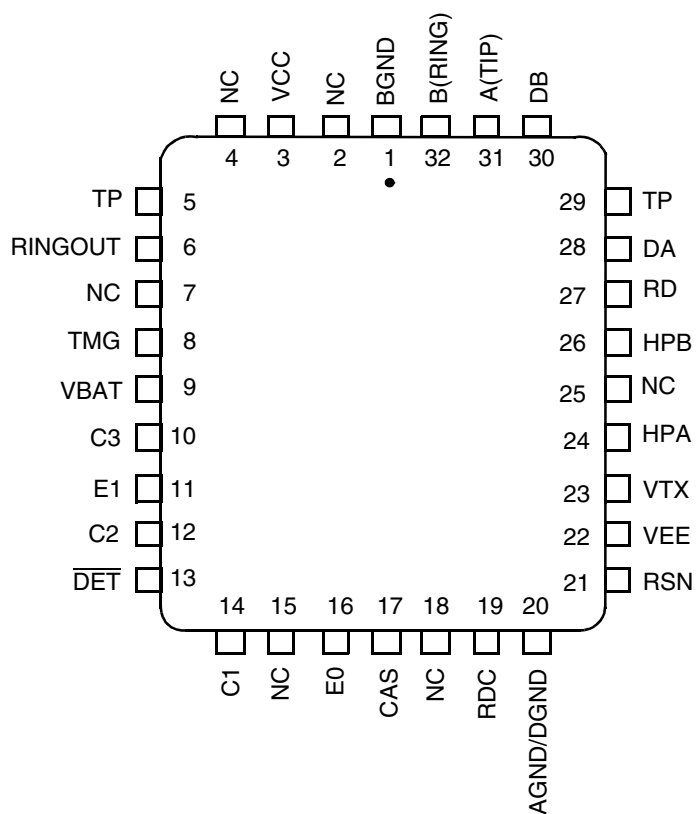
#### Note:

\* Functionality of the device from 0°C to +70°C is guaranteed by production testing. Performance from -40°C to +85°C is guaranteed by characterization and periodic sampling of production units.

## CONNECTION DIAGRAM

### Top View

#### 32-Pin PLCC



#### Notes:

1. Pin 1 is marked for orientation.
2. TP is a thermal conduction pin tied to substrate.
3. NC = No Connect

## PIN DESCRIPTIONS

Pin Names	Type	Description
AGND/DGND	Gnd	Analog and Digital ground
A(TIP)	Output	Output of A(TIP) power amplifier
BGND	Gnd	Battery (power) ground
B(RING)	Output	Output of B(RING) power amplifier
C3–C1	Input	Decoder. TTL compatible. C3 is MSB and C1 is LSB.
CAS	Capacitor	Anti-saturation pin for capacitor to filter reference voltage when operating in anti-saturation region.
DA	Input	Ring-trip negative. Negative input to ring-trip comparator.
DB	Input	Ring-trip positive. Positive input to ring-trip comparator.
$\overline{\text{DET}}$	Output	Switchhook detector. When enabled, a logic Low indicates the selected detector is tripped. The detector is selected by the logic inputs (C3–C1, E1–E0). The output is open-collector with a built-in 15 k $\Omega$ pull-up resistor.
E0	Input	$\overline{\text{DET}}$ Enable. A logic High enables $\overline{\text{DET}}$ . A logic Low disables $\overline{\text{DET}}$ . ( $\overline{\text{DET}}$ = Logic High). (PLCC only)
E1	Input	Ground-Key Enable. E1 = Low connects the ground-key or ring-trip detector to $\overline{\text{DET}}$ . E1 = High connects the off-hook or ring-trip detector to $\overline{\text{DET}}$ . (PLCC only)
HPA	Capacitor	High-Pass Filter Capacitor. A(TIP) side of high-pass filter capacitor.
HPB	Capacitor	High-Pass Filter Capacitor. B(RING) side of high-pass filter capacitor.
RD	Resistor	Detector resistor. Threshold modification and filter point for the off-hook detector.
RDC	Resistor	DC feed resistor. Connection point for the DC feed current programming network. The other end of the network connects to the receiver summing node (RSN). The sign of $V_{\text{RDC}}$ is negative for normal polarity and positive for reverse polarity.
RINGOUT	Output	Ring Relay Driver. Open-collector driver with emitter internally connected to BGND.
RSN	Input	Receive Summing Node. The metallic current (AC and DC) between A(TIP) and B(RING) is equal to 200 times the current into this pin. The networks that program receive gain, two-wire impedance, and feed current all connect to this node.
TMG	—	Thermal management. A resistor connected from this pin to VBAT reduces the on-chip power dissipation in the normal polarity, Active state only. Refer to Table 2.
TP	Thermal	Thermal pin. Connection for heat dissipation. Internally connected to substrate (VBAT). Leave as open circuit or connected to VBAT. In both cases, the TP pins can connect to an area of copper on the board to enhance heat dissipation.
VBAT	Battery	Battery supply
VCC	Power	+5 V power supply
VEE	Power	–5 V power supply
VTX	Output	Transmit Audio. This output is a unity gain version of the A(TIP) and B(RING) metallic voltage. VTX also sources the two-wire input impedance programming network.

## ABSOLUTE MAXIMUM RATINGS

Storage temperature	−55°C to +150°C
$V_{CC}$ with respect to AGND/DGND	−0.4 V to +7.0 V
$V_{EE}$ with respect to AGND/DGND	+0.4 V to −7.0 V
$V_{BAT}$ with respect to AGND/DGND:	
Continuous	+0.4 V to −70 V
10 ms	+0.4 V to −75 V
BGND with respect to AGND/DGND	+3 V to −3 V
A(TIP) or B(RING) to BGND:	
Continuous	−70 V to +1 V
10 ms (f = 0.1 Hz)	−70 V to +5 V
1 ms (f = 0.1 Hz)	−80 V to +8 V
10 $\mu$ s (f = 0.1 Hz)	−90 V to +12 V
Current from A(TIP) or B(RING)	$\pm 150$ mA
Current from TMG	100 mA
Voltage on RINGOUT:	
During transient	BGND to +10 V
During steady state	BGND to +7 V
Current through relay drivers	60 mA
DA and DB inputs	
Voltage on ring-trip inputs	$V_{BAT}$ to 0 V
Current into ring-trip inputs	$\pm 10$ mA
C3–C1, E0, E1	
to AGND/DGND	−0.4 V to $V_{CC}$ +0.4 V
Maximum power dissipation, $T_A = 85^\circ\text{C}$	
No heat sink (see note):	
In 32-pin PLCC package	1.4 W
Thermal data	$\theta_{JA}$
In 32-pin PLCC package	43°C/W typ

**Note:** Thermal limiting circuitry on chip will shut down the circuit at a junction temperature of about 165°C. The device should never be exposed to this temperature. Operation above 145°C junction temperature may degrade device reliability. See the SLIC Packaging Considerations for more information.

Stresses above those listed under Absolute Maximum Ratings may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to Absolute Maximum Ratings for extended periods may affect device reliability.

## OPERATING RANGES

### Commercial (C) Devices

Ambient temperature	0°C to +70°C*
$V_{CC}$	4.75 V to 5.25 V
$V_{EE}$	−4.75 V to −5.25 V
$V_{BAT}$	−19 V to −56.5 V
AGND/DGND	0 V
BGND with respect to	
AGND/DGND	−100 mV to +100 mV
Load resistance on VTX to ground	10 k $\Omega$ min

Operating Ranges define those limits between which device functionality is guaranteed.

\* Functionality of the device from 0°C to +70°C is guaranteed by production testing. Performance from −40°C to +85°C is guaranteed by characterization and periodic sampling of production units.

## ELECTRICAL CHARACTERISTICS

Description	Test Conditions (See Note 1)	Min	Typ	Max	Unit	Note
Analog ( $V_{TX}$ ) output impedance			3		$\Omega$	
Analog ( $V_{TX}$ ) output offset	$-40^{\circ}\text{C}$ to $+85^{\circ}\text{C}$	-35 -40		+35 +40	mV	— 4
Analog (RSN) input impedance	300 Hz to 3.4 kHz		1	20	$\Omega$	4
Longitudinal impedance at A or B				35		
Overload level	4-wire and 2-wire Active state	-2.5		+2.5	Vpk	2a
	On-hook, $R_{LAC} = 900 \Omega$ , Active or OHT state	0.95			Vrms	2b
<b>Transmission Performance</b>						
2-wire return loss (See Test Circuit D)	200 to 3400 Hz	26			dB	4, 8
<b>Longitudinal Balance (2-Wire and 4-Wire, See Test Circuit C); <math>R_L = 740 \Omega</math> at <math>V_{BAT} = 48 \text{ V}</math></b>						
Longitudinal to metallic L-T, L-4	200 Hz to 1 kHz	-1*	52		dB	—
	normal polarity $0^{\circ}\text{C}$ to $+70^{\circ}\text{C}$	-2	63			—
	normal polarity $-40^{\circ}\text{C}$ to $+85^{\circ}\text{C}$	-2	58			4
	reverse polarity	-2	58			—
	1 kHz to 3.4 kHz	-1*	52			—
	normal polarity $0^{\circ}\text{C}$ to $+70^{\circ}\text{C}$	-2	58			—
	normal polarity $-40^{\circ}\text{C}$ to $+85^{\circ}\text{C}$	-2	54			4
	reverse polarity	-2	54			—
Longitudinal signal generation 4-L	300 Hz to 800 Hz normal polarity	42				
Longitudinal current per pin	Active state and OHT state	27	35		mArms	
<b>Insertion Loss (2- to 4-Wire and 4- to 2-Wire, See Test Circuits A and B) <math>BAT = -48 \text{ V}</math>, <math>R_L = 900 \Omega</math></b>						
Gain accuracy	0 dBm, 1 kHz				dB	—
	$0^{\circ}\text{C}$ to $+70^{\circ}\text{C}$	-0.15		+0.15		—
	$-40^{\circ}\text{C}$ to $+85^{\circ}\text{C}$	-0.20		+0.20		4
Gain accuracy, OHT state	-10 dBm, on-hook, $R_{LAC} = 900 \Omega$	-0.5		+0.5		4
Variation with frequency	300 to 3400 Hz					—
	relative to 1 kHz $0^{\circ}\text{C}$ to $+70^{\circ}\text{C}$	-0.10		+0.10		—
	$-40^{\circ}\text{C}$ to $+85^{\circ}\text{C}$	-0.15		+0.15		4
Gain tracking	+7 dBm to -55 dBm Reference: 0 dBm	-0.1		+0.1		4 —
<b>Balance Return Signal (4- to 4-Wire, See Test Circuit B) <math>BAT = -48 \text{ V}</math>, <math>R_L = 900 \Omega</math></b>						
Gain accuracy	0 dBm, 1 kHz				dB	—
	$0^{\circ}\text{C}$ to $+70^{\circ}\text{C}$	-0.15		+0.15		3
	$-40^{\circ}\text{C}$ to $+85^{\circ}\text{C}$	-0.20		+0.20		4
Variation with frequency	300 to 3400 Hz					—
	relative to 1 kHz $0^{\circ}\text{C}$ to $+70^{\circ}\text{C}$	-0.1		+0.1		3
	$-40^{\circ}\text{C}$ to $+85^{\circ}\text{C}$	-0.15		+0.15		4
Gain tracking	+3 dBm to -55 dBm Reference: 0 dBm					—
	$0^{\circ}\text{C}$ to $+70^{\circ}\text{C}$	-0.1		+0.1		—
	$-40^{\circ}\text{C}$ to $+85^{\circ}\text{C}$	-0.15		+0.15		3, 4
Group delay	$f = 1 \text{ kHz}$		4		$\mu\text{s}$	4, 8

**Note:**

\* P.G. = Performance Grade

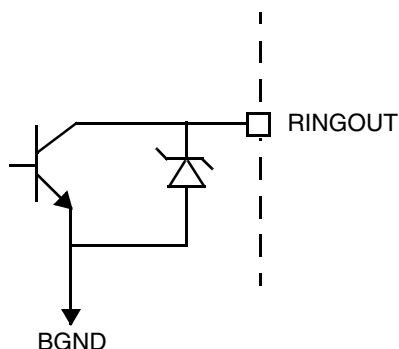
## ELECTRICAL CHARACTERISTICS (continued)

Description	Test Conditions (See Note 1)	Min	Typ	Max	Unit	Note
Total Harmonic Distortion (2- to 4-Wire or 4- to 2-Wire) (See Test Circuits A and B)						
BAT = -48 V, R <sub>L</sub> = 900 Ω						
Harmonic distortion 300 Hz to 3400 Hz	2-wire level = 0 dBm 2-wire level = +7 dBm		-64 -55	-50 -40	dB	
Idle Channel Noise (2-wire and 4-wire)						
C-message weighted noise	0°C to +85°C -40°C to 0°C		+7 +7	+10 +12	dBrnC	— 4
Psophometric weighted noise	0°C to +85°C -40°C to 0°C		-83	-80 -78	dBmp	— 4
Line Characteristics, Active State (See Figure 1)						
Short loops, Active state	BAT = -43 V, R <sub>LDC</sub> = 600 Ω BAT = -48 V, R <sub>LDC</sub> = 600 Ω	25.0	27.0	29.0	mA	
Long loops, Active state	BAT = -43 V, R <sub>LDC</sub> = 1.4 kΩ BAT = -48 V, R <sub>LDC</sub> = 1.9 kΩ	20.0 18.0	23.8 20.4			
OHT state	BAT = -48 V, R <sub>LDC</sub> = 600 Ω	16.0	18.0	20.0		
Standby state	$I_L = \frac{ V_{BAT}  - 3 \text{ V}}{R_L + 1800} \quad T_A = 25^\circ\text{C}$	0.7I <sub>L</sub>	I <sub>L</sub>	1.3I <sub>L</sub>		
	R <sub>L</sub> = 600 Ω, BAT = -48 V T <sub>A</sub> = 70°C	15.0	17.4			
Loop current	Tip Open, R <sub>L</sub> = 0 Disconnect, R <sub>L</sub> = 0 Tip Open, Bwire to GND Tip Open, Bwire = V <sub>BAT</sub> + 6 V		— — 30 30	100 100 — —	μA μA mA mA	
I <sub>L</sub> LIM (I <sub>tip</sub> + I <sub>ring</sub> )	Tip and ring shorted to GND		100	130	mA	
Ground-start signaling (tip voltage)	Active state R <sub>TIP</sub> to -48 V = 7.0 kΩ R <sub>RING</sub> to GND = 100 Ω	-7.5	-5.0		V	4 — —
Open circuit voltage	Active and OHT BAT = -48 V	40.5	42.0			
Power Dissipation, Normal Loop Polarity, BAT = -48 V						
On hook, Open Circuit state			25	70	mW	
On hook, OHT state			120	210		
On hook, Active state	R <sub>TMG</sub> = Open R <sub>TMG</sub> = 1700 Ω		160 195	260 280		
On hook, Standby state			35	85		
Off hook, OHT state	R <sub>L</sub> = 300 Ω, R <sub>TMG</sub> = ∞ BAT = -48 V		735	1050		
Off hook, Active state	R <sub>L</sub> = 300 Ω, R <sub>TMG</sub> = ∞ BAT = -48 V		1.25	1.45	W	
	R <sub>L</sub> = 300 Ω, R <sub>TMG</sub> = ∞		0.57	0.85		
Off hook, Standby state	R <sub>L</sub> = 600 Ω, T <sub>A</sub> = 25°C		0.68	1.0		

## ELECTRICAL CHARACTERISTICS (continued)

Description	Test Conditions (See Note 1)	Min	Typ	Max	Unit	Note
Supply Currents, BAT = -48 V						
V <sub>CC</sub> on-hook supply current	Open Circuit state OHT state Standby state Active state		1.7 4.9 2.2 6.3	2.5 7.5 3.0 8.5	mA	
V <sub>EE</sub> on-hook supply current	Open Circuit state OHT state Standby state Active state		0.7 2.0 0.77 2.1	2.0 3.5 2.0 5.0		
V <sub>BAT</sub> on-hook supply current	Open Circuit state OHT state Standby state Active state		0.18 1.9 0.45 4.2	1.0 4.7 1.5 5.7		
Power Supply Rejection Ratio (V <sub>RIPPLE</sub> = 50 mVrms), Active Normal State						
V <sub>CC</sub>	50 Hz to 3400 Hz	33	40		dB	5
V <sub>EE</sub>	50 Hz to 3400 Hz	29	35			
V <sub>BAT</sub>	50 Hz to 3400 Hz	30	50			
Effective internal resistance	CAS pin to GND	85	170	255	kΩ	4
RFI rejection	100 kHz to 30 MHz (See Figure E)			1.0	mVrms	4
Off-Hook Detector						
Current threshold	I <sub>DET</sub> = $\frac{375}{R_D}$	-10		+10	%	
Ground-Key Detector Thresholds, Active State, BAT = -48 V						
Ground-key resistance threshold	B(RING) to GND	2.0	5.0	10.0	kΩ	
Ground-key current threshold	B(RING) to GND		9		mA	
Ring-Trip Detector Input						
Bias current		-0.5	-0.05		μA	
Offset voltage	Source resistance = 2 MΩ	-50	0	+50	mV	6
Logic Inputs (C3-C1, E0, E1)						
Input High voltage		2.0			V	
Input Low voltage				0.8		
Input High current	All inputs except C3 and E1 Input C3 Input E1	-75 -75 -75		40 200 45	μA	
Input Low current		-0.4			mA	
Logic Output ( $\overline{DET}$ )						
Output Low voltage	I <sub>OUT</sub> = 0.8 mA			0.4	V	
Output High voltage	I <sub>OUT</sub> = -0.1 mA	2.4				
Relay Driver Output (RINGOUT)						
On voltage	35 mA sink		+0.25	+0.4	V	
Off leakage	V <sub>OH</sub> = +5 V			100	μA	
Zener breakover	100 μA	6	7.2		V	
Zener on voltage	30 mA		10			

## RELAY DRIVER SCHEMATIC

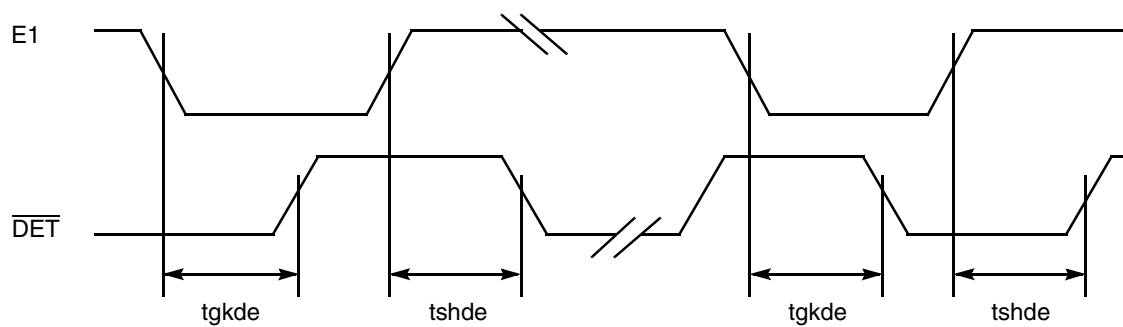


## SWITCHING CHARACTERISTICS (32-pin PLCC only)

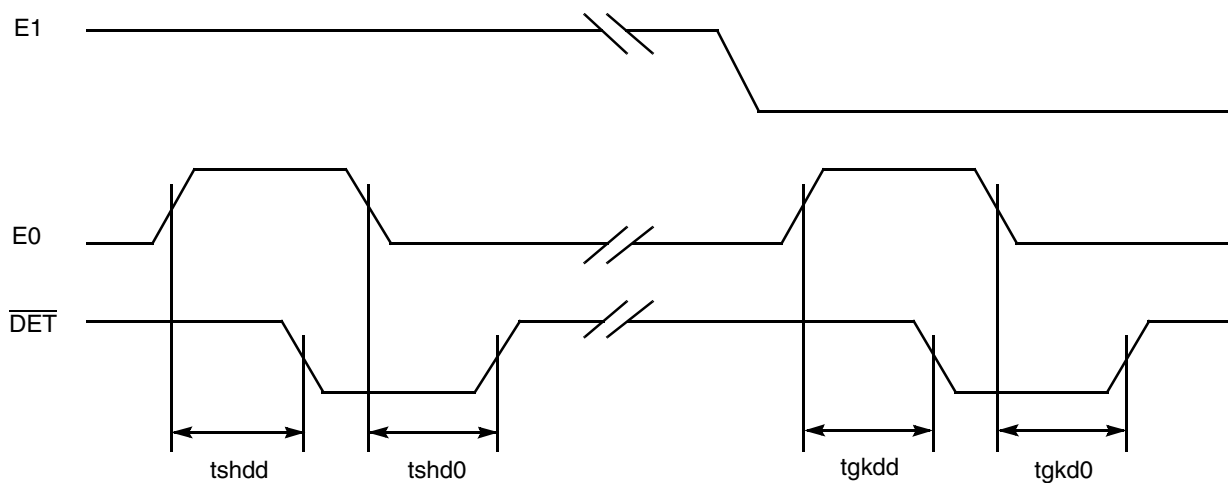
Symbol	Parameter	Test Conditions	Temperature Range	Min	Typ	Max	Unit	Note
tgkde	E1 Low to $\overline{\text{DET}}$ High (E0 = 1) E1 Low to $\overline{\text{DET}}$ Low (E0 = 1)	Ground-Key Detect state $R_L$ open, $R_G$ connected (See Figure G)	0°C to 70°C –40° to +85°C			3.8 4.0	$\mu\text{s}$	4
tgkdd	E0 High to $\overline{\text{DET}}$ Low (E1 = 0)		0°C to 70°C –40° to +85°C			1.1 1.6		
tgkd0	E0 Low to $\overline{\text{DET}}$ High (E1 = 0)		0°C to 70°C –40° to +85°C			3.8 4.0		
tshde	E1 High to $\overline{\text{DET}}$ Low (E0 = 1) E1 High to $\overline{\text{DET}}$ High (E0 = 1)	Switchhook Detect state $R_L = 600\ \Omega$ , $R_G$ open (See Figure F)	0°C to 70°C –40° to +85°C			1.2 1.7		
tshdd	E0 High to $\overline{\text{DET}}$ Low (E1 = 1)		0°C to 70°C –40° to +85°C			1.1 1.6		
tshd0	E0 Low to $\overline{\text{DET}}$ High (E1 = 1)		0°C to 70°C –40° to +85°C			3.8 4.0		

## SWITCHING WAVEFORMS

### E1 to $\overline{\text{DET}}$



### E0 to $\overline{\text{DET}}$

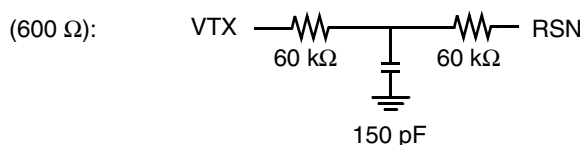
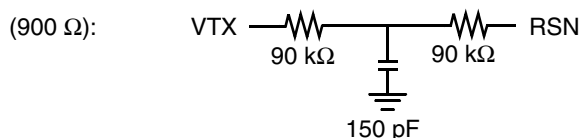


**Note:**

All delays measured at 1.4 V level.

**Notes:**

1. Unless otherwise noted, test conditions are  $V_{CC} = +5\text{ V}$ ,  $V_{EE} = -5\text{ V}$ ,  $C_{HP} = 0.33\text{ }\mu\text{F}$ ,  $R_{DC1} = R_{DC2} = 9.26\text{ k}\Omega$ ,  $C_{DC} = 0.33\text{ }\mu\text{F}$ ,  $R_d = 35.4\text{ k}\Omega$ ,  $C_{CAS} = 0.33\text{ }\mu\text{F}$ , no fuse resistors,  $BAT = -48\text{ V}$ ,  $R_L = 900\text{ }\Omega$ , and  $R_{TMG} = 1700\text{ }\Omega$ .
2. a. Overload level is defined when  $THD = 1\%$ .  
b. Overload level is defined when  $THD = 1.5\%$ .
3. Balance return signal is the signal generated at  $V_{TX}$  by  $V_{RX}$ . This specification assumes the two-wire AC load impedance matches the programmed impedance.
4. Not tested in production. This parameter is guaranteed by characterization or correlation to other tests.
5. This parameter is tested at 1 kHz with a termination impedance of  $900\text{ }\Omega$  and an  $R_L$  of  $600\text{ }\Omega$  in production. Performance at other frequencies is guaranteed by characterization.
6. Tested with  $0\text{ }\Omega$  source impedance.  $2\text{ M}\Omega$  is specified for system design only.
7. Assumes the following  $Z_T$  networks:



8. Group delay can be considerably reduced by using a  $Z_T$  network such as that shown in Note 7 above. The network reduces the group delay to less than  $2\text{ }\mu\text{s}$ . The effect of group delay on the linecard performance may be compensated for by using the QSLAC™ or DSLAC™ device.

**Table 1. SLIC Decoding**

State	C3 C2 C1	Two-wire Status	$\overline{\text{DET}}$ Output	
			E1 = 1	E1 = 0
0	0 0 0	Open Circuit	Ring trip	Ring trip
1	0 0 1	Ringin	Ring trip	Ring trip
2	0 1 0	Active	Loop detector	Ground key
3	0 1 1	On-hook TX (OHT)	Loop detector	Ground key
4	1 0 0	Tip Open	Loop detector	Ground key
5	1 0 1	Standby	Loop detector	Ground key
6	1 1 0	Active Polarity Reversal	Loop detector	Ground key
7	1 1 1	OHT Polarity Reversal	Loop detector	Ground key

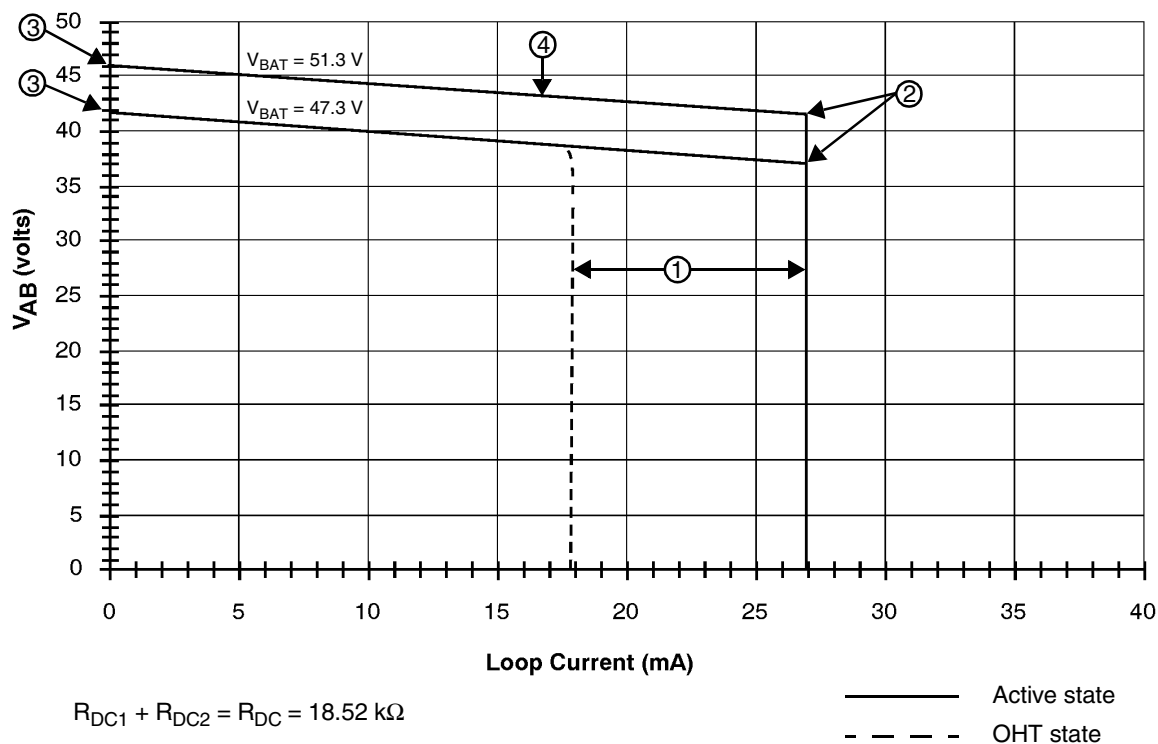
**Note:**

E0 High enables the  $\overline{\text{DET}}$  pin.

**Table 2. User-Programmable Components**

$Z_T = 200(Z_{2WIN} - 2R_F)$	$Z_T$ is connected between the VTX and RSN pins. The fuse resistors are $R_F$ and $Z_{2WIN}$ is the desired 2-wire AC input impedance. When computing $Z_T$ , the internal current amplifier pole and any external stray capacitance between VTX and RSN must be taken into account.
$Z_{RX} = \frac{Z_L}{G_{42L}} \bullet \frac{200 \bullet Z_T}{Z_T + 200(Z_L + 2R_F)}$	$Z_{RX}$ is connected from $V_{RX}$ to RSN. $Z_T$ is defined above and $G_{42L}$ is the desired receive gain.
$R_{DC1} + R_{DC2} = \frac{500}{I_{LOOP}}$ $C_{DC} = 1.5 \text{ ms} \bullet \frac{R_{DC1} + R_{DC2}}{R_{DC1} \bullet R_{DC2}}$	$R_{DC1}$ , $R_{DC2}$ , and $C_{DC}$ form the network connected to the RDC pin. $R_{DC1}$ and $R_{DC2}$ are approximately equal. $I_{LOOP}$ is the desired loop current in the constant-current region.
$R_D = \frac{375}{I_T}, C_D = \frac{0.5 \text{ ms}}{R_D}$	$R_D$ and $C_D$ form the network connected from RD to $-5 \text{ V}$ and $I_T$ is the threshold current between on hook and off hook.
$I_{OHT} = \frac{500 \text{ V} \bullet 0.66}{R_{DC1} + R_{DC2}}$	OHT loop current (constant-current region)
$C_{CAS} = \frac{1}{3.4 \bullet 10^5 \pi f_c}$	$C_{CAS}$ is the regulator filter capacitor and $f_c$ is the desired filter cut-off frequency.
<b>Thermal Management Equations (Normal Active and Tip Open states)</b>	
$R_{TMG} = \frac{V_{BAT} - 6 \text{ V}}{I_{LOOP}}$	$R_{TMG}$ is connected from TMG to $V_{BAT}$ and is used to limit power dissipation within the SLIC in Normal Active and Tip Open states only.
$P_{RTMG} = \frac{(V_{BAT} - 6 \text{ V} - (I_L \bullet R_L))^2}{R_{TMG}}$	Power dissipated in the thermal management resistor, $R_{TMG}$ , during Active and Tip Open states
$P_{SLIC} = V_{BAT} \bullet I_L - P_{RTMG} - R_L(I_L)^2 + 0.12 \text{ W}$	Power dissipated in the SLIC while in Active and Tip Open states
<b>Thermal Management Equations (Polarity Reverse State)</b> <b>Note: SLIC die temperature should not exceed 140°C.</b>	
$P_{SLIC} = V_{BAT} \bullet I_L - R_L(I_L)^2 + 0.12 \text{ W}$	Power dissipated in the SLIC while in the Polarity Reverse state
$T_{SLIC} = P_{SLIC} \bullet \theta_{JA} + T_{Ambient}$	Total die temperature
$\theta_{JA} (\theta_{JA}) \text{ PLCC} = 43^\circ\text{C/watt}$	Thermal impedance of the 32-pin plastic leaded chip carrier package

## DC FEED CHARACTERISTICS



### Notes:

#### 1. Constant-current region:

Active state,

$$I_L = \frac{500}{R_{DC}}$$

OHT state,

$$I_L = \frac{2}{3} \cdot \frac{500}{R_{DC}}$$

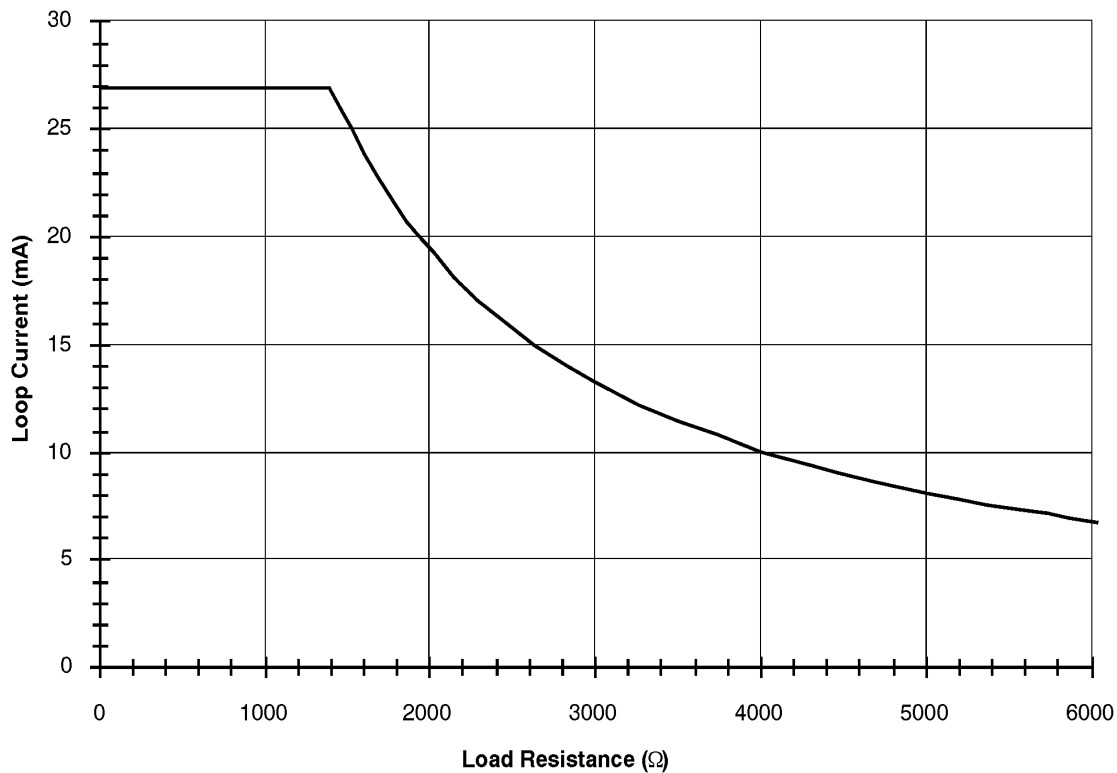
#### 2. Anti-sat (battery tracking) turn-on: $V_{AB} = 1.017|V_{BAT}| - 10.7$

#### 3. Open circuit voltage: $V_{AB} = 1.017|V_{BAT}| - 6.3$

#### 4. Anti-sat (battery tracking) region: $V_{AB} = 1.017|V_{BAT}| - 6.3 - I_L \frac{R_{DC}}{120}$

### a. $V_A - V_B$ ( $V_{AB}$ ) Voltage vs. Loop Current (Typical)

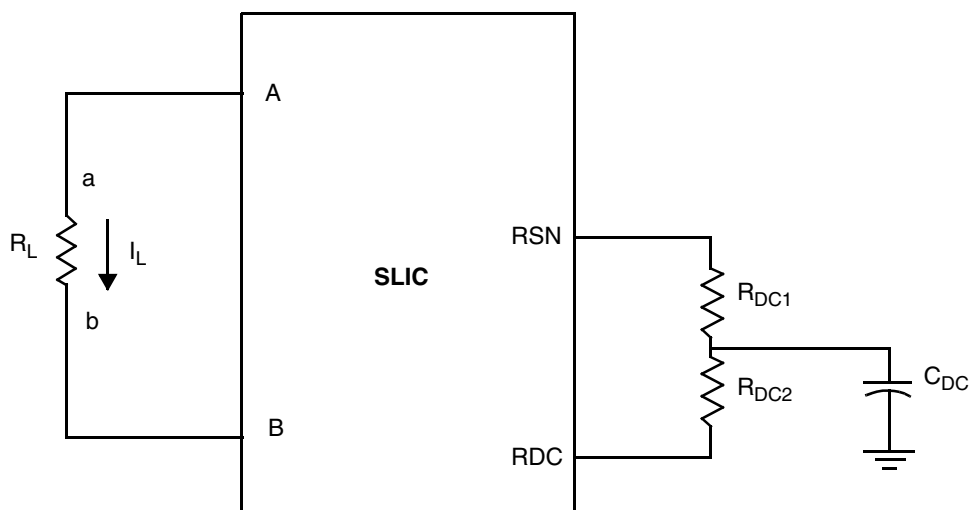
## DC FEED CHARACTERISTICS (continued)



$$R_{DC1} + R_{DC2} = R_{DC} = 18.52 \text{ k}\Omega$$

$$V_{BAT} = 47.3 \text{ V}$$

### b. Loop Current vs. Load Resistance (Typical)

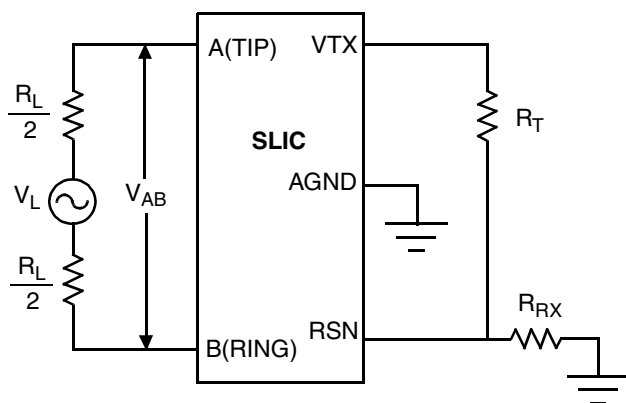


Feed current programmed by  $R_{DC1}$  and  $R_{DC2}$

### c. Feed Programming

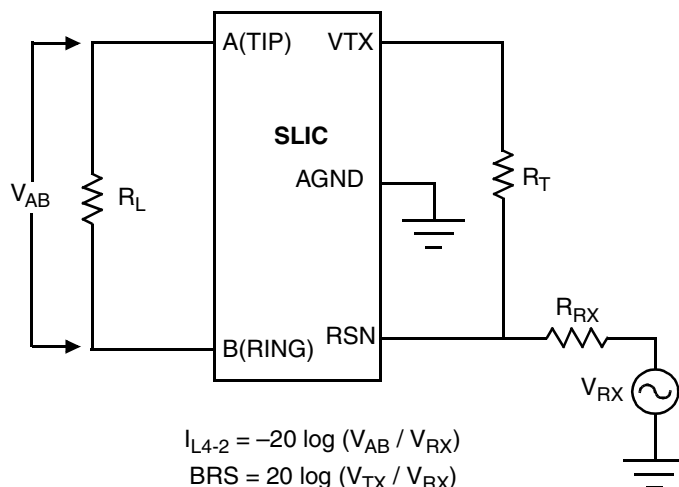
**Figure 1. DC Feed Characteristics**

## TEST CIRCUITS



$$I_{L2-4} = -20 \log (V_{TX} / V_{AB})$$

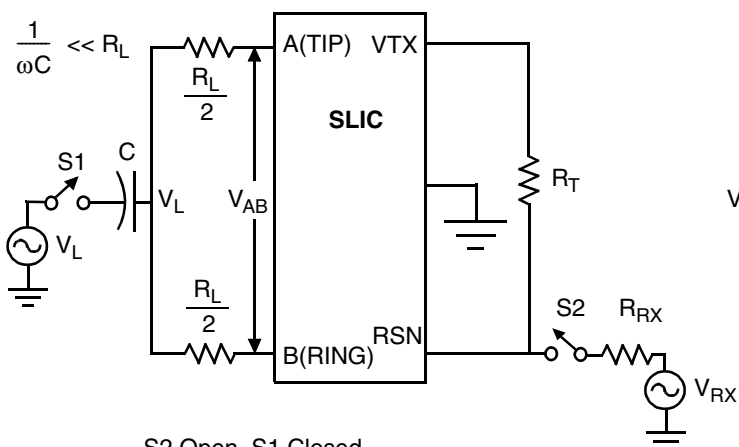
A. Two- to Four-Wire Insertion Loss



$$I_{L4-2} = -20 \log (V_{AB} / V_{RX})$$

$$BRS = 20 \log (V_{TX} / V_{RX})$$

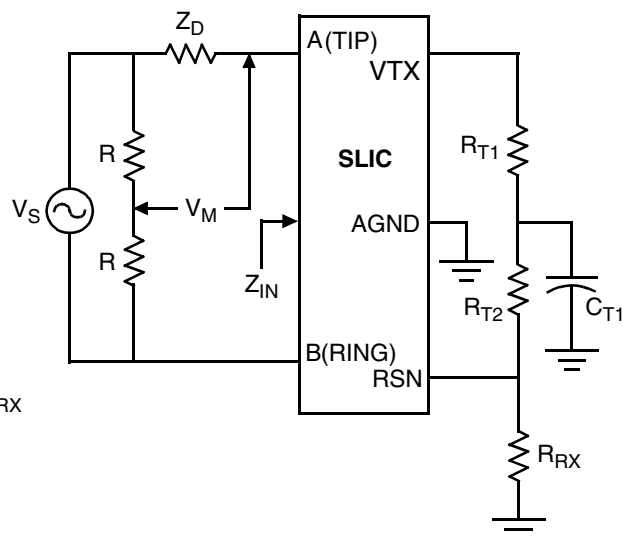
B. Four- to Two-Wire Insertion Loss and Balance Return Signal



S2 Open, S1 Closed  
L-T Long. Bal. =  $20 \log (V_{AB} / V_L)$   
L-4 Long. Bal. =  $20 \log (V_{TX} / V_L)$

S2 Closed, S1 Open  
4-L Long. Sig. Gen. =  $20 \log (V_L / V_{RX})$

C. Longitudinal Balance



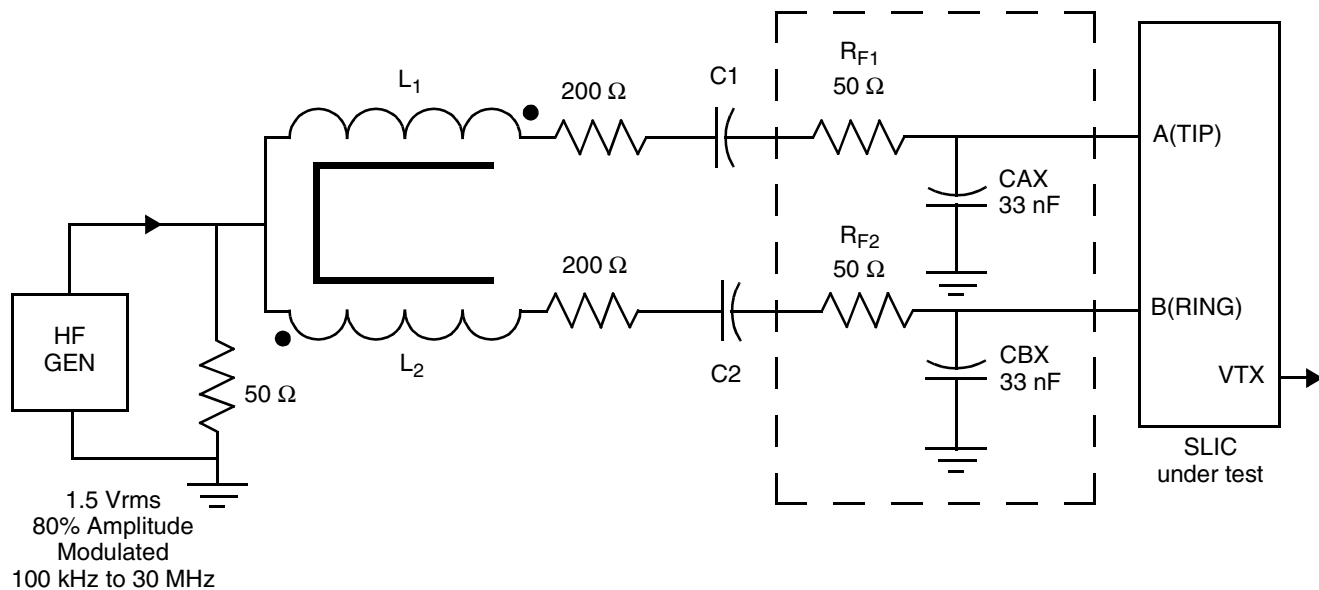
**Note:**

$Z_D$  is the desired impedance (e.g., the characteristic impedance of the line).

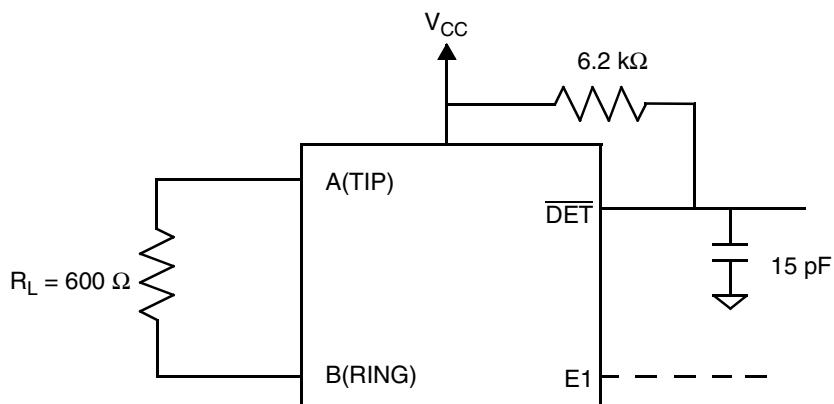
$$R_L = -20 \log (2 V_M / V_S)$$

D. Two-Wire Return Loss Test Circuit

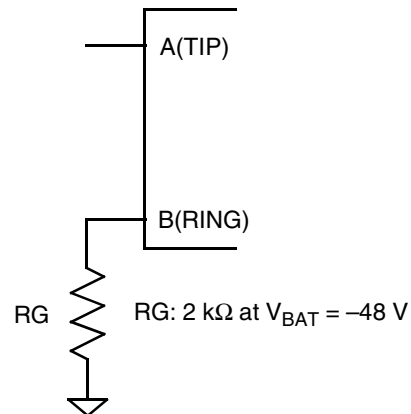
## TEST CIRCUITS (continued)



**E. RFI Test Circuit**

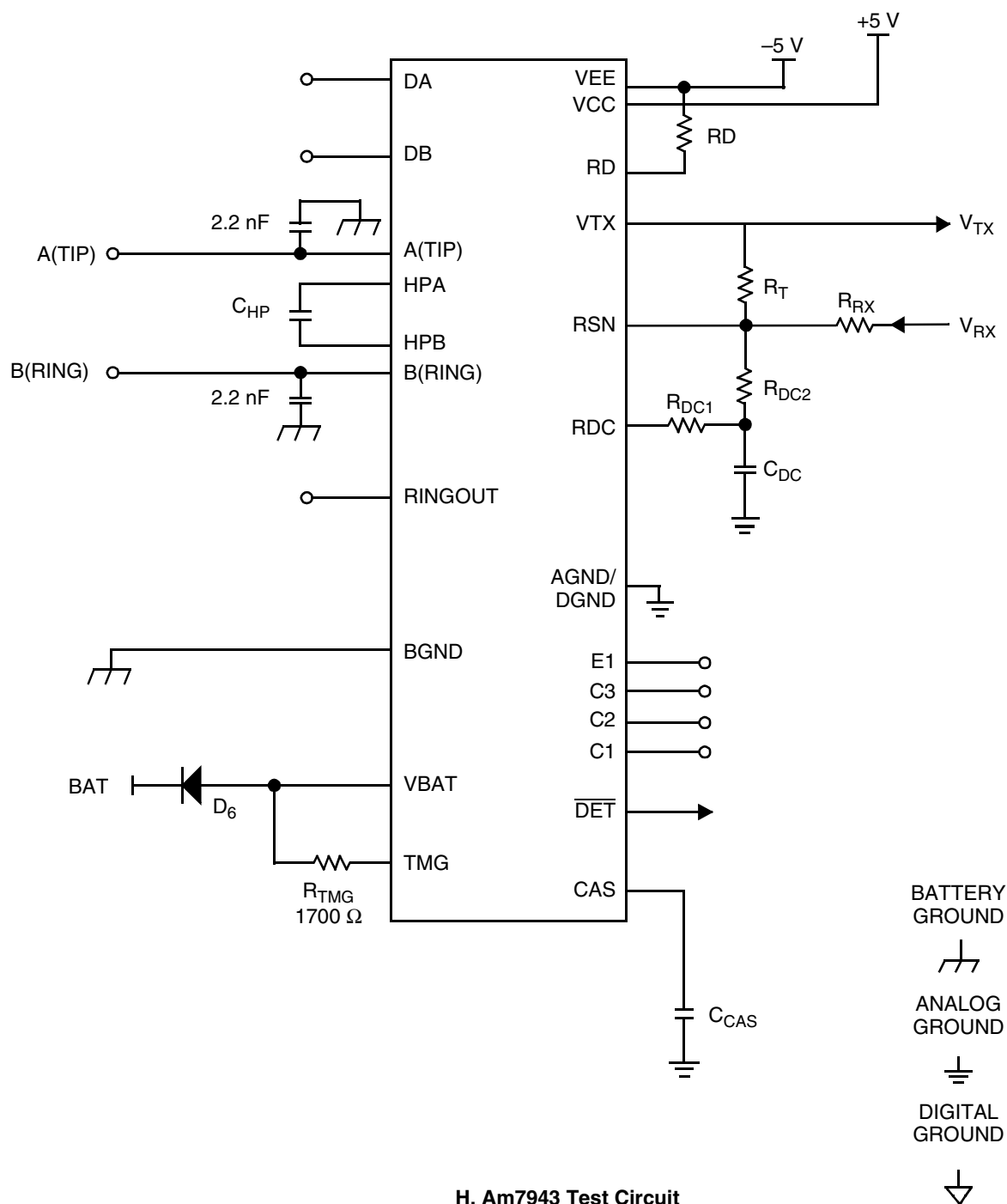


**F. Loop-Detector Switching**



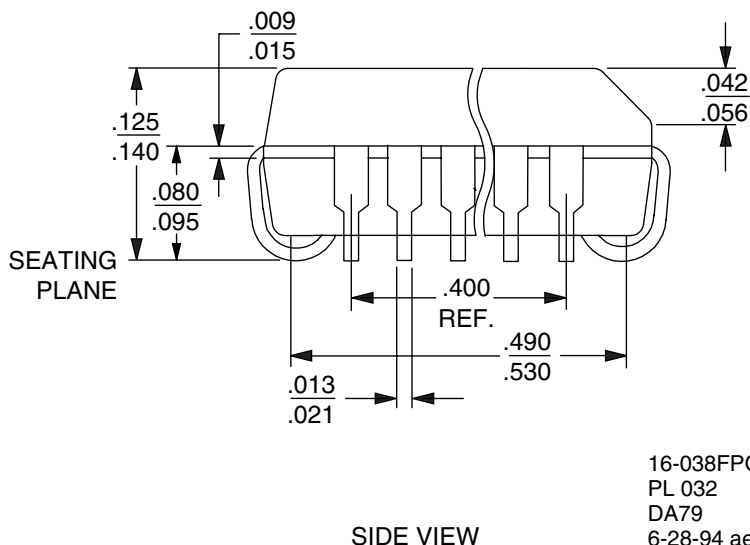
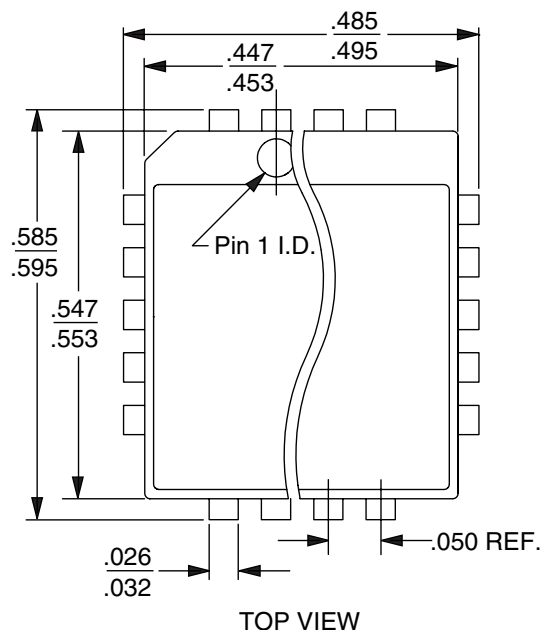
**G. Ground-Key Switching**

## TEST CIRCUITS (continued)



## PHYSICAL DIMENSION

### PL032



16-038FPO-5  
PL 032  
DA79  
6-28-94 ae

## REVISION SUMMARY

### Revision A to B

- Minor changes were made to the data sheet style and format to conform to Legerity standards.

### Revision B to Revision C

- In Pin Description table, inserted/changed TP pin description to: "Thermal pin. Connection for heat dissipation. Internally connected to substrate (VBAT). Leave as open circuit or connected to VBAT. In both cases, the TP pins can connect to an area of copper on the board to enhance heat dissipation."
- Minor changes were made to the data sheet style and format to conform to Legerity standards.

### Revision C to Revision D

- The physical dimension (PL032) was added to the Physical Dimension section.
- Deleted the Ceramic DIP and Plastic DIP packages and references to them.
- Updated the Pin Description table to correct inconsistencies.

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