FINAL

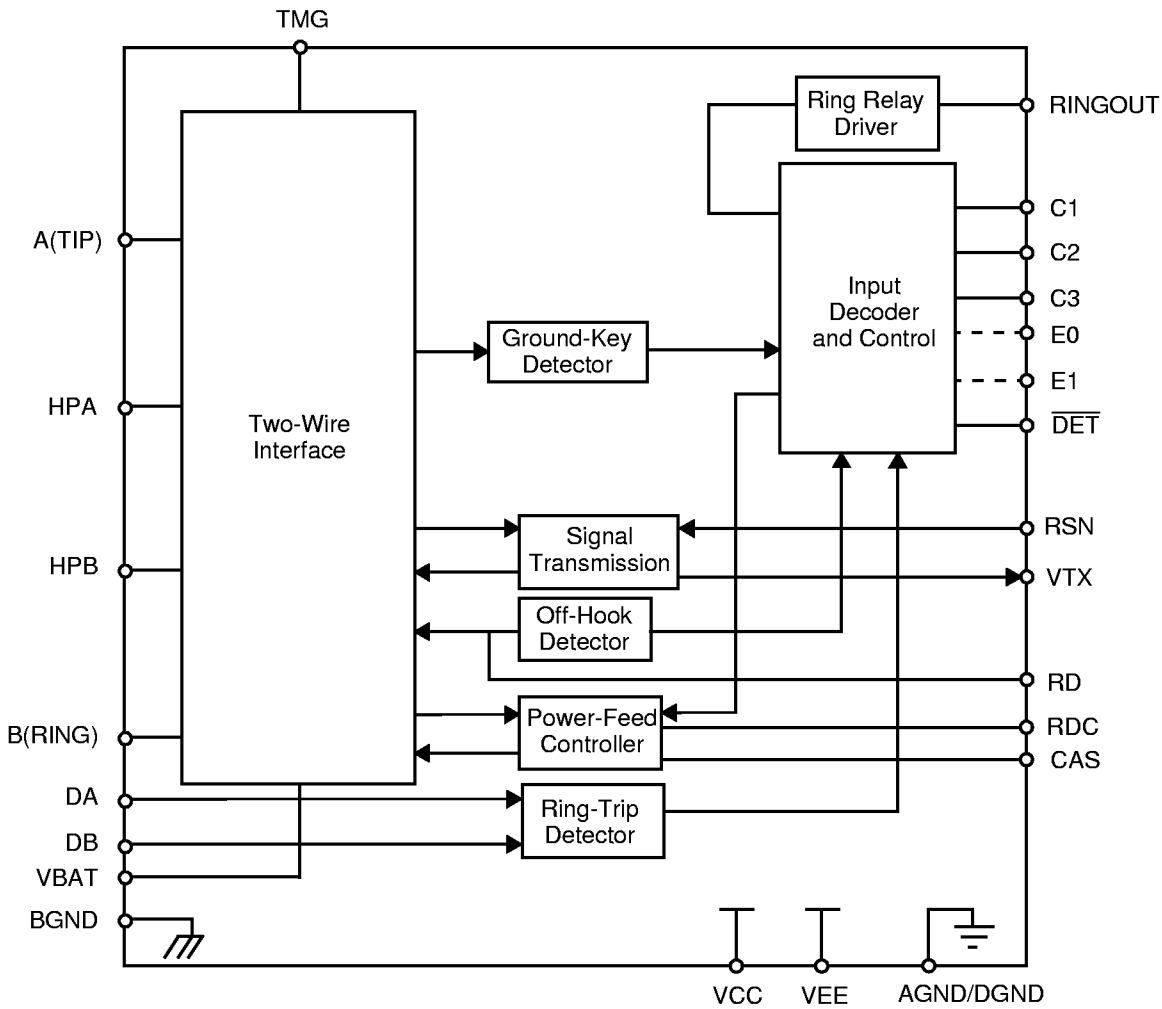
Am7943

Subscriber Line Interface Circuit

DISTINCTIVE CHARACTERISTICS

- Programmable constant-current feed
- Current gain = 200
- Programmable loop-detect threshold
- Low power Standby state
- Performs polarity reversal
- Ground-key detector
- Tip Open state for ground-start lines
- –19 V to –58 V battery operation
- Two-wire impedance set by single external impedance
- On-hook transmission
- On-chip ring relay driver and relay snubber circuit
- On-chip Thermal Management (TMG) feature
- Ideal for DLC and PABX applications

BLOCK DIAGRAM



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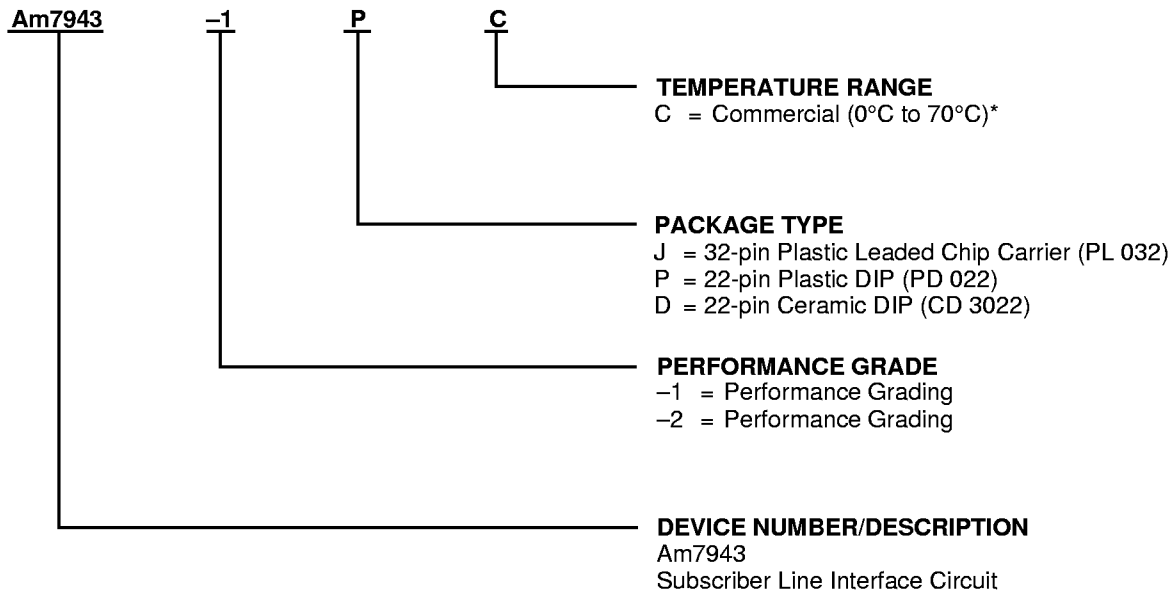
ORDERING INFORMATION

Standard Products

AMD standard products are available in several packages and operating ranges. The order number (Valid Combination) is formed by a combination of the elements below.



Valid Combinations		
Am7943	–1 –2	DC JC PC

Valid Combinations

Valid Combinations list configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations, to check on newly released combinations, and to obtain additional data on AMD's standard military grade products.

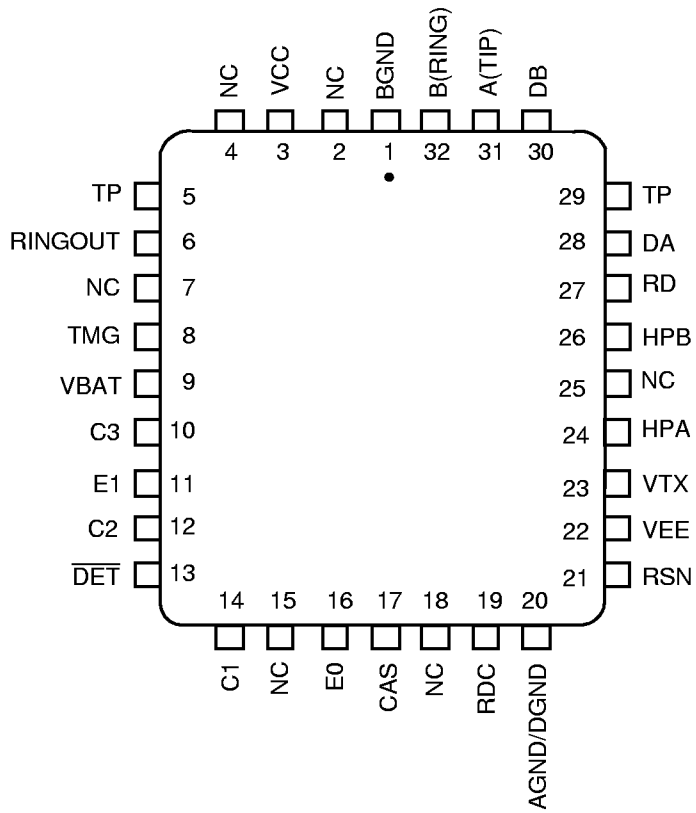
Note:

** Functionality of the device from 0°C to +70°C is guaranteed by production testing. Performance from –40°C to +85°C is guaranteed by characterization and periodic sampling of production units.*

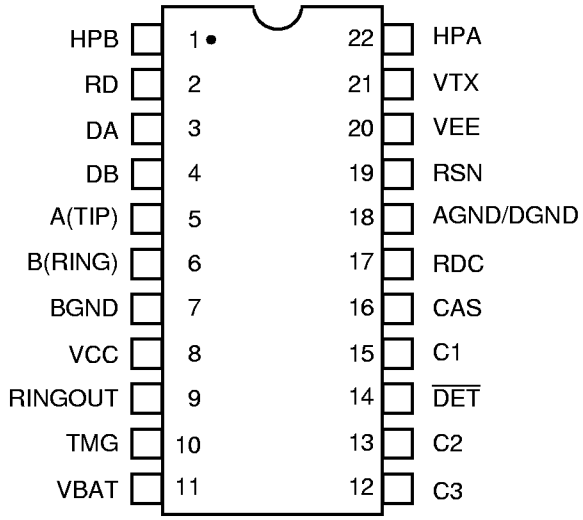
CONNECTION DIAGRAMS

Top View

32-Pin PLCC



22-Pin Plastic DIP
or
22-Pin Ceramic DIP



Notes:

1. *Pin 1 is marked for orientation.*
2. *TP is a thermal conduction pin tied to substrate.*
3. *NC = No Connect*

PIN DESCRIPTIONS

Pin Names	Type	Description
AGND/DGND	Gnd	Analog and Digital ground.
A(TIP)	Output	Output of A(TIP) power amplifier.
BGND	Gnd	Battery (power) ground.
B(RING)	Output	Output of B(RING) power amplifier.
C3–C1	Input	Decoder. TTL compatible. C3 is MSB and C1 is LSB.
CAS	Capacitor	Anti-saturation pin for capacitor to filter reference voltage when operating in anti-saturation region.
DA	Input	Ring-trip negative. Negative input to ring-trip comparator.
DB	Input	Ring-trip positive. Positive input to ring-trip comparator.
$\overline{\text{DET}}$	Output	Switchhook detector. When enabled, a logic Low indicates the selected detector is tripped. The detector is selected by the logic inputs (C3–C1, E1–E0). The output is open-collector with a built-in 15 kΩ pull-up resistor.
E0	Input	$\overline{\text{DET}}$ Enable. A logic High enables $\overline{\text{DET}}$. A logic Low disables $\overline{\text{DET}}$. ($\overline{\text{DET}}$ = Logic High). (PLCC only)
E1	Input	Ground-Key Enable. E1 = High connects the ground-key detector to $\overline{\text{DET}}$. E1 = Low connects the off-hook or ring-trip detector to $\overline{\text{DET}}$. (PLCC only)
HPA	Capacitor	High-Pass Filter Capacitor. A(TIP) side of high-pass filter capacitor.
HPB	Capacitor	High-Pass Filter Capacitor. B(RING) side of high-pass filter capacitor.
RD	Resistor	Detector resistor. Detector threshold set and filter pin.
RDC	Resistor	DC feed resistor. Connection point for the DC feed current programming network. The other end of the network connects to the receiver summing node (RSN). Connection point for the DC feed current programming network. The other end of the network connects to the receiver summing node (RSN). The sign of V_{RDC} is negative for normal polarity and positive for reverse polarity.
RINGOUT	Output	Ring Relay Driver. Open-collector driver with emitter internally connected to BGND.
RSN	Input	Receive Summing Node. The metallic current (AC and DC) between A(TIP) and B(RING) is equal to 200 times the current into this pin. The networks that program receive gain, two-wire impedance, and feed current all connect to this node.
TMG	—	Thermal management. A resistor connected from this pin to VBAT reduces the on-chip power dissipation in the normal polarity, Active state only. Refer to Table 2.
TP	Thermal	Thermal pin. Connection for heat dissipation. Internally connected to substrate (VBAT). Leave as open circuit or connected to VBAT. In both cases, the TP pins can connect to an area of copper on the board to enhance heat dissipation
VBAT	Battery	Battery supply.
VCC	Power	+5 V power supply.
VEE	Power	–5 V power supply.
VTX	Output	Transmit Audio. This output is a unity gain version of the A(TIP) and B(RING) metallic voltage. VTX also sources the two-wire input impedance programming network.

ABSOLUTE MAXIMUM RATINGS

Storage temperature . . . . . –55°C to +150°C

V_{CC} with respect to AGND/DGND . . .–0.4 V to +7.0 V

V_{EE} with respect to AGND/DGND . . .+0.4 V to –7.0 V

V_{BAT} with respect to AGND/DGND:
- Continuous . . . . . +0.4 V to –70 V
- 10 ms . . . . . +0.4 V to –75 V

BGND with respect to AGND/DGND . . . .+3 V to –3 V

A(TIP) or B(RING) to BGND:
- Continuous . . . . . .–70 V to +1 V
- 10 ms (f = 0.1 Hz) . . . . . .–70 V to +5 V
- 1 ms (f = 0.1 Hz) . . . . . .–80 V to +8 V
- 10 µs (f = 0.1 Hz) . . . . . .–90 V to +12 V

Current from A(TIP) or B(RING). . . . . .±150 mA

Current from TMG . . . . . 100 mA

Voltage on RINGOUT:
- During transient . . . . . BGND to +10 V
- During steady state. . . . . BGND to +7 V

Current through relay drivers . . . . . 60 mA

DA and DB inputs
- Voltage on ring-trip inputs . . . . . .V_{BAT} to 0 V
- Current into ring-trip inputs . . . . . .±10 mA

C3–C1, E0, E1
- to AGND/DGND . . . . . .–0.4 V to V_{CC} +0.4 V

Maximum power dissipation, T_A = 85°C

No heat sink (see note):
- In 22-pin ceramic DIP package. . . . . 1.2 W
- In 22-pin plastic DIP package . . . . . 1.0 W
- In 32-pin PLCC package. . . . . 1.4 W

Thermal data . . . . . .θ_{JA}
- In 22-pin ceramic package . . . . . .50°C/W typ
- In 22-pin plastic package . . . . . .56°C/W typ
- In 32-pin PLCC package. . . . . .43°C/W typ

Note: *Thermal limiting circuitry on chip will shut down the circuit at a junction temperature of about 165°C. The device should never be exposed to this temperature. Operation above 145°C junction temperature may degrade device reliability. See the SLIC Packaging Considerations for more information.*

Stresses above those listed under Absolute Maximum Ratings may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to Absolute Maximum Ratings for extended periods may affect device reliability.

OPERATING RANGES

Commercial (C) Devices

Ambient temperature . . . . . 0°C to +70°C*

V_{CC} . . . . . 4.75 V to 5.25 V

V_{EE} . . . . . –4.75 V to –5.25 V

V_{BAT} . . . . . .–19 V to –56.5 V

AGND/DGND . . . . . 0 V

BGND with respect to AGND/DGND. . . . . –100 mV to +100 mV

Load resistance on VTX to ground . . . . . 10 kΩ min

Operating Ranges define those limits between which device functionality is guaranteed.

** Functionality of the device from 0°C to +70°C is guaranteed by production testing. Performance from –40°C to +85°C is guaranteed by characterization and periodic sampling of production units.*

ELECTRICAL CHARACTERISTICS

Description	Test Conditions (See Note 1)	Min	Typ	Max	Unit	Note
Analog (V_{TX}) output impedance			3		Ω	
Analog (V_{TX}) output offset		–35		+35	mV	—
	–40°C to +85°C	–40		+40		4
Analog (RSN) input impedance	300 Hz to 3.4 kHz		1	20	Ω	4
Longitudinal impedance at A or B				35		
Overload level	4-wire and 2-wire Active state	–2.5		+2.5	Vpk	2a
	On-hook, R_{LAC} = 900 Ω, Active or OHT state	0.95			Vrms	2b
Transmission Performance						
2-wire return loss (See Test Circuit D)	200 to 3400 Hz	26			dB	4, 8
Longitudinal Balance (2-Wire and 4-Wire, See Test Circuit C); R_L = 740 Ω at V_{BAT} = 48 V						
Longitudinal to metallic L-T, L-4	200 Hz to 1 kHz –1*	52			dB	—
	normal polarity 0°C to +70°C –2	63				—
	normal polarity –40°C to +85°C –2	58				4
	reverse polarity –2	58				—
	1 kHz to 3.4 kHz –1*	52				—
	normal polarity 0°C to +70°C –2	58				—
	normal polarity –40°C to +85°C –2	54				4
	reverse polarity –2	54				—
Longitudinal signal generation 4-L	300 Hz to 800 Hz normal polarity	42				
Longitudinal current per pin	Active state and OHT state	27	35		mArms	
Insertion Loss (2- to 4-Wire and 4- to 2-Wire, See Test Circuits A and B) BAT = –48 V, R_L = 900 Ω						
Gain accuracy	0 dBm, 1 kHz				dB	—
	0°C to +70°C	–0.15		+0.15		—
	–40°C to +85°C	–0.20		+0.20		4
Gain accuracy, OHT state	–10 dBm, on-hook, R_{LAC} = 900 Ω	–0.5		+0.5		4
Variation with frequency	300 to 3400 Hz relative to 1 kHz 0°C to +70°C	–0.10		+0.10		—
	–40°C to +85°C	–0.15		+0.15		4
Gain tracking	+7 dBm to –55 dBm Reference: 0 dBm	–0.1		+0.1		4
						—
Balance Return Signal (4- to 4-Wire, See Test Circuit B) BAT = –48 V, R_L = 900 Ω						
Gain accuracy	0 dBm, 1 kHz				dB	—
	0°C to +70°C	–0.15		+0.15		3
	–40°C to +85°C	–0.20		+0.20		4
Variation with frequency	300 to 3400 Hz relative to 1 kHz 0°C to +70°C	–0.1		+0.1		—
	–40°C to +85°C	–0.15		+0.15		3
						4
Gain tracking	+3 dBm to –55 dBm Reference: 0 dBm					—
						—
	0°C to +70°C	–0.1		+0.1		3, 4
	–40°C to +85°C	–0.15		+0.15		4
Group delay	f = 1 kHz		4		µs	4, 8

Note:
** P.G. = Performance Grade*

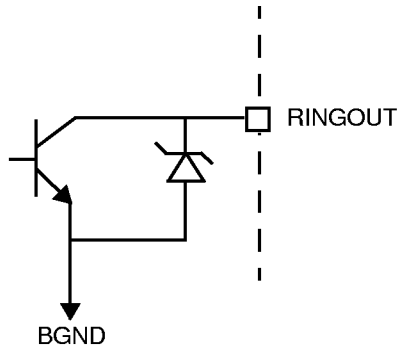
ELECTRICAL CHARACTERISTICS (continued)

Description	Test Conditions (See Note 1)	Min	Typ	Max	Unit	Note
Total Harmonic Distortion (2- to 4-Wire or 4- to 2-Wire) (See Test Circuits A and B) **BAT = –48 V, R_L = 900 Ω**						
Harmonic distortion 300 Hz to 3400 Hz	2-wire level = 0 dBm 2-wire level = +7 dBm		–64 –55	–50 –40	dB	
Idle Channel Noise (2-wire and 4-wire)						
C-message weighted noise	0°C to +85°C –40°C to 0°C		+7 +7	+10 +12	dBrnC	— 4
Psophometric weighted noise	0°C to +85°C –40°C to 0°C		–83	–80 –78	dBmp	— 4
Line Characteristics, Active State (See Figure 1)						
Short loops, Active state	BAT = –43 V, R_{LDC} = 600 Ω BAT = –48 V, R_{LDC} = 600 Ω	25.0	27.0	29.0		
Long loops, Active state	BAT = –43 V, R_{LDC} = 1.4 kΩ BAT = –48 V, R_{LDC} = 1.9 kΩ	20.0 18.0	23.8 20.4			
OHT state	BAT = –48 V, R_{LDC} = 600 Ω	16.0	18.0	20.0	mA	
Standby state	$I_L = \frac{\lvert V_{BAT}\rvert - 3\ V}{R_L + 1800}$ T_A = 25°C	0.7I_L	I_L	1.3I_L		
	R_L = 600 Ω, BAT = –48 V T_A = 70°C	15.0	17.4			
Loop current	Tip Open, R_L = 0 Disconnect, R_L = 0 Tip Open, Bwire to GND Tip Open, Bwire = V_{BAT} + 6 V		— — 30 30	100 100 — —	µA µA mA mA	
I_LLIM (Itip + Iring)	Tip and ring shorted to GND		100	130	mA	
Ground-start signaling (tip voltage)	Active state R_{TIP} to –48 V = 7.0 kΩ R_{RING} to GND = 100 Ω	–7.5	–5.0		V	4 — —
Open circuit voltage	Active and OHT BAT = –48 V	40.5	42.0			
Power Dissipation, Normal Loop Polarity, BAT = –48 V						
On hook, Open Circuit state			25	70		
On hook, OHT state			120	210		
On hook, Active state	R_{TMG} = Open R_{TMG} = 1700 Ω		160 195	260 280	mW	
On hook, Standby state			35	85		
Off hook, OHT state	R_L = 300 Ω, R_{TMG} = ∞ BAT = –48 V		735	1050		
Off hook, Active state	R_L = 300 Ω, R_{TMG} = ∞ BAT = –48 V		1.25	1.45	W	
	R_L = 300 Ω, R_{TMG} = ∞		0.57	0.85		
Off hook, Standby state	R_L = 600 Ω, T_A = 25°C		0.68	1.0		

ELECTRICAL CHARACTERISTICS (continued)

Description	Test Conditions (See Note 1)	Min	Typ	Max	Unit	Note
Supply Currents, BAT = –48 V						
V_{CC} on-hook supply current	Open Circuit state OHT state Standby state Active state		1.7 4.9 2.2 6.3	2.5 7.5 3.0 8.5	mA	
V_{EE} on-hook supply current	Open Circuit state OHT state Standby state Active state		0.7 2.0 0.77 2.1	2.0 3.5 2.0 5.0		
V_{BAT} on-hook supply current	Open Circuit state OHT state Standby state Active state		0.18 1.9 0.45 4.2	1.0 4.7 1.5 5.7		
Power Supply Rejection Ratio (V_{RIPPLE} = 50 mVrms), Active Normal State						
V_{CC}	50 Hz to 3400 Hz	33	40		dB	5
V_{EE}	50 Hz to 3400 Hz	29	35			
V_{BAT}	50 Hz to 3400 Hz	30	50			
Effective internal resistance	CAS pin to GND	85	170	255	kΩ	4
RFI rejection	100 kHz to 30 MHz (See Figure E)			1.0	mVrms	4
Off-Hook Detector						
Current threshold	$I_{DET} = \frac{375}{R_D}$	–10		+10	%	
Ground-Key Detector Thresholds, Active State, BAT = –48 V						
Ground-key resistance threshold	B(RING) to GND	2.0	5.0	10.0	kΩ	
Ground-key current threshold	B(RING) to GND		9		mA	
Ring-Trip Detector Input						
Bias current		–0.5	–0.05		µA	
Offset voltage	Source resistance = 2 MΩ	–50	0	+50	mV	6
Logic Inputs (C3–C1, E0, E1)						
Input High voltage		2.0			V	
Input Low voltage				0.8		
Input High current	All inputs except C3 and E1 Input C3 Input E1	–75 –75 –75		40 200 45	µA	
Input Low current		–0.4			mA	
Logic Output ($\overline{DET}$)						
Output Low voltage	I_{OUT} = 0.8 mA			0.4	V	
Output High voltage	I_{OUT} = –0.1 mA	2.4				
Relay Driver Output (RINGOUT)						
On voltage	35 mA sink		+0.25	+0.4	V	
Off leakage	V_{OH} = +5 V			100	µA	
Zener breakover	100 µA	6	7.2		V	
Zener on voltage	30 mA		10			

RELAY DRIVER SCHEMATIC

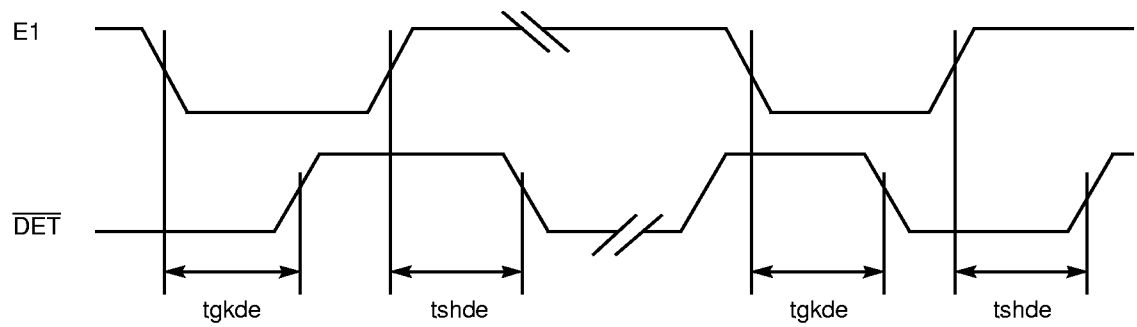


SWITCHING CHARACTERISTICS
(32-pin PLCC only)

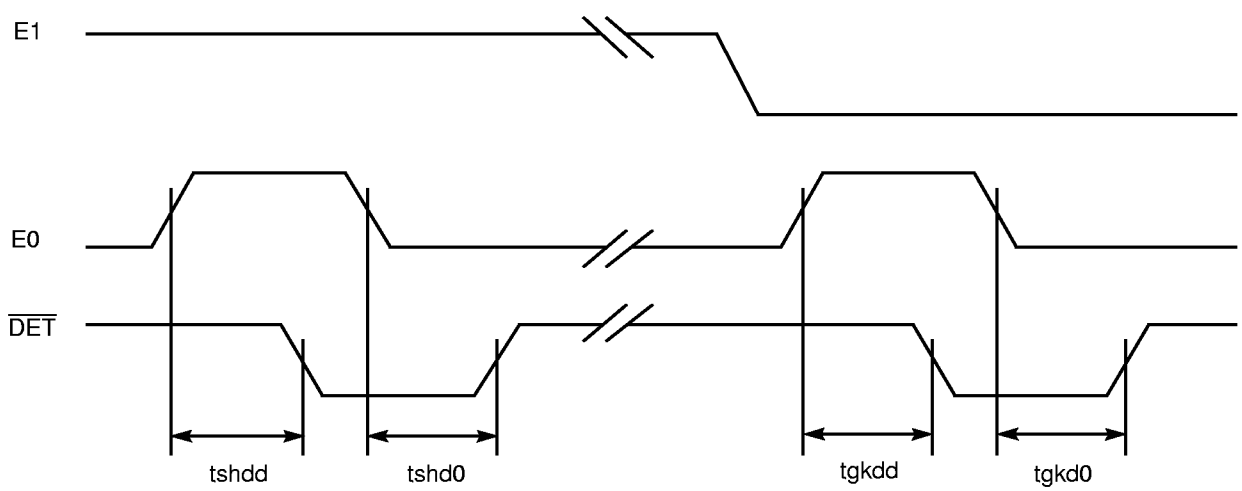
Symbol	Parameter	Test Conditions	Temperature Range	Min	Typ	Max	Unit	Note
tgkde	E1 Low to $\overline{DET}$ High (E0 = 1)	Ground-Key Detect state R_L open, R_G connected (See Figure G)	0°C to 70°C –40° to +85°C			3.8 4.0	µs	4
	E1 Low to $\overline{DET}$ Low (E0 = 1)		0°C to 70°C –40° to +85°C			1.1 1.6		
tgkdd	E0 High to $\overline{DET}$ Low (E1 = 0)		0°C to 70°C –40° to +85°C			1.1 1.6		
tgkd0	E0 Low to $\overline{DET}$ High (E1 = 0)		0°C to 70°C –40° to +85°C			3.8 4.0		
tshde	E1 High to $\overline{DET}$ Low (E0 = 1)	Switchhook Detect state R_L = 600 Ω, R_G open (See Figure F)	0°C to 70°C –40° to +85°C			1.2 1.7		
	E1 High to $\overline{DET}$ High (E0 = 1)		0°C to 70°C –40° to +85°C			3.8 4.0		
tshdd	E0 High to $\overline{DET}$ Low (E1 = 1)		0°C to 70°C –40° to +85°C			1.1 1.6		
tshd0	E0 Low to $\overline{DET}$ High (E1 = 1)		0°C to 70°C –40° to +85°C			3.8 4.0		

SWITCHING WAVEFORMS

E1 to $\overline{\text{DET}}$



E0 to $\overline{\text{DET}}$

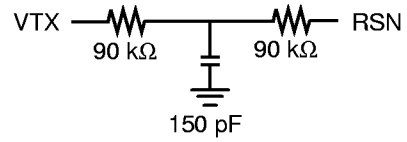


Note:
All delays measured at 1.4 V level.

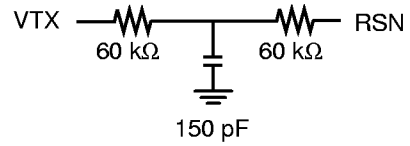
Notes:

1. *Unless otherwise noted, test conditions are V_{CC} = +5 V, V_{EE} = –5 V, C_{HP} = 0.33 µF, R_{DC1} = R_{DC2} = 9.26 kΩ, C_{DC} = 0.33 µF, R_d = 35.4 kΩ, C_{CAS} = 0.33 µF, no fuse resistors, BAT = –48 V, R_L = 900 Ω, and R_{TMG} = 1700 Ω.*
2. *a. Overload level is defined when THD = 1%.*
   b. Overload level is defined when THD = 1.5%.
3. *Balance return signal is the signal generated at V_{TX} by V_{RX}. This specification assumes the two-wire AC load impedance matches the programmed impedance.*
4. *Not tested in production. This parameter is guaranteed by characterization or correlation to other tests.*
5. *This parameter is tested at 1 kHz with a termination impedance of 900 Ω and an R_L of 600 Ω in production. Performance at other frequencies is guaranteed by characterization.*
6. *Tested with 0 Ω source impedance. 2 MΩ is specified for system design only.*
7. *Assumes the following Z_T networks:*

(900 Ω):



(600 Ω):



8. *Group delay can be considerably reduced by using a Z_T network such as that shown in Note 7 above. The network reduces the group delay to less than 2 µs. The effect of group delay on the linecard performance may be compensated for by using the QSLAC™ or DSLAC™ device.*

Table 1. SLIC Decoding

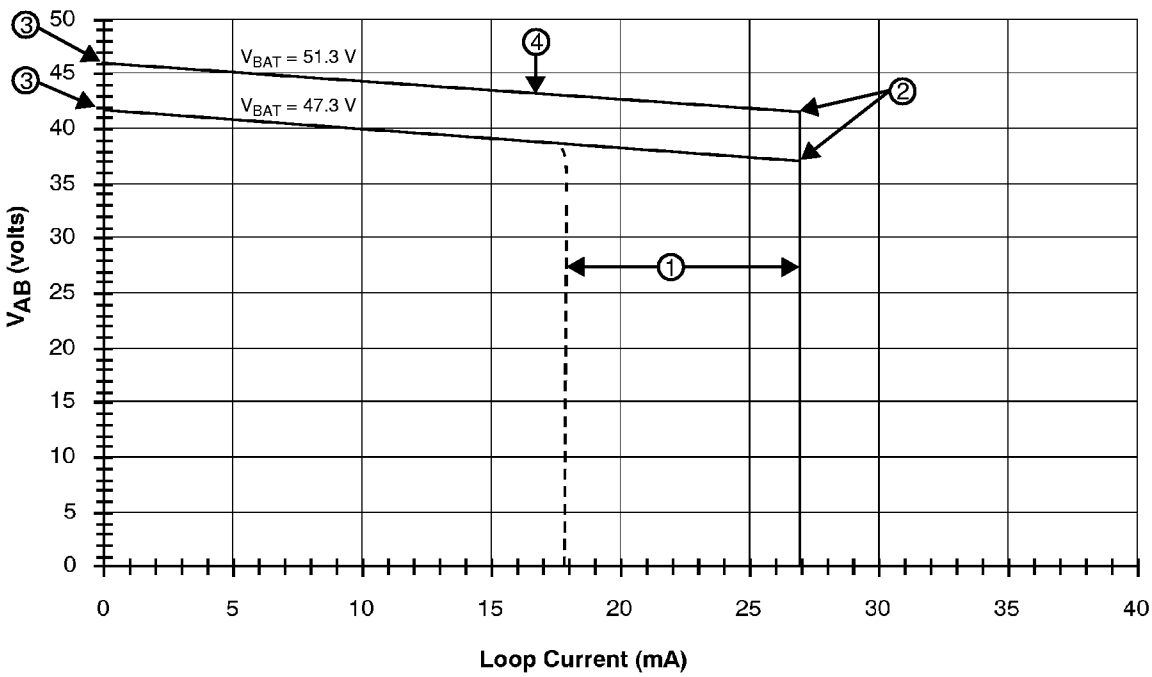
				$\overline{\text{DET}}$ Output	
State	**C3**	**C2**	**C1**	**Two-wire Status**	**E1 = 1**	**E1 = 0**
0	0	0	0	Open Circuit	Ring trip	Ring trip
1	0	0	1	Ringing	Ring trip	Ring trip
2	0	1	0	Active	Loop detector	Ground key
3	0	1	1	On-hook TX (OHT)	Loop detector	Ground key
4	1	0	0	Tip Open	Loop detector	Ground key
5	1	0	1	Standby	Loop detector	Ground key
6	1	1	0	Active Polarity Reversal	Loop detector	Ground key
7	1	1	1	OHT Polarity Reversal	Loop detector	Ground key

Note:
E0 and E1 are internally pulled High in the 22-pin DIP package option. E0 High enables the $\overline{DET}$ pin.

Table 2. User-Programmable Components

$Z_T = 200(Z_{2WIN} - 2R_F)$	Z_T is connected between the VTX and RSN pins. The fuse resistors are R_F and Z_{2WIN} is the desired 2-wire AC input impedance. When computing Z_T, the internal current amplifier pole and any external stray capacitance between VTX and RSN must be taken into account.
$Z_{RX} = \frac{Z_L}{G_{42L}} \bullet \frac{200 \bullet Z_T}{Z_T + 200(Z_L + 2R_F)}$	Z_{RX} is connected from V_{RX} to RSN. Z_T is defined above and G_{42L} is the desired receive gain.
$R_{DC1} + R_{DC2} = \frac{500}{I_{LOOP}}$ $C_{DC} = 1.5\ ms \bullet \frac{R_{DC1} + R_{DC2}}{R_{DC1} \bullet R_{DC2}}$	R_{DC1}, R_{DC2}, and C_{DC} form the network connected to the RDC pin. R_{DC1} and R_{DC2} are approximately equal. I_{LOOP} is the desired loop current in the constant-current region.
$R_D = \frac{375}{I_T}$, $C_D = \frac{0.5\ ms}{R_D}$	R_D and C_D form the network connected from RD to –5 V and I_T is the threshold current between on hook and off hook.
$I_{OHT} = \frac{500\ V \bullet 0.66}{R_{DC1} + R_{DC2}}$	OHT loop current (constant-current region)
$C_{CAS} = \frac{1}{3.4 \bullet 10^5 \pi f_c}$	C_{CAS} is the regulator filter capacitor and f_c is the desired filter cut-off frequency.
Thermal Management Equations (Normal Active and Tip Open states)	
$R_{TMG} = \frac{V_{BAT} - 6\ V}{I_{LOOP}}$	R_{TMG} is connected from TMG to V_{BAT} and is used to limit power dissipation within the SLIC in Normal Active and Tip Open states only.
$P_{RTMG} = \frac{(V_{BAT} - 6\ V - (I_L \bullet R_L))^2}{R_{TMG}}$	Power dissipated in the thermal management resistor, R_{TMG}, during Active and Tip Open states
$P_{SLIC} = V_{BAT} \bullet I_L - P_{RTMG} - R_L(I_L)^2 + 0.12\ W$	Power dissipated in the SLIC while in Active and Tip Open states
Thermal Management Equations (Polarity Reverse State) **Note: SLIC die temperature should not exceed 140°C.**	
$P_{SLIC} = V_{BAT} \bullet I_L - R_L(I_L)^2 + 0.12\ W$	Power dissipated in the SLIC while in the Polarity Reverse state
$T_{SLIC} = P_{SLIC} \bullet \theta_{JA} + T_{Ambient}$	Total die temperature
Theta JA (θ_{JA}) PDIP = 60°C/watt	Thermal impedance of the 22-pin plastic dip package
Theta JA (θ_{JA}) CDIP = 55°C/watt	Thermal impedance of the 22-pin ceramic dip package
Theta JA (θ_{JA}) PLCC = 43°C/watt	Thermal impedance of the 32-pin plastic leaded chip carrier package

DC FEED CHARACTERISTICS



$R_{DC1} + R_{DC2} = R_{DC} = 18.52\ k\Omega$

Notes:

1. *Constant-current region:*

   Active state, $I_L = \frac{500}{R_{DC}}$

   OHT state, $I_L = \frac{2}{3} \bullet \frac{500}{R_{DC}}$

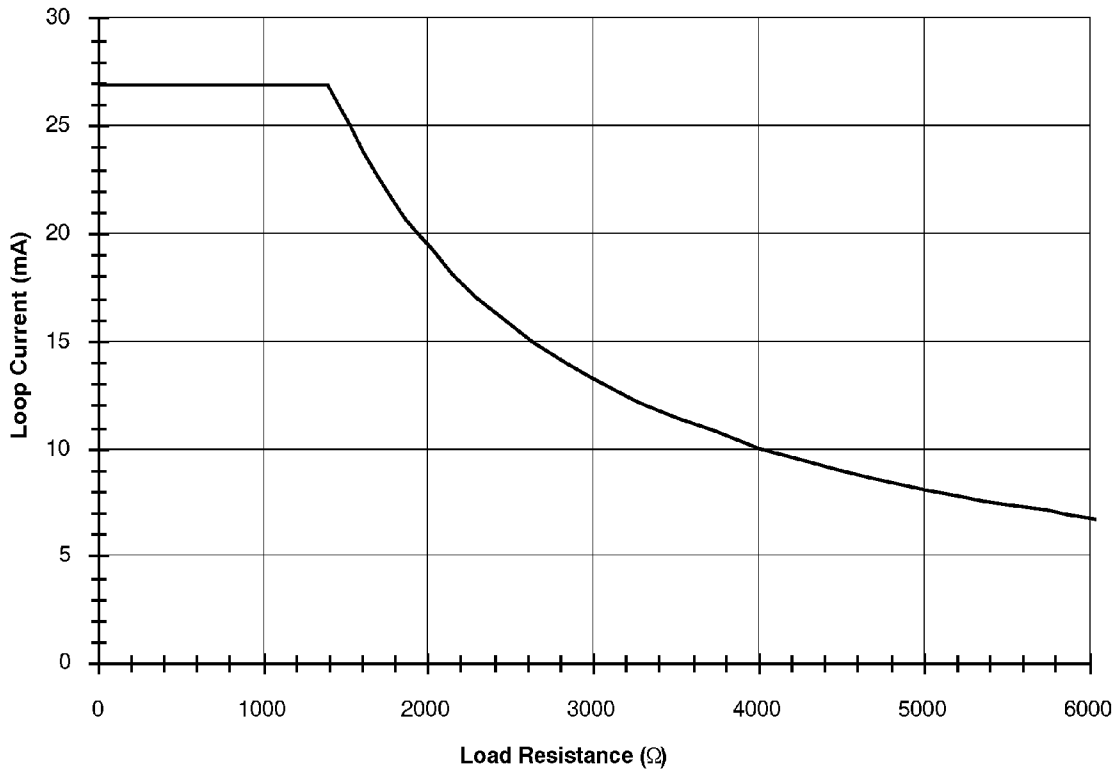
2. *Anti-sat (battery tracking) turn-on:* $V_{AB} = 1.017|V_{BAT}| - 10.7$

3. *Open circuit voltage:* $V_{AB} = 1.017|V_{BAT}| - 6.3$

4. *Anti-sat (battery tracking) region:* $V_{AB} = 1.017|V_{BAT}| - 6.3 - I_L \frac{R_{DC}}{120}$

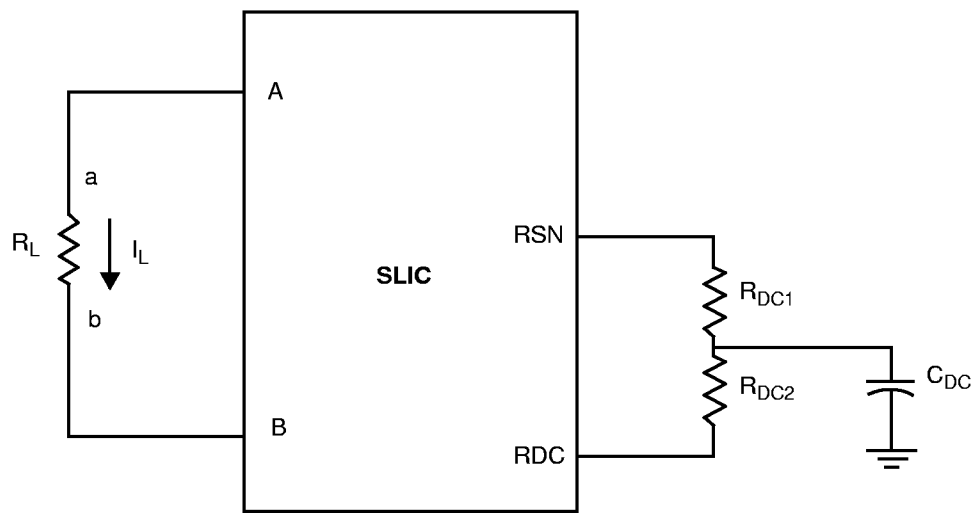
a. V_A–V_B (V_{AB}) Voltage vs. Loop Current (Typical)

DC FEED CHARACTERISTICS (continued)



$R_{DC1} + R_{DC2} = R_{DC} = 18.52\ k\Omega$
$V_{BAT} = 47.3\ V$

b. Loop Current vs. Load Resistance (Typical)

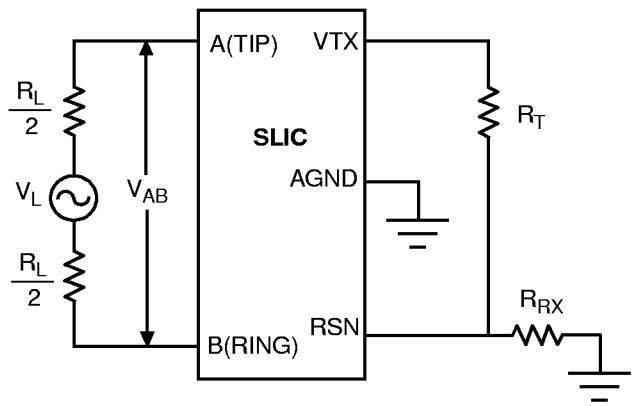


Feed current programmed by R_{DC1} and R_{DC2}

c. Feed Programming

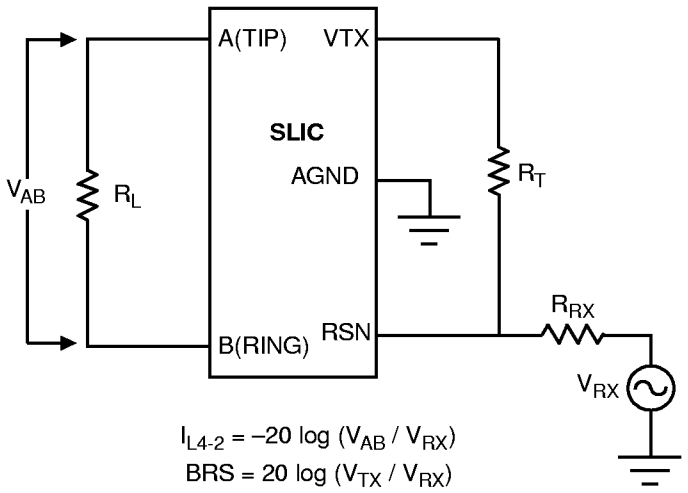
Figure 1. DC Feed Characteristics

TEST CIRCUITS



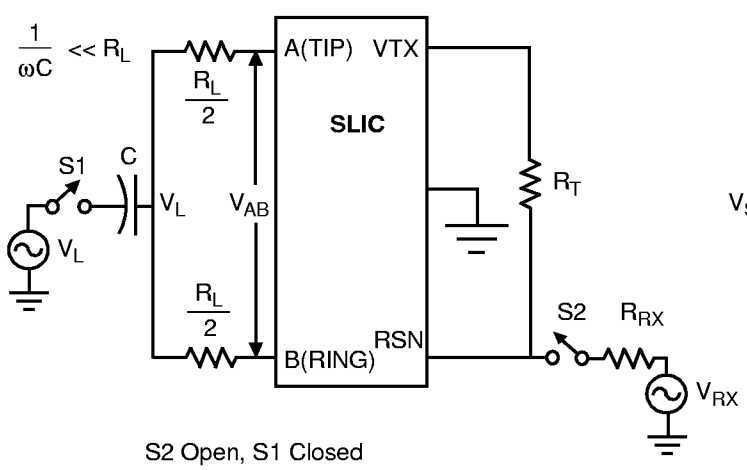
$I_{L2\text{-}4} = -20 \log (V_{TX} / V_{AB})$

A. Two- to Four-Wire Insertion Loss



$I_{L4\text{-}2} = -20 \log (V_{AB} / V_{RX})$
$BRS = 20 \log (V_{TX} / V_{RX})$

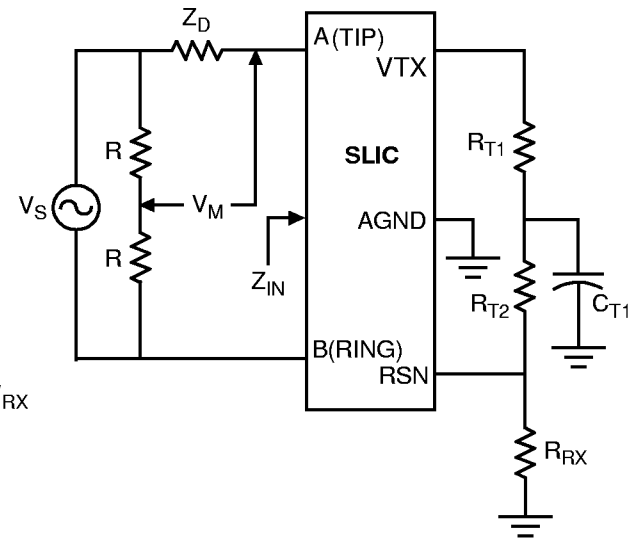
B. Four- to Two-Wire Insertion Loss and Balance Return Signal



S2 Open, S1 Closed
L-T Long. Bal. = 20 log (V_{AB} / V_L)
L-4 Long. Bal. = 20 log (V_{TX} / V_L)

S2 Closed, S1 Open
4-L Long. Sig. Gen. = 20 log (V_L / V_{RX})

C. Longitudinal Balance

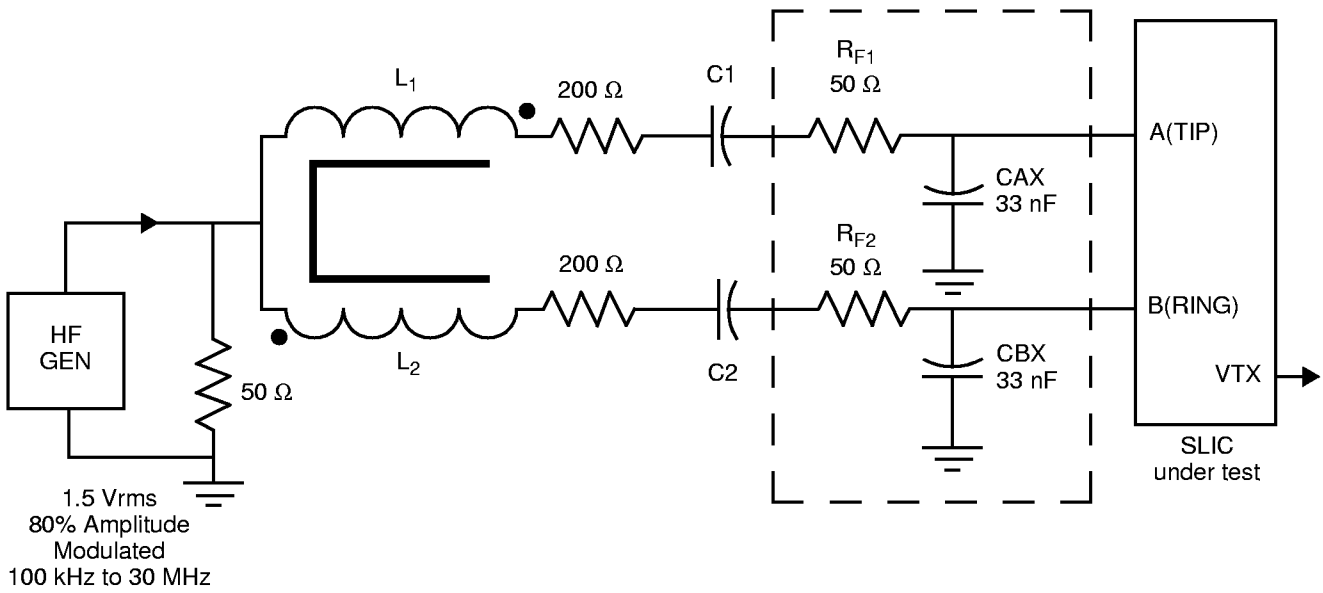


Note:
Z_D is the desired impedance (e.g., the characteristic impedance of the line).

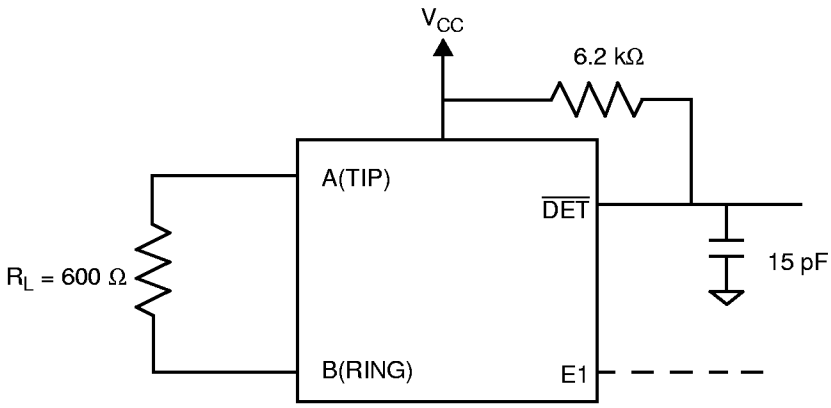
$R_L = -20 \log (2\ V_M / V_S)$

D. Two-Wire Return Loss Test Circuit

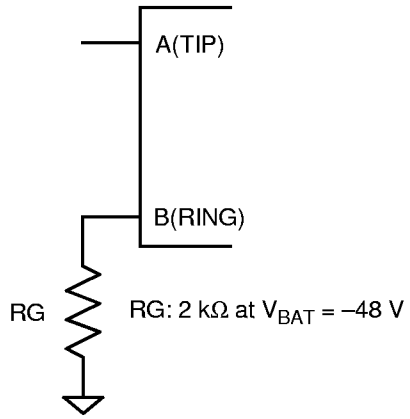
TEST CIRCUITS (continued)



E. RFI Test Circuit

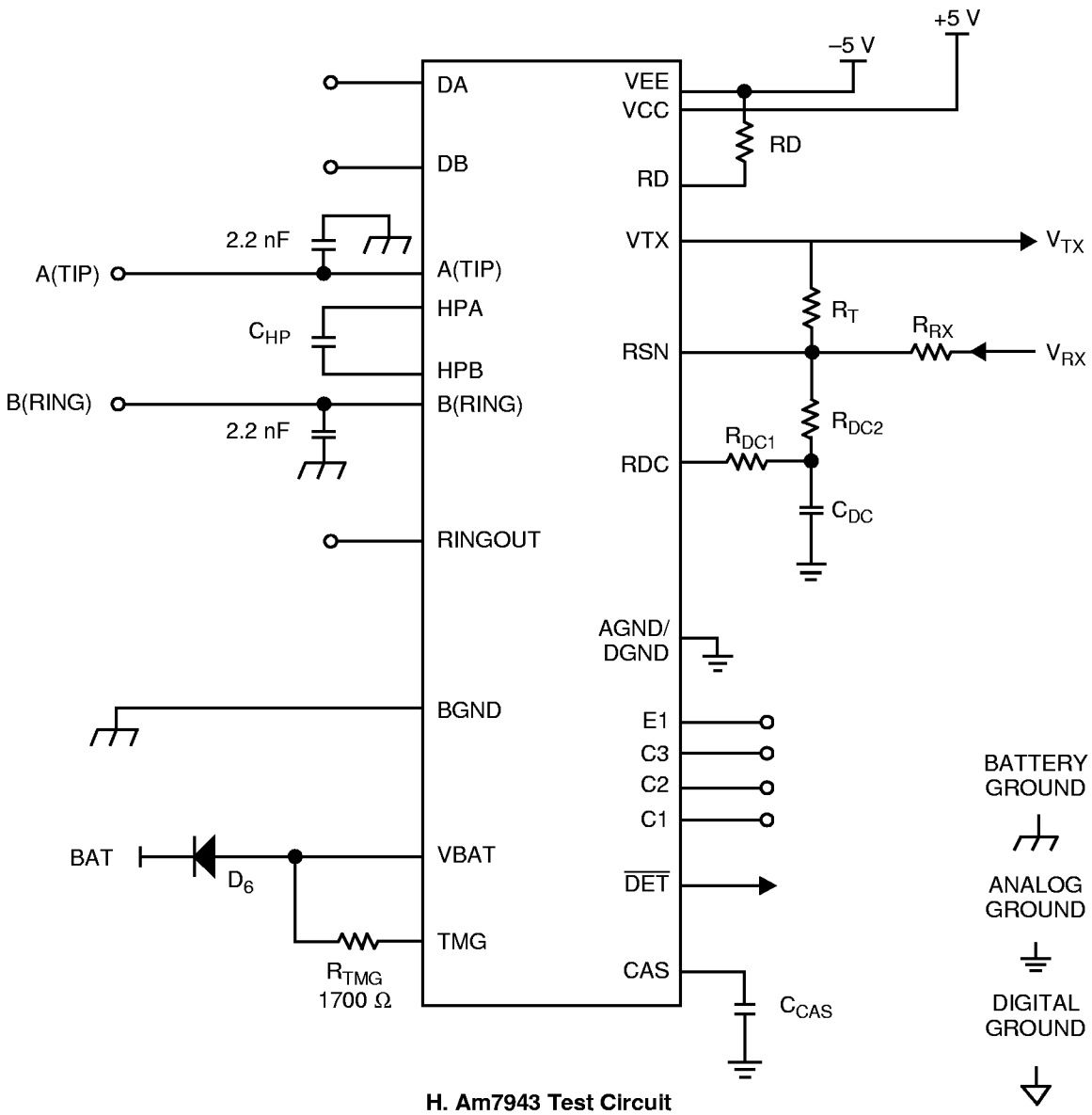


F. Loop-Detector Switching



G. Ground-Key Switching

TEST CIRCUITS (continued)



H. Am7943 Test Circuit

REVISION SUMMARY

Revision A to B

- Minor changes were made to the data sheet style and format to conform to AMD standards.

Revision B to Revision C

- In Pin Description table, inserted/changed TP pin description to: “Thermal pin. Connection for heat dissipation. Internally connected to substrate (QBAT). Leave as open circuit or connected to QBAT. In both cases, the TP pins can connect to an area of copper on the board to enhance heat dissipation.”
- Minor changes were made to the data sheet style and format to conform to AMD standards.

MC

The Maximum Count bit is set whenever the timer reaches its final maximum count value. If the timer is configured in dual MAX COUNT register mode, this bit will be set each time the value in MAX COUNT register A is reached, and each time the value in MAX COUNT register B is reached. This bit is set regardless of the timer's interrupt-enable bit. The MC bit gives the user the ability to monitor timer status through software instead of through interrupts.

Programmers' intervention is required to clear this bit.

RTG

Retrigger bit is only active for internal clocking (EXT = 0). In this case it determines the control function provided by the input pin.

If RTG = 0, the input level gates the internal clock on and off. If the input pin is High, the timer will count; if the input pin is Low, the timer will hold its value. As indicated previously, the input signal may be asynchronous with respect to the 80C186 clock.

When RTG = 1, the input pin detects Low-to-High transitions. The first such transition starts the timer running, clearing the timer value to 0 on the first clock, and then incrementing thereafter. Further transitions on the input pin will again reset the timer to 0, from which it will start counting up again. If CONT = 0, when the timer has reached maximum count, the EN bit will be cleared, inhibiting further timer activity.

P

The Prescaler bit is ignored unless internal clocking has been selected (EXT = 0). If the P bit is a 0, the timer will count at one-fourth the internal CPU clock rate. If the P bit is a 1, the output of Timer 2 will be used as a clock for the timer. Note that the user must initialize and start Timer 2 to obtain the prescaled clock.

EXT

The External bit selects between internal and external clocking for the timer. The external signal may be asynchronous with respect to the 80C186 clock.

If this bit is set, the timer will count Low-to-High transitions on the input pin. If cleared, it will count an internal clock while using the input pin for control. In this mode, the function of the external pin is defined by the RTG bit. The maximum input to output transition latency time may be as much as six clocks. However, clock inputs may be pipelined as closely together as every four clocks without losing clock pulses.

ALT

The ALT bit determines which of two MAX COUNT registers is used for count comparison. If ALT = 0, register A for that timer is always used, while if ALT = 1, the comparison will alternate between register A and register B when each maximum count is reached. This alternation allows the user to change one MAX COUNT register while the other is being used, and thus provides a method of generating non-repetitive waveforms. Square waves and pulse outputs of any duty cycle are a subset of available signals obtained by not changing the final count registers. The ALT bit also determines the function of the timer output pin. If ALT is 0, the output pin will go Low for one clock, the clock after the maximum count is reached. If ALT is 1, the output pin will reflect the current MAX COUNT register being used (0/1 for B/A).

CONT

Setting the CONT bit causes the associated timer to run continuously, while resetting it causes the timer to halt upon maximum count. If CONT = 0 and ALT = 1, the timer will count to the MAX COUNT register A value, reset, count to the register B value, reset, and halt.

Not all mode bits are provided for Timer 2. Certain bits are hardwired as indicated below:

ALT = 0, EXT = 0, P = 0, RTG = 0, RIU = 0

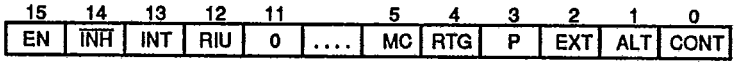
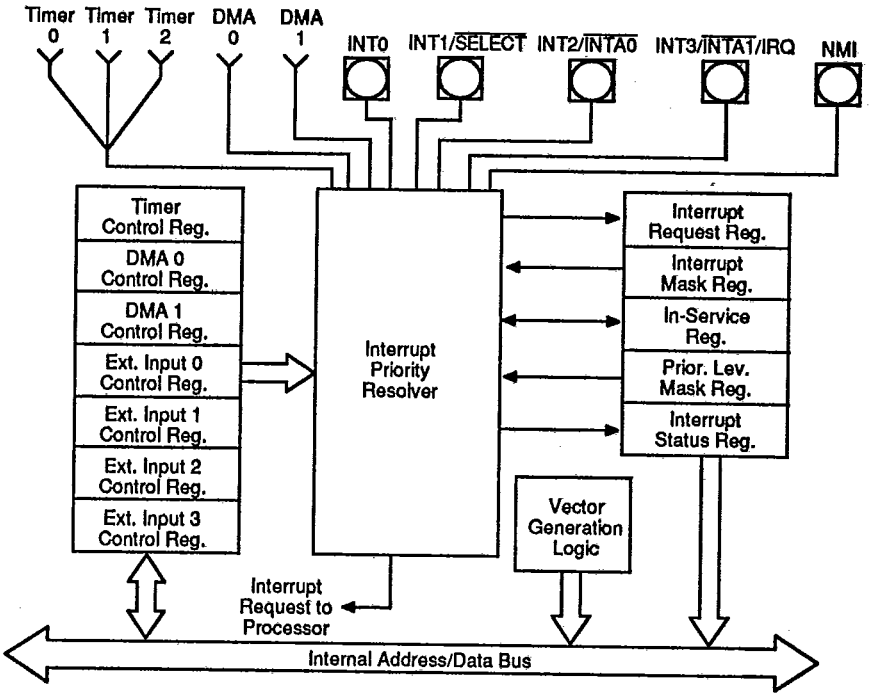


Figure 18. Timer Mode/Control Register 13087D-019



13087D-020

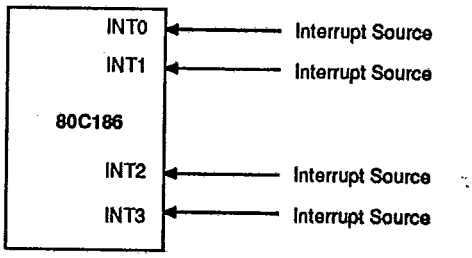
Figure 19. Interrupt Controller Block Diagram

Master Mode Features

Programmable Priority

The user can program the interrupt sources into any of eight different priority levels. The programming is done by placing a 3-bit priority level (0–7) in the control register of each interrupt source. (A source with a priority level of 4 has higher priority over all priority levels from 5 to 7. Priority registers containing values lower than 4 have greater priority.) All interrupt sources have preprogrammed default priority levels (see Table 3).

If two requests with the same programmed priority level are pending at once, the priority ordering scheme shown in Table 3 is used. If the serviced interrupt routine reenables interrupts, it allows other interrupt requests to be serviced.



13087D-021

Figure 20. Fully Nested (Direct) Mode Interrupt Controller Connections

SWITCHING CHARACTERISTICS (continued) T-49-17-15

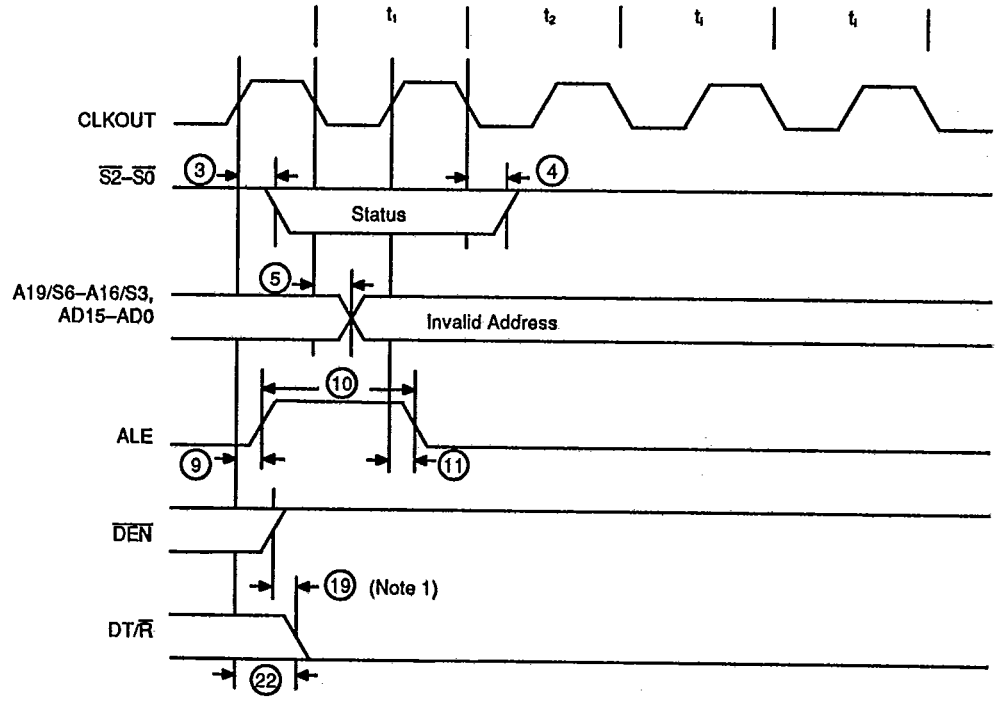
Software Halt Cycle Timings

T_A = 0°C to +70°C, V_{CC} = 5 V ±10% except V_{CC} = 5 V ±5% at f > 12.5 MHz

No	Symbol	Parameter	Preliminary								Unit
			80C186		80C186-12		80C186-16		80C186-20		
			Min	Max	Min	Max	Min	Max	Min	Max	
80C186 General Timing Responses (Listed More Than Once)											
3	t_{CHSV}	Status Active Delay	5	45	5	35	5	31	5	25	ns
4	t_{CLSH}	Status Inactive Delay	5	46	5	35	5	30	5	25	ns
5	t_{CLAV}	Address Valid Delay	5	44	5	36	5	33	5	30	ns
9	t_{CHLH}	ALE Active Delay		30		25		20		20	ns
10	t_{LHLL}	ALE Width	$t_{CLCL}-15$		$t_{CLCL}-15$		$t_{CLCL}-15$		$t_{CLCL}-15$		ns
11	t_{CHLL}	ALE Inactive Delay		30		25		20		20	ns
19	t_{OXDL}	$\overline{DEN}$ Inactive to DT/$\overline{R}$ Low*		0		0		0	0	0	ns
22	t_{CHCTV}	Control Active Delay 2	5	44	5	37	5	31	5	27	ns

All timings are measured at 1.5 V and 100 pF loading on CLKOUT unless otherwise noted.
All output test conditions are with C_L = 50–200 pF (10 MHz) and C_L = 50–100 pF (12.5–20 MHz).
For AC tests, input V_{IL} = 0.45 V and V_{IH} = 2.4 V except at X_1 where V_{IH} = V_{CC} − 0.5 V.
*Equal Loading

Software Halt Cycle Waveforms



Note: 1. For write cycle followed by halt cycle.

SWITCHING CHARACTERISTICS (continued)

Clock Timings

T_A = 0°C to +70°C, V_{CC} = 5 V ±10% except V_{CC} = 5 V ±5% at f > 12.5 MHz

No	Symbol	Parameter	Preliminary 80C186 Min	80C186 Max	80C186-12 Min	80C186-12 Max	80C186-16 Min	80C186-16 Max	80C186-20 Min	80C186-20 Max	Unit
80C186 CLKIN Requirements Measurements taken with following conditions. External clock input to X1 and X2 not connected (float).											
36	t_{CKIN}	CLKIN Period	50		40		31.25		25		ns
37	t_{CLCK}	CLKIN Low Time 1.5 V[2]	20		16		13		7		ns
38	t_{CHCK}	CLKIN High Time 1.5 V[2]	20		16		13		8		ns
39	t_{CKHL}	CLKIN Fall Time 3.5 to 1.0 V		5		5		5		5	ns
40	t_{CKLH}	CLKIN Rise Time 1.0 to 3.5 V		5		5		5		5	ns
80C186 CLKOUT Timing											
41	t_{CICO}	CLKIN to CLKOUT Skew		25		21		17		13	ns
42	t_{CLCL}	CLKOUT Period	100		80		62.5		50		ns
43	t_{CLCH}	CLKOUT Low Time									
		C_L = 100 pF[2]	0.5 t_{CLCL}−8		0.5 t_{CLCL}−7		0.5 t_{CLCL}−7		0.5 t_{CLCL}−7		ns
		C_L = 50 pF[3]	0.5 t_{CLCL}−6		0.5 t_{CLCL}−5		0.5 t_{CLCL}−5		0.5 t_{CLCL}−5		ns
44	t_{CHCL}	CLKOUT High Time									
		C_L = 100 pF[4]	0.5 t_{CLCL}−8		0.5 t_{CLCL}−7		0.5 t_{CLCL}−7		0.5 t_{CLCL}−7		ns
		C_L = 50 pF[3]	0.5 t_{CLCL}−6		0.5 t_{CLCL}−5		0.5 t_{CLCL}−5		0.5 t_{CLCL}−5		ns
45	t_{CH1CH2}	CLKOUT Rise Time 1.0 to 3.5 V		10		10		10		10	ns
46	t_{CL2CL1}	CLKOUT Fall Time 3.5 to 1.0 V		10		10		10		10	ns

All timings are measured at 1.5 V and 100 pF loading on CLKOUT unless otherwise noted.
All output test conditions are with C_L = 50–200 pF (10 MHz) and C_L = 50–100 pF (12.5–20 MHz).
For AC tests, input V_{IL} = 0.45 V and V_{IH} = 2.4 V except at X_1 where V_{IH} = V_{CC} − 0.5 V.

Notes: 1. t_{CLCK} and t_{CHCK} (CLKIN Low and High times) should not have a duration less than 40% of t_{CKIN}.
2. Tested under worst case conditions: V_{CC} = 5.5 V (5.25 V @ 20 MHz), T_A = 70°C.
3. Not tested.
4. Tested under worst case conditions: V_{CC} = 4.5 V (4.75 V @ 20 MHz), T_A = 0°C.

Clock Waveforms