PRELIMINARY

Am79530/Am79531/ Am79534/Am79535

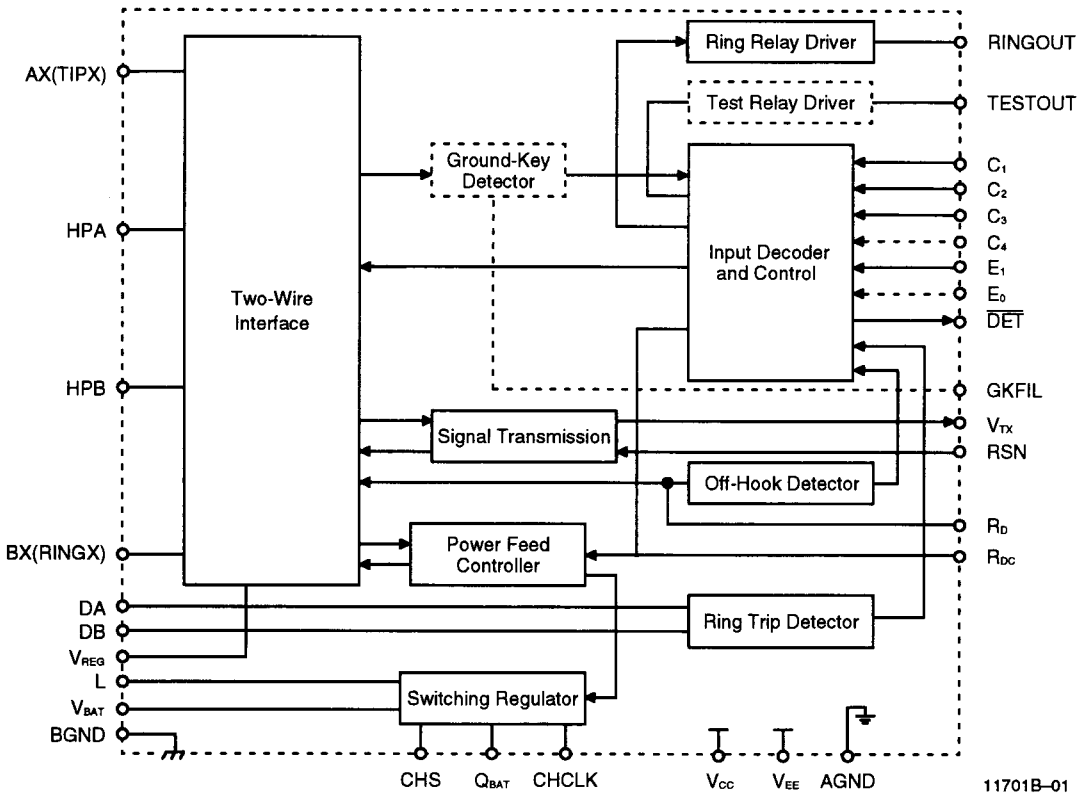
Subscriber Line Interface Circuit

Advanced Micro Devices

DISTINCTIVE CHARACTERISTICS

- Programmable constant current feed
- Line-feed characteristics independent of battery variations
- Programmable loop detect threshold
- On-chip switching regulator for low-power dissipation
- Pin for external ground-key noise filter capacitor available
- Ground-key detect
- Low standby power
- Two-wire impedance set by single external impedance
- Polarity reversal feature
- Tip open state for ground start lines
- Test relay driver optional

BLOCK DIAGRAM

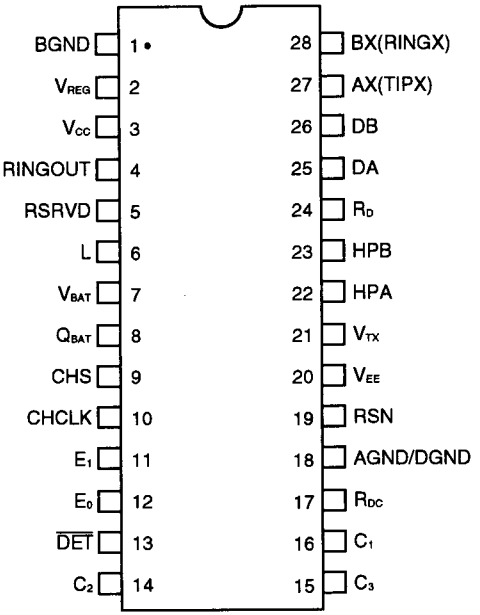


Notes: Am79530—E_0 and E_1 inputs; ring relay sourced internally to BGND; no test relay driver.
Am79531—E_0 and E_1 inputs; ring relay sourced internally to BGND; no test relay driver; ground-key filter pin.
Am79534—E_0 and E_1 inputs; ring and test relay drivers sourced internally to BGND.
Am79535—E_0 and E_1 inputs; ring relay driver sourced internally to BGND; ground-key filter pin.
Current gain (K_I) = 1000 for all parts.

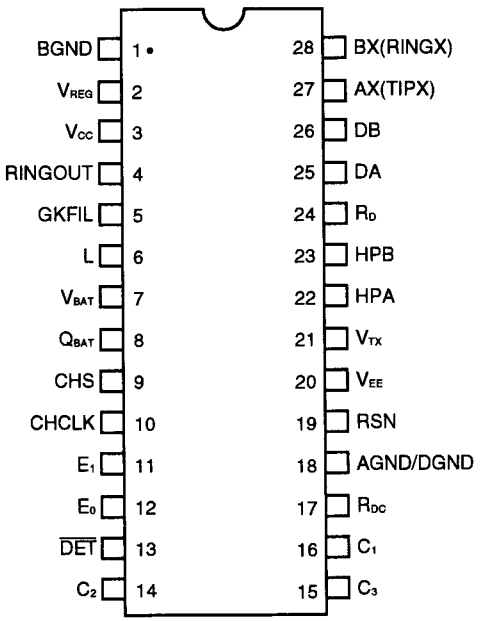
Publication #: 16854 Rev. A Amendment /0
Issue Date: June 1992

CONNECTION DIAGRAMS
Top View

Am79530



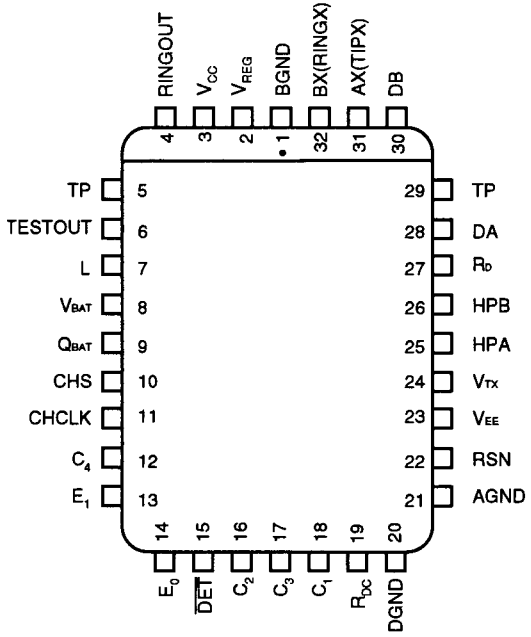
Am79531



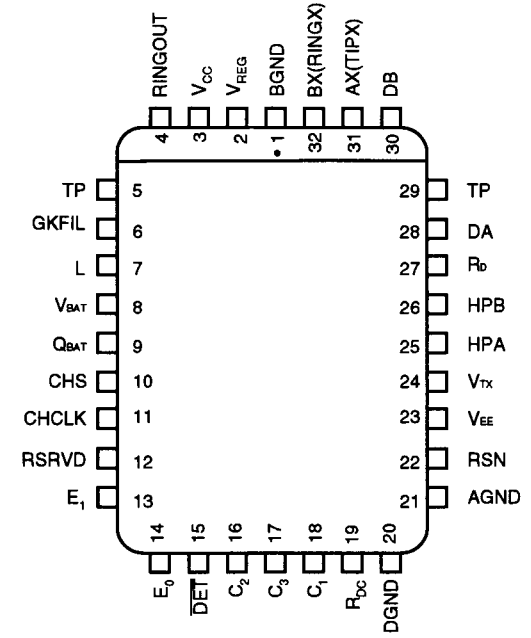
Note: Pin 1 is marked for orientation.

CONNECTION DIAGRAMS (continued)

Am79534



Am79535

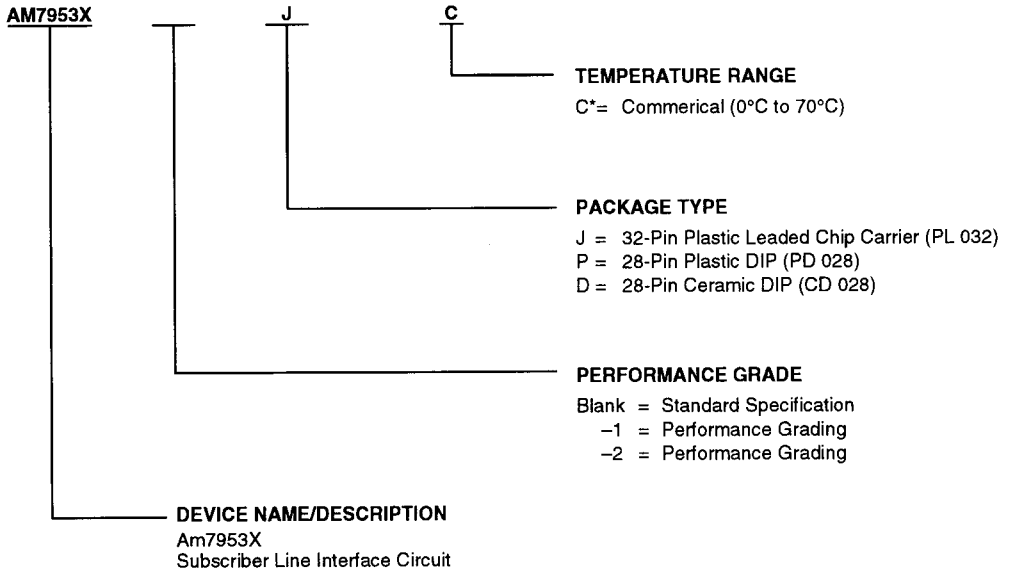


Notes: 1. Pin 1 is marked for orientation.
2. TP is a thermal conduction pin tied to substrate (Q_{BAT}).

ORDERING INFORMATION

Standard Products

AMD standard products are available in several packages and operating ranges. The order number (Valid Combination) is formed by a combination of the elements below.



Valid Combinations	
AM7953X	DC, JC, PC
	–1DC, –1JC, –1PC
	–2DC, –2JC, –2PC

Valid Combinations

Valid Combinations list configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations, to check on newly released combinations, and to obtain additional data on AMD's standard military grade products.

*The performance specifications contained in this data sheet are valid for the commercial temperature range only. See the SLIC Extended Temperature Supplement for information on industrial temperature range (–40°C to +85°C) specifications.

PIN DESCRIPTION

AGND

Ground (Am79534 and Am79535)

Analog (Quiet) ground.

DGND

Ground (Am79534 and Am79535)

Digital ground.

AGND/DGND

Ground (Am79530, Am79531)

Analog and digital ground are connected internally to a single pin.

AX(TIPX)

(Output)

Output of A(TIP) power amplifier.

BGND

Ground

Battery (power) ground.

BX(RINGX)

(Output)

Output of B(RING) power amplifier.

C_3–C_1

Decoder (Inputs)

TTL compatible. C_3 is MSB and C_1 is LSB.

C_4

Test Relay Driver Command (Input) (Am79534)

TTL compatible. A logic Low enables the driver.

CHCLK

Chopper Clock (Input)

Input to switching regulator (TTL compatible). Frequency = 256 kHz (Nominal).

CHS

Chopper Stabilization (Input)

Connection for external stabilization components.

DA

Ring Trip Negative (Input)

Negative input to ring trip comparator.

DB

Ring Trip Positive (Input)

Positive input to ring trip comparator.

$\overline{DET}$

Detector (Output)

When enabled, a logic Low indicates that the selected detector is tripped. The detector is selected by the logic inputs (C_3–C_1, E_0, E_1). The output is open-collector with a built-in 15K pull-up resistor.

E_0

Read Enable (Input)
(Am79530, Am79531, and Am79534)

A logic High enables $\overline{DET}$. A logic Low disables $\overline{DET}$.

E_1

Ground Key Enable (Input)

When E_0 is High, E_1 = High connects the ground-key detector to $\overline{DET}$, and E_1 = Low connects the off-hook or ring trip detector to $\overline{DET}$.

GKFIL

Ground-Key Filter Capacitor Connection
(Am79531 and Am79535)

An external capacitor for filtering out high-frequency noise from the ground-key loop can be connected to this pin. An internal 36K –20%, +40% resistor is provided to form an RC filter with the external capacitor.

In versions which have a GKFIL pin, 3.3 nF minimum capacitance must be connected from the GKFIL pin to ground.

HPA

A(TIP) side of high-pass filter capacitor.

HPB

B(RING) side of high-pass filter capacitor.

L

Switching Regulator Power Transistor (Output)

Connection point for filter inductor and anode of catch diode. This pin will have up to 60 V of pulse waveform on it and must be isolated from sensitive circuits. Extreme care must be taken to keep the diode connections short because of the high currents and high di/dt.

Q_{BAT}

Quiet Battery

Filtered battery supply for the signal processing circuits.

R_D

Threshold modification and filter point for the off-hook detector.

R_{DC}

Connection point for the DC feed current programming network. The other end of the network connects to the Receiver Summing Node (RSN). The sign of V_{RDC} is minus for normal polarity and plus for reverse polarity.

RINGOUT

Ring Relay Driver (Output)

Sourcing from BGND with internal diode to Q_{BAT}.

TESTOUT

Test Relay Driver (Output) (Am79534)

Sourcing from BGND with internal diode to Q_{BAT}.

RSN

Receive Summing Node (Input)

The metallic current (both AC and DC) between A(TIP) and B(RING) is equal to 1000 times the current into this pin. The networks that program receive gain, two-wire impedance, and feed current all connect to this node. This node is extremely sensitive. Care should be taken to route the 256-kHz chopper clock and switch lines away from the RSN node.

V_{BAT}

Connected to office battery supply through an external protection diode.

V_{CC}

+5-V power supply.

V_{EE}

–5-V power supply.

V_{REG}

Regulated Voltage (Input)

Provides negative power supply for power amplifiers and connection point for inductor, filter capacitor, and chopper stabilization.

V_{TX}

Transmit Audio (Output)

This output is a unity gain version of the AX(TIPX) and BX(RINGX) metallic voltage. The other end of the two-wire input impedance programming network connects here.

ABSOLUTE MAXIMUM RATINGS

Storage Temperature ..... –55°C to +150°C

V_{CC} with respect to AGND/DGND .. –0.4 V to +7.0 V

V_{EE} with respect to AGND/DGND .. +0.4 V to –7.0 V

V_{BAT} with respect to AGND/DGND ... +0.4 V to –70 V

Note: Rise time of V_{BAT} (dv/dt) must be limited to 27 V/µs or less when Q_{BAT} bypass = 0.33 µF.

BGND with respect to
AGND/DGND ..... +1.0 V to –3.0 V

AX(TIPX) or BX(RINGX) to BGND:

Continuous ..... –70 V to +1.0 V
10 ms (F = 0.1 Hz) ..... –70 V to +5.0 V
1 µs (F = 0.1 Hz) ..... –90 V to +10 V
250 ns (F = 0.1 Hz) ..... –120 V to +15 V

Current from AX(TIP) or BX(RING) ..... ±150 mA

Voltage on RINGOUT .... BGND to 70 V above Q_{BAT}

Voltage on TESTOUT .... BGND to 70 V above Q_{BAT}

Current through Relay Drivers ..... 60 mA

Voltage on Ring Trip Inputs
(DA and DB) ..... V_{BAT} to 0 V

Current into Ring Trip Inputs ..... ±10 mA

Peak Current into Regulator
Switch (L pin) ..... 150 mA

Switcher Transient Peak Off
Voltage on L pin ..... +1.0 V

C4–C1, E1, CHCLK to
AGND/DGND ..... –0.4 V to V_{CC} + 0.4 V

Maximum Power Dissipation, T_A (see note) ... 70°C
In 28-pin ceramic DIP package ..... 2.58 W
In 28-pin plastic DIP package ..... 1.4 W
In 32-pin PLCC package ..... 1.74 W

Note: Thermal limiting circuitry on chip will shut down the circuit at a junction temperature of about 165°C. The device should never see this temperature and operation above 145°C junction temperature may degrade device reliability. See SLIC Packaging Considerations section for more information.

Stresses above those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to absolute maximum ratings for extended periods may effect device reliability.

OPERATING RANGES

Commercial (C) Devices

Ambient Temperature ..... 0°C to +70°C

V_{CC} ..... 4.75 V to 5.25 V

V_{EE} ..... –4.75 V to –5.25 V

V_{BAT} ..... –40 V to –63 V

AGND/DGND ..... 0 V

BGND with respect to
AGND/DGND ..... –100 mV to +100 mV

Load Resistance on V_{TX} to Ground .... 10 Kohm Min

"–2" performance grade SLICs are functional from –40°C to +85°C. See the SLIC Extended Temperature Supplement for information on industrial temperature range (–40°C to +85°C) specifications.

Operating ranges define those limits between which the functionality of the device is guaranteed.

ELECTRICAL CHARACTERISTICS over operating range

Am79530/Am79531/Am79534/Am79535 (see Note 1)

Description	Test Conditions	Preliminary P.G.*	Min	Typ	Max	Unit
Analog (V_{TX}) Output Impedance (Note 5)				3		ohm
Analog (V_{TX}) Output Offset			–35		+35	mV
		–1	–30		+30	
Analog (RSN) Input Impedance (Note 5)	300 Hz to 3.4 kHz			1	20	ohm
Longitudinal Impedance at AX or BX					35	
Overload Level	four-wire		–3.1		+3.1	Vpk
Z_{ZWIN} = 600 to 900 ohms (Note 2)	two-wire					
Transmission Performance, two-wire impedance						
Two-Wire Return Loss	300 Hz to 500 Hz		26			dB
(See Test Circuit D)	500 Hz to 2500 Hz		26			
(Notes 5, 10)	2500 Hz to 3400 Hz		20			
Longitudinal Balance (two-wire and four-wire, see Test Circuit C)						
R_L = 600 ohms	300 Hz to 3400 Hz		48			dB
Longitudinal to Metallic L-T, L-4		–1	52			
Longitudinal to Metallic L-T and	200 Hz to 1000 Hz	–2**	63	70		
L-4 for trimmed version (consult factory)	1000 Hz to 3400 Hz		58	70		
	200 Hz to 3400 Hz (Reverse polarity)		54			
Longitudinal Signal Generation 4-L	300 Hz to 800 Hz		40			dB
	300 Hz to 800 Hz	–1	42			
Longitudinal Current Capability	Active State			25		mA
per Wire (Note 5)	Disable State			18		RMS
Insertion Loss (two-wire to four-wire and four-wire to two-wire, see Test Circuits A and B)						
Gain Accuracy	0 dBm, 1 kHz		–0.15		+0.15	dB
		–1	–0.1		+0.1	
Variation with Frequency (Note 5)	300 Hz to 3400 Hz Relative to 1 kHz		–0.1		+0.1	dB
Gain Tracking (Note 5)	+7 dBm to –55 dBm Reference: 0 dBm		–0.1		+0.1	dB
Balance Return Signal (four-wire to four-wire, see Test Circuit B)						
Gain Accuracy (Note 3)	0 dBm, 1 kHz		–0.15		+0.15	dB
		–1	–0.1		+0.1	
Variation with Frequency (Notes 3, 5)	300 Hz to 3400 Hz Relative to 1 kHz		–0.1		+0.1	dB
Gain Tracking (Note 5)	+3 dBm to –55 dBm Reference: 0 dBm		–0.1		+0.1	dB
Group Delay (Notes 5, 12)	F = 1 kHz			5.3		µs
Total Harmonic Distortion (two-wire to four-wire or four-wire to two-wire, see Test Circuits A and B)						
Total Harmonic Distortion	0 dBm, 300 Hz–3.4 kHz			–64	–50	dB
	+9 dBm, 300 Hz–3.4 kHz			–55	–40	

*P.G. = Performance Grade
**All other performance parameters equivalent to –1 grade.
Normal Polarity only.

ELECTRICAL CHARACTERISTICS (continued)

Description	Test Conditions	Preliminary P.G.	Min	Typ	Max	Unit
Idle Channel Noise						
C-Message Weighted Noise (Notes 5, 7)	two-wire			+7	+15	dBrnC
		–1		+7	+12	
	four-wire			+7	+15	dBrnC
		–1		+7	+12	
Psophometric Weighted Noise (Note 7)	two-wire			–83	–75	dBmp
		–1		–83	–78	
	four-wire			–83	–75	dBmp
		–1		–83	–78	
Single Frequency Out-of-Band Noise (see Test Circuit E)						
Metallic	4 kHz to 9 kHz			–76		dBm
(Notes 4, 5, 9)	9 kHz to 1 MHz			–76		
(Notes 4, 5)	256 kHz and harmonics			–57		
Longitudinal	1 kHz to 15 kHz			–70		dBm
(Notes 4, 5, 9)	Above 15 kHz			–85		
(Notes 4, 5)	256 kHz and harmonics			–57		
DC Feed Currents (see Figures 1a, 1b, 1c) Battery = –48 V						
Active Mode Loop Current Accuracy	I_{LOOP} (nominal) = 40 mA		–7.5		+7.5	%
Disable Mode	R_L = 600 ohms		18	20	22	mA
Tip Open Mode	R_L = 600 ohms				1.0	
Open Circuit Mode	R_L = 0 ohms				1.0	
Fault Current Limit, I_{LLIM} (I_{AX} + I_{BX})	AX and BX shorted to ground				130	mA
Power Dissipation Battery = –48 V, Normal Polarity						
On-Hook Open Circuit				35	120	mW
		–1		35	80	
On-Hook Disable Mode				135	250	
		–1		135	200	
On-Hook Active Mode				200	400	
		–1		200	300	
Off-Hook Disable Mode	R_L = 600 ohms			500	750	
Off-Hook Active Mode	R_L = 600 ohms			650	1000	
Supply Currents						
V_{CC} On-Hook Supply Current	Open Circuit Mode			3.0	4.5	mA
	Disable Mode			6.0	10.0	
	Active Mode			7.5	12.0	
V_{EE} On-Hook Supply Current	Open Circuit Mode			1.0	2.3	mA
	Disable Mode			2.2	3.5	
	Active Mode			2.7	6.0	
V_{BAT} On-Hook Supply Current	Open Circuit Mode			0.4	1.0	mA
	Disable Mode			3.0	5.0	
	Active Mode			4.0	6.0	

ELECTRICAL CHARACTERISTICS (continued)

Description	Test Conditions	Preliminary P.G.	Min	Typ	Max	Unit
Power Supply Rejection Ratio (Vripple = 50 mV RMS)						
V_{CC} (Notes 6, 7)	50 Hz to 3400 Hz		25	45		dB
		–1	30	45		
	3.4 kHz to 50 kHz		22	35		dB
		–1	25	35		
V_{EE} (Notes 6, 7)	50 Hz to 3400 Hz		20	40		dB
		–1	25	40		
	3.4 kHz to 50 kHz		10	25		dB
		–1	10	25		
V_{BAT} (Notes 6, 7)	50 Hz to 3400 Hz		27	45		dB
		–1	30	45		
	3.4 kHz to 50 kHz		20	40		dB
		–1	25	40		
Off-Hook Detector						
Current Threshold Accuracy	I_{DET} = 365/R_D Nominal		–20		+20	%
Ground-Key Detector Thresholds, Active Mode, Battery = –48 V (see Test Circuit F)						
Ground-Key Resistance Threshold	B(Ring) to GND		2.0	5.0	10.0	Kohm
Ground-Key Current Threshold (Note 8)	B(Ring) to GND			9		mA
	Midpoint to GND			9		
Ring Trip Detector Input						
Bias Current			–5	–0.05		µA
Offset Voltage (Note 11)	Source Resistance 0 to 2 Mohm		–50	0	+50	mV
Logic Inputs (C_1, C_2, C_3, C_4, E_0, E_1, and CHCLK)						
Input High Voltage			2.0			V
Input Low Voltage					0.8	V
Input High Current			–75		40	µA
Input Low Current			–0.4			mA
Logic Output ($\overline{DET}$)						
Output Low Voltage	I_{OUT} = 0.8 mA				0.4	V
Output High Voltage	I_{OUT} = –0.1 mA		2.4			V

SWITCHING CHARACTERISTICS
Am79530/Am79531/Am79534/Am79535

Parameter		Test Conditions	Min	Typ	Max	Unit
tgkde	E_1 High to $\overline{DET}$ High (E_0 = 1)	Ground-Key Detect Mode R_L Open, R_G Connected (see Test Circuit H)			3.8	µs
	E_1 High to $\overline{DET}$ Low (E_0 = 1)				1.1	
tshde	E_1 Low to $\overline{DET}$ Low (E_0 = 1)	Switch Hook Detect Mode R_L = 600 ohms, R_G Open (see Test Circuit G)			1.2	µs
	E_1 Low to $\overline{DET}$ High (E_0 = 1)				3.8	
tshdd	E_0 High to $\overline{DET}$ Low (E_1 = 0)				1.1	µs
tshd0	E_0 Low to $\overline{DET}$ High (E_1 = 0)				3.8	
tgkdd	E_0 High to $\overline{DET}$ Low (E_1 = 1)				1.1	µs
tgkd0	E_0 Low to $\overline{DET}$ High (E_1 = 1)				3.8	

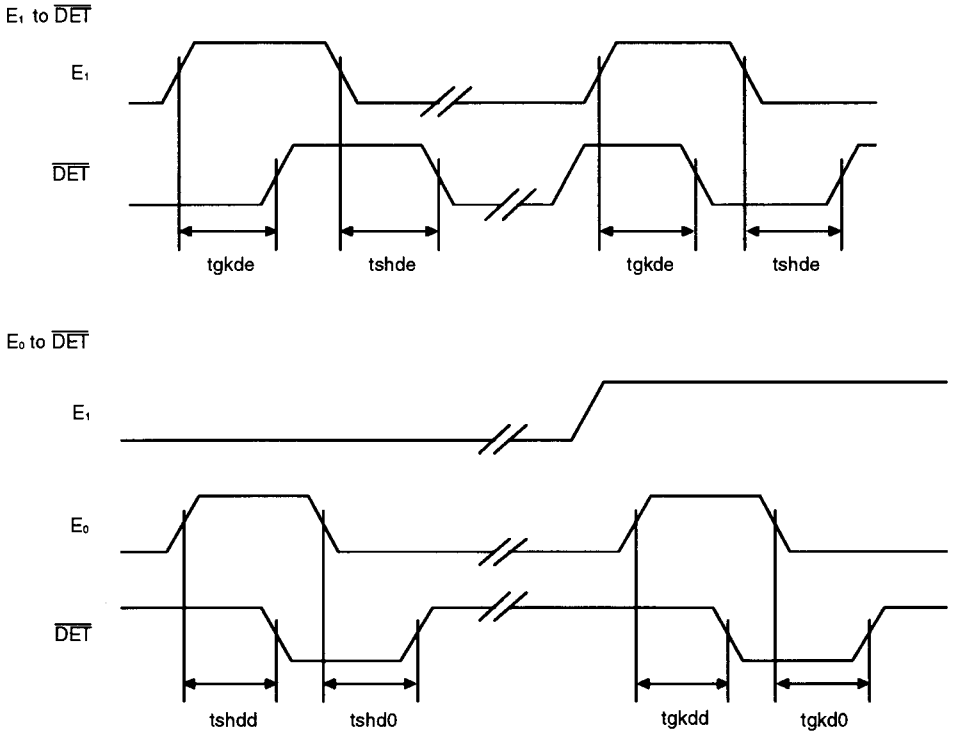
Table 1. SLIC Decoding

					$\overline{DET}$ Output	
State	C_3	C_2	C_1	Two-Wire Status	E_0 = 1* E_1 = 0	E_0 = 1* E_1 = 1
0	0	0	0	Open Circuit	Ring Trip	Ring Trip
1	0	0	1	Ringing	Ring Trip	Ring Trip
2	0	1	0	Active	Loop Det.	Ground Key
3	0	1	1	Disable	Loop Det.	Ground Key
4	1	0	0	Tip Open	Loop Det.	—
5	1	0	1	Reserved	Loop Det.	—
6	1	1	0	Active Polarity Reversal	Loop Det.	Ground Key
7	1	1	1	Disable Polarity Reversal	Loop Det.	Ground Key

For the Am79530, Am79531, Am79534, and Am79535, a logic Low on E_0 disables the $\overline{DET}$ output into the open-collector state.

SWITCHING WAVEFORMS

Am79530/Am79531/Am79534/Am79535

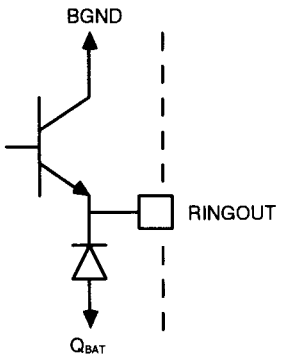


11701B–002

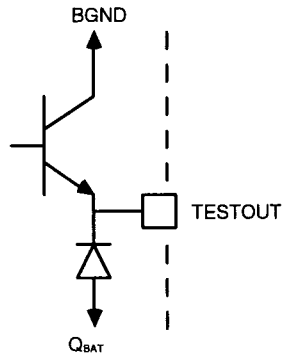
Note: All delays measured at 1.4-V level.

Relay Driver Specifications

Am79530/Am79531/
Am79534/Am79535



Am79534



11701B–003

Description	Test Conditions	Min	Typ	Max	Unit
Relay Driver Outputs (RINGOUT, TESTOUT)					
On Voltage	50 mA Source	BGND –2	BGND – 0.95		V
Off Leakage			0.5	100	µA
Clamp Voltage	50 mA Sink	Q_{BAT} –2			V

Notes:

1. Unless otherwise noted, test conditions are: Battery = –48 V, V_{CC} = +5 V, V_{EE} = –5 V, R_L = 600 ohms, C_{HP} = 0.22 µF, $R_{DC1} = R_{DC2} = 31.25K$, $C_{DC} = 0.1$ µF, $R_d = 51.1K$, no fuse resistors, two-wire AC output impedance, programming impedance (Z_T) = 600K resistive, receive input summing impedance (Z_{RX}) = 300K resistive. (See Table 2 for component formulas.)

2. Overload level is defined when THD = 1%.

3. Balance return signal is the signal generated at V_{TX} by V_{RX}. This spec assumes that the two-wire AC load impedance matches the impedance programmed by Z_T.

4. These tests are performed with a longitudinal impedance of 90 ohms and metallic impedance of 300 ohms for frequencies below 12 kHz and 135 ohms for frequencies greater than 12 kHz. These tests are extremely sensitive to circuit board layout.

5. Not tested in production. This parameter is guaranteed by characterization or correlation to other tests.

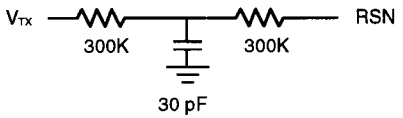
6. This parameter is tested at 1 kHz in production. Performance at other frequencies is guaranteed by characterization.

7. When the SLIC is in the Anti-sat 2 operating region, this parameter will be degraded. The exact degradation will depend on system design. The Anti-sat 2 region occurs at high loop resistances when $|V_{BAT}| - |V_{AX} - V_{BX}|$ is less than approximately 11 V.

8. "Midpoint" is defined as the connection point between two 300-ohm series resistors connected between A(TIP) and B(RING).

9. Fundamental and harmonics from 256-kHz switch-regulator chopper are not included.

10. Assumes the following Z_T network:



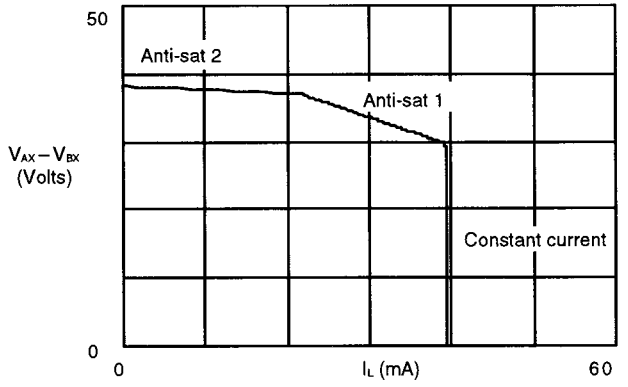
11. Tested with 0 ohm source impedance. Two Mohms is specified for system design purposes only.

12. Group delay can be considerably reduced by using a Z_T network such as that shown in Note 10 above. The network will reduce the group delay to less than 2 µs. The effect of group delay on linecard performance may be compensated for by using SLAC or DSLAC devices.

Table 2. User-Programmable Components

$Z_T = 1000(Z_{2WIN} - 2R_F)$	Z_T is connected between the V_{TX} and RSN pins. The fuse resistors are R_F, and Z_{2WIN} is the desired two-wire AC input impedance. When computing Z_T, the internal current amplifier pole and any external stray capacitance between V_{TX} and RSN must be taken into account.
$Z_{RX} = \frac{Z_L}{G42L} \cdot \frac{1000\ Z_T}{Z_T + 1000(Z_L + 2R_F)}$	Z_{RX} is connected from V_{RX} to the RSN pin and Z_T is defined above and G42L is the desired receive gain.
$R_{DC1} + R_{DC2} = 2500/I_{FEED}$ $C_{DC} = (1.5\ ms)(R_{DC1} + R_{DC2})/(R_{DC1}R_{DC2})$	R_{DC1}, R_{DC2}, and C_{DC} form the network connected to the R_{DC} pin. R_{DC1} and R_{DC2} are approximately equal.
$R_D = 365/I_T$, $C_D = 0.5\ ms/R_D$	R_D and C_D form the network connected from R_D to –5 V, and I_T is the threshold current between on-hook and off-hook.

$V_{BAT} = -47.3$ V
$R_{DC1} + R_{DC2} = R_{DC} = 62.5K$



Constant current region: $I_L = \frac{2500}{R_{DC}}$

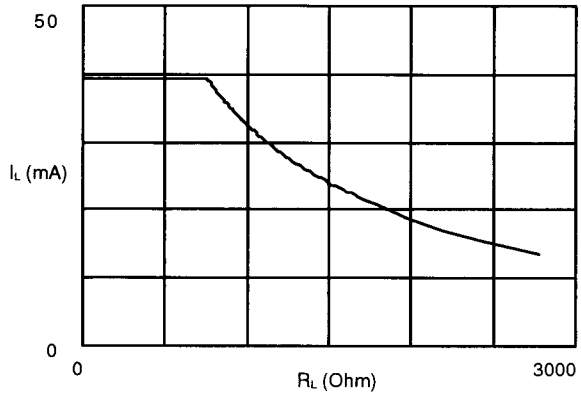
Anti-sat 1 region: $V_{AX-BX} = 45.78 - \frac{R_{DC}}{152.6} I_L$

Anti-sat 2 region: $V_{AX-BX} = 1.067 | V_{BAT} | - 12.22 - \left(0.0128 + \frac{R_{DC}}{1523}\right) I_L$

See Figure 1c.

11701B–004

Figure 1a. Load Line (Typical)

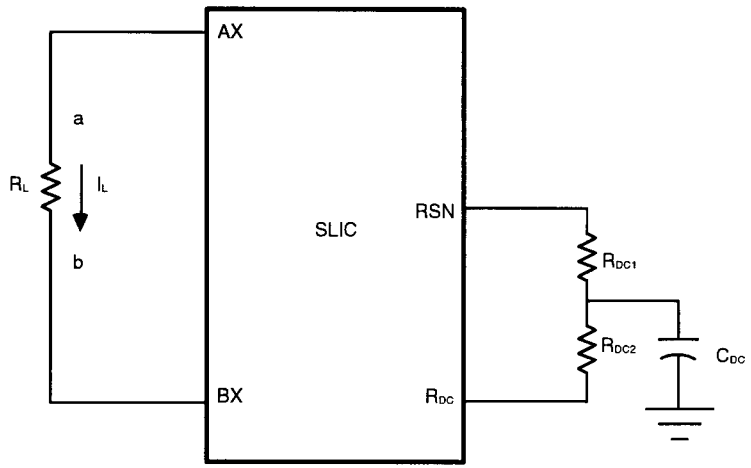


Load Current versus Load Resistance—Am79530/Am79531/Am79534/Am79535
V_{BAT} = –47.3 V
R_{DC} = 62.5K

See Figure 1c.

11701B–005

Figure 1b. Feed Characteristics (Typical)

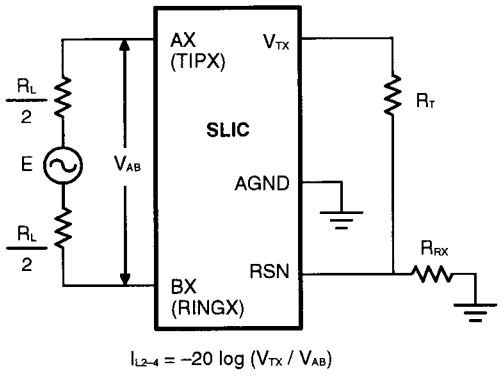


Current programmed by R_{DC1} and R_{DC2}.

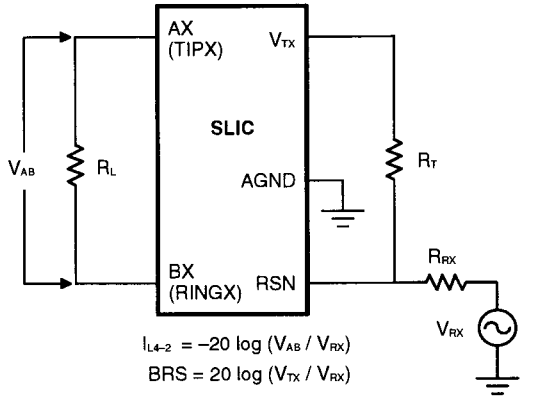
11701B–006

Figure 1c. Feed Programming

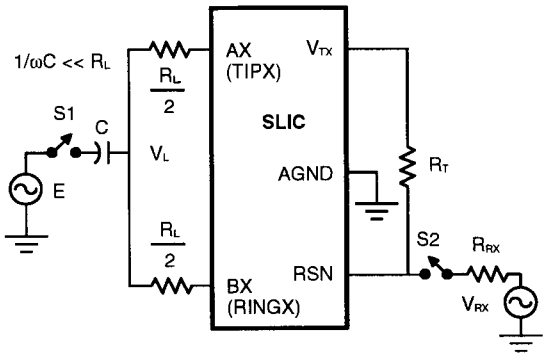
TEST CIRCUITS



A. Two-to-Four Wire Insertion Loss



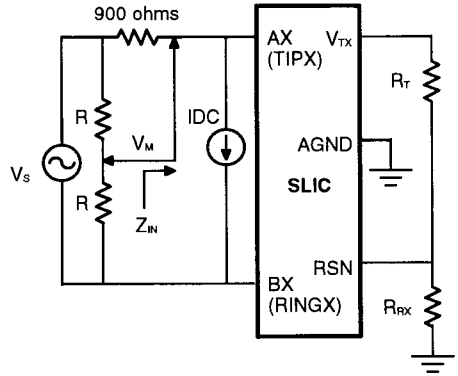
B. Four-to-Two Wire Insertion Loss and Balance Return Signal



S2 Open, S1 Closed:
L-T Long. Bal. = 20 log (V_{AB}/E)
L-4 Long. Rej. = 20 log (V_{TX}/E)

S2 Closed, S1 Open:
4-L Long. Sig. Gen. = 20 log (V_L/V_{RX})

C. Longitudinal Balance



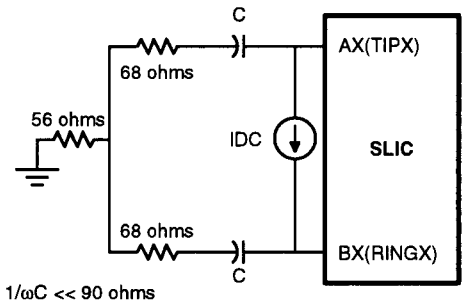
Z_D: The desired impedance (e.g., the characteristic impedance of the line).

Return Loss = $-20 \log (2 V_M / V_S)$

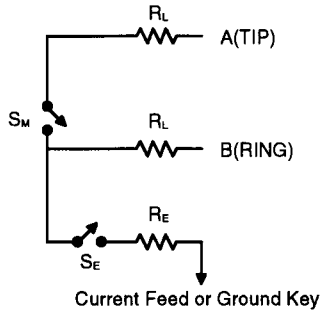
D. Two-Wire Return Loss Test Circuit

15772A–017a

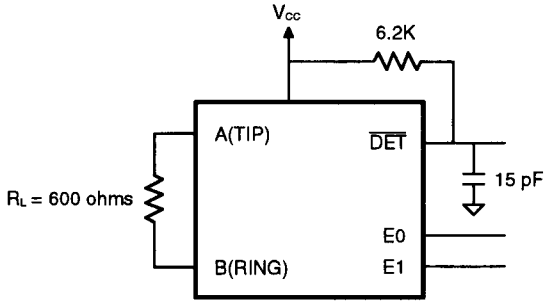
TEST CIRCUITS (continued)



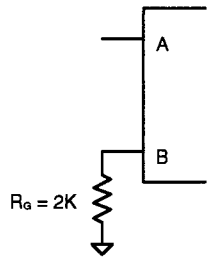
E. Single-Frequency Noise



F. Ground-Key Detection



G. Loop Detector Switching



H. Ground-Key Switching

15772A–017b