Preliminary

T-75-49

Am79865/Am79866

Physical Data Transmitter/Physical Data Receiver

Advanced Micro Devices

DISTINCTIVE CHARACTERISTICS

- Parallel input to the PDT is a 5-bit encoded NRZ symbol clocked by LSCLK
- Parallel output from the PDR is a 5-bit unframed NRZ symbol clocked by RSCLK
- The on-chip Phase-Locked-Loop (PLL) only requires an external frequency reference
- 125 MBaud (100 Mbps) serial link data rate
- PECL serial I/Os connect to most Fiber Optic Transmitters and Receivers directly with proper termination
- Dedicated pins provide electrical loopback data path
- 20-pin Plastic Leaded Chip Carrier (PLCC)
- Single +5 V power supply operation

GENERAL DESCRIPTION

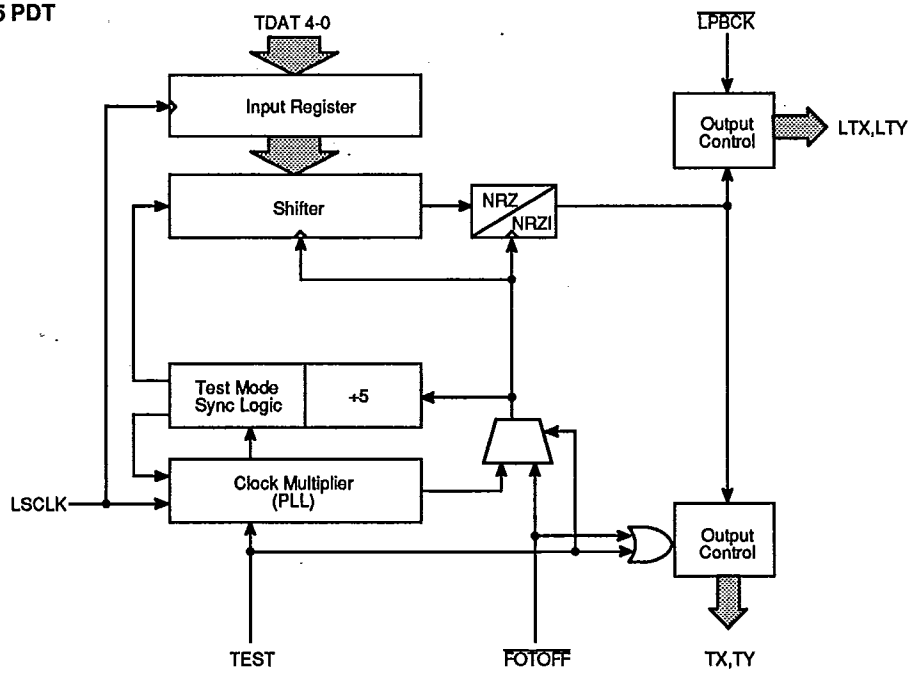
The SUPERNET® 2 FDDI Physical Layer Protocol (PHY) chip set includes the Physical Layer Controller (PLC), the Physical Data Transmitter (PDT) and the Physical Data Receiver (PDR). The PLC, PDT and PDR are collectively known as the AmPHY. The PLC performs FDDI physical layer functions which includes, among others, the 4B5B encoding and decoding.

The PDT converts encoded symbols into a serial NRZI data stream. The on-chip PLL generates a bit rate clock from the LSCLK reference.

The PDR uses a built-in clock recovery PLL to extract clock information from the received data stream. The recovered clock is used for serial-to-parallel data conversion.

BLOCK DIAGRAM

Am79865 PDT



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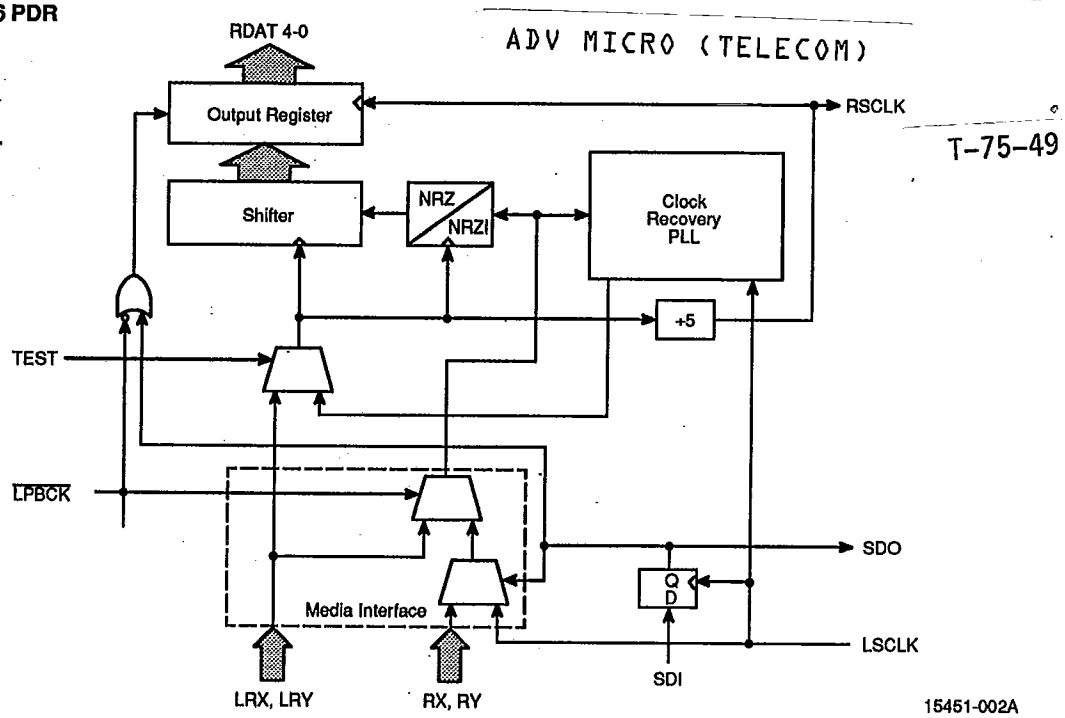
BLOCK DIAGRAM
Am79866 PDR



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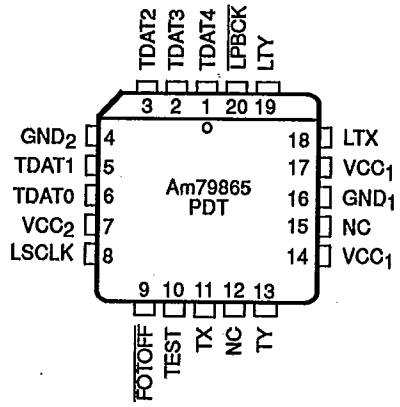
CONNECTION DIAGRAMS
Top View

20-Pin PLCC



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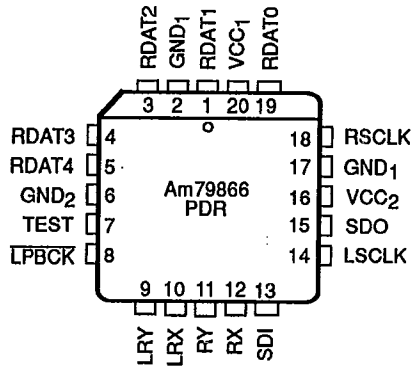
20-Pin PLCC



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LOGIC SYMBOLS

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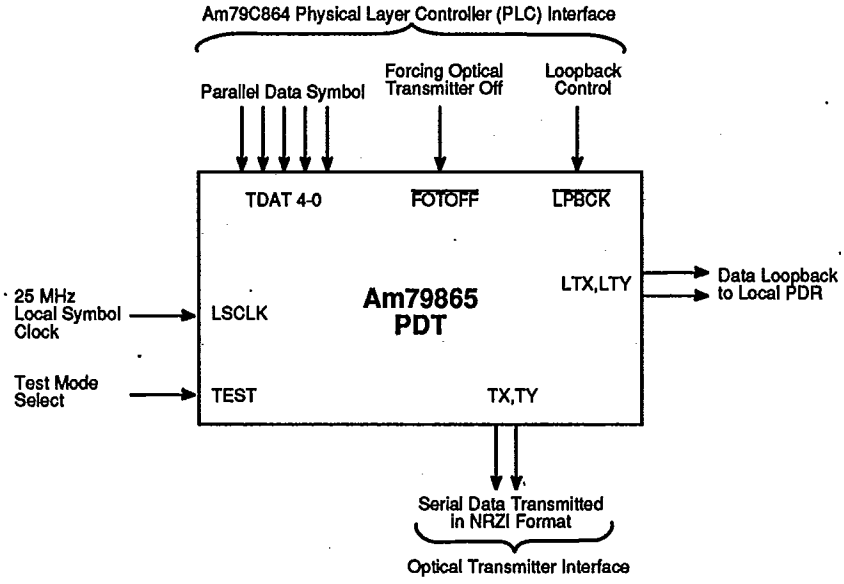

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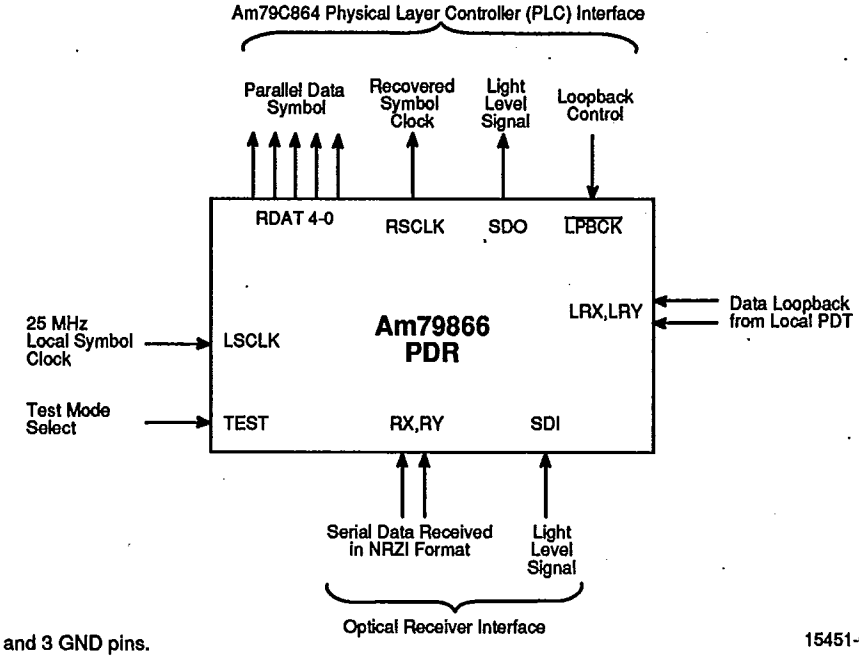
Note:

1. 3 Vcc pins and 2 GND pins.



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Note:

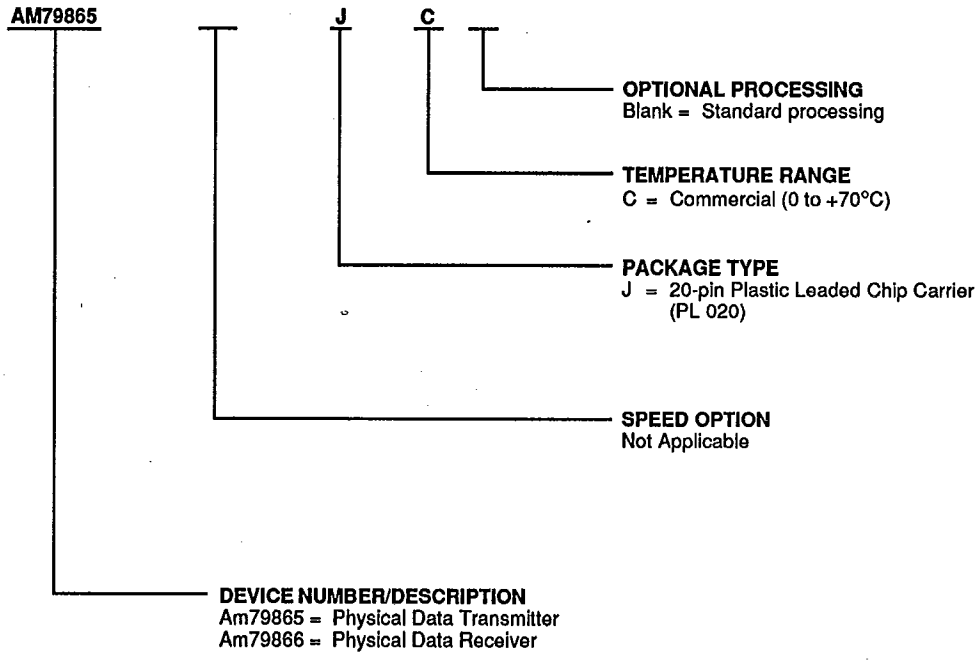
1. 2 Vcc pins and 3 GND pins.

ORDERING INFORMATION

Standard Products

AMD standard products are available in several packages and operating ranges. The order number (Valid Combination) is formed by a combination of:

Device Number
Speed Option (if applicable)
Package Type
Temperature Range
Optional Processing



Valid Combinations	
AM79865	JC
AM79866	JC

Valid Combinations

Valid Combinations list configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations, and to check on newly released valid combinations.

Am79865 PDT PIN DESCRIPTION

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TDAT 4-0
Transmit Data (TTL Inputs)

These five inputs accept data symbols from the Am79C864 PLC, latched by the rising edge of LSCLK.

LSCLK
Local Symbol Clock (TTL Input)

This pin supplies the frequency and phase reference to the internal PLL clock multiplier. It should be driven by an external 25 MHz crystal-controlled clock source.

$\overline{\text{FOTOFF}}$
Fiber Optic Transmitter Off (TTL Input, active LOW)

When held LOW, the TX output is forced LOW and TY output is forced HIGH so that the Fiber Optic Transmitter will output logical 0. In test mode, $\overline{\text{FOTOFF}}$ is used as the test clock input and does not control TX/TY.

$\overline{\text{LPBCK}}$
Loopback Control (TTL Input, active LOW)

When asserted, the LTX/LTY outputs transmit the NRZI serial bit stream to the PDR to establish the loopback data path. When deasserted, the LTX output is forced LOW and LTY output is forced HIGH.

TEST
Test Mode Enable (TTL Input)

When asserted, the PDT is in Test mode. For normal operation, TEST pin must be tied LOW.

TX,TY**
Transmit Data (PECL Differential Outputs)

These transmit outputs carry differential NRZI data. They can be forced to logical 0 (TX LOW, TY HIGH) by asserting the $\overline{\text{FOTOFF}}$ input.

LTX,LTY**
Loopback Transmit Data (PECL Differential Outputs)

These differential outputs carry the same signal as TX/TY when the $\overline{\text{LPBCK}}$ input is asserted (LOW). LTX/LTY should be connected to the LRX/LRY pins of Am79866 PDR to perform loopback function. When $\overline{\text{LPBCK}}$ is deasserted (HIGH), LTX is forced LOW and LTY is forced HIGH.

V_{CC1},V_{CC2}
Power Supply

V_{CC1},V_{CC2} are +5.0V nominal power supply pins. V_{CC1} powers all TTL and ECL I/O circuits. V_{CC2} powers all internal logic gates and analog circuits. They must be connected to a common external supply.

GND_1,GND_2
Ground Pins

GND_1 is TTL and ECL I/O ground. GND_2 is the internal logic and analog ground. They must be connected to a common external ground reference.

**All differential PECL outputs carry data at ECL voltage levels referenced to +5.0 V (PECL levels). The external terminations required are shown in the Interface Connection Diagram in the Appendix.

Am79866 PDR PIN DESCRIPTION

LSCLK
Local Symbol Clock (TTL Input)

LSCLK is driven by an external frequency source at the 25 MHz symbol rate. This signal is used as a frequency reference for the PDR clock-recovery PLL.

$\overline{\text{LPBCK}}$
Loopback (TTL Input, active LOW)

When active, $\overline{\text{LPBCK}}$ selects the serial data stream at LRX/LRY inputs as the received data. When HIGH, RX/RY are selected. This function is used during system loopback test to bypass the transmission medium.

TEST
TEST Mode Enable (TTL Input)

When asserted, the PDR is in Test mode. For normal operation, TEST pin must be tied LOW.

RDAT 4-0
Received Data (TTL Outputs)

These 5-bit parallel outputs are clocked by the falling edge of RSCLK and carry the NRZ data symbols to the PLC.

RSCLK
Recovered Symbol Clock (TTL Output)

RSCLK is derived from the clock synchronization PLL circuit. It is synchronous to the received serial data, and is the recovered bit clock divided-by-five. This is a 25 MHz clock.

SDI
Signal Detect Input (PECL Single-ended Input)

SDI typically comes from the fiber optic receiver to indicate that the received optical signal is above the detection threshold. When asserted (HIGH), the data on RX/RY are used for the input to the PDR. When deasserted (LOW), the RX/RY data stream is gated off and the PLL locks onto the LSCLK.

SDO
Signal Detect Output (TTL Output)

SDO is the SDI input synchronized by LSCLK. It has the same logical sense as SDI, i.e., HIGH indicates the received optical signal is above the detection threshold.

RX,RY*
Received Data (PECL Differential Line Receiver Inputs)

These pins receive NRZI data.

LRX,LRY*
Loopback Received Data (PECL Differential Line Receiver Inputs)

This input pair should be connected to the PDT LTX/LTY outputs through properly terminated lines to establish the loopback data path. When $\overline{\text{LPBCK}}$ is asserted, LRX/LRY carry the data to be used as the input to the PDR. In Test mode, LRX/LRY become the test clock input.

V_{CC1},V_{CC2}
Power Supply

V_{CC1},V_{CC2} are +5.0 V nominal power supply pins. V_{CC1} powers all TTL and ECL I/O circuits. V_{CC2} powers all internal logic gates and analog circuits. They must be connected to a common external supply.

GND_1,GND_2
Ground Pins

GND_1 is TTL and ECL I/O ground. GND_2 is the internal logic and analog ground. They must be connected to a common external ground reference.

*RX/RY and LRX/LRY are differential line receivers which have high input sensitivity and wide common-mode range. They can also accept PECL voltage swings and shall be driven by properly terminated transmission lines.

FUNCTIONAL DESCRIPTION

Normal Operation Mode

The Am79865 PDT accepts encoded data symbols at TDAT 4-0 pins. The 5-bit symbol is latched into the PDT by the rising edge of LSCLK, serialized, converted to NRZI format and shifted to the outputs (TDAT4 bit is transmitted first). There are two pairs of serial data outputs capable of driving either Fiber Optic Interface hardware or wire transmission lines without external buffering. The TX/TY pair is connected to the serial link and the LTX/LTY pair is used in the loopback connection to the Am79866 PDR.

The PDT uses LSCLK as the frequency reference to generate the serial link data rate. The external clock source must be crystal controlled and continuous. All of the internal logic of PDT runs on an internal clock that is PLL-multiplied from the external reference source. The PDT's internal PLL is referenced to the rising edges of LSCLK only.

The input clock frequency required to achieve 125 MBaud on the serial link is 25 MHz at LSCLK. In order to generate the serial output waveforms conforming to the FDDI specification, the external reference clock (LSCLK) must meet FDDI frequency and stability requirements. The PDT serial output typically contains less than 0.4 ns peak-to-peak jitter at 125 MBaud. The latency from the LSCLK to the serial output is typically 4 to 6 bits (8 ns/bit).

The Am79866 PDR accepts encoded NRZI serial data on the RX/RY inputs and converts them to NRZ format. It then latches the unframed symbol (5 bits) to the RDAT 4-0 outputs on the falling edge of RSCLK.

The heart of the Am79866 PDR chip is its clock-recovery PLL which extracts encoded clock information from the serial NRZI data stream and recovers the data. The PLL examines every data transition in the received serial stream and aligns its internal bit clock with these data transitions. In order to guarantee the correct operation of the PLL, the encoding scheme (such as the FDDI 4B5B code) must insure adequate transition density of the encoded data stream.

The PDR has input jitter tolerance characteristics that meet or exceed the recommendations of Physical Layer Medium Dependent (PMD) FDDI document. Typically, at 125 MBaud (8 ns/bit), the peak-to-peak Duty-Cycle Distortion (DCD) tolerance is 1.4 ns, the peak-to-peak Data-Dependent Jitter (DDJ) tolerance is 2.2 ns, and the peak-to-peak Random Jitter (RJ) tolerance is 2.27 ns. The total combined peak-to-peak jitter tolerance is typically 5 ns with bit error rate (BER) less than 2.5×10^{-10}.

The PDR's PLL typically has an acquisition time of 100 µs or less when 'Master' symbols (one data transition within ten bits) are received. The acquisition time reduces with increasing transition density in the data stream.

The SDI input qualifies the data at RX/RY. When SDI is LOW, the PDR uses LSCLK as the PLL input and forces LOW at the Output Register. The $\overline{\text{LPBCK}}$ input selects the data source between RX/RY and LRX/LRY. When $\overline{\text{LPBCK}}$ is LOW, the SDI input is ignored.

When SDI is HIGH and the RX/RY input stream contains no data transition for PLL input, the PLL operating frequency range is limited by the LSCLK reference. The observed RSCLK output frequency is generally within 0.5 % of the LSCLK frequency.

Under normal conditions, the frequency of LSCLK multiplied by five must be within 0.25 % of the expected received data for the PLL to operate correctly. (Note, FDDI specifies the two frequencies to be within 50 ppm or 0.005 % of each other.)

Am79865 PDT Functional Block Description

Clock Multiplier

LSCLK supplies the reference frequency which is multiplied by five using an on-chip PLL. The transmission rate and all serialization logic are controlled by the internally generated bit clock.

Input Register

TDAT 4-0 are clocked into the Input Register by the rising edge of LSCLK.

Shifter

Parallel data are loaded from the Input Register into the Shifter at the internally generated symbol boundary, and serially shifted at the bit clock rate.

NRZ-to-NRZI Converter

The NRZ output of the Shifter is converted into NRZI data patterns for transmission.

Output Control

The differential outputs carry the encoded serial NRZI bit stream. The TX/TY pair can be forced to logical 0 (TX LOW, TY HIGH) by asserting $\overline{\text{FOTOFF}}$ input. The LTX/LTY pair can be forced to logical 0 (LTX LOW, LTY HIGH) by deasserting the $\overline{\text{LPBCK}}$ input.

Am79866 PDR Functional Block Description

Clock-Recovery PLL

The clock-recovery PLL separates the input data stream into clock and data patterns. The PLL operating frequency is established by the reference at LSCLK. The PLL is capable of tracking data correctly within ± 0.25 %

of LSCLK (exceeds the frequency range defined by the FDDI specification).

Media Interface

The RX/RY inputs are typically driven by differential PECL voltages, referenced to +5 V. These inputs accept the encoded NRZI serial data. LRX/LRY are also differential line receiver inputs which accept the loopback data stream from the local PDT LTX/LTY outputs.

NRZI-TO-NRZ Converter

Serial data are retimed and associated jitter is removed. Retimed data are converted into NRZ format prior to the Shifter input.

Shifter

The Shifter is serially loaded from the NRZI_TO_NRZ converter, using the recovered bit clock.

Output Register

The Output Register is clocked by RSCLK falling edges. RSCLK is the recovered bit clock divided-by-five and is synchronous to the received serial data.

Test Mode

Asserting PDT TEST input pin forces PDT into its test mode. This allows testing of the internal logic without the PLL clock multiplier. The internal clock source is replaced by the test clock provided at the $\overline{\text{FOTOFF}}$ input. An automatic test system can clock the PDT through functional test patterns at any rate, typically less than 25 MHz, or any sequence to facilitate logic verification.

In PDT test mode, LSCLK strobes data into the Input Register and provides initialization to the internal counter.

The PDR test mode allows testing of the internal logic without the PLL. When TEST is HIGH, the internal clock source is replaced by the test clock provided at the LRX/LRY inputs. (Note: The loopback data path in the Am79866 PDR cannot be tested in test mode.)

An automatic test system can clock the PDR through functional test patterns at any rate, typically less than 25 MHz, or any sequence to facilitate logic verification.

ABSOLUTE MAXIMUM RATINGS

Storage Temperature	−65°C to +150°C
Ambient Temperature under bias	−55°C to +125°C
Supply Voltage (V_{CC}) to Ground Potential Continuous	−0.5 V to +7.0 V
DC Voltage Applied to Outputs	−0.5 to V_{CC} Max.
DC Input Voltage	−0.5 V to +5.5 V
DC Output Current	±100 mA
DC Input Current	−30 to +5.0 mA

Stresses above those listed under Absolute Maximum Ratings may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to absolute maximum ratings for extended periods may affect device reliability.

OPERATING RANGES

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Commercial (C) Devices

Ambient Temperature (T_A)	0°C to 70°C
Supply Voltage (V_{CC})	+4.75 V to +5.25 V

Operating ranges define those limits between which the functionality of the device is guaranteed.

DC CHARACTERISTICS over operating range unless otherwise specified

Am79865 PDT

Parameter Symbol	Parameter Description	Test Conditions	Min.	Typ. (Note 2)	Max.
TTL Inputs: TDAT 4-0, LSCLK, $\overline{\text{FOTOFF}}$, $\overline{\text{LPBCK}}$, TEST					
V_{IH}	Input HIGH Voltage	V_{CC} = Max. (Note 3)	2.0 V		
V_{IL}	Input LOW Voltage	V_{CC} = Max. (Note 3)			0.8 V
V_I	Input Clamp Voltage	V_{CC} = Min., I_{IN} = −18 mA			−1.5 V
I_{IH}	Input HIGH Current	V_{CC} = Max., V_{IN} = 2.7 V			50 µA
I_{IL}	Input LOW Current	V_{CC} = Max., V_{IN} = 0.4 V			−400 µA
I_I	Input Leakage Current	V_{CC} = Max., V_{IN} = 5.5 V			50 µA
PECL Outputs: TX,$\overline{\text{TX}}$; LTX,$\overline{\text{LTY}}$					
V_{OH}	Output HIGH Voltage	PECL load (Note 4)	V_{CC}−1.025 V		V_{CC}−0.88 V
V_{OL}	Output LOW Voltage	PECL load (Note 4)	V_{CC}−1.81 V		V_{CC}−1.62 V
Power Supplies					
I_{CC1}	V_{CC1} Supply Current	V_{CC1} = V_{CC2} = Max. (Note 5)		15 mA	
I_{CC2}	V_{CC2} Supply Current	V_{CC1} = V_{CC2} = Max.		65 mA	

DC CHARACTERISTICS over operating range unless otherwise specified

Am79866 PDR

Parameter Symbol	Parameter Description	Test Conditions	Min.	Typ. (Note 2)	Max.
TTL Inputs: LSCLK, $\overline{\text{LPBCK}}$, TEST					
V_{IH}	Input HIGH Voltage	V_{CC} = Max. (Note 3)	2.0 V		
V_{IL}	Input LOW Voltage	V_{CC} = Max. (Note 3)			0.8 V
V_I	Input Clamp Voltage	V_{CC} = Min., I_{IN} = –18 mA			–1.5 V
I_{IH}	Input HIGH Current	V_{CC} = Max., V_{IN} = 2.7 V			50 µA
I_{IL}	Input LOW Current	V_{CC} = Max., V_{IN} = 0.4 V			–400 µA
I_I	Input Leakage Current	V_{CC} = Max., V_{IN} = 5.5 V			50 µA
TTL Outputs: RDAT 4-0, SDO, RSCLK					
V_{OH}	Output HIGH Voltage	V_{CC} = Min., I_{OH} = –1 mA	2.4 V		
V_{OL}	Output LOW Voltage	V_{CC} = Min., I_{OL} = 4 mA			0.45 V
I_{SC}	Output Short Circuit Current	V_{CC} = Max., (Note 6)	–15 mA		–85 mA
Differential PECL Inputs: RX,RY; LRX,LRY					
V_{IN}	Input Voltage (Absolute High or Low)	V_{CC} = Max., (Note 3)	2.5 V		V_{CC}
V_{dif}	Input Differential Voltage	V_{CC} = Max., (Note 3,7)	50 mV		1.1 V
I_{IH}	Input HIGH Current	V_{CC} = Max., V_{IN} = V_{CC} – 0.88 V			220 µA
I_{IL}	Input LOW Current	V_{CC} = Max., V_{IN} = V_{CC} –1.81 V	0.5 µA		
Single-ended PECL Input: SDI					
V_{IHS}	Input Single-ended HIGH Voltage	V_{CC} = Max., (Note 3,8)	V_{CC} –1.165 V		V_{CC} –0.88 V
V_{ILS}	Input Single-ended LOW Voltage	V_{CC} = Max., (Note 3,8)	V_{CC} –1.81 V		V_{CC} –1.475 V
I_{IH}	Input HIGH Current	V_{CC} = Max., V_{IN} = V_{CC} – 0.88 V			220 µA
I_{IL}	Input LOW Current	V_{CC} = Max., V_{IN} = V_{CC} –1.81 V	0.5 µA		
Power Supplies					
I_{CC1}	V_{CC1} Supply Current	V_{CC1}= V_{CC2} = Max.		15 mA	
I_{CC2}	V_{CC2} Supply Current	V_{CC1}= V_{CC2} = Max.		120 mA	

SWITCHING CHARACTERISTICS over operating range unless otherwise specified

Am79865 PDT

No.	Parameter Symbol	Parameter Description	Test Condition (Note 9)	Min.	Max.	Units
1	t_P	LSCLK Period		40	40	ns
2	t_{PW}	LSCLK Pulse Width HIGH		15		ns
3	t_{PW}	LSCLK Pulse Width LOW		15		ns
4	t_S	TDAT 4-0 to LSCLK Rise Setup Time		12		ns
5	t_H	TDAT 4-0 to LSCLK Rise Hold Time		3		ns
6	t_R†	TX,TY,LTX,LTY Rise Time	PECL load	0.3	3	ns
7	t_F†	TX,TY,LTX,LTY Fall Time	PECL load	0.3	3	ns
8	t_{SK}†	TX/TY, LTX/LTY Skew	PECL load		±200	ps

Am79866 PDR

21	f_{OS}	LSCLK to received data frequency offset	(Note 10)		±0.25	%
22	t_{PW}	LSCLK Pulse Width HIGH		15		ns
23	t_{PW}	LSCLK Pulse Width LOW		16		ns
24	t_{PW}	RSCLK Pulse Width HIGH	TTL load (Note 11)	10		ns
25	t_{PW}	RSCLK Pulse Width LOW	TTL load (Note 11)	20		ns
26	t_{PD}	RDAT 4-0Valid to RSCLK Rise	TTL load (Note 12)	13		ns
27	t_{PD}	RSCLK Rise to $RDAT_{4-0}$ Invalid	TTL load (Note 12)	10		ns
28	t_S	SDI to LSCLK Rise Setup Time		5		ns
29	t_H	SDI to LSCLK Rise Hold Time		7		ns
30	t_{PD}	LSCLK Rise to SDO Delay	TTL load		30	ns

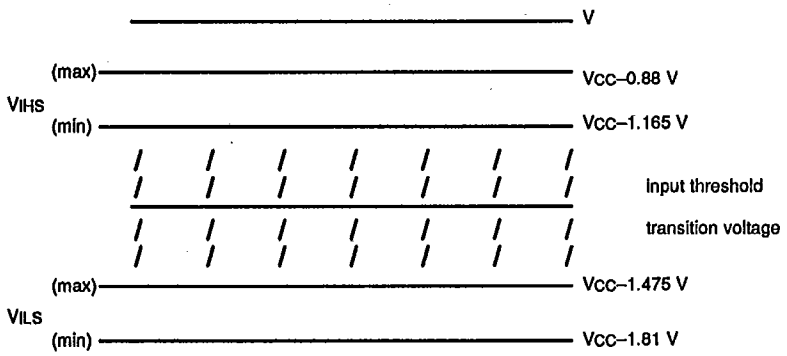
Notes:

†: not included in the production test.

1. For conditions shown as Min. or Max, use the appropriate values specified under operating range.
2. Typical limits are at V_{CC}=5.0 V, 25°C ambient and maximum loading.
3. Typically measured with device in Test mode while monitoring output logic states.
4. Tested for V_{CC}=Min, shown limits are specified over entire V_{CC} operating range.
5. PDT I_{CC1} is tested with all PECL outputs terminated to V_{CC} (unloaded). The PECL outputs contribute 25 mA/pair nominally to I_{CC1} when they are loaded with PECL loads, 50 ohms to (V_{CC}–2). In calculating the chip power dissipation, the contribution by the output loads shall be multiplied by 1 V instead of by V_{CC}.
6. Not more than one output should be shorted at a time. Duration of the short circuit test should not exceed one second.

Notes (Continued):

7. V_{dif} is tested with each input voltage within the V_{IN} range.
8. Device thresholds on the SDI pin are verified during production test by ensuring that the input threshold is less than V_{IHS} (min) and greater than V_{ILS} (max). The figure below shows the acceptable range (shaded area) for the transition voltage.



9. All timing references are made with respect to + 1.5 V for TTL-level signals or to the 50% point between V_{OH} and V_{OL} for PECL signals. PECL input rise and fall times must be 2ns±0.2 ns between 20 % and 80 % points. TTL input rise and fall times must be 2 ns between 1 V and 2 V.
10. Received data frequency is determined by serial data inputs. Multiply LSCLK frequency by 5 to convert the receive data bit rate.
11. Tested for 125 MBaud received data rate (1 bit-time is 8 ns). t_{PW}(HIGH) is functionally 2 bit-time wide. t_{PW}(LOW) is functionally 3 bit-time wide.
12. Tested for 125 MBaud received data rate (1 bit-time is 8 ns).

SWITCHING WAVEFORMS
Am79865 PDT

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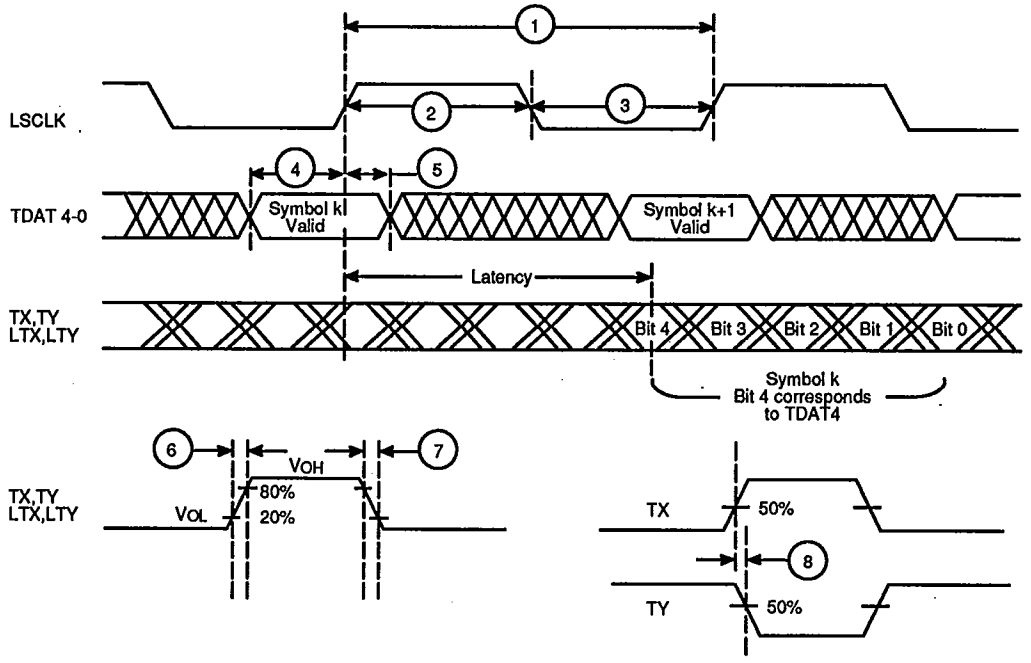

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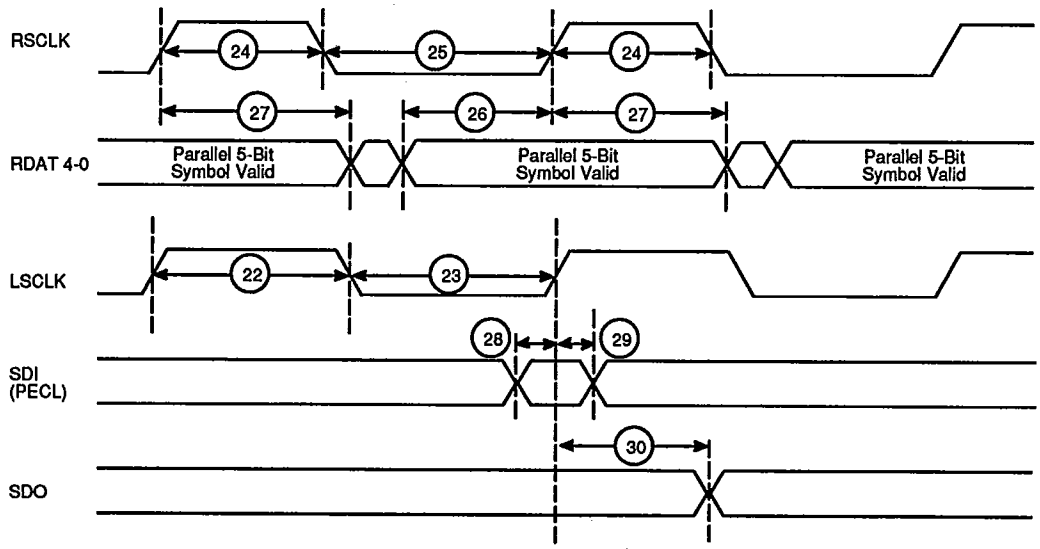
Am79866 PDR



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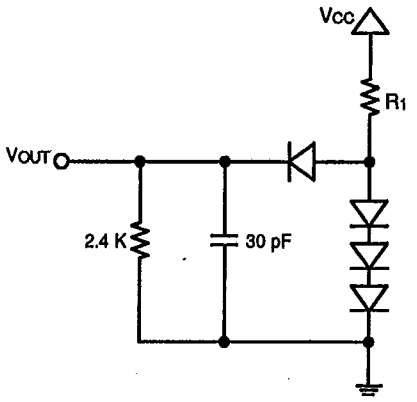
KEY TO SWITCHING WAVEFORMS

WAVEFORM	INPUTS	OUTPUTS
	Must Be Steady	Will Be Steady
	May Change from H to L	Will Be Changing from H to L
	May Change from L to H	Will Be Changing from L to H
	Don't Care, Any Change Permitted	Changing, State Unknown
	Does Not Apply	Center Line is High Impedance "Off" State

KS000010

SWITCHING TEST CIRCUITS

TTL Output Load



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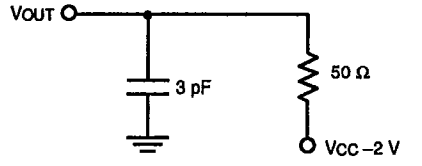
Notes:

1. R_1 = 1 KΩ for the I_{OL} = 4 mA
2. All diodes IN916 or IN3064, or equivalent.
3. C_L = 30 pF includes scope probe, wiring and stray capacitances without device in text fixture.
4. AMD uses constant current (A.T.E.) load configurations and forcing functions. This figure is for reference only.

PECL Output Load



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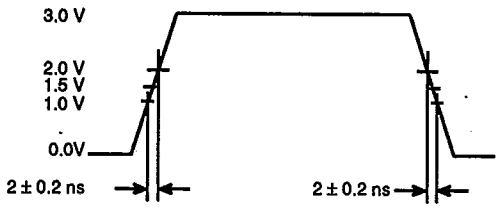
Notes:

1. C_L = 3 pF includes scope probe, wiring and stray capacitances without device in text fixture.
2. AMD uses Automatic test equipment (A.T.E.) load configurations and forcing functions. This figure is for reference only.

SWITCHING TEST WAVEFORMS

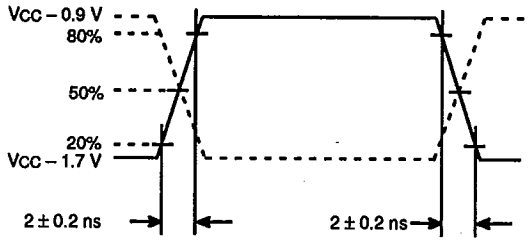
T-75-49

TTL Input Waveform



15451-012A

ECL Input Waveform



15451-013A