IEEE 802.3/Ethernet/Cheapernet Transceiver ADVANCED INFORMATION

DISTINCTIVE CHARACTERISTICS

- Compatible with Ethernet version 2 and IEEE 802.3 Rev D (10 Base 5 Type A and 10 Base 2 Type B)
- Signal Quality Error (SQE) test generated after each transmission
- Internal Jabber Controller prevents excessive transmission time
- · Noise rejection filter ensures only valid data is transmitted onto network
- Collision detection on both transmit and receive data

GENERAL DESCRIPTION

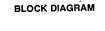
The Am7995 IEEE 802.3/Ethernet/Cheapernet Transceiver supports Ethernet Version 2, IEEE 802.3 (Type A), and IEEE 802.3 (Type B — "Cheapernet") transceiver applications. Transmit, receive, and collision detect functions at the coaxial media interface to the Data Terminal Equipment (DTE) are all performed by this single device.

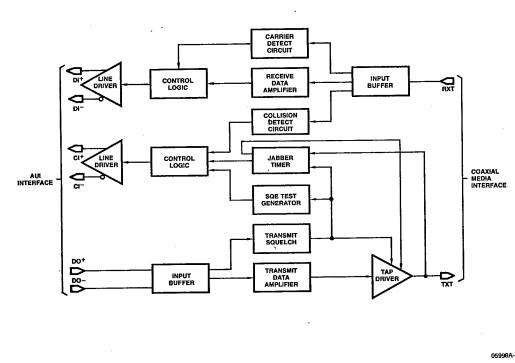
In an IEEE 802.3 (Type A)/Ethernet application, the Am7995 interfaces the coaxial (0.4" diameter) media to the DTE through an isolating pulse transformer and the 78 ohm Attachment Unit Interface (AUI) cable. In IEEE 802.3 (Type B "Cheapernet") applications, the Am7995 typically resides inside the DTE with its signals to the DTE isolated and the coaxial (0.2" diameter) media directly connected to the DTE. Transceiver power and ground in both applications are isolated from that of the DTE.

The Am7995's tap driver provides controlled skew and current drive for data signaling onto the media. The Jabber Controller prevents the node from transmitting excessively. While transmitting, collisions on the media are detected if one or more additional stations are transmitting. The Am7995 indicates operational status of its CI pair to the DTE by sending a signal on the CI pair at the end of every transmission at the node (SQE test).

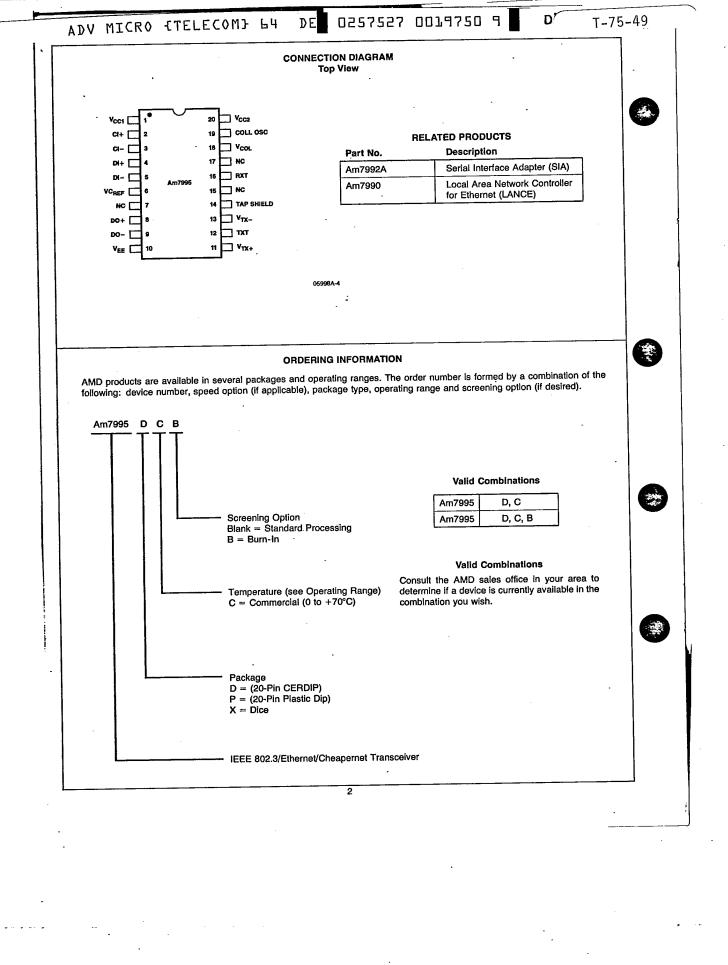
Advanced Micro Devices

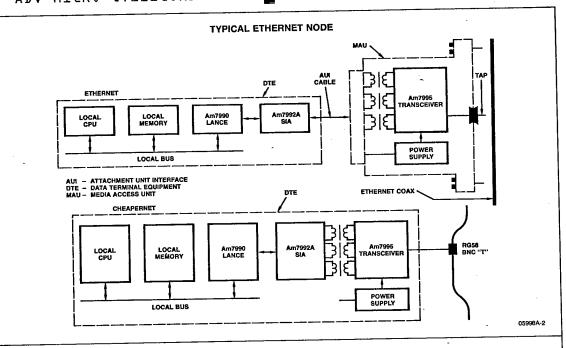
February





This document contains information on a product under development at Advanced Micro Devices, Inc. The information is intended to help you to evaluate this product. AMD reserves the right to change or discontinue work on this proposed product without notice. Order # 05998A





PIN DE Pin No. 1 2 3	ESCRIPT Name Vcc1 CI+, CIT		Description Positive Logic Supply Collision (Output). A Differential Line Output. This pair is intended to operate into terminated 78 ohm trans- mission lines. Signal Quality Error (SQE), detected at DO± inputs (exces- sive transmissions) or RXT input (during a collision), outputs the 10MHz internal oscillator signal to the AUI interface. For proper component values at COLL OSC, signaling at CI± meets require- ments of IEEE 802.3 Rev. D.	10 11 13	V _{EE} V _{TX+} ,	1	Transmit (Input). A Differential Input. A pair of internally biased line receivers consisting of a squelch detect receiver with offset and noise filtering, and a data receiver with zero offset for data signal processing. Signals meeting squelch requirements are waveshaped and output at TXT. Negative Logic Supply and IC Substrate Tap Node Driver Current Set (Inputs). A reference input for transmission level and external redundant jabber. Transmit level is set by an external resistor between V _{TX+} and V _{TX-} . For an 80mA peak level, R is 9.1 ohm. V _{TX-} may be
4 5	DI+, DI-	0	Receive (Output). A Differential Line Output. This pair is intended to operate into terminated 78 ohm transmission lines. Signals at RXT meeting bandwidth requirements and carrier sense levels are outputted at DI±. Signals	12	тхт	0	operated between VEE and VEE + 1 volts. When the voltage at V _{TX} goes more positive than V _{EE} + 2 volts, TXT is disabled and SQE message is output at the CI pair. Tap Node Driver (Input/Output). A
			naling at DI = meet requirements of IEEE 802.3 Rev. D.				controlled bandwidth current source and sense amplifier. This I/O port is to be connected to the media through an iso-
6	VC _{REF}	1	Timing Reference Set (Input). VC _{REF} is a compensated voltage reference input with respect to V _{EE} . When a resistor is connected between VC _{REF} and V _{EE} , then internal transmit and receive squelch timing, SQE oscillator frequency, and receive and SQE output drive levels are set. SQE frequency set is also determined by components connected between V _{CC1} and COLL OSC.				lation network and a low pass filter. Signals meeting DO± squelch and jabber timing requirements are output at TXT as a controlled rise and fall time current pulse. When operated into a double terminated 50 ohms transmission line, signaling meets IEEE 802.3 Rev. D. recommendations for amplitude, pulse width distortion, rise and fall times, and harmonic content. The sense amplifier
7	N.C.		No Connection				monitors TXT faults and inhibits trans-

TAP

N.C.

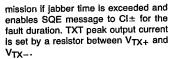
RXT

SHIELD

14

15

16



 V_{TX-}

Low Noise Media Cable Return

(Input). This input is the return for V_{COL} reference and the receive signal from the Media. External connection is to positive power supply.

No Connection

Media Receive (input). Media Signal Receiver Input. RXT connects to the Media through a 4: 1 attenuator of 100K ohms total resistance (25K ohms and 75K ohms in series). Return for the attenuator is V_{COL} . RXT is an analog input with internal AC coupling for Manchester data signals and direct coupling for carrier detect and SQE average level detection. Signals at RXT meeting carrier squelch, enable data to the Di ± outputs. Data signals are AC coupled to DI ± with an 150ns time constant high pass filter. Signals meeting SQE levels enable COLL OSC frequency to CI± outputs.

RXT and N.C. (pins 15 and 17) provide a low capacitance input for media attachment. Input capacitance at RXT is approximately 1.3pF. Receive path node capacitance is compensated by placing one third 'C' in total across the 75K ohms portion of the input attenuator.

No Connection N.C. ì

17

18

19

VCOL

COLL

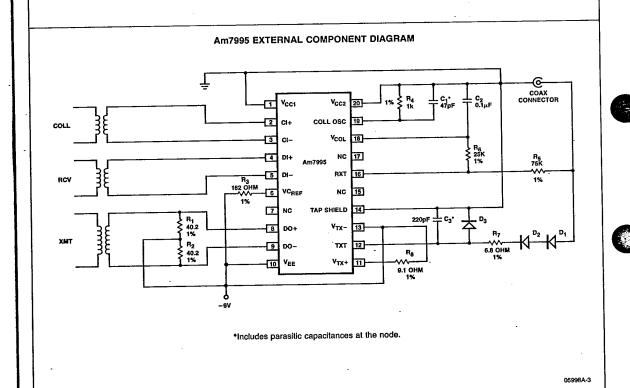
osc

V_{CC2}

SQE Reference Voltage (Bias Supply). SQE sense voltage and RXT input amplifier reference. An internally set analog reference for SQE level and data signal set at -1.600V nominal with a source resistance of 150 ohms nominal. This reference should be filtered with respect to tap shield.

SQE Timing Set (Input). Timing input for SQE oscillator. For a properly set input at VCREF, SQE oscillator period is set at 2.1RC. For a 10MHz SQE oscillator frequency, R should be 1K ohms and C, 47pF including interconnect and device capacitance.

SQE Timing Reference (Positive Supply Voltage). Timing reference return for SQE oscillator and analog signal ground.



FUNCTIONAL DESCRIPTION

The Am7995 IEEE 802.3/Ethernet/Cheapernet Transceiver consists of four sections: a) Transmit — receives signals from DTE and sends it to the coaxial medium, b) Receive — obtains data from media and sends it to DTE, c) Jabber — guards medium from node transmissions that are excessive in length, d) Collision detect — indicates to DTE any collision on the media.

TRANSMIT

The Am7995 receives differential signals from the DTE (in the case of Am7990 Family applications from the Am7992A — Serial Interface Adapter — SIA). For IEEE 802.3 (Type A)/Ethernet applications, this signal is received through the AUI cable and isolation transformer. In IEEE 802.3 Type B "Cheapernet" applications, the AUI cable is optional.

Data is received through a noise rejection filter that rejects signals with pulse widths less than 7ns (negative going), or greater than 160ns (positive going), or with levels less than -175mV peak. Only signals greater than -275mV peak from the DTE are enabled. This minimizes false starts due to noise and ensures no valid packets are missed.

The Am7995's Tap Driver provides the driving capability to ensure adequate signal level at the end of the maximum length network segment (500m) under the worst case number of connections (100). Required rise and fall times of data transmitted on the network is maintained by the Am7995 driver. The tap driver's output is connected to the media through external isolating diodes. To safeguard network integrity, the driver is disabled whenever power falls below the minimum operation voltage.

During transmission, the Am7995's Jabber Controller counts the duration that the transmit tap driver is active and disables the driver if the jabber time is exceeded. This prevents network tie-up due to a "babbling" transceiver. Once disabled, the driver is reset 400ms after the DO pair Is idle and there is no fault on TXT. During the disable time, an SQE signal is sent on the CI pair to the DTE.

At the end of every transmission on the network the Am7995 generates an SQE test. This signal is a self test indication to the DTE that the MAU collision pair is operational.

RECEIVE AND CARRIER DETECT

Signal is acquired from the tap through a high impedance (100K ohms) resistive divider. A high input impedance (low capacitance, high bandwidth, low noise) DC coupled input amplifier in the Am7995 receives the signal. The received signal passes through a high pass filter to minimize inter-symbol distortion, and then through a data slicer.

The Am7995's carrier detect compares received signals to a reference. Signals meeting carrier squelch enable data to the differential line driver within 5 bit times from the start of packet.

Received data is transmitted from the DI pair through an isolation transformer to the AUI cable (Ethernet/IEEE Type A — in IEEE 802.3 Type B "Cheapernet" the AUI cable is optional). Following the last transition of the packet, the DI pair is held high for 2 bit times and then decreases to idle level within 20 bit times.

COLLISION DETECT

The Am7995 detects collisions on transmit if one or more additional stations are transmitting on the network.

Received signals are compared against the collision threshold reference. If the level is more negative than the reference, an enable signal is generated to the collision pair. The collision threshold can be modified by external components to suit other applications.

The Collision Oscillator is a 10MHz oscillator which drives the differential CI pair to the DTE through an isolation transformer. This signal is gated to the CI pair whenever there is a collision, the SQE test is in progress, or the Jabber Controller is activated. The oscillator is also utilized in counting time for the Jabber timer and SQE test.

The CI \pm output meets the drive requirements for the AUI interface. The output stays high for 2 bit times at end of packet decreasing to the idle level within 20 bit times.

JABBER FUNCTION

The Am7995's Jabber timer monitors the activity on the DO pair and senses TXT faults. It inhibits transmission if the tap driver is active for longer than the jabber time (26ms). An SQE message is enabled on the CI pair for the fault duration.

After the fault is removed, the Jabber timer counts the unjab time of 400ms before it enables the driver.

If desired, a redundant Jabber function can be implemented externally, and the output driver disabled by removing the driver supply at V_{TX} ... The Am7995 senses this condition and forces an SQE message on the CI pair, during the disable time.

SOF TEST

At the end of every transmission, the Am7995 generates an SQE test which gates a 10MHz signal to the Cl pair. The SQE test ensures that the twisted pair assigned for collision notification to the DTE is intact and operational. The SQE test starts 8 bit times after the last transition of the transmitted signal and lasts for a duration of 8 bit times.

ABSOLUTE MAXIMUM RATINGS

 Supply Voltages V_{EE}, V_{TX} -12 to +0.5V

 Input Voltage DO+, DO-, TXT, RXT
 -12 to 0.5V

 Storage Temperature Range
 -65 to 150°C

DC CHARACTERISTICS

DC CHARACTERISTICSThe following conditions apply unless otherwise specified: Commercial $T_A = 0$ to $\pm 70^{\circ}$ C $V_{EE} = -9V \pm 5\%$

Parameter	Description	Test Condition	Min	Тур	Max	Units
	Input Current (DO+, DO-)	V _{IN} = 0 to V _{EE}			TBA	mA
l _{IT}	Carrier Sense Threshold (Note 1)		TBA	-500	TBA	mV
V _{CAT}	Collision-Sense Threshold (Note 1)		TBA	-1600	TBA	mV
V _{COT}		R _I = 25 ohms	À	-2.05		V
V _{TXTL}	Transmit Output LOW Voltage (Note 1)	R _i = 25 ohms	N. A.	-0.05		V
V _{TXTH}	Transmit Output HIGH Voltage (Note 1)	1000 1000				
V _{TXT}	Transmit Average DC Voltage with 50% Duty-Cycle into DO+, DO- (Note 1)	Ri = 25 phms	<i>3</i>	-1.025	1	V
		*BL = 78 ohms Voo+	JBA	+670	тва	m∨
V _{OD}	Differential Output Voltage (DI+, DI-, CI+ CI-)	YOP E	TBA	670.	TBA	
V _{CMT}	Common Mode Output (D[±_DI-, DI+, DI+, DI+, DI+, DI+, DI+, DI+, DI+	RL 78 ohms	тва 🖁	2.5	*TBA	
	Differential Input Resistance (DO+,DO-	V _{IN} = 0 to V _{EE}	`TBA∙	₹ 8		K ohms
RIDF	Compon Mode Input Resistance (DOT, 30-)	VINCO to VEE	TBA	2		K ohms
RICM	Common stode input resistance (2011)	A PACE AND A SECOND		1.7		
C _{RXT}	RXT Input Capacillance	VEE 0 to Max Plastic		1.1		pF
I _{BXT} .	RXT lippit Current	(V _{IN} = 1 to −2.5V	_	±0.01	TBA	μA
VICM	DO+, DO- Common Mode Blas Voltage	N = 0	TBA	V _{EE} +1.5	TBA	V
V _{ODI}	Differential Output Voltage Imbalance	R _L = 78 ohms	· ·	±5	ТВА	m∨
V _{OD} OFF	Differential Output (die Voltage (DI+, DI-, CI+, CI-)		ļ.,	±0.5	TBA	mV
I _{OD} OFF	Differential Output Idle Current (DI+, DI-, CI+, CI-)	R _L = 0	<u> </u>	±0.01	TBA	mA
VIDC	Differential input Squelch Threshold (DO+, DO-)		TBA	-225	TBA	mV_
	Supply Current - Non-Transmitting	R _L = 25 ohms	TBA	88.0	TBA	mA mA
lcc	Supply Current - Transmitting	R _L = 25 ohms	TBA	128,0	TBA	

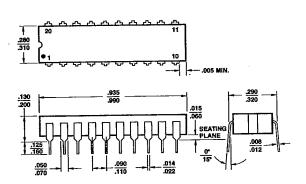
AC CHARACTERISTICS Over Operating Range TRANSMIT SPECIFICATIONS

Number	Parameter	Description	Test Conditions	Min	Тур	Max	Units
- 1	tewney	DO± Input Pulse Width to Reject (DO± > V _{IDC} , Min)			15	TBA	ns
2	tewton	DO± Input Pulse Width to Turn On (DO± > VIDC, Mex)		TBA	15		ns
3	tpwson	DO± Input Pulse Width to Stay On (DO± < V _{IDC} , Max)				105	ns
4	tpwoff	DO± Input Pulse Width to Turn Off (DO± < VIDC, Min)		ТВА	180		ns
5	t _{TON}	Transmit Driver Turn-On Delay				TBA	ns
6	tTOFF	Transmit Driver Tum-Off Delay				ТВА	ns
7	t _{TSD}	Transmit Static Delay (Zero Crossing to 50% Point to Coax)			30	TBA	ns
8	t _{TXTR}	Transmit Driver Rise Time		73×	25		ns
9	tTXTF	Transmit Driver Fall Time		164	25		ns
10	t _{DBF}	Difference in Driver Rise and Fall Times tTXTR-TXTF			±0.5		ns
11	tskew	Output Driver Skew - Transmit Data Symmetry			±1.0	-	ns
12	tict	Jabber Control Time		20	26	35	ms
13	URT	Jabber Reset Time	The second	840	¥19 (600	ms
14	UREC	Jabber Recovery Time				TBA	пѕ

	8 5-€ 1	SPECIFICATIONS Description	Test Conditions (Note 2)	Min	Тур	Max	Units
Number 15	Parameter	Receiver Turn-On Delay (Note 3)	VCAT > +600mV	T 1	250	TBA	ns
16	tron troff	Receiver Turn-Off Delay (Note 3)	VgAT <-400mV	ТВА		TBA	ns
17	t _{RSD}	Receiver Static Delay	50% Point at RXT to Zero Crossing at DI± Outputs		30	ТВА	ns
18	¥68. ₹	Receive Data Symmetry (Note 3)		48		52	%
19	IRRA TA	QI± and C)± Rise Time	.20-80%, R _L = 78 ohms	TBA		TBA	ns
20	t _{RF}	DI± and CI± Fall Time	80-20%, R _L = 78 ohms	TBA		TBA	ns
21	tcon	Cl± Turn-On Delay (Note 4)				TBA	ns
22	tCOFF	Ci± Turn-Off Delay (Note 4)				TBA	ns
23	toL	CI± LOW Time				70.5	ns
24	t _{CH}	CI± HIGH Time		35			ns
25	fcı	Collision Frequency		8.5	10.0	11.5	MHz
26	t _{STD}	SQE Test Delay Time (Note 4)	F _{Cl} = 10.0MHz	600		1000	ns
27	tstr.	SQE Test Length (Note 4)	F _{Cl} = 10.0MHz	600		1000	ns

Notes: 1. Parameters are measured at coax tap.
2. Inputs are applied at the coax tap for all receive/collision specifications.
3. Inputs are applied at the coax tap, outputs are measured at the DI ± pins.
4. Inputs are applied at the coax tap, outputs are measured at the CI ± pins.

PHYSICAL DIMENSIONS CD 020



The International Standard of Quality guarantees a 0.05% AQL on all electrical parameters, AC and DC, over the entire operating range.

INTSID'500

ADVANCED MICRO DEVICES 901 Thompson Pl., P.O. Box 3453, Sunnyvale, CA 94088, USA TEL: (408) 732-2400 • TWX: 910-339-9280 • TELEX: 34-6306 • TOLL FREE: (800) 538-8450

© 1985 Advanced Micro Devices, Inc. Printed in U.S.A. CD-B-15M-2/85-0

INTERNATIONAL SALES OFFICES

BELGIUM Advanced Micro Devices Belgium S.A.—N.V. Avenue de Tervueren, 412, ble 9 B-1150 Bruxelles Tel: (02) 771 99 93 TELEX: 61028 FAX: 7623712

FRANCE Advanced Micro Devices, S.A. Silic 314, Immeuble Helsinki 74, rue d'Arcueil F-94588 Rungis Cedex Tei: (01) 687.36.66 TELEX: 202053 FAX: 686.21.85

GERMANY Advanced Micro Devices GmbH Rosenheimer Strasse 143B D-8000 München 80, West Germany Tel: (089) 4114-0 TELEX: 05-23883 FAX: 406 490 GERMANY Advanced Micro Devices GmbH Feuerseeplatz 4/5 D-7000 Stuttgart 1 Tel: (0711) 62 33 77 TELEX: 07-21882 FAX: 625 187

Advanced Micro Devices GmbH Wünning Weg 4 D-3108 Winsen/Aller Tel: (05143) 5055 TELEX: 925287 FAX: (05143) 5553

HONG KONG Advanced Micro Devices Room 1602 World Finance Centre South Tower Harbour City 17 Canton Road Tsimshatsui, Kowloon Tel: (852) 3 695377 TELEX: 50426 FAX: (852) 123 4276 ITALY Advanced Micro Devices S.R.L. Centro Direzionale Via Novara, 570 I-20153 Milano Tel: (02) 3533241 TELEX: 315286 FAX: (39) 349 8000

JAPAN
Advanced Micro Devices, K.K.
Shinjuku Kokusai Building
6-6-2 Nishi-Shinjuku
Shinju-ku, Tokyo 160
Tel: (03) 345-8241
TELEX: 24064
FAX: 03 (342) 5196

SWEDEN Advanced Micro Devices AB Box 2028 Rissneleden 144, 5tr S-172 02 Sundbyberg Tel: (08) 733 03 50 TELEX: 1502 FAX: 7332285 UNITED KINGDOM Advanced Micro Devices (U.K.) Ltd. A.M.D. House, Goldsworth Road, Woking, Surrey GU21 1JT Tel: Woking (04862) 22121 TELEX: 859103 FAX: 22179

Advanced Micro Devices (U.K.) Ltd.
The Genesis Centre
Garrett Field
Science Park South
Birchwood
Warrington WA3 7BH
Tel: Warrington (0925) 828008
TELEX: 828824
FAX: 827693

Advanced Micro Devices cannot assume responsibility for use of any circuitry described other than circuitry embodied in an Advanced Micro Devices' product.