PRELIMINARY

Am79C02/3(A)

Dual Subscriber Line Audio-Processing Circuit (DSLAC™ Device)

Advanced Micro Devices

DISTINCTIVE CHARACTERISTICS

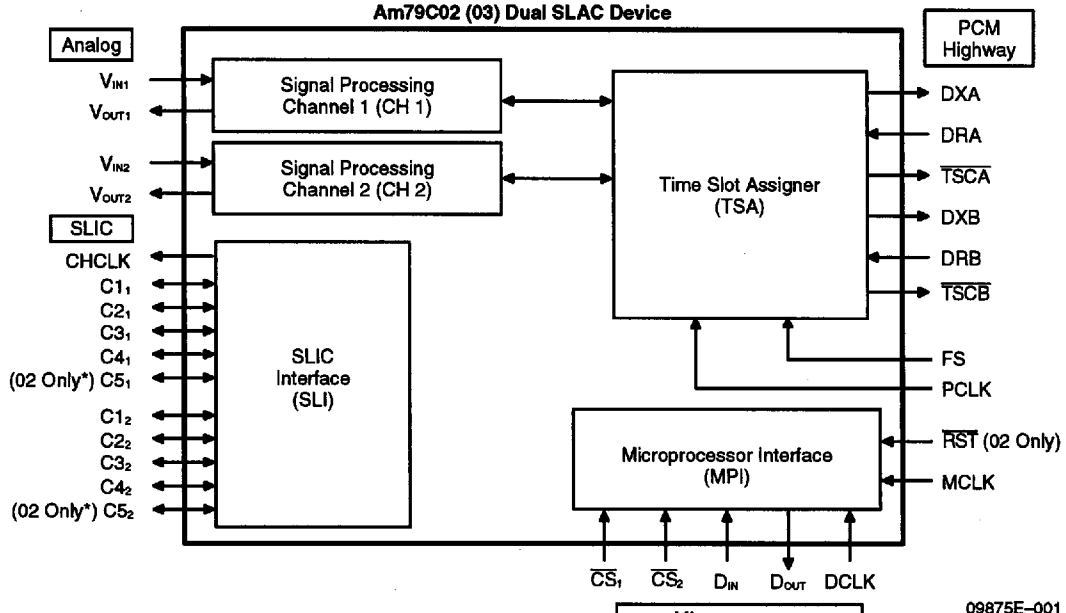
- **Software programmable:**
  - –SLIC impedance
  - –Trans-hybrid balance
  - –Transmit and Receive gains
  - –Equalization
  - –Digital I/O pins
  - –Time Slot Assigner
  - –PCM transmit clock edge options
- **Adaptive trans-hybrid balance filter (Am79C02/3A only)**
- **A-law or μ-law coding**
- **Dual PCM ports**
  - –Up to 8.192 MHz (128 channels per port) through the PCM Interface
- **2.048- or 4.096-MHz master clock**
- **Direct transformer drive**
- **Built-in test modes**
- **Low-power CMOS**
- **Mixed mode (analog and digital) impedance scaling**
- **Performance characteristics guaranteed over 12-dB gain range**

GENERAL DESCRIPTION

The Am79C02/3(A) Dual Subscriber Line Audio-Processing Circuit (DSLAC device) integrates the key functions of an analog linecard into one programmable, high-performance dual Codec-filter device. The DSLAC device is based on the proven design of the reliable Am7901A Subscriber Line Audio-Processing Circuit (SLAC™ device). The advanced architecture of the DSLAC device implements two independent channels and employs digital filters to allow software control of transmission, thus providing a cost-effective solution for the four-wire-to-PCM section of a linecard.

Advanced CMOS technology makes the Am79C02/3(A) DSLAC device an economical device that has both the functionality and the low-power consumption needed by linecard designers to maximize linecard density at minimum cost. When used with two SLICs, the DSLAC device provides a complete, software-configurable solution to the BORSCHT function.

BLOCK DIAGRAM



09875E-001

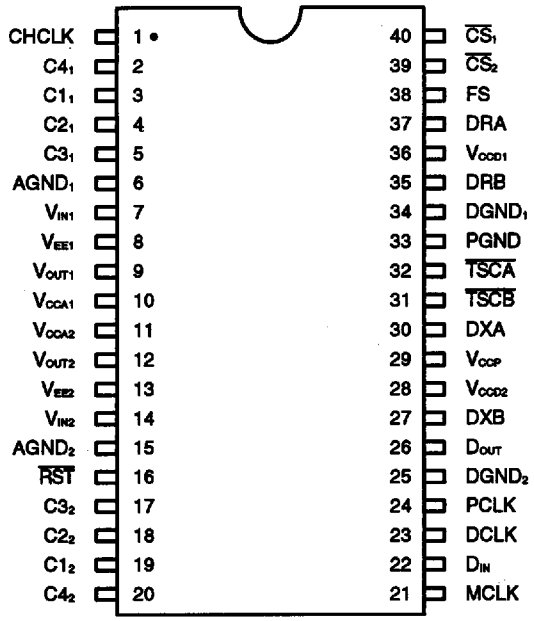
*$C5_1$ and $C5_2$ not on DIP version.

Publication #: 09875 Rev. F Amendment /0
Issue Date: June 1992

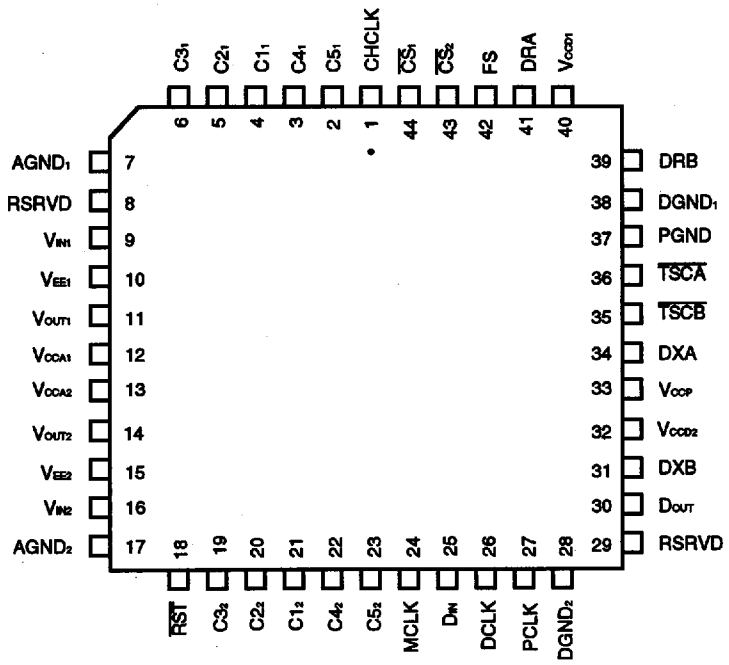
CONNECTION DIAGRAMS
Top View (Am79C02 only)

ADV MICRO (TELECOM)

40-Pin DIP



44-Pin PLCC

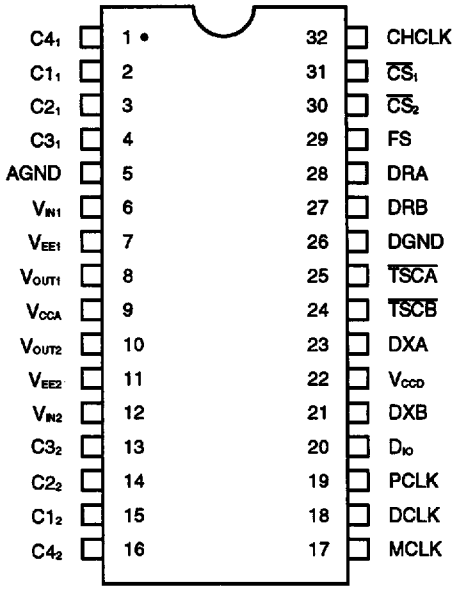


Note: 1. Pin 1 is marked for orientation purposes.
2. RSRVD = Reserved pin, should not be connected externally to any signal or supply.

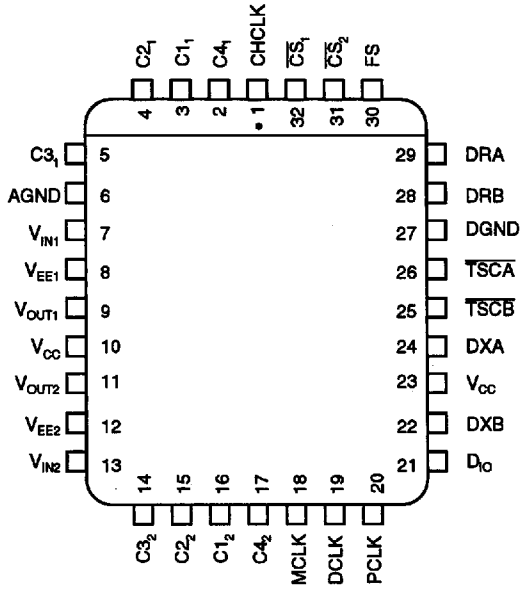
CONNECTION DIAGRAMS
Top View (Am79C03 only)

ADV MICRO (TELECOM)

32-Pin DIP



32-Pin PLCC

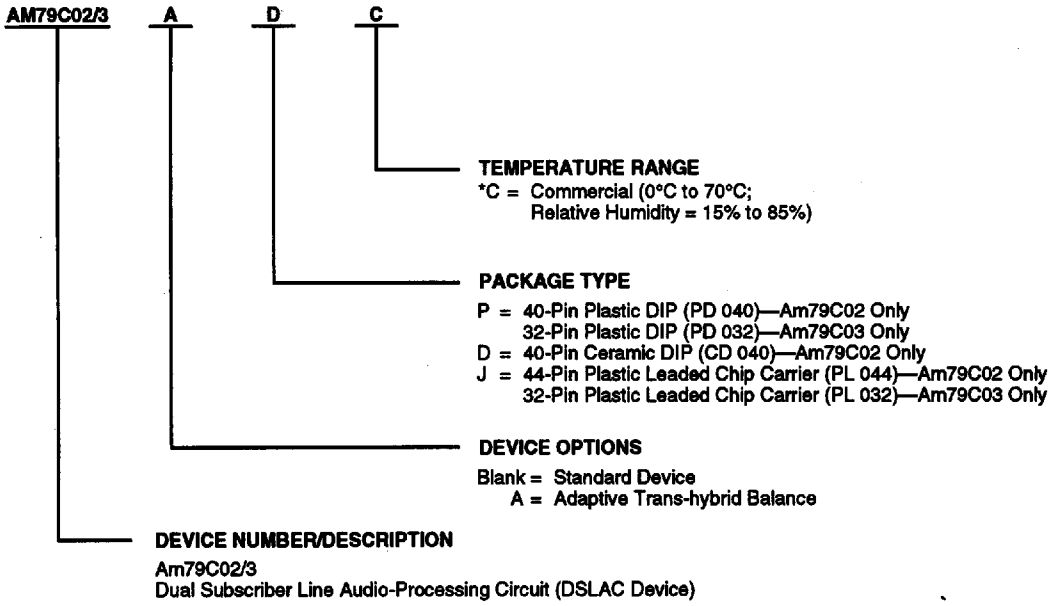


Note: Pin 1 is marked for orientation purposes.

ADV MICRO (TELECOM)

ORDERING INFORMATION
Standard Products

AMD® standard products are available in several packages and operating ranges. The order number (Valid Combination) is formed by a combination of the elements below.



Valid Combinations	
AM79C02	ADC, AJC, APC
	DC, JC, PC
AM79C03	APC, PC, JC

Valid Combinations

Valid Combinations list configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations, to check on newly released combinations, and to obtain additional data on the AMD standard military grade products.

*The performance specifications contained in this data sheet are valid for the commercial temperature range only. See the DSLAC Extended Temperature Supplement (page 2-153) for information on industrial temperature range (–40°C to +85°C) specifications.

PIN DESCRIPTION

$C1_1$–$C5_1$, $C1_2$–$C5_2$
SLIC Inputs/Outputs (Inputs/Outputs)

The five SLIC control lines per channel are TTL compatible and bi-directional. They can be used to monitor or control the operation of a SLIC or any other device associated with the subscriber line. Lines $C1_1$–$C5_1$ are associated with Channel 1, and lines $C1_2$–$C5_2$ are associated with Channel 2. The $C5_1$ and $C5_2$ lines are only available on the 44-pin PLCC version of the Am79C02(A).

CHCLK
SLIC Clock (Output)

This output provides a 256-kHz, 50%-duty cycle, TTL-compatible clock for use by two SLICs. The CHCLK frequency is synchronous to MCLK but the phase relationship to MCLK is random. CHCLK is capable of driving two TTL inputs.

$\overline{CS}_1$, $\overline{CS}_2$
Chip Selects (Inputs, Active Low)

The Chip Select inputs enable the device to read or write control data. $\overline{CS}_1$ is for the Channel 1 microprocessor interface. $\overline{CS}_2$ is for the Channel 2 microprocessor interface.

DCLK
Data Clock (Input)

The Data Clock input shifts data either into or out of the Microprocessor Interface of the DSLAC device. The maximum clock rate is 4.096 MHz.

D_{IN}
Data Input (Input)

Control data is serially written into the DSLAC device via the D_{IN} pin with the most significant bit first. The Data Clock determines the data rate. D_{IN} and D_{OUT} may be strapped together to reduce the number of connections to the microprocessor. (Not available on the Am79C03.)

D_{OUT}
Data Output (Output)

Control data is serially read out of the DSLAC device via the D_{OUT} pin with the most significant bit first. The Data Clock determines the data rate. D_{OUT} is high impedance except when data is being transmitted from the DSLAC device under control of $\overline{CS}_1$ or $\overline{CS}_2$. D_{IN} and D_{OUT} may be strapped together to reduce the number of connections to the microprocessor. (Not available on the Am79C03.)

D_{IO}
Data Input/Output

Control data is serially written into and read out of the Am79C03(A) DSLAC device via the D_{IO} pin with the most significant bit first. The Data Clock determines the data rate. D_{IO} is high impedance except when data is being transmitted from the DSLAC device under control of $\overline{CS}_1$ or $\overline{CS}_2$. D_{IO} replaces D_{IN} and D_{OUT} found on the Am79C02(A).

DRA, DRB
PCM Inputs (Inputs)

The Receive PCM data for Channels 1 and 2 is serially received on either the DRA or the DRB port with port selection under user program control. Eight bits are received with the most significant bit first. Data for each channel is received in 8-bit bursts every 125 µs at the PCLK rate.

DXA, DXB
PCM Outputs (Outputs)

The Transmit PCM data from Channels 1 and 2 is sent serially through either the DXA or DXB port with port selection under user program control. Eight bits are transmitted with the most significant bit first. The output is available every 125 µs and the data is shifted out in 8-bit bursts at the PCLK rate. DXA and DXB are high impedance between bursts and while the device is in the Inactive mode.

FS
Frame Sync (Input)

The Frame Sync pulse is an 8-kHz signal that identifies the beginning of a frame. The DSLAC device references individual time slots with respect to this input, which must be synchronized to PCLK.

MCLK
Master Clock (Input)

The Master Clock must be a 2.048-MHz or 4.096-MHz clock input for use by the digital signal processor. MCLK may be asynchronous to PCLK.

PCLK
PCM Clock (Input)

The PCM clock determines the rate at which PCM data is serially shifted into or out of the PCM ports. PCLK is an integer multiple of the frame sync frequency. The maximum clock frequency is 8.192 MHz and the minimum clock frequency is 128 kHz. The PCLK clock may be asynchronous to MCLK.

$\overline{RST}$
Reset (Input, Active Low)

A TTL Low signal on this input resets the DSLAC device to its default state. (Not available on the Am79C03.)

$\overline{TSCA}$, $\overline{TSCB}$
Time Slot Control (Outputs, Open Drain, Active Low)

The Time Slot Control outputs are open drain (requiring pull-up resistors) and are normally inactive (high impedance). $\overline{TSCA}$ is active (Low) when PCM data is present on the DXA output and $\overline{TSCB}$ is active (Low) when PCM data is present on the DXB output.

ADV MICRO (TELECOM)

V_{IN1}, V_{IN2}

Analog Inputs (Inputs)

The analog input is applied to the transmit path of the DSLAC device. The signal is sampled, digitally processed and encoded for the PCM output. V_{IN1} is the input for Channel 1 and V_{IN2} is the input for Channel 2.

V_{OUT1}, V_{OUT2}

Analog Outputs (Outputs)

The received PCM data is digitally processed and converted to an analog signal at the V_{OUT} pin. V_{OUT1} is the output from Channel 1 and V_{OUT2} is the output for Channel 2. These outputs can directly drive a transformer SLIC.

For Am79C02:

$AGND_1$	Analog Ground (Channel 1)
$AGND_2$	Analog Ground (Channel 2)
$DGND_1$	Digital Ground 1
$DGND_2$	Digital Ground 2
PGND	PCM I/O Ground
V_{CCA1}	+5-V Analog Power Supply (Channel 1)
V_{CCA2}	+5-V Analog Power Supply (Channel 2)
V_{CCD1}	+5-V Digital Power Supply. Internally connected to substrate on the IC.
V_{CCD2}	+5-V Digital Power Supply. Internally connected to substrate on the IC.
V_{CCP}	+5-V PCM I/O Power Supply. Internally connected to substrate on the IC.
V_{EE1}	–5-V Power Supply (Channel 1)
V_{EE2}	–5-V Power Supply (Channel 2)

For Am79C03:

AGND	Analog Ground
DGND	Digital Ground
V_{CCA}	+5-V Analog Power Supply
V_{CCD}	+5-V Digital Power Supply. Internally connected to substrate on the IC.
V_{EE1}	–5-V Power Supply (Channel 1)
V_{EE2}	–5-V Power Supply (Channel 2)

The many separate power supply inputs are intended to provide for good power supply decoupling techniques. Note that all of the +5-V inputs should be connected to the same source, all of the ground inputs should be connected to the same source, and both of the –5-V inputs should be connected to the same source.

FUNCTIONAL DESCRIPTION

The DSLAC device performs the Codec/filter functions associated with the four-wire section of the subscriber line circuitry in a digital switch. These functions involve converting an analog voice signal into digital PCM samples and converting digital PCM samples back into an analog signal. During conversion, digital filters are used to band-limit the voice signals.

Independent channels allow the DSLAC device to function as two SLAC devices. All of the digital filtering is performed in digital signal processors operating from either a 2.048-MHz or 4.096-MHz external clock. The A/D, D/A, and signal processing is separate for each channel and each channel has its own chip select ($\overline{CS}_1$ and $\overline{CS}_2$) to allow separate programming.

The user-programmable filters set the receive and transmit gain, perform the trans-hybrid balancing function, permit adjustment of the two-wire termination impedance, and provide frequency attenuation adjustment (equalization) of the receive and transmit paths. All programmable digital filter coefficients can be calculated using the AmSLAC2™ software. The PCM codes can be either 8-bit companded A-law or μ-law. The PCM data is read or written to the PCM highway in user-programmable time slots at rates of 128 kHz to 8.192 MHz. The output hold time and the transmit clock edge can be selected for compatibility with other devices which can be connected to the PCM highway.

Two pin configurations of the DSLAC device are offered with the PCM interface described above. The Am79C02(A), the original version of the DSLAC device, is available in both 40-pin DIP and 44-pin PLCC packages. The PLCC version has one extra SLIC I/O line per channel. The Am79C03(A) is a reduced pin-count version obtained by consolidating a number of ground and power supply buses on-chip, and eliminating the hardware reset function. The Am79C03(A) is available in both 32-pin plastic DIP and 32-pin PLCC packages. The "A" version of both devices (e.g., Am79C02A) offers an adaptive trans-hybrid balance feature described in the Adaptive B-Filter Overview.

The following documentation describes the operation of a single channel of the DSLAC device. The description is valid for either Channel 1 or 2. V_{IN} in this data sheet refers to either V_{IN1} or V_{IN2}, V_{OUT} refers to either V_{OUT1} or V_{OUT2}, and $\overline{CS}$ refers to either $\overline{CS}_1$ or $\overline{CS}_2$.

Operational Modes

Active Mode

Each channel of the DSLAC device can operate in either the active (operational) or inactive (standby) mode. In the active mode, the DSLAC device is able to transmit and receive PCM and analog information. This is the normal operating mode when a telephone call is in progress. The Activate command, Microprocessor Interface (MPI) Command #5, puts the device into this state. Bringing the DSLAC device into the active mode is only possible through the MPI.

Inactive Mode

The Am79C02(A) DSLAC device is forced into the inactive (standby) mode at power-up, by a hardware or software reset, or is programmed into this mode by the inactivate command (Command #1). The Am79C03 DSLAC device is forced into the standby mode at power-up or by a software reset. No transmission or reception of PCM data takes place, but the circuits which contain programmed information retain their data. Power is switched off from all non-essential circuitry, though the MPI remains active to receive new commands. The analog output is tied to ground through an approximately 3-Kohm resistor.

Reset State

An active Low, hardware Reset pin ($\overline{RST}$) is available on the Am79C02 which resets the device to the following default state. (For the Am79C03, when power is first applied, an internal power-on reset puts the device into the following default state.)

1. A-law is selected.
2. B, X, R, and Z filters are disabled and AISN gain is zero.
3. Digital (GX and GR) gain blocks are disabled, resulting in unity gain, and analog (AX and AR) gains are set to unity.
4. SLIC input/output direction is set to the input mode.
5. Normal conditions are selected (see Command #4).
6. The B-filter adaptive mode is turned off.
7. Both channels are placed in the Inactive (standby) mode.
8. Transmit time, receive time, and clock slots are set to zero.
9. DXA/DRA ports are selected for Channel 1.
10. DXB/DRB ports are selected for Channel 2.
11. MCLK is selected to be 4.096 MHz.
12. The transmit outputs are selected to change on the negative edge of PCLK.
13. PCM Delay is inserted.

Reset states 1 to 7 are identical to those of the software reset (Command #2), but the hardware (or power-on) reset applies to both channels simultaneously. When power is initially applied to the DSLAC device or when $\overline{RST}$ is asserted (Am79C02 only), the following sequence of actions is necessary to ensure correct operation of the DSLAC device.

1. Select MCLK frequency (Command #6).
2. Software reset (Command #2).
3. Program filter coefficients and all other required parameters.

Upon initial application of power, a minimum of 1 ms is needed before $\overline{CS_1}$ or $\overline{CS_2}$ may go Low and an MPI command initiated. If the power supply (V_{CCD1} or V_{CCD2}) falls below approximately 2.0 V, the device is software-reset and will require complete reprogramming with the above sequence. Bit 7 of the SLIC Direction Register will read back as a logical 1 to indicate a power interruption has been detected. This bit is cleared when a software reset command is sent to the DSLAC device. The $\overline{RST}$ pin may be tied to +5 V if it is not needed in the system (Am79C02 only).

Signal Processing

Overview of Digital Filters

Several of the blocks in the signal processing section are user programmable. These allow the user to optimize the performance of the DSLAC device for the system. Figure 1 shows DSLAC device signal processing and indicates the programmable blocks.

The advantages of digital filters are:

–high reliability;
–no drift with time or temperature;
–unit-to-unit repeatability; and,
–superior transmission performance.

Two-Wire Impedance Matching

Two feedback paths on the DSLAC device modify the effective two-wire input impedance of the SLIC by providing programmable feedback from V_{IN} to V_{OUT}. The Analog Impedance Scaling Network (AISN) provides a programmable analog gain of –0.9375 to +0.9375 from V_{IN} to V_{OUT}. The Z filter is a programmable digital filter, also connecting V_{IN} to V_{OUT}.

Distortion Correction and Equalization

The DSLAC device contains programmable filters in the receive (R) and transmit (X) directions. These may be programmed for line equalization and to correct any attenuation distortion caused by the Z filter.

Trans-Hybrid Balancing

The DSLAC device's programmable B filter is used to adjust trans-hybrid balance. The filter has a single-pole IIR section (B-IIR) and an eight-tap FIR section (B-FIR), both operating at 16 kHz. The DSLAC device has an optional adaptive mode for the B filter which may be used to achieve optimum performance. The Echo Path Gain (EPG) and Error Level Threshold (ELT) registers contain values which determine the adaptive mode performance.

Gain Adjustment

The DSLAC device transmit path has two programmable gain blocks. Gain block AX is an analog gain of 0 dB or 6.02 dB, located immediately before the A/D converter. Gain block GX is a digital gain that is programmable to any gain from 0 dB to +12 dB with a worst case step size of 0.1 dB for gain settings below +10 dB, and a worst case step size of 0.3 dB for gain settings above +10 dB. The filters provide a net gain in the range of 0 dB to 18 dB.

The DSLAC device receive path has two programmable loss blocks. Loss block GR is a digital loss that is programmable from 0 dB to 12 dB with a worst case step size of 0.1 dB. Loss block AR is an analog loss of 0 dB or 6.02 dB, located immediately after the D/A converter. This provides a net loss in the range of 0 dB to 18 dB.

Transmit Signal Processing

In the transmit path, the analog input signal is A/D converted, filtered, companded (A- or μ-law), and made available for output to the PCM highway. The signal processor contains an ALU, RAM, ROM, and control logic to implement the filter sections. The B, X, and GX blocks are user-programmable digital filter sections with

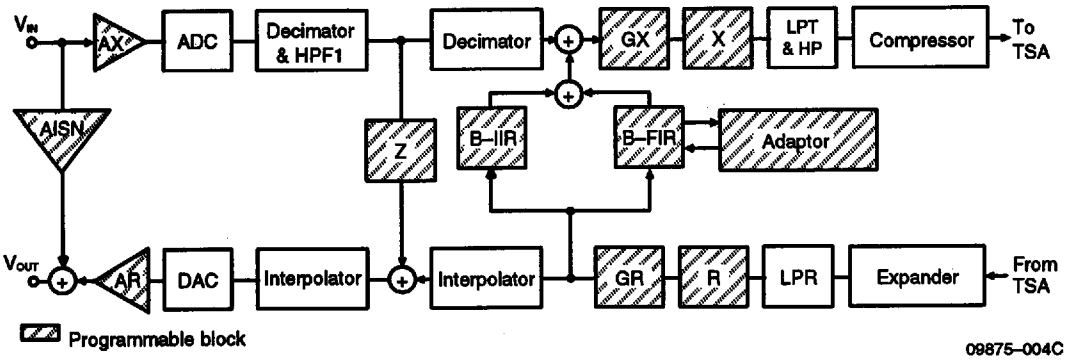


Figure 1. DSLAC Device Signal Processing

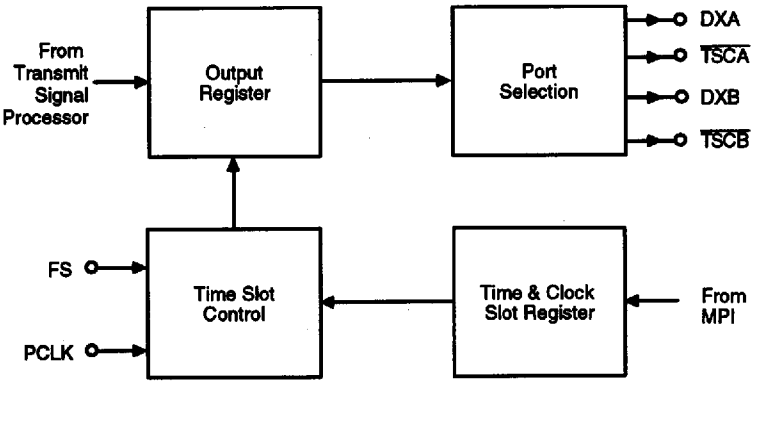


Figure 2. Transmit PCM Interface

coefficients stored in the coefficient RAM. AX is an analog amplifier which can be programmed for 0-dB or 6.02-dB gain. The filters may be made transparent when not required in a system.

The decimator reduces the high input sampling rate to 16 kHz for input to the B, GX, and X filters. The X filter is a 6-tap FIR section which is part of the frequency response correction network. The B filter operates on samples from the receive signal path in order to provide trans-hybrid balancing in the loop. The high-pass filter rejects low frequencies such as 50 or 60 Hz and may be disabled.

Transmit PCM Interface

The transmit PCM interface receives an 8-bit compressed code from the digital A-/μ-law compressor. The transmit PCM interface logic (Figure 2) controls the transmission of the data onto the PCM highway through the output port selection circuitry and the time and clock slot control block.

The frame sync (FS) pulse identifies the beginning of a transmit frame and all channels (time slots) are referenced to it. The logic contains user-programmable Transmit Time Slot and Transmit Clock Slot registers.

The Time Slot register is 7 bits wide and allows up to 128 8-bit channels (using a PCLK of 8.192 MHz) in each frame. This feature allows any clock frequency between 128 kHz and 8.192 MHz (2 to 128 channels) in a system. The Clock Slot register is 3 bits wide and may be programmed to offset the time slot assignment by 0 to 7 PCLK periods to eliminate any clock skew in the system. The data is transmitted in bytes with the most significant bit first.

The PCM data may be user-programmed for output onto either the DXA or DXB port. Correspondingly, either $\overline{\text{TSCA}}$ or $\overline{\text{TSCB}}$ is Low during transmission.

The DXA/DXB and $\overline{\text{TSCA}}$/$\overline{\text{TSCB}}$ outputs can be programmed to change either on the negative or positive edge of PCLK. In the first case, an extra delay (PCM

delay) in the timing of the DXA and DXB signals may be programmed to allow timing compatibility with other devices on the PCM highway.

Receive Signal Processing

In the receive path, the digital signal is expanded, filtered, converted to analog, and passed to the V_{OUT} pin. The signal processor contains an ALU, RAM, ROM, and Control logic to implement the filter sections. The Z, R, and GR blocks are user-programmable filter sections with their coefficients stored in the coefficient RAM while AR is an analog amplifier which can be programmed for a 0-dB or 6.02-dB loss. The filters may be made transparent when not required in a system.

The low-pass filter band limits the signal. The R filter is a 6-tap FIR section operating at a 16-kHz sampling rate and is part of the frequency response correction network. The analog impedance scaling network (AISN) is a user-programmable gain block providing feedback from V_{IN} to V_{OUT} to emulate different Z_{SLIC} impedances from a single external Z_{SLIC} impedance. The Z filter provides feedback from the transmit signal path to the receive path and is used to modify the effective input impedance to the system. The interpolator increases the sampling rate prior to D/A conversion.

Receive PCM Interface

The receive PCM interface logic (Figure 3) controls the reception of data bytes from the PCM highway, transfers the data to the A-/μ-law expansion logic, and then passes the data to the receive path of the signal processor. The frame sync (FS) pulse identifies the beginning of a receive frame, and all channels (time slots) are referenced to it.

The logic contains user-programmable Receive Time Slot and Receive Clock Slot registers. The Time Slot register is 7 bits wide and allows up to 128 8-bit channels (using a PCLK of 8.192 MHz) in each frame. This feature allows any clock frequency between 128 kHz and 8.192 MHz (2 to 128 channels) in a system. The Clock Slot register is 3 bits wide and may be programmed to offset the time slot assignment by 0 to 7 PCLK periods to eliminate any clock skews in the system. The PCM data may be user-programmed for input from either the DRA or DRB port.

Analog Impedance Scaling Network (AISN)

The AISN is incorporated in the DSLAC device to scale the value of the external Z_{SLIC} impedance. Scaling this external impedance with the AISN (along with the Z filter) allows matching of many different line conditions using a single impedance value. Linecards may be designed for many different specifications without any hardware changes.

The AISN is a programmable gain that is connected across the DSLAC device input from V_{IN} to V_{OUT}. The gain can be varied from –0.9375 to +0.9375 in 31 steps of 0.0625. The AISN gain is given by the following equation:

$$h_{AISN} = 0.0625\,[(A \cdot 2^4 + B \cdot 2^3 + C \cdot 2^2 + D \cdot 2^1 + E \cdot 2^0) - 16]$$

where A, B, C, D, and E = 1 or 0.

The AISN gain is used to alter the input impedance of the DSLAC device and SLIC as shown in Figure 4.

The input impedance into the DSLAC device from the SLIC is given by:

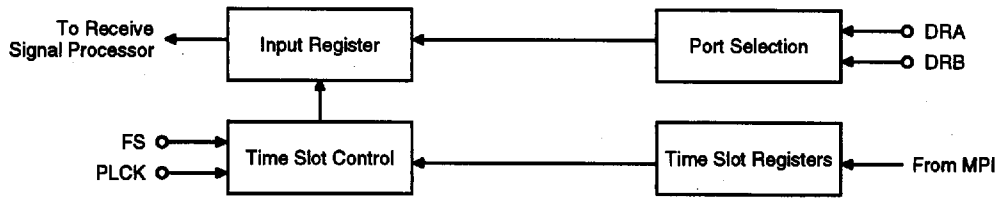
$$Z_{IN} = \frac{1 - G_{44}\,h_{AISN}}{1 - G_{440}\,h_{AISN}}\,Z_{SL},$$

where G_{440} (defined as $G_{24}\,G_{42} + G_{44}$) is the echo gain into an open circuit and G_{44} is the echo gain into a short circuit.

There are two special cases to the formula for h_{AISN}: 1) value of ABCDE = 00000 will specify a gain of 0 (or cutoff), and 2) a value of ABCDE = 10000 is a special case where the AISN circuitry is disabled and the V_{OUT} pad is connected internally to V_{IN} with a gain of 0 dB. This allows a digital-to-digital loopback mode wherein a digital PCM input signal is completely processed through the receive section all the way to the V_{OUT} pin. The signal is then connected internally to V_{IN} where it is processed through the transmit section and output as digital PCM data.

Speech Coding

The A/D and D/A conversion follows either the A-law or the μ-law as they are defined in CCITT Rec. G.711. A-law or μ-law operation is programmed using MPI Command #19. Alternate bit inversion is performed as part of the A-law coding.



09875–007C

Figure 3. Receive PCM Interface

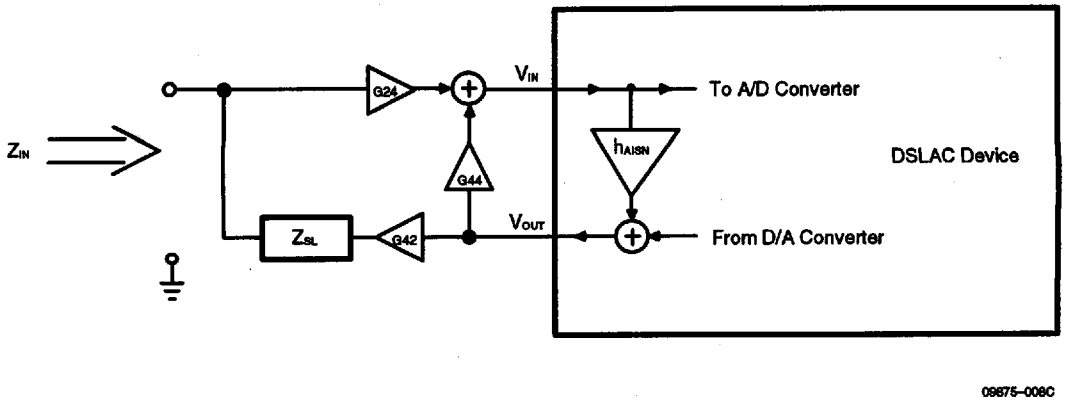


Figure 4. Input Impedance Modification Due to AISN

Command Description and Formats

Microprocessor Interface Description

A microprocessor may be used to program the DSLAC device and control its operation using the Microprocessor Interface (MPI). Data programmed previously may be read out for verification. For each channel, commands are provided to assign values to the following parameters.

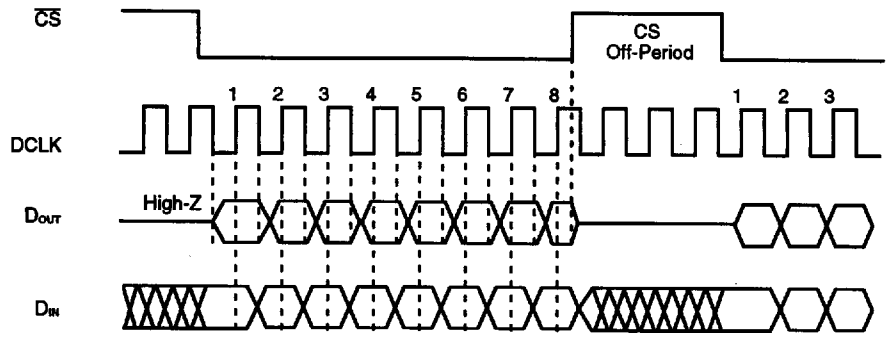
–Transmit time slot
–Receive time slot.
–Transmit clock slot
–Receive clock slot
–Transmit gain
–Receive loss
–B-filter coefficients
–X-filter coefficients
–R-filter coefficients
–Z-filter coefficients
–Adaptive B filter parameters
–AISN coefficient
–Read/Write SLIC Input/Output
–Select A-law or μ-law code
–Select Transmit PCM Port A or B
–Select Transmit PCM clock edge
–Select Transmit PCM delay
–Select Receive PCM Port A or B
–Enable/disable B filter
–Enable/disable Z filter
–Enable/disable X filter
–Enable/disable R filter
–Enable/disable GX filter
–Enable/disable GR filter
–Enable/disable AX amplifier
–Enable/disable AR amplifier
–Enable/disable adaptive B filter
–Select test modes
–Select active or inactive (standby) mode

The following description of the MPI is valid for either Channel 1 or 2. Whenever $\overline{CS}$ is specified, it refers to either $\overline{CS}_1$ or $\overline{CS}_2$. If desired, both channels may be programmed simultaneously with identical information by activating $\overline{CS}_1$ and $\overline{CS}_2$ at the same time.

The MPI consists of serial data input (D_{IN} or D_{IO} on Am79C03), output (D_{OUT} or D_{IO} on Am79C03), data clock (DCLK), and a separate chip select ($\overline{CS}_1$ and $\overline{CS}_2$) input for each channel (Figure 5). The serial input consists of 8-bit command words which may be followed with additional bytes of input data or may be followed by the DSLAC device sending out bytes of data. All data input and output is MSB (D_7) first and LSB (D_0) last. All data bytes are read or written one at a time, with $\overline{CS}$ going High for at least the minimum off-period before the next byte is read or written.

All commands requiring additional input data to the device must have the input data as the next N words written into the device (for example, framed by the next N transitions of $\overline{CS}$). All commands followed by output data will cause the device to output data for the next N transitions of $\overline{CS}$ going Low. The DSLAC device will not accept any input commands until all the data has been shifted out. Unused bits in the data bytes are read out as zeros.

A command sequence to one channel must be finished before a command can be sent to the other channel.



09875–009C

Figure 5. Microprocessor Interface Timing Diagram

An MPI cycle is defined by transitions of $\overline{CS}$ and DCLK. If the $\overline{CS}$ lines are held in the High state between accesses, the DCLK may run continuously with no change to the internal control data. Using this method, the same DCLK may be run to a number of DSLAC devices and the individual $\overline{CS}$ lines will select the appropriate device to access. Between command sequences, DCLK can stay in the High state indefinitely with no loss of internal control information regardless of any transitions on the $\overline{CS}$ lines. Between bytes of a multi-byte read or write command sequence, DCLK can also stay in the High state indefinitely; however, each low-going transition of the $\overline{CS}$ line will still advance the byte counter. DCLK can stay in the Low state indefinitely with no loss of internal control information, provided the $\overline{CS}$ lines remain at a High level.

Summary of MPI Commands**

C#	Hex	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	Description
1.	00	0	0	0	0	0	0	0	0	Inactivate (Standby mode)
2.	02	0	0	0	0	0	0	1	0	Reset
3.	06	0	0	0	0	0	1	1	0	No Operation
4.	08	0	0	0	0	1	0	0	0	Reset to Normal Conditions
5.	0E	0	0	0	0	1	1	1	0	Activate
6.	1*	0	0	0	1	0	0	*	0	MCLK Selection
7.	40	0	1	0	0	0	0	0	0	Write TX Time Slot & PCM Highway
8.	41	0	1	0	0	0	0	0	1	Read TX Time Slot & PCM Highway
9.	42	0	1	0	0	0	0	1	0	Write RX Time Slot & PCM Highway
10.	43	0	1	0	0	0	0	1	1	Read RX Time Slot & PCM Highway
11.	44	0	1	0	0	0	1	0	0	Write RX & TX Clock Slot and TX Clock Edge
12.	45	0	1	0	0	0	1	0	1	Read RX & TX Clock Slot and TX Clock Edge
13.	50	0	1	0	1	0	0	0	0	Write AISN, PCM delay, Analog Gains
14.	51	0	1	0	1	0	0	0	1	Read AISN, PCM delay, Analog Gains
15.	52	0	1	0	1	0	0	1	0	Write SLIC Input/Output Register
16.	53	0	1	0	1	0	0	1	1	Read SLIC Input/Output Register
17.	54	0	1	0	1	0	1	0	0	Write SLIC Input/Output Direction
18.	55	0	1	0	1	0	1	0	1	Read SLIC I/O Direction, Power Interruption Bit, and Channel Status Bit
19.	60	0	1	1	0	0	0	0	0	Write Operating Functions
20.	61	0	1	1	0	0	0	0	1	Read Operating Functions
21.	70	0	1	1	1	0	0	0	0	Write Operating Conditions
22.	71	0	1	1	1	0	0	0	1	Read Operating Conditions
23.	73	0	1	1	1	0	0	1	1	Read Revision Code Number
24.	80	1	0	0	0	0	0	0	0	Write GX-Filter Coefficients
25.	81	1	0	0	0	0	0	0	1	Read GX-Filter Coefficients
26.	82	1	0	0	0	0	0	1	0	Write GR-Filter Coefficients
27.	83	1	0	0	0	0	0	1	1	Read GR-Filter Coefficients
28.	84	1	0	0	0	0	1	0	0	Write Z-Filter Coefficients
29.	85	1	0	0	0	0	1	0	1	Read Z-Filter Coefficients
30.	86	1	0	0	0	0	1	1	0	Write B-Filter Coefficients
31.	87	1	0	0	0	0	1	1	1	Read B-Filter Coefficients
32.	88	1	0	0	0	1	0	0	0	Write X-Filter Coefficients
33.	89	1	0	0	0	1	0	0	1	Read X-Filter Coefficients
34.	8A	1	0	0	0	1	0	1	0	Write R-Filter Coefficients
35.	8B	1	0	0	0	1	0	1	1	Read R-Filter Coefficients
36.	8C	1	0	0	0	1	1	0	0	Write Echo Path Gain
37.	8D	1	0	0	0	1	1	0	1	Read Echo Path Gain
38.	8E	1	0	0	0	1	1	1	0	Write Error Level Threshold
39.	8F	1	0	0	0	1	1	1	1	Read Error Level Threshold

*Code changes with function.
**All codes not listed are reserved by AMD and should not be used.

THE COMMAND STRUCTURE

This section describes in detail each of the MPI commands. Each of the commands is shown along with the format of any additional data bytes that follow. For details on the filter coefficients of the form $C_{xy}m_{xy}$, please refer to the Description of Coefficients section.

1. Inactivate (Standby Mode)

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
0	0	0	0	0	0	0	0

During the inactive mode (of one or both channels):
a) All of the programmed information is retained.
b) The Microprocessor Interface (MPI) remains active.
c) The PCM outputs are in high impedance and the PCM inputs are disabled.
d) The analog output is tied to zero volts through an internal resistor (~3 Kohm).

2. Reset

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
0	0	0	0	0	0	1	0

The reset state of the device is:
a) A-law is selected.
b) B, X, R, and Z filters are disabled and AISN gain is zero.
c) Digital (GX and GR) gain blocks are disabled resulting in unity gain, and analog (AX and AR) gains are set to unity.
d) All SLIC I/O lines are configured as inputs.
e) Normal conditions are selected (see Command #4).
f) The B-filter Adaptive mode is reset.
g) The channel is placed in the inactive (standby) mode.

3. No Operation

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
0	0	0	0	0	1	1	0

4. Reset to Normal Conditions

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
0	0	0	0	1	0	0	0

Reset to Normal Conditions performs the following operations:
a) Does not insert 6 dB loss in receive path.
b) Receive & transmit paths are not cutoff.
c) High pass filter is enabled.
d) Test modes are turned off.

5. Activate (Operational Mode)

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
0	0	0	0	1	1	1	0

This command places the device in the active mode. No valid PCM data is transmitted until after the second FS pulse is received following the execution of the Activate command.

6. MCLK Selection

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
0	0	0	1	0	0	A	0

MCLK may be selected to operate from a 2.048-MHz or 4.096-MHz external clock. MCLK selection on either channel affects both channels.
A = 0: 2.048 MHz
A = 1: 4.096 MHz

7. Write Transmit Time Slot and PCM Highway Selection

	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
Command:	0	1	0	0	0	0	0	0
Output data:	PCM	TS	TS	TS	TS	TS	TS	TS

PCM = 0: Highway A
PCM = 1: Highway B
TS: Time slot number 0 to 127

The Transmit section of both channels must not be set to the same time slot on the same output port simultaneously.

8. Read Transmit Time Slot and PCM Highway Selection

	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
Command:	0	1	0	0	0	0	0	1
Output data:	PCM	TS	TS	TS	TS	TS	TS	TS

9. Write Receive Time Slot and PCM Highway Selection

	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
Command:	0	1	0	0	0	0	1	0
Input data:	PCM	TS	TS	TS	TS	TS	TS	TS

PCM = 0: Highway A
PCM = 1: Highway B
TS: Time slot number 0 to 127

10. Read Receive Time Slot and PCM Highway Selection

	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
Command:	0	1	0	0	0	0	1	1
Output data:	PCM	TS	TS	TS	TS	TS	TS	TS

11. Write Transmit Clock Slot, Receive Clock Slot, and Transmit Clock Edge

	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
Command:	0	1	0	0	0	1	0	0
Input data:	—	XE	RCS	RCS	RCS	TCS	TCS	TCS

TCS: Transmit Clock Slot number 0 to 7
RCS: Receive Clock Slot number 0 to 7

XE = 0 Transmit changes on negative edge of PCLK
XE = 1 Transmit changes on positive edge of PCLK

Note: XE = 1 should not be programmed unless the PCM delay is removed, (i.e., PCD = 1). XE must be written on Channel 1, but affects both channels. If XE = 1, the maximum PCM clock rate becomes 4.096 MHz.

12. Read Transmit Clock Slot, Receive Clock Slot, and Transmit Clock Edge

	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
Command:	0	1	0	0	0	1	0	1
Output data:	—	XE	RCS	RCS	RCS	TCS	TCS	TCS

13. Write AISN, PCM Delay, and Analog Gains

	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
Command:	0	1	0	1	0	0	0	0
Input data:	PCD	AX	AR	A	B	C	D	E

PCM Delay: PCD = 0 Delay inserted (SLAC device compatible)
PCD = 1 Delay removed (high speed)

Transmit Analog Gain: AX = 0 0-dB gain
AX = 1 6.02-dB gain

Receive Analog Loss: AR = 0 0-dB loss
AR = 1 6.02-dB loss

AISN coefficient: A, B, C, D, E

The Analog Impedance Scaling Network (AISN) gain can be varied from –0.9375 to 0.9375 in multiples of 0.0625. The gain coefficient is decoded using the following equation:

$$h_{AISN} = 0.0625\,[(A \cdot 2^4 + B \cdot 2^3 + C \cdot 2^2 + D \cdot 2^1 + E \cdot 2^0) - 16]$$

where h_{AISN} is the gain of the AISN and A, B, C, D, and E = 0 or 1. A value of ABCDE = 10000 implements a special digital loopback mode, and a value of ABCDE = 00000 indicates a gain of 0 (cutoff).

14. Read AISN, PCM Delay, and Analog Gains

	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
Command:	0	1	0	1	0	0	0	1
Output data:	PCD	AX	AR	A	B	C	D	E

15. Write SLIC Output Register

	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
Command:	0	1	0	1	0	0	1	0
Input data:	—	—	—	C5	C4	C3	C2	C1

C1 through C5 are set to 1 or 0. The data will appear latched on the C1 through C5 SLIC I/O pins, provided they were set in the output mode (see Command #17). The data sent to any of the pins set to the input mode will be latched, but will not appear at the pins.

16. Read SLIC Pins

	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
Command:	0	1	0	1	0	0	1	1
Output data:	—	—	—	C5	C4	C3	C2	C1

The logic state of pins C1 through C5 is read regardless of the direction programmed into the Input/Output register.

17. Write SLIC Input/Output Direction

	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
Command:	0	1	0	1	0	1	0	0
Input data:	—	—	—	A	B	C	D	E

Pins C1 through C5 are set to input or output modes individually. The input mode is set when the appropriate data bit is a 0, and the output mode is set when the data bit is a 1. All unused SLIC I/O pins should be programmed as outputs to reduce power consumption.

Data bit A sets pins $C5_1$ or $C5_2$.
Data bit B sets pins $C4_1$ or $C4_2$.
Data bit C sets pins $C3_1$ or $C3_2$.
Data bit D sets pins $C2_1$ or $C2_2$.
Data bit E sets pins $C1_1$ or $C1_2$.

18. Read SLIC Input/Output Direction, Channel Status Bit, and Power Interrupt Bit

	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
Command:	0	1	0	1	0	1	0	1
Output data:	PI	CS	—	A	B	C	D	E

PI = 0 There has not been a power interruption since the last software reset command.

PI = 1 A power interruption has been previously detected requiring the DSLAC device to be completely reprogrammed. This bit is cleared by issuing a software reset command.

CS = 0 Channel is inactive (standby mode).

CS = 1 Channel is active.

19. Write Operating Functions

	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
Command:	0	1	1	0	0	0	0	0
Input data:	ABF	A/μ	EGR	EGX	EX	ER	EZ	EB

Adaptive B-Filter: ABF = 0 B-filter non-adaptive mode
ABF = 1 B-filter adaptive mode

A-law/μ-law: A/μ = 0 A-law coding
A/μ = 1 μ-law coding

GR Filter: EGR = 0 GR filter disabled
EGR = 1 GR filter enabled

GX Filter: EGX = 0 GX filter disabled
EGX = 1 GX filter enabled

X Filter: EX = 0 X filter disabled
EX = 1 X filter enabled

R Filter: ER = 0 R filter disabled
ER = 1 R filter enabled

Z Filter: EZ = 0 Z filter disabled
EZ = 1 Z filter enabled

B Filter: EB = 0 B filter disabled
EB = 1 B filter enabled

Note: The enable adaptive B-filter command is only effective when used with the enable B-filter command.

ADV MICRO (TELECOM)

20. Read Operating Functions

	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
Command:	0	1	1	0	0	0	0	1
Output data:	ABF	A/U	EGR	EGX	EX	ER	EZ	EB

21. Write Operating Conditions

	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
Command:	0	1	1	1	0	0	0	0
Input data:	CTP	CRP	HPF	RG	ALB	TLB	—	—

Cut off Transmit Path: CTP = 0 Transmit path connected
CTP = 1 Transmit path cut off
Cut off Receive Path: CRP = 0 Receive path connected
CRP = 1 Receive path cut off
High-Pass Filter: HPF = 0 High-pass filter enabled
HPF = 1 High-pass filter disabled
Receive Path Gain: RG = 0 6-dB loss not inserted
RG = 1 6-dB loss inserted
Analog Loopback: ALB = 0 Analog loopback disabled
ALB = 1 Analog loopback enabled
TSA Loopback: TLB = 0 TSA loopback disabled
TLB = 1 TSA loopback enabled

22. Read Operating Conditions

	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
Command:	0	1	1	1	0	0	0	1
Output data:	CTP	CRP	HPF	RG	ALB	TLB	—	—

23. Read Revision Code Number

	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
Command:	0	1	1	1	0	0	1	1
Output data:	#	#	#	#	#	#	#	#

This command returns an 8-bit number describing the revision number of the DSLAC device. It can be read on either channel.

24. Write GX-Filter Coefficients

	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
Command:	1	0	0	0	0	0	0	0
Input data byte 1:	C40		m40		C30		m30	
Input data byte 2:	C20		m20		C10		m10	

The coefficient for the GX filter is defined as:

$$H_{GX} = 1 + \left(C_{10} \cdot 2^{-m10}\{1 + C_{20} \cdot 2^{-m20}[1 + C_{30} \cdot 2^{-m30}(1 + C_{40} \cdot 2^{-m40})]\}\right).$$

25. Read GX-Filter Coefficients

	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
Command:	1	0	0	0	0	0	0	1
Output data byte 1:	C40 m40				C30 m30			
Output data byte 2:	C20 m20				C10 m10			

26. Write GR-Filter Coefficients

	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
Command:	1	0	0	0	0	0	1	0
Input data byte 1:	C40 m40				C30 m30			
Input data byte 2:	C20 m20				C10 m10			

The coefficient for the GR filter is defined as:

$$H_{GR} = C_{10} \cdot 2^{-m10}\{1 + C_{20} \cdot 2^{-m20}[1 + C_{30} \cdot 2^{-m30}(1 + C_{40} \cdot 2^{-m40})]\}.$$

27. Read GR-Filter Coefficients

	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
Command:	1	0	0	0	0	0	1	1
Output data byte 1:	C40 m40				C30 m30			
Output data byte 2:	C20 m20				C10 m10			

ADV MICRO (TELECOM)

28. Write Z Filter Coefficients

	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
Command:	1	0	0	0	0	1	0	0
Input data byte 1:	C45 m45				C35 m35			
Input data byte 2:	C25 m25				C15 m15			
Input data byte 3:	C40 m40				C30 m30			
Input data byte 4:	C20 m20				C10 m10			
Input data byte 5:	C41 m41				C31 m31			
Input data byte 6:	C21 m21				C11 m11			
Input data byte 7:	C42 m42				C32 m32			
Input data byte 8:	C22 m22				C12 m12			
Input data byte 9:	C43 m43				C33 m33			
Input data byte 10:	C23 m23				C13 m13			
Input data byte 11:	C44 m44				C34 m34			
Input data byte 12:	C24 m24				C14 m14			
Input data byte 13:	C46 m46				C36 m36			
Input data byte 14:	C26 m26				C16 m16			

The Z-transform equation for the Z filter is defined as:

$$H_Z(z) = Z_0 + Z_1 z^{-1} + Z_2 z^{-2} + Z_3 z^{-3} + Z_4 z^{-4} + \frac{Z_5}{1 - Z_6 z^{-1}}$$

The coefficients are defined as:

$$Z_i = C_{1i} \cdot 2^{-m1i}\{1 + C_{2i} \cdot 2^{-m2i}[1 + C_{3i} \cdot 2^{-m3i}(1 + C_{4i} \cdot 2^{-m4i})]\}$$

for i = 0,1,2,3,4,5,6.

29. Read Z-Filter Coefficients

	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
Command:	1	0	0	0	0	1	0	1
Output data byte 1:	C45 m45				C35 m35			
Output data byte 2:	C25 m25				C15 m15			
Output data byte 3:	C40 m40				C30 m30			
Output data byte 4:	C20 m20				C10 m10			
Output data byte 5:	C41 m41				C31 m31			
Output data byte 6:	C21 m21				C11 m11			
Output data byte 7:	C42 m42				C32 m32			
Output data byte 8:	C22 m22				C12 m12			
Output data byte 9:	C43 m43				C33 m33			
Output data byte 10:	C23 m23				C13 m13			
Output data byte 11:	C44 m44				C34 m34			
Output data byte 12:	C24 m24				C14 m14			
Output data byte 13:	C46 m46				C36 m36			
Output data byte 14:	C26 m26				C16 m16			

30. Write B-Filter Coefficients

	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
Command:	1	0	0	0	0	1	1	0
Input data byte 1:	C30		m30		C20		m20	
Input data byte 2:	C10		m10		C31		m31	
Input data byte 3:	C21		m21		C11		m11	
Input data byte 4:	C32		m32		C22		m22	
Input data byte 5:	C12		m12		C33		m33	
Input data byte 6:	C23		m23		C13		m13	
Input data byte 7:	C34		m34		C24		m24	
Input data byte 8:	C14		m14		C35		m35	
Input data byte 9:	C25		m25		C15		m15	
Input data byte 10:	C36		m36		C26		m26	
Input data byte 11:	C16		m16		C37		m37	
Input data byte 12:	C27		m27		C17		m17	
Input data byte 13:	C48		m48		C38		m38	
Input data byte 14:	C28		m28		C18		m18	

The z-transform equation for the B filter is defined as:

$$H_B(z) = B_0 + B_1z^{-1} + B_2z^{-2} + B_3z^{-3} + B_4z^{-4} + B_5z^{-5} + B_6z^{-6} + \frac{B_7z^{-7}}{1 - B_8z^{-1}}$$

The coefficients for the FIR B section and the gain of the IIR B section are defined as:

$$B_i = C_{1i} \cdot 2^{-m1i}[1 + C_{2i} \cdot 2^{-m2i}(1 + C_{3i} \cdot 2^{-m3i})].$$

The feedback coefficient of the IIR B section is defined as:

$$B_8 = C_{18} \cdot 2^{-m18}\ \{1 + C_{28} \cdot 2^{-m28}[1 + C_{38} \cdot 2^{-m38}(1 + C_{48} \cdot 2^{-m48})]\}.$$

Warning: Not all B-filter coefficients are "legal" to initiate adaptive balance. One legal coefficient is set as: 2A F2 AF 2A F2 AF 2A F2 AF 2A F2 AF 0A 80, which corresponds to all FIR coefficients (B_0 through B_7) equal to zero, and the IIR denominator coefficient (B_8) equal to 1/2. Other legal coefficients that may reduce the time to convergence of the algorithm may be obtained by reading back the registers after adaptive balance has been run (see Command #31).

ADV MICRO (TELECOM)

31. Read B-Filter Coefficients

	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
Command:	1	0	0	0	0	1	1	1
Output data byte 1:	C30		m30		C20		m20	
Output data byte 2:	C10		m10		C31		m31	
Output data byte 3:	C21		m21		C11		m11	
Output data byte 4:	C32		m32		C22		m22	
Output data byte 5:	C12		m12		C33		m33	
Output data byte 6:	C23		m23		C13		m13	
Output data byte 7:	C34		m34		C24		m24	
Output data byte 8:	C14		m14		C35		m35	
Output data byte 9:	C25		m25		C15		m15	
Output data byte 10:	C36		m36		C26		m26	
Output data byte 11:	C16		m16		C37		m37	
Output data byte 12:	C27		m27		C17		m17	
Output data byte 13:	C48		m48		C38		m38	
Output data byte 14:	C28		m28		C18		m18	

32. Write X-Filter Coefficients

	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
Command:	1	0	0	0	1	0	0	0
Input data byte 1:	C40		m40		C30		m30	
Input data byte 2:	C20		m20		C10		m10	
Input data byte 3:	C41		m41		C31		m31	
Input data byte 4:	C21		m21		C11		m11	
Input data byte 5:	C42		m42		C32		m32	
Input data byte 6:	C22		m22		C12		m12	
Input data byte 7:	C43		m43		C33		m33	
Input data byte 8:	C23		m23		C13		m13	
Input data byte 9:	C44		m44		C34		m34	
Input data byte 10:	C24		m24		C14		m14	
Input data byte 11:	C45		m45		C35		m35	
Input data byte 12:	C25		m25		C15		m15	

The z-transform equation for the X filter is defined as:

$$H_X(z) = X_0 + X_1 z^{-1} + X_2 z^{-2} + X_3 z^{-3} + X_4 z^{-4} + X_5 z^{-5}.$$

The coefficients for the X filter are defined as:

$$X_I = C_{1I} \cdot 2^{-m1I}\{1 + C_{2I} \cdot 2^{-m2I}[1 + C_{3I} \cdot 2^{-m3I}(1 + C_{4I} \cdot 2^{-m4I})]\}.$$

33. Read X-Filter Coefficients

	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
Command:	1	0	0	0	1	0	0	1
Output data byte 1:	C40	m40			C30	m30		
Output data byte 2:	C20	m20			C10	m10		
Output data byte 3:	C41	m41			C31	m31		
Output data byte 4:	C21	m21			C11	m11		
Output data byte 5:	C42	m42			C32	m32		
Output data byte 6:	C22	m22			C12	m12		
Output data byte 7:	C43	m43			C33	m33		
Output data byte 8:	C23	m23			C13	m13		
Output data byte 9:	C44	m44			C34	m34		
Output data byte 10:	C24	m24			C14	m14		
Output data byte 11:	C45	m45			C35	m35		
Output data byte 12:	C25	m25			C15	m15		

34. Write R-Filter Coefficients

	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
Command:	1	0	0	0	1	0	1	0
Input data byte 1:	C40	m40			C30	m30		
Input data byte 2:	C20	m20			C10	m10		
Input data byte 3:	C41	m41			C31	m31		
Input data byte 4:	C21	m21			C11	m11		
Input data byte 5:	C42	m42			C32	m32		
Input data byte 6:	C22	m22			C12	m12		
Input data byte 7:	C43	m43			C33	m33		
Input data byte 8:	C23	m23			C13	m13		
Input data byte 9:	C44	m44			C34	m34		
Input data byte 10:	C24	m24			C14	m14		
Input data byte 11:	C45	m45			C35	m35		
Input data byte 12:	C25	m25			C15	m15		

The z-transform equation for the R filter is defined as:

$$H_R(z) = R_0 + R_1z^{-1} + R_2z^{-2} + R_3z^{-3} + R_4z^{-4} + R_5z^{-5}.$$

The coefficients for the R filter are defined as:

$$R_I = C_{1I} \cdot 2^{-m1I}\{1 + C_{2I} \cdot 2^{-m2I}[1 + C_{3I} \cdot 2^{-m3I}(1 + C_{4I} \cdot 2^{-m4I})]\}.$$

ADV MICRO (TELECOM)

35. Read R-Filter Coefficients

	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
Command:	1	0	0	0	1	0	1	1
Output data byte 1:	C40		m40		C30		m30	
Output data byte 2:	C20		m20		C10		m10	
Output data byte 3:	C41		m41		C31		m31	
Output data byte 4:	C21		m21		C11		m11	
Output data byte 5:	C42		m42		C32		m32	
Output data byte 6:	C22		m22		C12		m12	
Output data byte 7:	C43		m43		C33		m33	
Output data byte 8:	C23		m23		C13		m13	
Output data byte 9:	C44		m44		C34		m34	
Output data byte 10:	C24		m24		C14		m14	
Output data byte 11:	C45		m45		C35		m35	
Output data byte 12:	C25		m25		C15		m15	

36. Write Echo Path Gain

	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
Command:	1	0	0	0	1	1	0	0
Input data byte 1:	C80		m80		C70		m70	
Input data byte 2:	C60		m60		C50		m50	
Input data byte 3:	C40		m40		C30		m30	
Input data byte 4:	C20		m20		C10		m10	

The equation for the Echo Path Gain is defined as:

$$EPG = 8 \cdot C_{10} \cdot 2^{-m10} \left(1 + C_{50} \cdot 2^{-m50}\{1 + C_{60} \cdot 2^{-m60}[1 + C_{70} \cdot 2^{-m70}(1 + C_{80} \cdot 2^{-m80})]\}\right),$$

C_{20}, M_{20}, C_{30}, M_{30}, C_{40}, and M_{40} must be zero.

37. Read Echo Path Gain

	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
Command:	1	0	0	0	1	1	0	1
Output data byte 1:	C80		m80		C70		m70	
Output data byte 2:	C60		m60		C50		m50	
Output data byte 3:	C40		m40		C30		m30	
Output data byte 4:	C20		m20		C10		m10	

38. Write Error Level Threshold

	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
Command:	1	0	0	0	1	1	1	0
Input data byte 1:	C20 m20				C10 m10			

The equation for the Error Level Threshold is defined as:

$$ELT = C_{10} \cdot 2^{-m10}(1 + C_{20} \cdot 2^{-m20}).$$

39. Read Error Level Threshold

	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
Command:	1	0	0	0	1	1	1	1
Output data byte 1:	C20 m20				C10 m10			

Programmable Filters

General Description of CSD Coefficients

The filter functions are performed by a series of multiplications and accumulations. A multiplication is accomplished by repeatedly shifting the multiplicand and summing the result with the previous value at that summation node. The method used in the DSLAC device is known as Canonic Signed Digit (CSD) multiplication and splits each coefficient into a series of CSD coefficients.

Each programmable FIR filter section has the following general transfer function:

$$HF(z) = h_0 + h_1z^{-1} + h_2z^{-2} + \ldots + h_nz^{-n} \qquad \text{Eq. (1)}$$

where the number of taps in the filter = n + 1.

The transfer function for the IIR part of the Z and B filters is:

$$HI(z) = \frac{1}{1 - h_{(n+1)}z^{-1}} \qquad \text{Eq. (2)}$$

The values of the user-defined coefficients (h_i) are assigned via the MPI. Each of the coefficients (h_i) is defined in the following general equation:

$$h_I = B_12^{-M_1} + B_22^{-M_2} + \ldots + B_N2^{-M_N}, \qquad \text{Eq. (3)}$$

where:

the number of shifts = $M_I \leq M_{I+1}$

sign = $B_I = \pm 1$

N = Number of CSD coefficients.

The value of h_I in Eq. (3) represents a decimal number which is broken down into a sum of successive values of:

± 1.0 multiplied by 2^{-0}, or 2^{-1}, or $2^{-2} \ldots 2^{-7} \ldots$

or

± 1.0 multiplied by 1, or 1/2, or 1/4 ... 1/128....

The limit on the negative powers of 2 is determined by the length of the registers in the ALU.

The coefficient h_I in Eq. (3) can be considered to be a value made up of N binary 1s in a binary register where the leftmost part represents whole numbers, the rightmost part represents decimal fractions, and a decimal point separates them. The first binary 1 is shifted M_1 bits to the right of the decimal point, the second binary 1 is shifted M_2 bits to the right of the decimal point, the third binary 1 is shifted M_3 bits to the right of the decimal point, and so on.

Note that when M_1 is 0, the resulting value is a binary 1 in front of the decimal point, that is, no shift. If M_2 is also 0, the result is another binary 1 in front of the decimal point, giving a total value of binary 10 in front of the decimal point (i.e., a decimal value of 2.0). The value of N, therefore, determines the range of values the coefficient h_I can take (e.g., if N = 3 the maximum and minimum values are ± 3, and if N = 4 the values are between ± 4).

Detailed Description of DSLAC Device Coefficients

The CSD coding scheme in the DSLAC device uses a value called m_I, where m_1 represents the distance shifted right of the decimal point for the first binary 1. m_2 represents the distance shifted to the right of the *previous* binary 1, and m_3 represents the number of shifts to the right of the second binary 1. Note that the range of values determined by N is unchanged. Eq. (3) is now modified (in the case of N = 4) to:

$$h_I = B_12^{-M1} + B_22^{-M2} + B_32^{-M3} + B_42^{-M4} \qquad \text{Eq. (4)}$$

$$h_I = C_12^{-m1} + C_1C_22^{-(m1+m2)} + C_1C_2C_32^{-(m1+m2+m3)} + C_1C_2C_3C_42^{-(m1+m2+m3+m4)} \qquad \text{Eq. (5)}$$

$$h_I = C_12^{-m1} \cdot \{1 + C_22^{-m2} \cdot [1 + C_32^{-m3} \cdot (1 + C_42^{-m4})]\} \qquad \text{Eq. (6)}$$

where:

$M_1 = m_1$ and $B_1 = C_1$

$M_2 = m_1 + m_2$ $B_2 = C_1 \cdot C_2$

$M_3 = m_1 + m_2 + m_3$ $B_3 = C_1 \cdot C_2 \cdot C_3$

$M_4 = m_1 + m_2 + m_3 + m_4$ $B_4 = C_1 \cdot C_2 \cdot C_3 \cdot C_4$

In the DSLAC device, a coefficient h_i consists of N CSD coefficients, each being made up of 4 bits and formatted as $C_{xy}m_{xy}$, where C_{xy} is one bit (MSB) and m_{xy} is 3 bits. Each CSD coefficient is broken down as follows.

C_{xy} is the sign bit (0 = positive, 1 = negative).

m_{xy} is the 3-bit shift code. It is encoded as a binary number as follows:

000:	0 shifts
001:	1 shifts
010:	2 shifts
011:	3 shifts
100:	4 shifts
101:	5 shifts
110:	6 shifts
111:	7 shifts

y is the coefficient number (the i in h_i).

x is the position of this CSD coefficient within the h_i coefficient. It represents the relative position of the binary 1 represented by this CSD coefficient within the h_i coefficient. The most significant binary 1 is represented by x = 1. The next most significant binary 1 is represented by x = 2, and so on.

Thus, $C_{13}m_{13}$ represents the sign and the relative shift position for the first (most significant) binary 1 in the 4th (h_3) coefficient.

The number of CSD coefficients, N, is limited to 4 in the GR, GX, R, X, Z, and the IIR part of the B filter, and 3 for the FIR part of the B filter. Note also that the GX filter coefficient equation is slightly different from that of the other filters.

$$h_{iGX} = 1 + h_i \qquad \text{Eq. (7)}$$

Please refer to the section detailing the commands for complete details on the programming of the coefficients.

Adaptive B-Filter Overview

The DSLAC device B filter is designed to work with pre-programmed coefficients or with coefficients determined by an adaptive algorithm. ***(Note that the adaptive trans-hybrid balance feature is only guaranteed on the A version of the Am79C02/3)***. The adaptive algorithm can be operated in a mode where it continuously adapts or where it adapts for a short period and then holds its value.

Operation with pre-programmed coefficients requires only the use of MPI Command #30 to feed in the coefficients. The adaptive mode uses some pre-programmed coefficients and generates new ones using an algorithm By a series of iterations, the algorithm minimizes the receive signal that is echoed in the transmit signal (due to mismatches in the SLIC, hybrid, and line). Adaptation only applies to the FIR part of the filter. Pre-programmed coefficients used to initiate the adaptive algorithm must be "legal" (shown under Command #30 on page 2-88). Other legal coefficients may be obtained by using this coefficient, running adaptive balance, and then reading back the registers (refer to #30 in command structure).

In the continuous adaptation mode, the algorithm is switched on (via MPI Command #19) after a call is connected and remains on until the call ends. In this way, the B filter is continually being optimized to the received signal.

In the adapt and freeze mode, the algorithm is used only when a line is brought into service and the DSLAC device is activated. The algorithm is switched on and is allowed to converge with the received signal, which is a band-limited white noise signal generated in the exchange for this purpose. The noise signal need only be injected for less than a second to yield converged coefficients. The adaptive mode is then switched off (via Command #19).

The converged coefficients may be read out of the DSLAC device (using MPI Command #31) and stored for future reference. The DSLAC device is now optimized for general input signals.

Adaptive Filter Programming

The purpose of the B filter is to cancel the received signal that leaks across the hybrid into the transmit path. The B-filter transfer function must match (as closely as possible) the transfer function of the echo path.

There are two programmable registers associated with the adaptive B filtering. The Echo Path Gain (EPG) is a programmable value that predicts the amount of the receive signal leaking across the hybrid to the transmit path. The EPG is used as part of an algorithm which stops the adaptive filter from iterating in the presence of signals from the subscriber line (near-end talker).

The Error Level Threshold (ELT) is a programmable value that determines the trans-hybrid loss the adaptive filter will attempt to meet. The adaptive algorithm will continue to iterate until it meets the loss requirement specified by the ELT. Both the EPG and ELT values are generated by the AmSLAC2 software program. Please refer to the AmSLAC2 Technical Manual.

User Test Modes

The DSLAC device supports testing by providing both digital and analog loopback paths as shown in Figure 6. In the TSA Loopback Mode, the DR input is connected to the DX output in the Time Slot Assigner circuitry. The TSA Loopback Mode is programmed via Command #21.

A different type of digital loopback is provided when the AISN register is programmed with a value of 10000. In this case, the AISN circuitry is disabled and the V_{OUT} pad is connected internally to V_{IN}. This allows the D/A and A/D converters to be included in the digital loopback test. This mode is programmed via Command #13. Note that the signal connected internally from V_{OUT} to V_{IN} is also present on the V_{OUT} pin.

The V_{IN} input can be connected to the V_{OUT} output through the Z filter for analog loopback. The response of the line to low frequencies can be tested by disabling the high-pass filter. Additionally, the receive and transmit paths may be cut off.

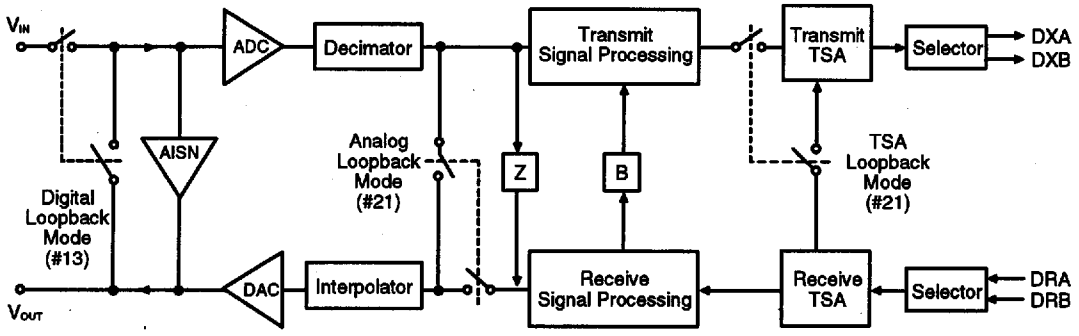
APPLICATIONS

The DSLAC device performs a programmable codec/filter function for two telephone lines. It interfaces to the telephone lines through either a transformer or an electronic SLIC such as the Am795XX series devices. The DSLAC device provides latched digital I/O to control and monitor two SLICs and has a 256-kHz clock output to operate the switched mode regulator in an Am795XX. When several line conditions must be matched, the physical SLIC can be constant, and its characteristics (such as apparent impedance, attenuation, and hybrid balance) can be altered by programming each DSLAC channel's coefficients to suit the line. For a transformer-based SLIC, the DSLAC device can drive the transformer without a buffer.

Connection to a dual PCM highway backplane is implemented by means of a simple buffer chip. Several DSLAC devices can be bussed together into one bus interface buffer. An intelligent bus interface chip is not required because each DSLAC device provides its own buffer control. The DSLAC device can be controlled through the Microprocessor Interface, either by a microprocessor on the linecard or by a central processor.

Figures 7 and 8 illustrate typical Am79C02 DSLAC device applications. Figure 7 shows the basic system architecture. Figure 8 illustrates the significant details of the interface to an Am795XX-based SLIC and to a transformer-based SLIC.

ADV MICRO (TELECOM)



09875-010C

Figure 6. Test Mode Operation

ADV MICRO (TELECOM)

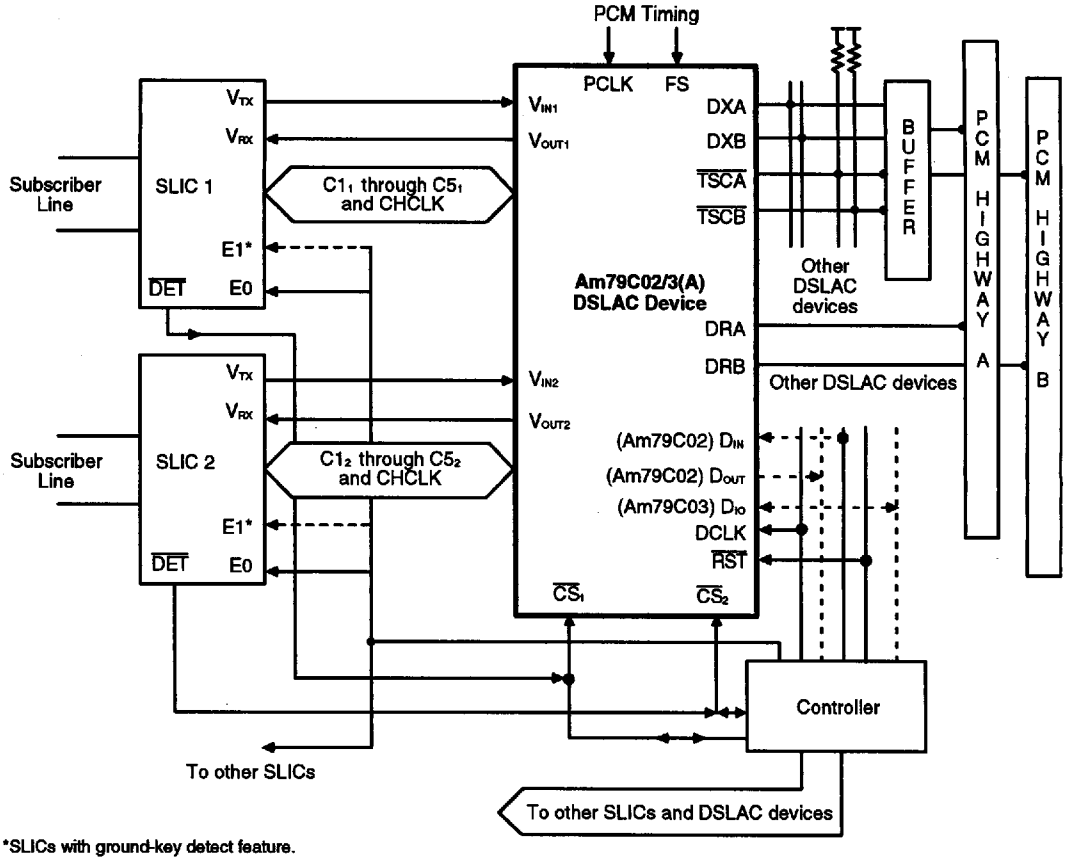
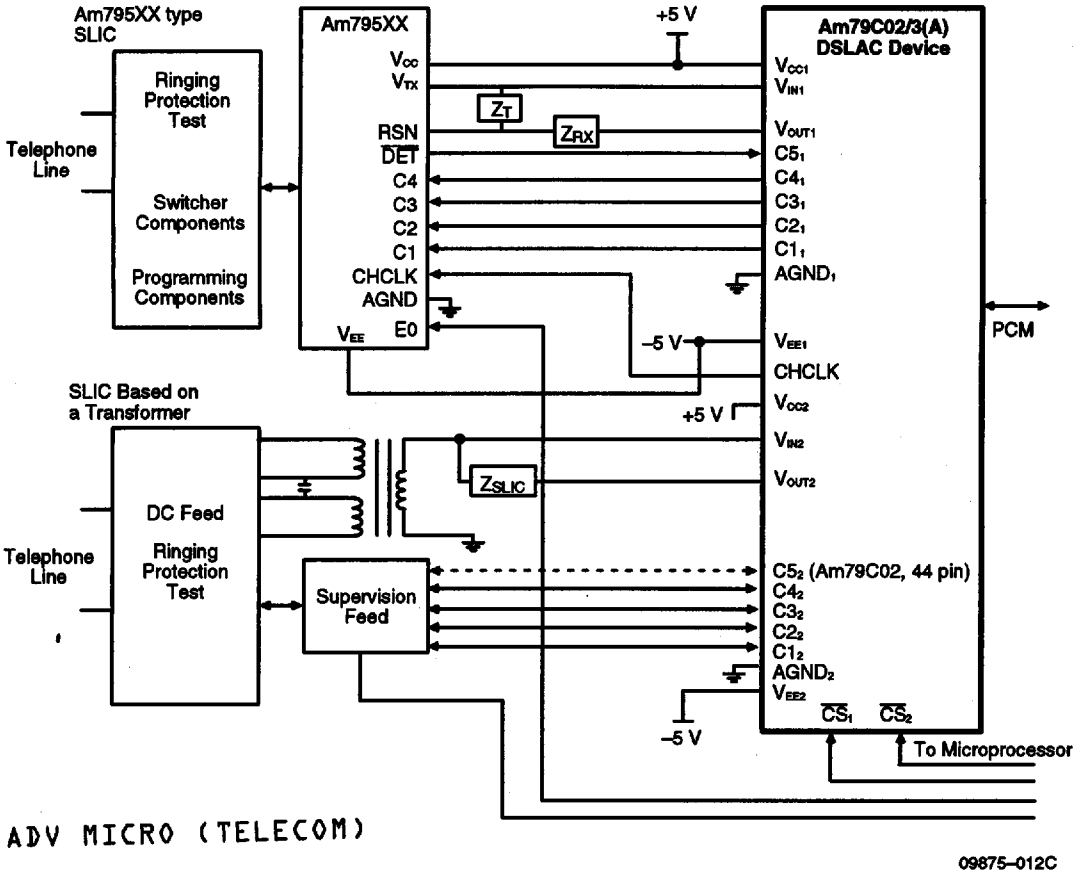


Figure 7. Basic System Architecture



ADV MICRO (TELECOM)

09875–012C

Figure 8. Typical SLIC Connections

Controlling the SLIC

SLIC Chopper Clock

The CHCLK output pin on the DSLAC device drives the CHCLK inputs for Am795XX series SLICs. The CHCLK output is a 256-kHz TTL-compatible signal that can drive two SLICs. It is only active when one or both channels are activated; otherwise it is held High internally.

SLIC Input/Output

The DSLAC device has five TTL-compatible I/O pins (C1 to C5) for each channel. On the 40-pin and 32-pin DSLAC devices, only C1 through C4 are available. On the 44-pin version, C5 (one for each channel) is also available and can be used for another function (for example, to control metering signal injection). The outputs are programmed using Command #15 and the status is read back using Command #16. The direction of the pins (input or output) is specified by programming the SLIC I/O direction register (Command #17).

Calculating Filter Coefficients with AmSLAC2 Software

AmSLAC2 software is a program which models the DSLAC device, the line conditions, the SLIC, and the other linecard components to obtain optimal coefficients for the programmable filters of the DSLAC device and some of the resulting transmission performance plots.

The following parameters relating to the desired line conditions and the components/circuits used in the linecard design are to be provided as input to the program:

1. **Line Impedance.** The line impedance or the balance impedance of the line which is usually specified by the local PTT.
2. **Desired Impedance.** This is the desired terminating impedance at the exchange. This impedance is also specified by the local PTT.
3. **SLIC Impedance.** This is the actual terminating impedance at the exchange.

4. **GR-Filter Attenuation**. This is the desired attenuation for the GR filter.
5. **GX-Filter Gain**. This is the desired gain of the GX filter.
6. **Receive Buffer Transfer Function**. It is quite common to use an amplifier and/or filter between the SLIC and the SLAC device in the design of the linecard. The transfer function of this amplifier/filter is called the Receive Buffer Transfer Function.
7. **Transmit Buffer Transfer Function**. Same as the Receive Buffer Transfer Function but for the Transmit path.
8. **Fuse Resistance and Coupling**. This is the value of the Fuse Resistance and the Coupling capacitor used in the linecard.
9. **Two-Wire Return Loss Template**. The Two-Wire Return Loss Template is usually specified by the local PTT.
10. **Four-Wire Return Loss Template**. The Four-Wire Return Loss Template is usually specified by the local PTT.

The output from the AmSLAC2 program includes the coefficients of the GR, GX, Z, R, X, B, and EPG filters as well as predicted transmission performance plots of (1) two-wire return loss, (2) receive and transmit path frequency response, and (3) four-wire return loss.

The software supports the use of the AMD Am795XX series SLICs or a transformer SLIC, or allows entry of the transfer functions describing the behavior of any type of SLIC (hybrid).

Systems for Customer Evaluation

The DSLAC Low Noise Evaluation Board is designed to demonstrate the high performance capabilities of the DSLAC device. The board is used to evaluate the DSLAC device available in a 40-pin DIP package.

The SLAC/DSLAC Computer Interface Board provides a user-friendly, computer-driven interface to control up to two DSLAC Low Noise Evaluation Boards or SLAC Low Noise Boards. The Computer Interface Board allows an IBM-compatible PC to control a SLAC device, DSLAC device, and a SLIC via its serial port. The board is designed to operate with the DSLAC.IF software program which runs on the PC. A block dia-gram of a typical lab setup is shown in Figure 9.

The Computer Interface Board can also interface to a Hewlett-Packard 3779 series PMA or a Wandel and Goltermann (W&G) PCM-4. These PCM Channel Measurement Sets are used to measure the quality of signal transmission through the DSLAC device.

An RS-232C serial port on the SLAC/DSLAC Computer Interface Board is designed to plug directly into a serial port on the back of a PC. The DSLACIF software program which controls the Computer Interface Board will operate on an IBM PC or compatible computer containing at least one serial port and having at least 512 Kb of memory. The program is capable of running from a floppy disk (360 Kb) or from a hard disk. The DSLACIF software program is completely menu driven and features extensive on-line help.

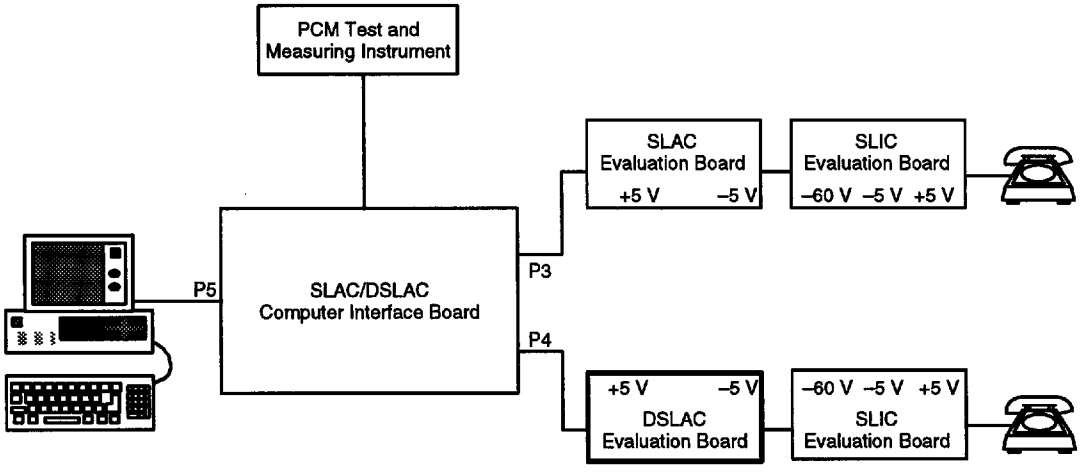


Figure 9. Evaluation System Block Diagram

ABSOLUTE MAXIMUM RATINGS

Storage Temperature ..... $-60°C \le T_A \le +125°C$
Ambient Operating Temperature . $-40°C \le T_A \le +85°C$
Ambient relative humidity
(noncondensing) ..... 5% to 100%
V_{CCA} with respect to AGND ..... −0.4 V to +7.0 V
V_{CCD} with respect to DGND ..... −0.4 V to +7.0 V
V_{CCP} with respect to PGND ..... −0.4 V to +7.0 V
V_{EE} with respect to AGND ..... +0.4 V to −7.0 V
V_{IN} with respect to V_{CCA}
(V_{EE} = −5 V) ..... +0.4 V to −10.0 V
V_{IN} with respect to V_{EE}
(V_{CCA} = +5 V) ..... −0.4 V to +10.0 V
Total combined C1–C5 current per channel
Source from V_{CC} ..... 32 mA
Sink into DGND ..... 24 mA
Latch-up immunity (any pin) ..... ±30 mA
Any other pin with respect to $DGND_1$ .. −0.4 V to V_{CC}

Stresses above those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to absolute maximum ratings for extended periods may affect device reliability.

OPERATING RANGES

Analog Supply V_{CCA1}, V_{CCA2} (V_{CCA}) ..... +5.0 V ±5%
Digital Supply V_{CCD1}, V_{CCD2}, V_{CCP} (V_{CCD}) .. +5.0 V ±5%
Analog Supply V_{EE1}, V_{EE2} ..... −5.0 V ±5%
$DGND_1$, $DGND_2$, PGND (DGND) ..... 0 V
$AGND_1$, $AGND_2$ (AGND) ..... ±50 mV
Ambient Temperature ..... $0°C \le T_A \le +70°C$
Ambient Relative Humidity ..... 15% to 85%

Operating ranges define those limits between which the functionality of the device is guaranteed.

ADV MICRO (TELECOM)

DC CHARACTERISTICS over COMMERCIAL operating range unless otherwise noted

Typical values are for T_A = 25°C and nominal supply voltages. Minimum and maximum specifications are over the temperature and supply voltage ranges shown in Operating Ranges.

Symbol	Parameter Descriptions	Preliminary Min	Typ	Max	Unit
V_{IL}	Input Low Voltage	−0.5		0.8	V
V_{IH}	Input High Voltage	2.0		V_{CC}	V
I_{IL}	Input Leakage Current			±10	µA
V_{OL}	Output Low Voltage				
	C1–C5 (I_{OL} = 6 mA) (Note 2)			0.4	V
	C1–C5 (I_{OL} = 15 mA) (Note 2)			1.0	V
	$\overline{TSCA}$, $\overline{TSCB}$ (I_{OL} = 14 mA)			0.4	V
	Other Digital Outputs (I_{OL} = 2 mA)			0.4	V
V_{OH}	Output High Voltage				
	C1–C5 (I_{OH} = 4 mA) (Note 2)	V_{CC} − 0.4			V
	C1–C5 (I_{OH} = 10 mA) (Note 2)	V_{CC} − 1.0			V
	Other Digital Outputs (I_{OH} = 400 µA)	2.4			V
I_{OL}	Output Leakage Current (H_i = Z State)			±10	µA
V_{IR}	Analog Input Voltage Range (AX = 0 dB)			±3.12	V
	(AX = 6.02 dB)			±1.56	V
V_{IOS}	Offset Voltage Allowed on V_{IN}			±160	mV
I_{IL} (V_{IL})	Input Leakage Current on V_{IN}			±10	µA
Z_{OUT}	V_{OUT} Output Impedance		1	10	ohms
I_{OUT}	V_{OUT} Output Current (f < 3400 Hz) (Note 1)			±6.3	mA

DC CHARACTERISTICS over COMMERCIAL operating range (continued)

Symbol	Parameter Descriptions		Preliminary Min	Typ	Max	Unit
V_{OR}	V_{OUT} Voltage Range	(AR = 0 dB) (AX = 6.02 dB)			±3.12 ±1.56	V V
V_{OOS}	V_{OUT} Offset Voltage (AISN off)				±40	mV
V_{OOSA}	V_{OUT} Offset Voltage (AISN on) (Note 3)				±80	mV
LIN_{AISN}	Linearity of AISN Circuitry (Input = 0 dBm0)				±1/4	LSB
PD	Power Dissipation (MCLK, PCLK = 2.048 MHz)	Both Channels Active 1 Channel Active Both Channels Inactive (Note 4)		180 120 10	240 160 19	mW mW mW
PD	Power Dissipation (MCLK, PCLK > 2.048 MHz)	Both Channels Active 1 Channel Active Both Channels Inactive (Note 4)		190 130 10	270 175 19	mW mW mW
I_{CC}	Total +5-V Current	Both Channels Active 1 Channel Active Both Channels Inactive (Note 4)		24.0 18.0 2.5		mA mA mA
I_{EE}	Total –5-V Current	Both Channels Active 1 Channel Active Both Channels Inactive (Note 4)		10.0 5.0 0.05		mA mA mA
C_I	Input Capacitance (Digital)			15		pF
C_O	Output Capacitance (Digital)			15		pF
PSRR	Power Supply Rejection Ratio (1.02 kHz, 100 mV_{RMS}, either supply or path, GX = GR = 0 dB)		40			dB

Notes: 1. When the DSLAC device is in the inactive mode, the analog output will present a 0-V output level through an ~3K resistor.

2. The C1–C5 outputs are resistive for less than a 1-V drop. Total current must not exceed absolute maximum ratings.

3. If there is an external DC path from V_{OUT} to V_{IN} with a gain of G_{DC} and the AISN has a gain of h_{AISN}, then the output offset will be multiplied by $1/[1-(h_{AISN} \cdot G_{DC})]$.

4. Power Dissipation in the inactive mode is measured with all digital inputs at $V_{ih} = V_{CC}$ and $V_{il} = V_{SS}$ and with no load connected to V_{OUT1} or V_{OUT2}.

Transmission Characteristics

When the gain in the receive path is set at 0 dB, a 1014-Hz PCM sine-wave input with level 0 dBm0 will correspond to a nominal RMS voltage of 1.55 V for μ-law and 1.56 V for A-law at the analog output. When the gain in the transmit path is set at 0 dB, a 1014-Hz sine-wave signal with a nominal RMS voltage of 1.55 V for μ-law and 1.56 V for A-law will correspond to a level of 0 dBm0 at the digital output.

When relative levels (dBm0) are used in any of the following transmission specifications, the specification holds for any setting of the AX + GX gain from 0 to 12 dB and the AR + GR loss from 0 to 12 dB. Performance specification for settings of the AX + GX gain from 12 to 18 dB and the AR + GR loss from 12 to 18 dB will be determined as the device is characterized.

These performance specifications are valid for the commercial temperature range device only. See the DSLAC Extended Temperature Supplement for information on performance over the industrial temperature range (–40°C to +85°C).

Gain Stability

For a 0 dBm0 1014-Hz sine-wave signal, the gains in the transmit and receive paths (with B = 0, Z = 0 & X = R = 1) will not deviate from their ideal value by more than ±0.2 dB at 25°C.

Over the full temperature range (specified in the Operating Ranges), the gains in the transmit and receive paths will not deviate from their ideal values by more than ±0.25 dB.

The variation of the digital to digital loop gain (when the analog input and output ports are connected together) or the analog to analog loop gain (when the digital input and output ports are connected together) will be within ±0.2 dB at 25°C.

Over the full temperature range (specified in the Operating Ranges), the variation of the digital to digital or the analog to analog loop gain will be within ±0.25 dB.

The above specifications apply with reference to temperature and supply voltage variations within the specifications of the Operating Ranges.

Attenuation Distortion

The attenuation of the signal in either path is nominally independent of the frequency. The deviations from nominal attenuation will stay within the limits shown. The reference frequency is 1014 Hz and the signal level is 0 dBm0. The deviation is less than ±0.125 dB for 300 Hz < f < 3000 Hz.

Group Delay Distortion

For either transmission path, the group delay distortion is within the limits shown in Figure 11. The minimum value of the group delay is taken as the reference. The signal level should be 0 dBm0.

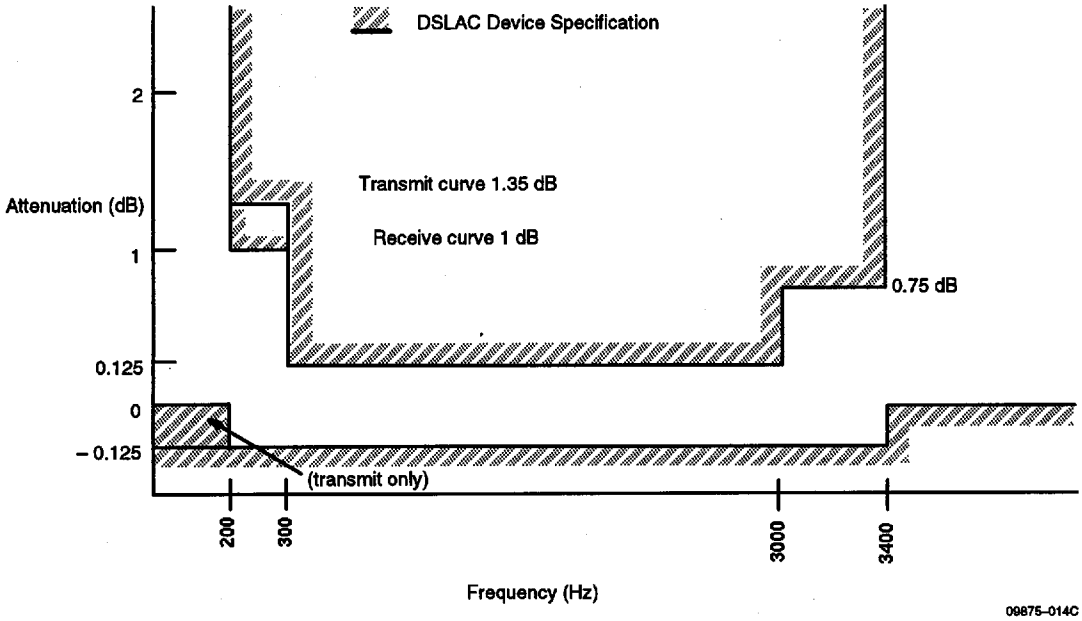


Figure 10. Attenuation Distortion (Single Ended)

Group Delay

The Group Delay specification is defined as the sum of the minimum values of the group delays for the transmit and the receive paths when the transmit and receive time slots are identical and the B, X, R, and Z filters are disabled. For PCLK frequencies greater than 1.53 MHz, the group delay is less than 630 µs. For PCLK frequencies less than 1.03 MHz, the group delay is less than 695 µs. (At PCLK frequencies between these two values, the group delay may vary from one cycle to the next.)

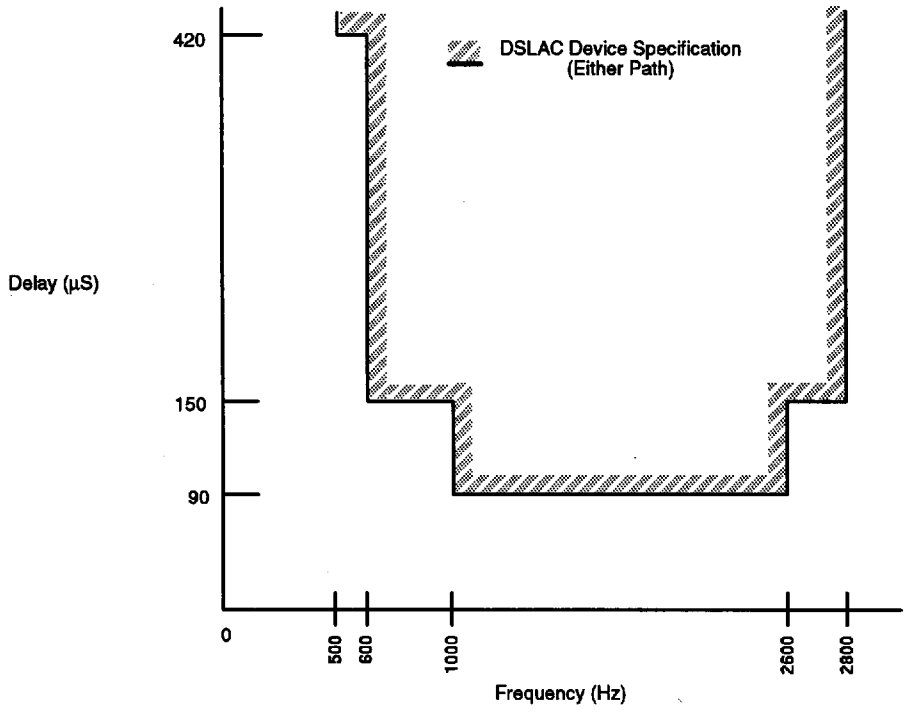


Figure 11. Group Delay Distortion

09875-015C

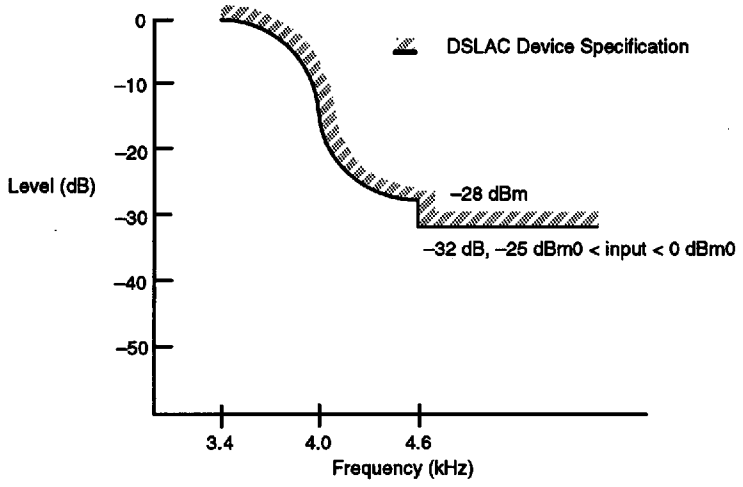
Discrimination Against Out-of-Band Input Signals

When an out-of-band sine-wave signal with frequency f and level A is applied to the analog input, there may be frequency components below 4 kHz at the digital output, caused by the out-of-band signal. These components are at least the specified dB level below the level of a signal at the same output originating from a 1014-Hz sine-wave signal with a level of A dBm0 also applied to the analog input. The minimum specifications are:

Frequency of Out-of-Band Signal	Amplitude of Out-of-Band Signal	Level below A
16.6 Hz <f<45 Hz	–25 dBm0<A≤ 0 dBm0	18 dB
45 Hz <f<65 Hz	–25 dBm0<A≤ 0 dBm0	25 dB
65 Hz <f<100 Hz	–25 dBm0<A≤ 0 dBm0	10 dB
3400 Hz <f<4600 Hz	–25 dBm0<A≤ 0 dBm0	see Figure 12
4600 Hz <f<100 kHz	–25 dBm0<A≤ 0 dBm0	32 dB

The attenuation of the waveform below amplitude A between 3400 Hz and 4600 Hz is given by the formula:

$$\text{Attenuation (dB)} = 14 - 14 \sin \frac{\pi(4000 - f)}{1200}$$



09875–016C

Figure 12. Discrimination Against Out-of-Band Signals

Discrimination Against 12- and 16-kHz Metering Signals

If the DSLAC device is used in a metering application where 12- or 16-kHz tone bursts are injected onto the telephone line toward the subscriber, a portion of those tones may also appear at the V_{IN} input terminal. These out-of-band signals may cause frequency components to appear below 4 kHz at the digital output. For a 12-kHz tone, the frequency components below 4 kHz will be reduced from the input by at least 48 dB, and for 16-kHz tones, the components are reduced by more than 70 dB.

To avoid degradation of in-band transmission performance, the input levels of these out-of-band tones must be limited. The maximum allowable level at 12 kHz is 100 mV rms, and is 500 mV rms at 16 kHz. An external notch filter at the V_{IN} input to the DSLAC device, incorporated along with the metering injection design, is effective in reducing these tone levels.

Spurious Out-of-Band Signals at the Analog Output

With PCM code words representing a sine-wave signal in the range of 300 Hz to 3400 Hz at a level of 0 dBm0 applied to the digital input, the level of the spurious out-of-band signals at the analog output is less than the limits shown below.

Frequency	Level
4.6 kHz to 40 kHz	–32 dBm0
40 kHz to 240 kHz	–46 dBm0
240 kHz to 1 MHz	–36 dBm0

With code words representing any sine-wave signal in the range 3.4 kHz to 4.0 kHz at a level of 0 dBm0 applied to the digital input, the level of the signals at the analog output are below the limits in Figure 13. The amplitude of the Spurious Out-of-Band signals between 3400 Hz and 4600 Hz is given by the formula:

$$A = -14 - 14 \sin \frac{\pi (f - 4000)}{1200} \quad \text{dBm0}$$

Single Frequency Distortion

The output signal level, at any single frequency in the range of 300 Hz to 3400 Hz, other than that due to an applied 0-dBm0 sine-wave signal with frequency f in the same frequency range, is less than –46 dBm0. With f swept between 0 to 300 Hz and 3400 to 12 kHz, any generated output signals other than f are less than –28 dBm0. This specification is valid for either transmission path.

Intermodulation Distortion

Two sine-wave signals of different frequencies f_1 and f_2 (not harmonically related) in the range 300 Hz to 3400 Hz and of equal levels in the range –4 dBm0 to –21 dBm0 do not produce any $2 \cdot f_1 - f_2$ products having a level greater than –42 dB relative to the level of the two input signals.

A sine-wave signal in the frequency band 300 Hz to 3400 Hz with input level –9 dBm0 and a 50-Hz signal with input level –23 dBm0, will not give any intermodulation products exceeding a level of –56 dBm0. These specifications are valid for either transmission path.

Idle Channel Noise

When the signal at the analog input is zero and the digital output (DXA or DXB) is connected to the digital input (DRA or DRB), the maximum levels of the noise measured at the analog output are:

Weighted noise:	–68 dBm0p
Unweighted noise (300–3400 Hz):	–55 dBm0

When the signal at the analog input is zero, the maximum level of the noise measured at the digital output does not exceed –68 dBm0p (A-law) or 19 dBrnc0 (μ-law). When PCM code words representing digital zero are applied to the digital input, the maximum level of the noise measured at the analog output does not exceed –78 dBm0p (A-law) or 12 dBrnc0 (μ-law). No single frequency component in the range above 3800 Hz may exceed a level of –55 dBm0.

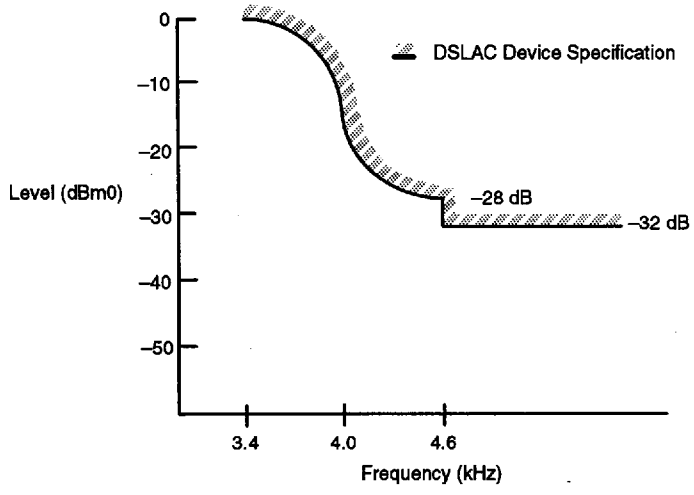


Figure 13. Spurious Out-of-Band Signals

Crosstalk

Transmit to Receive crosstalk within a channel. The crosstalk level at the analog output due to a 0 dBm0 sine-wave signal in the frequency range 300 Hz to 3400 Hz, applied to the analog input, is less than –75 dBm0.

Receive to Transmit crosstalk within a channel. The crosstalk level at the digital output due to a 0 dBm0 sine-wave signal in the frequency range 300 Hz to 3400 Hz, applied to the digital input, is less than –75 dBm0.

Transmit to Transmit crosstalk between channels. With a 0-dBm0 sine-wave signal in the frequency range 300 Hz to 3400 Hz applied to the analog input of one channel, the level at the digital output of the other channel does not exceed –76 dBm0.

Transmit to Receive crosstalk between channels. The crosstalk level at the analog output of one channel due to a 0 dBm0 sine-wave signal in the frequency range 300 Hz to 3400 Hz, applied to the analog input of the other channel, will be less than –78 dBm0.

Receive to Transmit crosstalk between channels. The crosstalk level at the digital output of one channel due to a 0 dBm0 sine-wave signal in the frequency range 300 Hz to 3400 Hz, applied to the digital input of the other channel, will be less than –76 dBm0.

Receive to Receive crosstalk between channels. The crosstalk level at the analog output of one channel due to a 0 dBm0 sine-wave signal in the frequency range 300 Hz to 3400 Hz, applied to the digital input of the other channel, will be less than –78 dBm0.

Variation of Gain with Input Level

The gain deviation relative to the gain at –10 dBm0 is within the limits shown in Figure 14 for either transmission path when the input signal is a noise signal (for example, CCITT Rec. O.131).

The gain deviation relative to the gain at –10 dBm0 is within the limits shown in Figure 15 for either transmission path when the input is a sine-wave signal of frequency 1014 Hz.

Total Distortion, Including Quantizing Distortion

The signal-to-total distortion ratio will exceed the limits shown in Figure 16 for the receive path when the input signal is a noise signal (for example, CCITT Rec. O.131). The transmit path specification is 1 dB less than that shown for the receive path.

The signal-to-total distortion will exceed the limits shown in Figure 17 for either transmission path when the input is a sine-wave signal of frequency 1014 Hz.

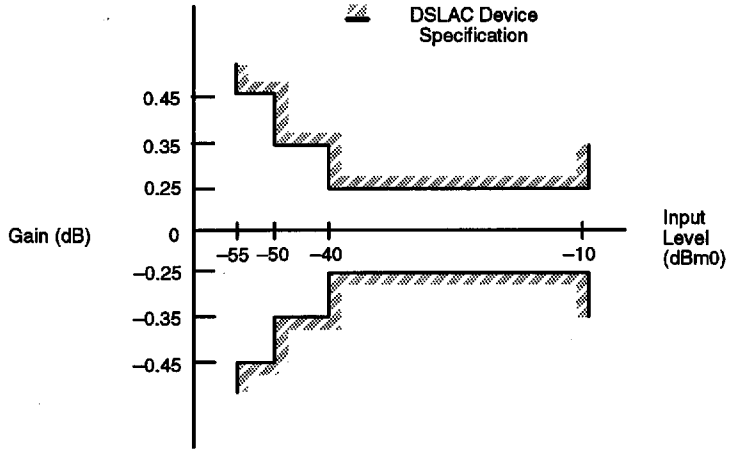


Figure 14. Gain Tracking with Noise Input

09875-018C

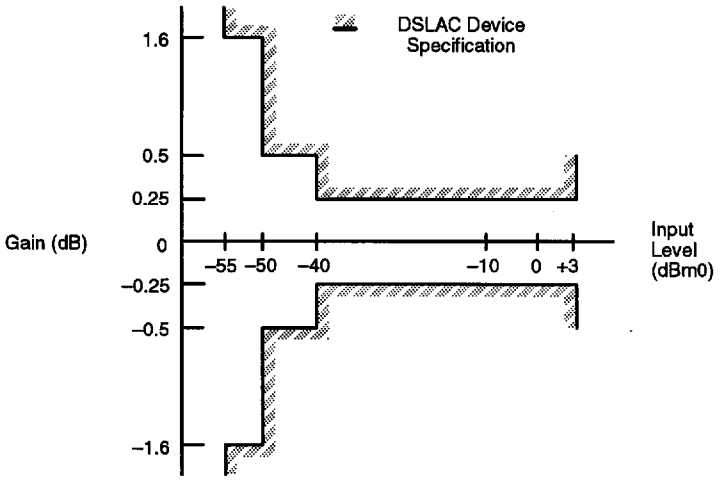


Figure 15. Gain Tracking with Tone Input

09875–019C

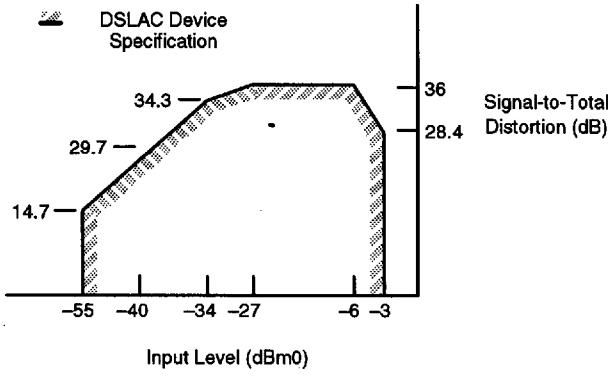


Figure 16. Total Distortion with Noise Input (Receive Path)

09875–020C

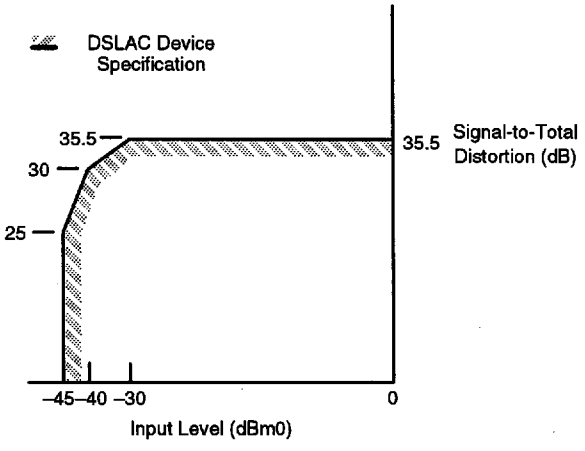


Figure 17. Total Distortion with Tone Input (Both Paths)

09875–021C

Overload Compression

Figure 18 shows the acceptable region of operation for input signal levels above the reference input power (0 dBm0). The conditions for this figure are: (1) 1 dB < GX ≤ 12 dB; (2) −12 dB ≤ GR < −1 dB; (3) PCM output connected to PCM input; and (4) measurement analog-to-analog.

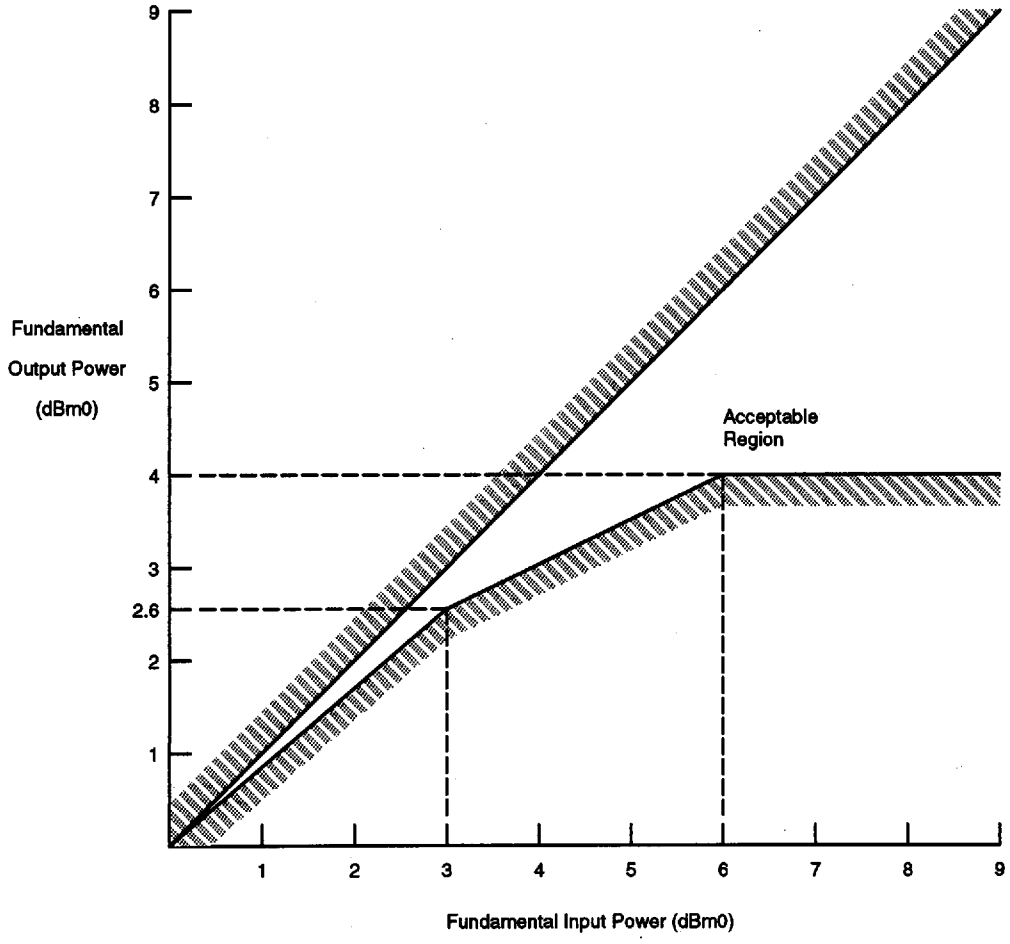


Figure 18. A/A Overload Compression

SWITCHING CHARACTERISTICS over operating range (unless otherwise noted)

Microprocessor Interface

Min and Max values are valid for all digital outputs with a 150-pF load, except C1 to C5 with a 30 pF load. Pull-up resistors of 360 ohms are attached to $\overline{TSCA}$ and $\overline{TSCB}$.

No.	Symbol	Parameter	Preliminary Min	Typ	Max	Units
1	t_{DCY}	Data Clock Period	244			ns
2	t_{DCH}	Data Clock High Pulse Width (Note 1)	97			ns
3	t_{DCL}	Data Clock Low Pulse Width (Note 1)	97			ns
4	t_{DCR}	Rise Time of Clock			25	ns
5	t_{DCF}	Fall Time of Clock			25	ns
6	t_{ICSS}	Chip Select Setup Time, Input Mode	70		$t_{DCY}-10$	ns
7	t_{ICSH}	Chip Select Hold Time, Input Mode	0		$t_{DCH}-20$	ns
8	t_{ICSL}	Chip Select Pulse Width, Input Mode		$8t_{DCY}$		ns
9	t_{ICSO}	Chip Select Off Time, Input Mode (Note 7)		5		µs
10	t_{IDS}	Input Data Setup Time	30			ns
11	t_{IDH}	Input Data Hold Time	30			ns
12	t_{OLH}	SLIC Output Latch Valid	20		1000	ns
13	t_{OCSS}	Chip Select Setup Time, Output Mode	70		$t_{DCY}-10$	ns
14	t_{OCSH}	Chip Select Hold Time, Output Mode	0		$t_{DCH}-20$	ns
15	t_{OCSL}	Chip Select Pulse Width, Output Mode		$8t_{DCY}$		ns
16	t_{OCSO}	Chip Select Off Time, Output Mode (Note 7)		5		µs
17	t_{ODD}	Output Data Turn On Delay (Note 5)			50	ns
18	t_{ODH}	Output Data Hold Time	0			ns
19	t_{ODOF}	Output Data Turn Off Delay			50	ns
20	t_{ODC}	Output Data Valid	0		50	ns

PCM Interface

ADV MICRO (TELECOM)

No.	Symbol	Parameter	Preliminary Min	Typ	Max	Units
21	t_{PCY}	PCM Clock Period (Note 2)	0.122		7.8125	µs
22	t_{PCH}	PCM Clock High Pulse Width	48		3890	ns
23	t_{PCL}	PCM Clock Low Pulse Width	48		3890	ns
24	t_{PCF}	Fall Time of Clock			15	ns
25	t_{PCR}	Rise Time of Clock			15	ns
26	t_{FSS}	FS Setup Time	25		$t_{PCY}-50$	ns
27	t_{FSH}	FS Hold Time	50			ns
28	t_{TSD}	Delay to $\overline{TSC}$ Valid (with Programmable Delay) (Note 3)	5 30		80 150	ns ns
29	t_{TSO}	Delay to $\overline{TSC}$ Off (with Programmable Delay) (Note 6)	5 30		80 150	ns ns
30	t_{DXD}	PCM Data Output Delay (with Programmable Delay) (Note 4)	3 30		80 150	ns ns
31	t_{DXH}	PCM Data Output Hold Time (with Programmable Delay) (Note 4)	5 30		80 150	ns ns
32	t_{DXZ}	PCM Data Output Delay to High-Z (with Programmable Delay) (Note 4)	5 30		80 150	ns ns
33	t_{DRS}	PCM Data Input Setup Time	25		70	ns
34	t_{DRH}	PCM Data Input Hold Time	5		150	ns

Master Clock

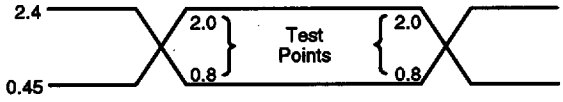
For 2.048 MHz ±100 ppm or 4.096 MHz ±100 ppm operation:

No.	Symbol	Parameter	Preliminary Min	Typ	Max	Units
35	t_{MCY}	Master Clock Period (2.048 MHz)	488.23	488.28	488.33	ns
		Master Clock Period (4.096 MHz)	244.11	244.14	244.17	ns
36	t_{MCR}	Rise Time of Clock		15		ns
37	t_{MCF}	Fall Time of Clock			15	ns
38	t_{MCH}	MCLK High Pulse Width (2.048 MHz)	200			ns
		MCLK High Pulse Width (4.096 MHz)	80			ns
39	t_{MCL}	MCLK Low Pulse Width (2.048 MHz)	200			ns
		MCLK Low Pulse Width (4.096 MHz)	80			ns

Notes
1. DCLK may be stopped in the High or Low state indefinitely without loss of information. If DCLK is stopped in the High state, $\overline{CS}$ can subsequently make any number of transitions without activating the Microprocessor Interface logic.
2. The PCM clock frequency must be an integer multiple of the frame sync frequency with a long term accuracy of 100 ppm. The maximum allowed PCM clock frequency is 8.192 MHz. The actual PCM clock rate is dependent on the number of channels allocated within a frame. The minimum clock frequency is 128 kHz. A PCLK of 1.544 MHz may easily be used for standard U.S. transmission systems.
3. $\overline{TSC}$ is delayed from FS by a typical value of N • t_{PCY}, where N is the value stored in the time/clock-slot register.
4. There is a special conflict detection circuitry which will prevent high-power dissipation from occurring when the DXA or DXB pins of two DSLAC devices are tied together and one DSLAC device starts to transmit before the other has gone into a high-impedance state.
5. The first data bit is enabled on the falling edge of $\overline{CS}$ or on the falling edge of DCLK, whichever occurs last.
6. t_{TSD} is defined as the time at which the output achieves the open circuit condition.
7. The DSLAC device requires 40 cycles of the 8-MHz internal clock (5 µs) between SIO operations. If the MPI is being accessed while the MCLK input is not active, a Chip Select Off time of 20 µs is required.

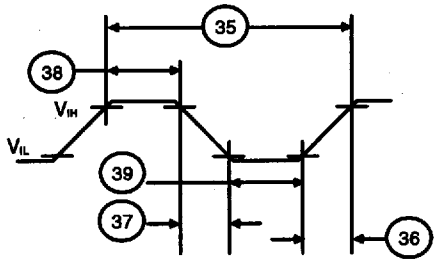
SWITCHING WAVEFORMS

Input and Output Waveforms for AC Tests



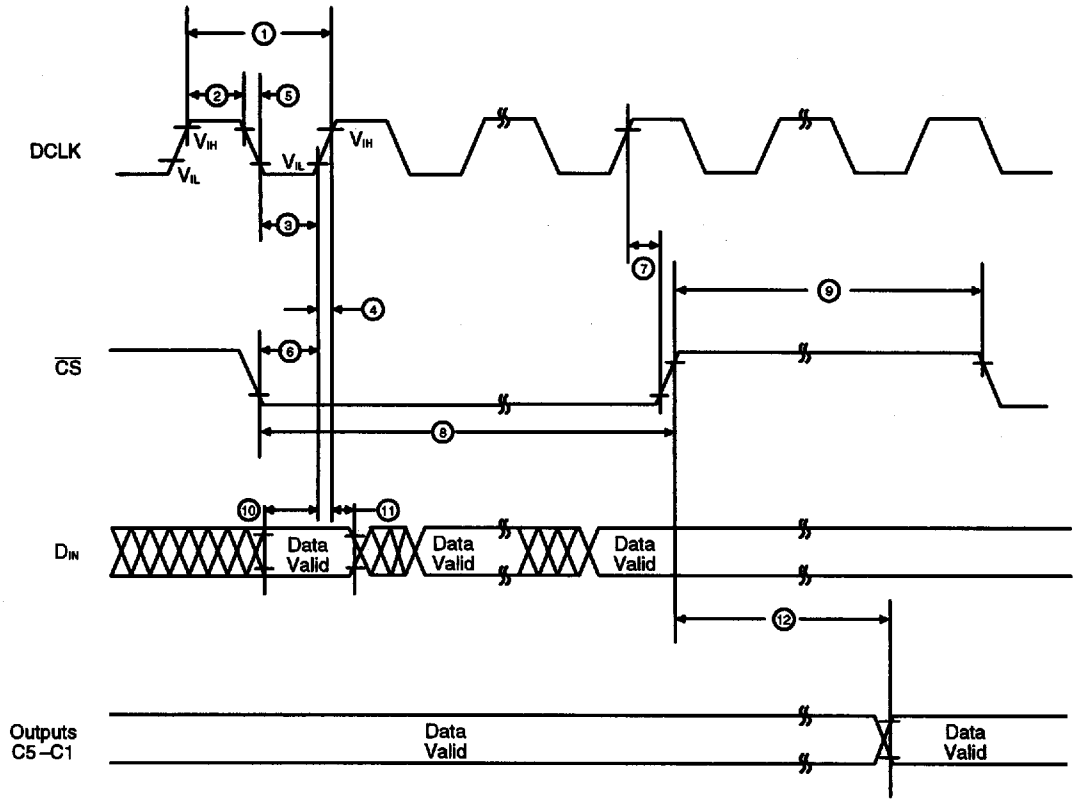
09875-023C

Master Clock Timing



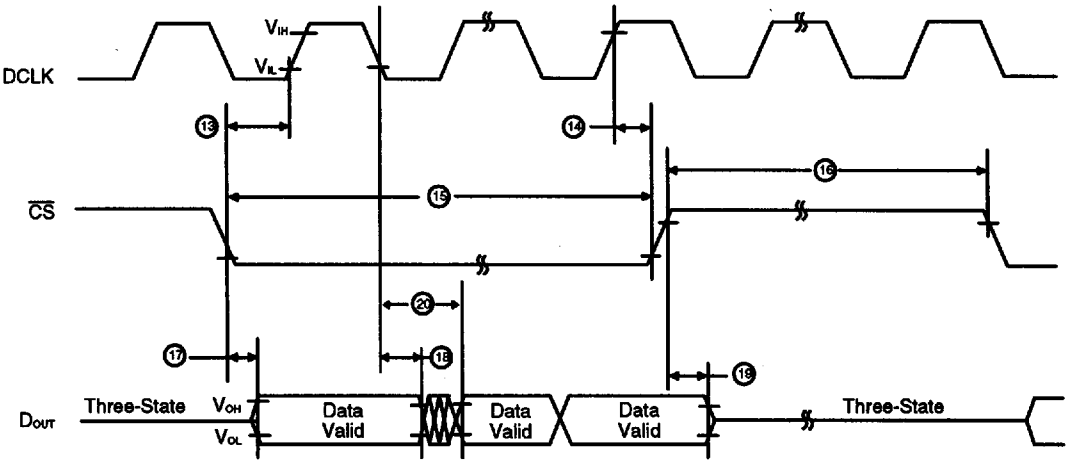
09875-024C

Microprocessor Interface (Input Mode)



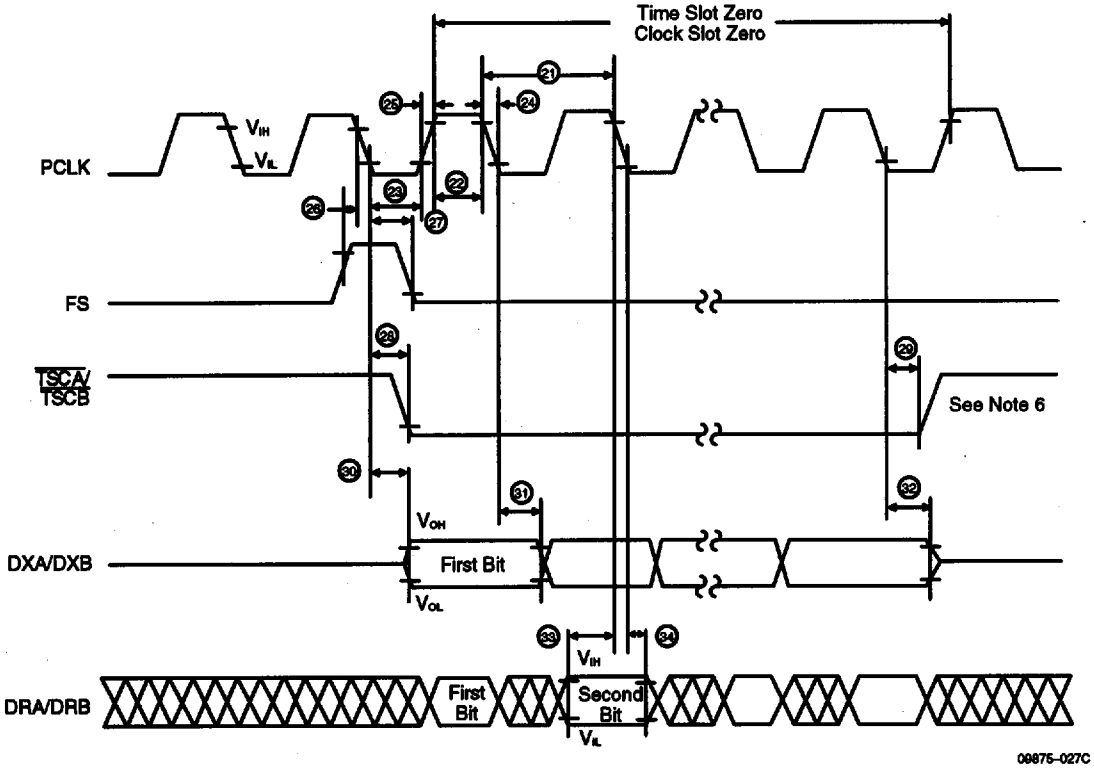
09675-025C

Microprocessor Interface (Output Mode)



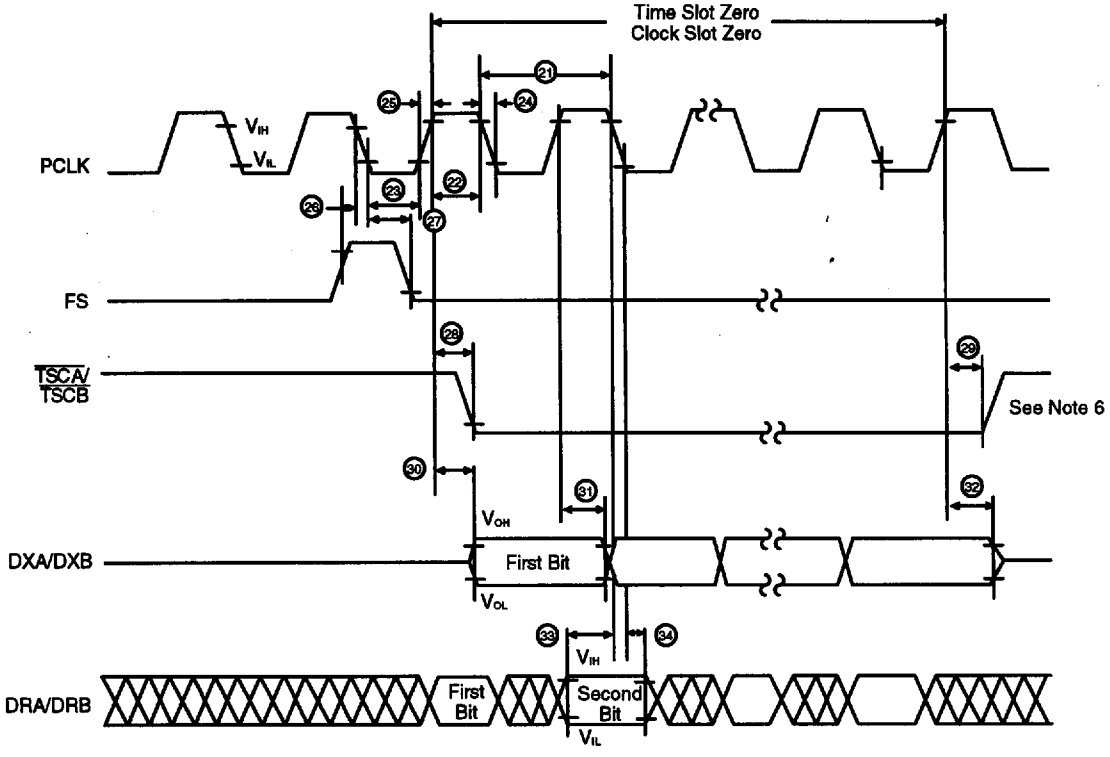
09675-026C

PCM Highway Timing for XE=0 (Transmit on Negative PCLK Edge)



ADV MICRO (TELECOM)

PCM Highway Timing for XE = 1 (Transmit on Positive PCLK Edge)



Note: In this mode, the PCM transmit timing is compatible with other CODEC IC's.

09875–027C

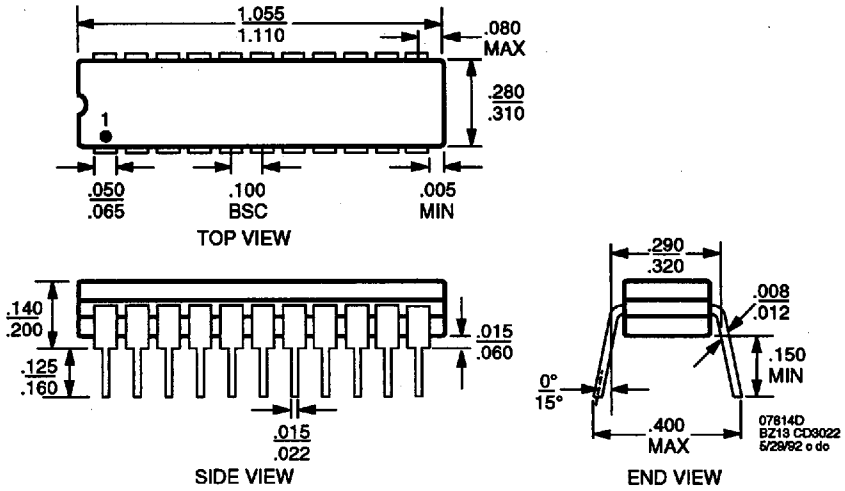
ADV MICRO (TELECOM)

PHYSICAL DIMENSIONS

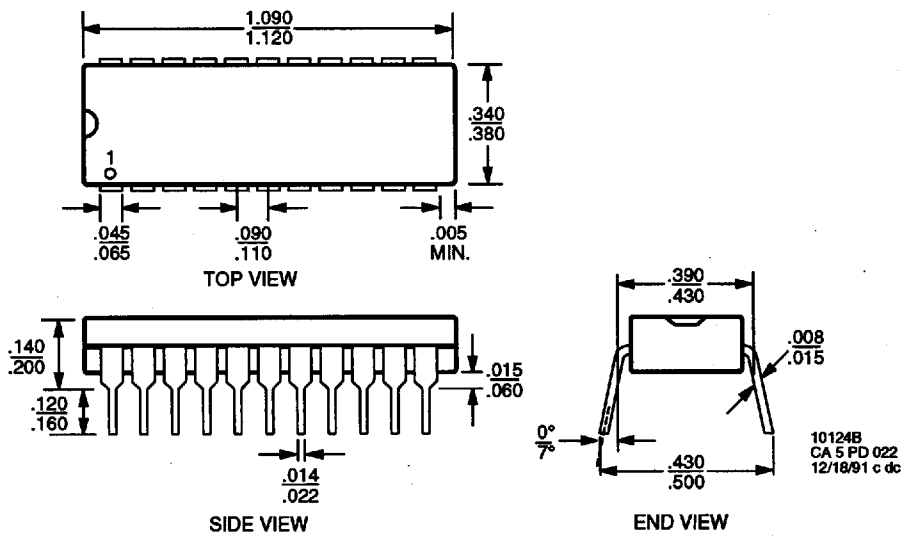
Preliminary; package in development. BSC is an ANSI standard for Basic Space Centering. Dimensions are measured in inches or millimeters.

T-90-20

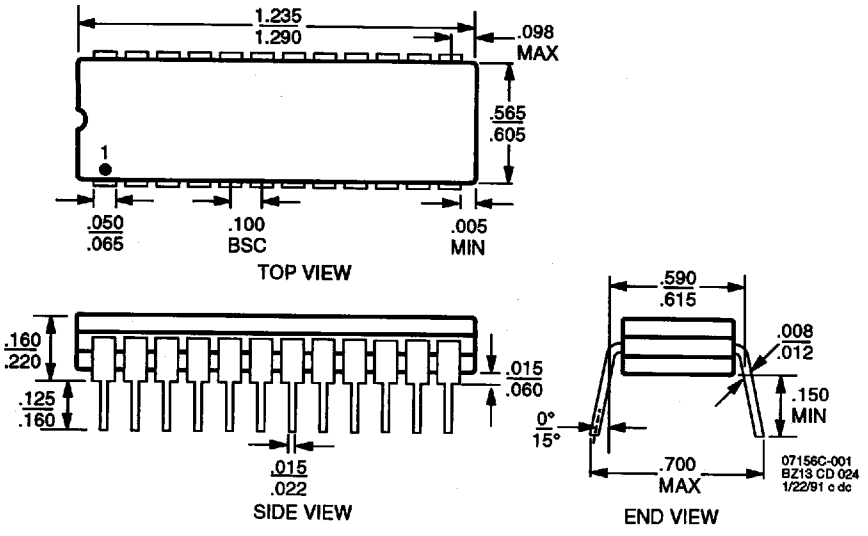
CD022



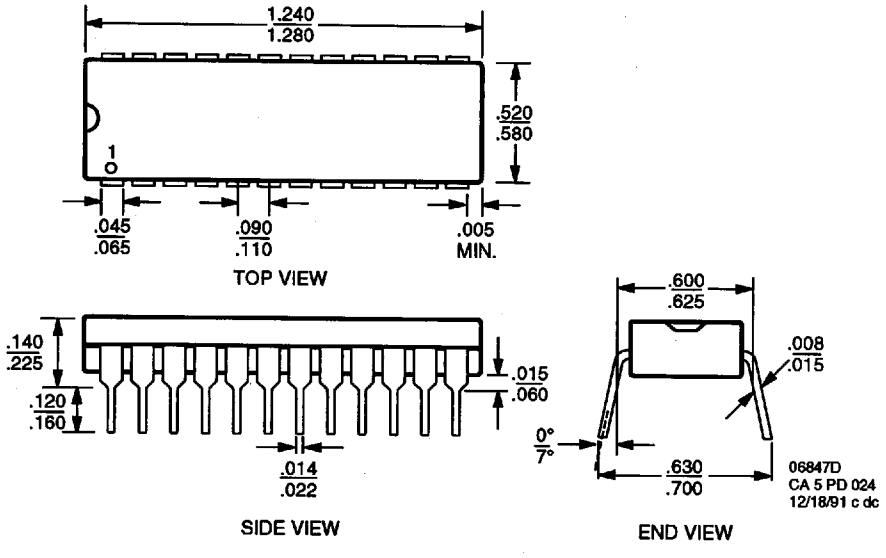
PD022



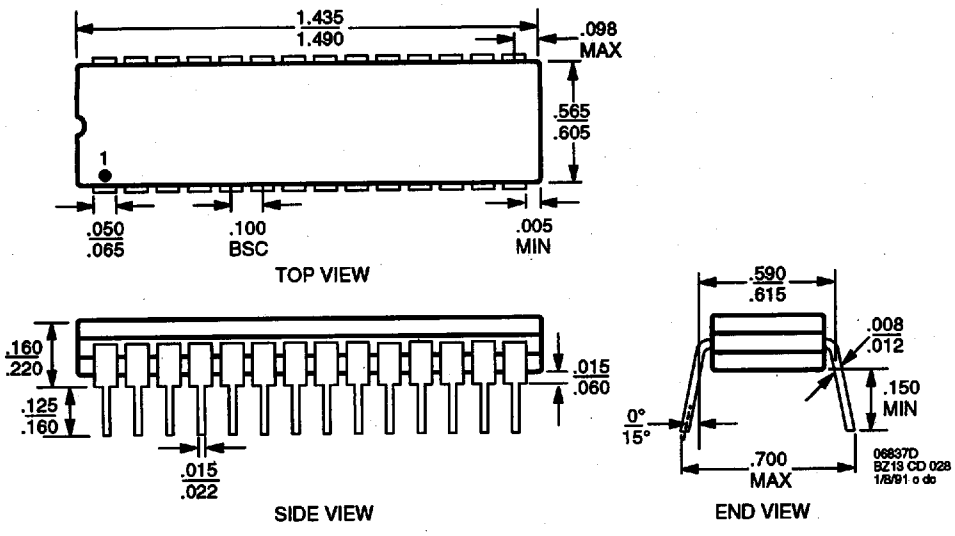
CD024



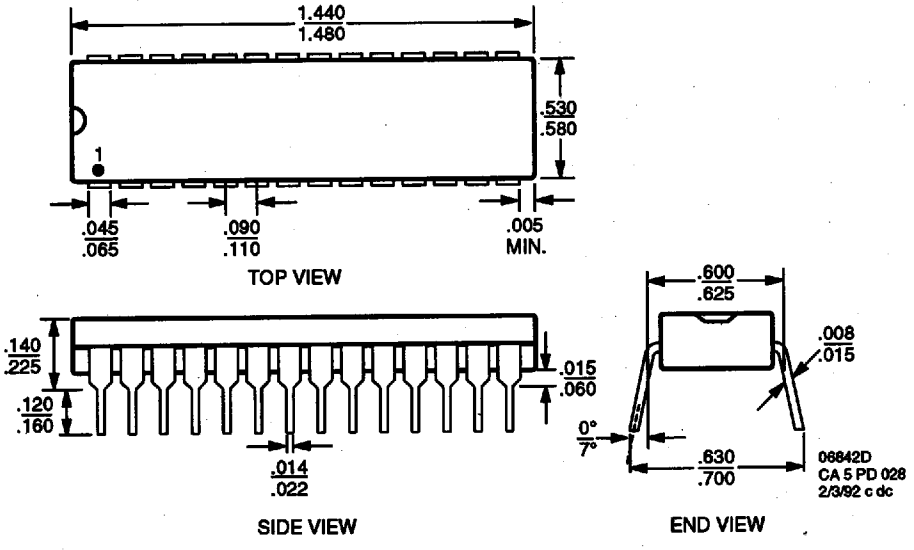
PD024



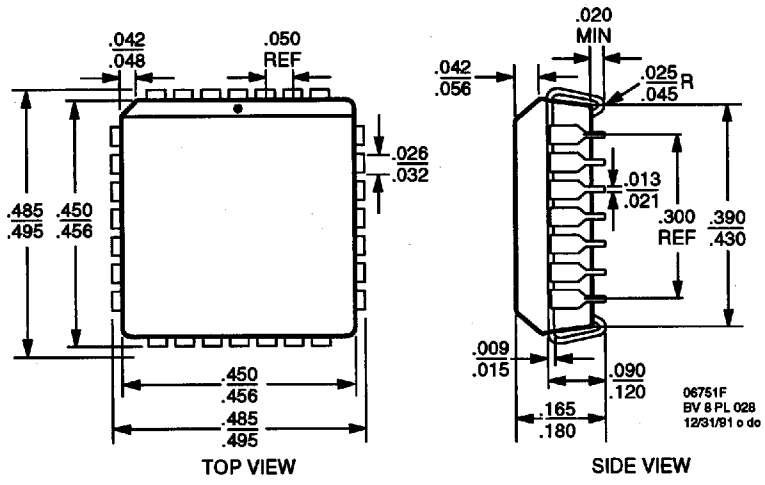
CD028



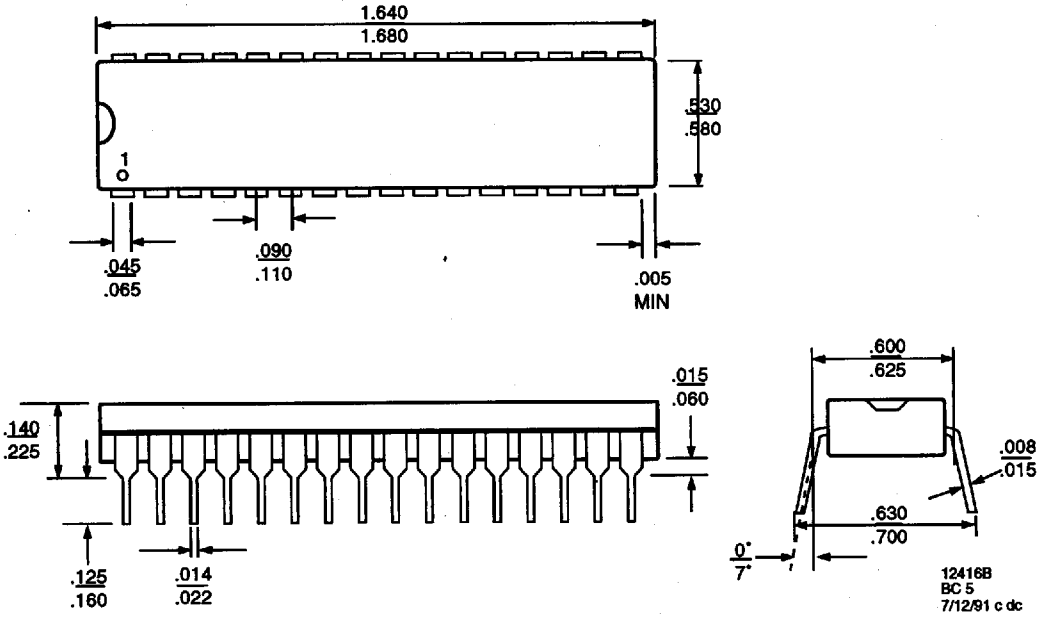
PD028



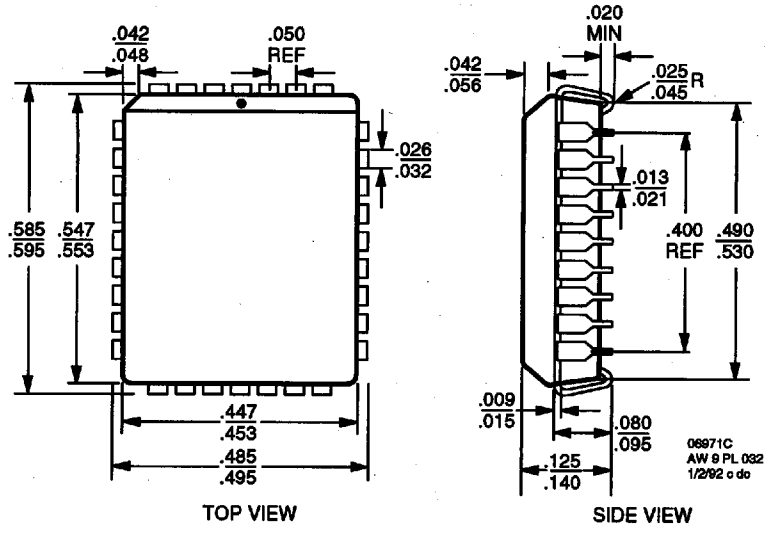
PL028



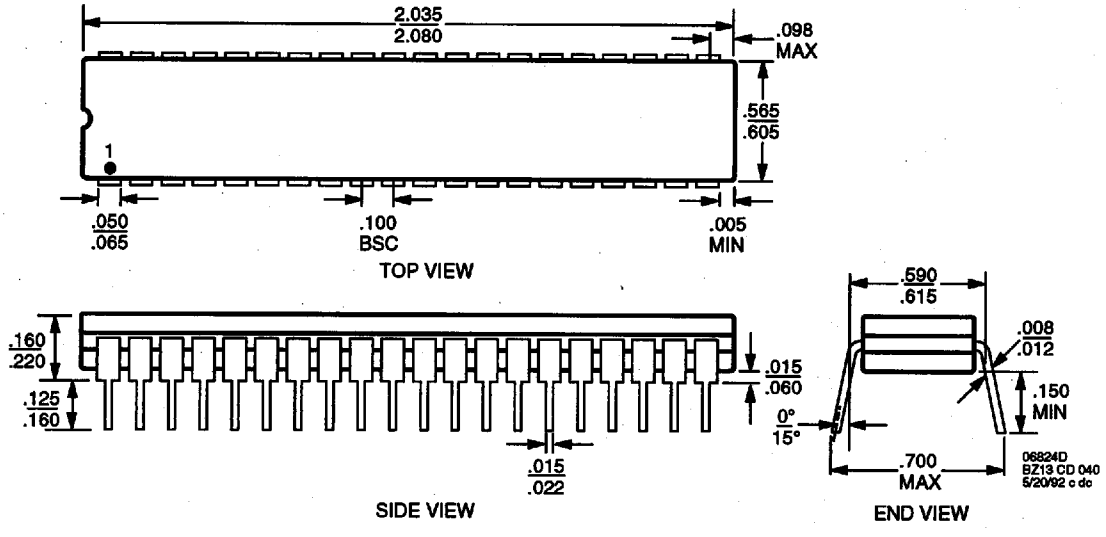
PD 032



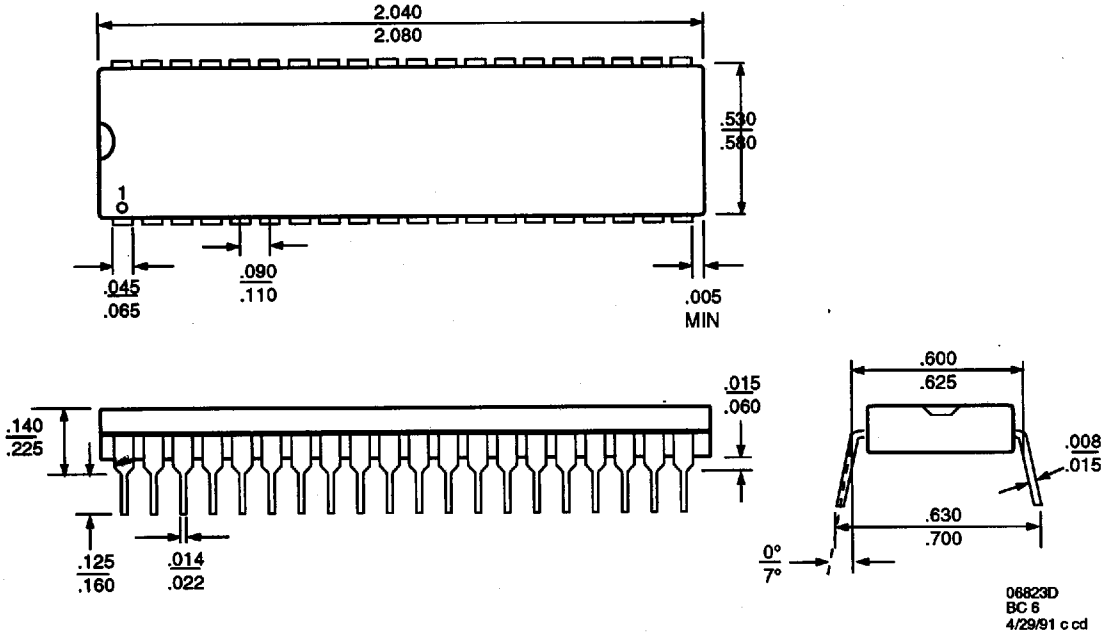
PL032



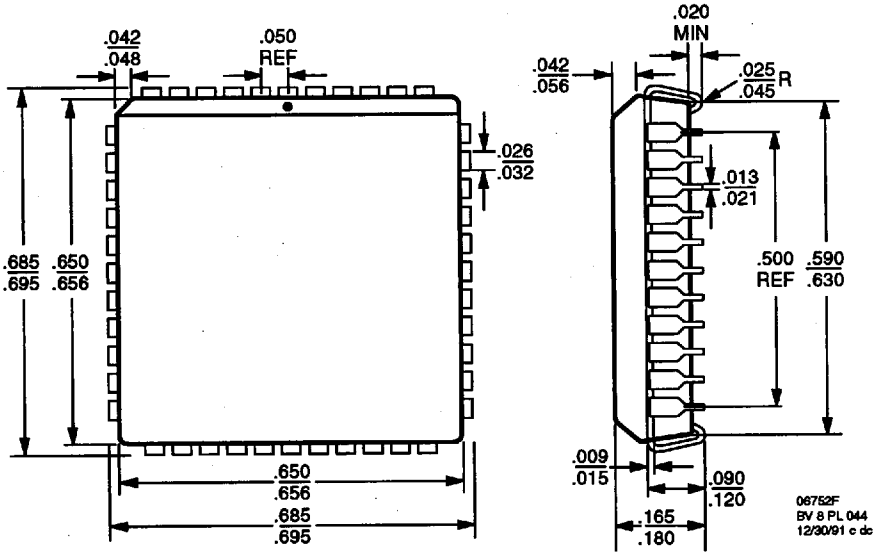
CD040



PD 040



PL044



12556B 7/92