FINAL

Am79C02/03/031(A)

Dual Subscriber Line Audio ProcessingCircuit (DSLAC™) Devices

TABLE OF CONTENTS

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LIST OF FIGURES

LIST OF TABLES

DISTINCTIVE CHARACTERISTICS

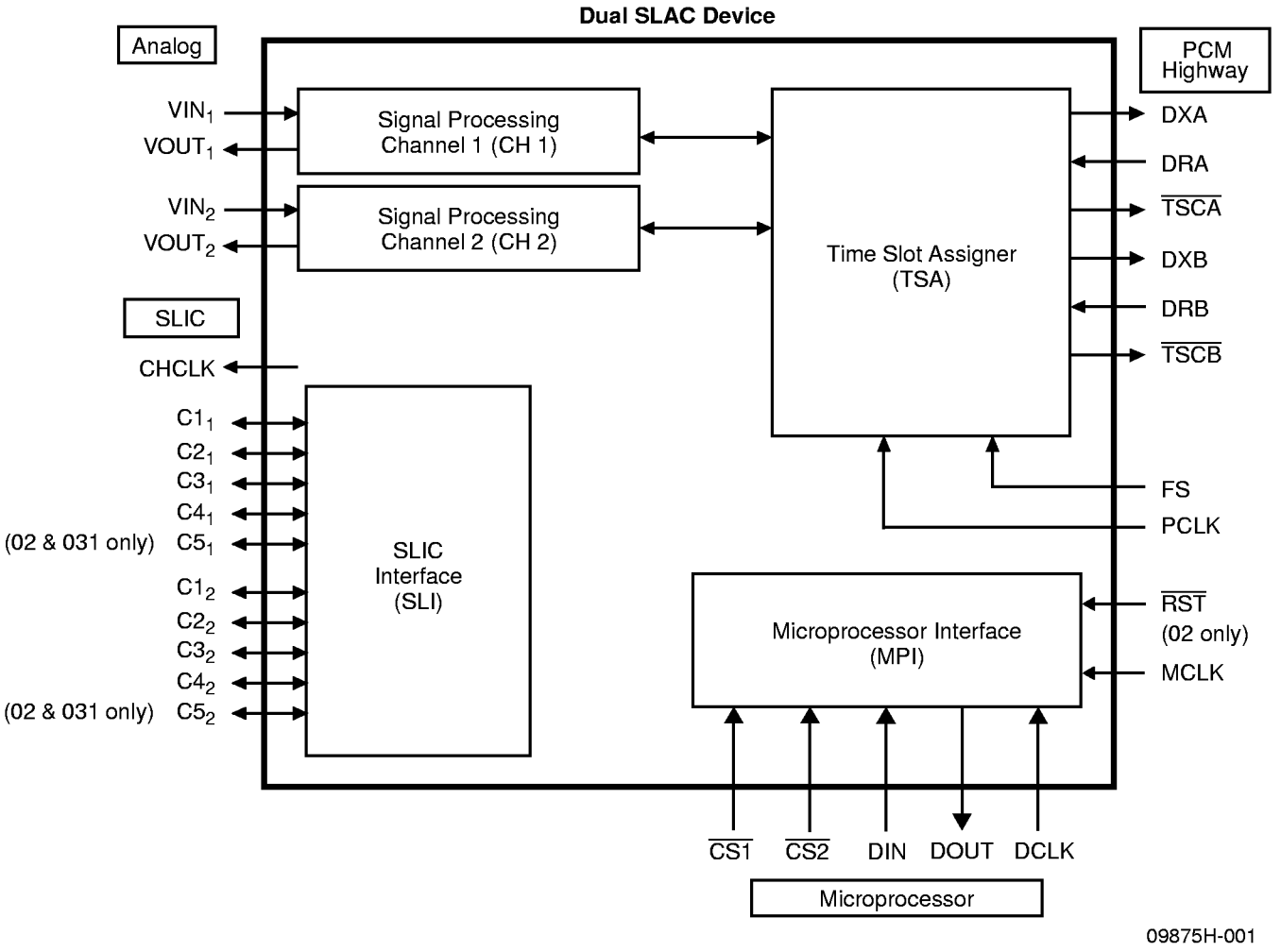
- **Software programmable:**
  - — SLIC impedance
  - — Transhybrid balance
  - — Transmit and receive gains
  - — Equalization
  - — Digital I/O pins
  - — Time Slot Assigner
  - — PCM transmit clock edge options
- **Adaptive transhybrid balance filter (A suffix only)**
- **A-law or µ-law coding**
- **Dual PCM ports**
  - — Up to 8.192 MHz each (128 channels per port)
- **2.048 MHz or 4.096 MHz master clock**
- **Direct transformer drive**
- **Built-in test modes**
- **Low power CMOS**
- ***Mixed mode* (analog and digital) impedance scaling**
- **Performance characteristics guaranteed over 12 dB gain range**

GENERAL DESCRIPTION

The Am79C02/03/031(A) Dual Subscriber Line Audio Processing Circuit (DSLAC device) integrates the key functions of an analog linecard into a single high-performance, programmable dual codec/filter device. The DSLAC device is based on the proven design of the reliable Am7901A Subscriber Line Audio Processing Circuit (SLAC device). The advanced architecture of the DSLAC device implements two independent channels and employs digital filters to allow software control of transmission, thus providing a cost effective solution for the analog to PCM function of a linecard.

The Am79C02/03/031(A) DSLAC device's advanced CMOS technology makes this an economical device that has both the functionality and the low power consumption needed in linecard designs to maximize linecard density at minimum cost. When used with two AMD SLICs, the DSLAC device provides software configurable solutions to the BORSCHT function.

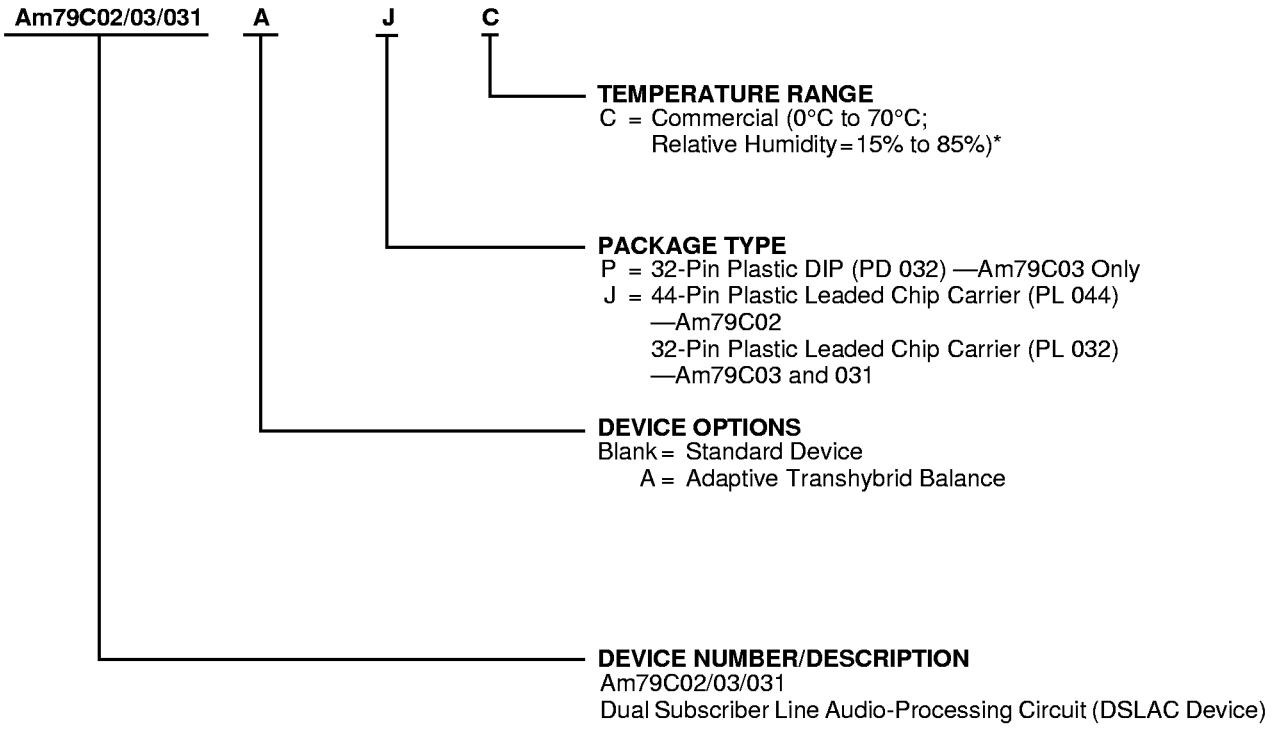
BLOCK DIAGRAM



ORDERING INFORMATION

Standard Products

AMD standard products are available in several packages and operating ranges. The order number (Valid Combination) is formed by a combination of the elements below.



Valid Combinations	
Am79C02	AJC, JC
Am79C03	AJC, APC, PC, JC
Am79C031	AJC, JC

Valid Combinations

Valid Combinations list configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations, to check on newly released combinations, and to obtain additional data on AMD's standard military grade products.

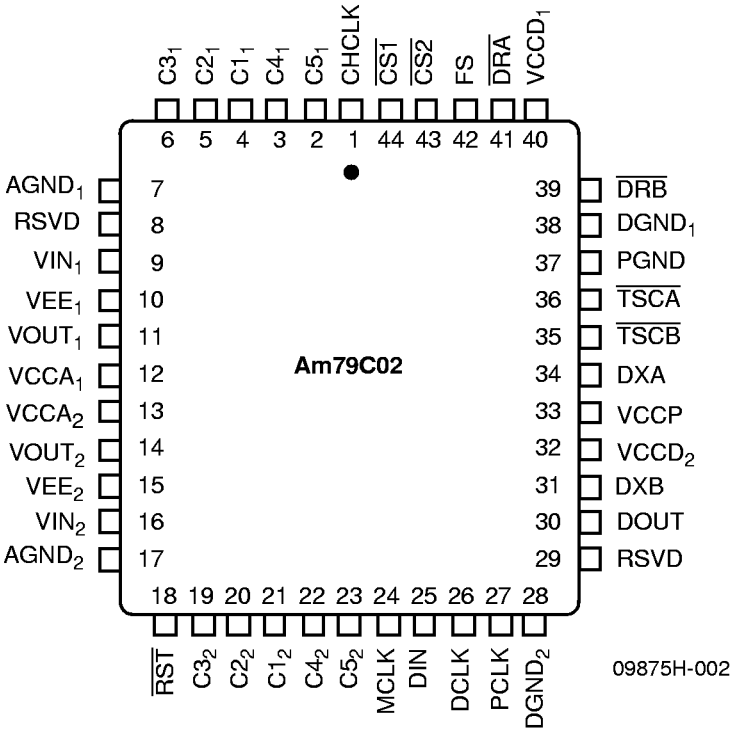
Note:

** Functionality of the device from 0°C to +70°C is guaranteed by production testing. Performance from –40°C to +85°C is guaranteed by characterization and periodic sampling of production units.*

CONNECTION DIAGRAMS

Top View

44-Pin PLCC



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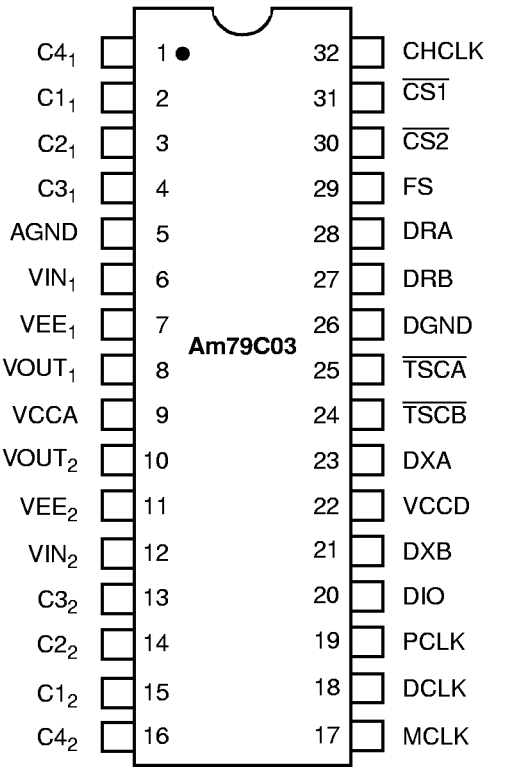
32-Pin DIP



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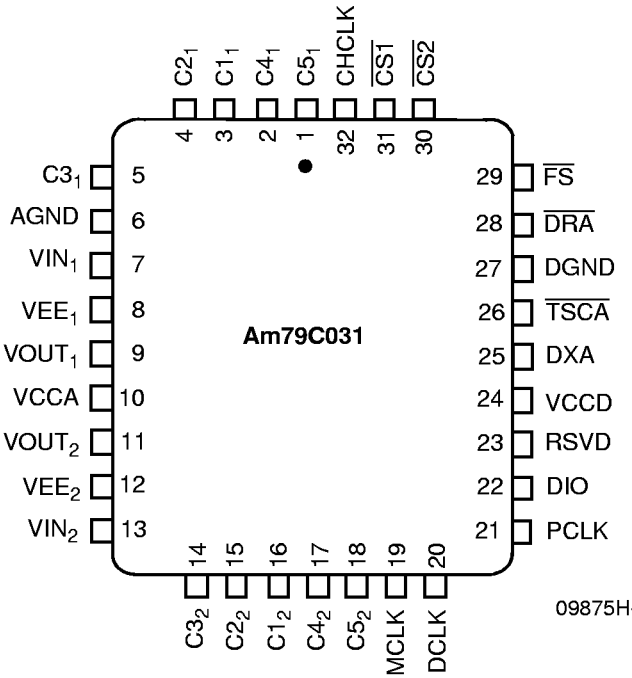
32-Pin PLCC



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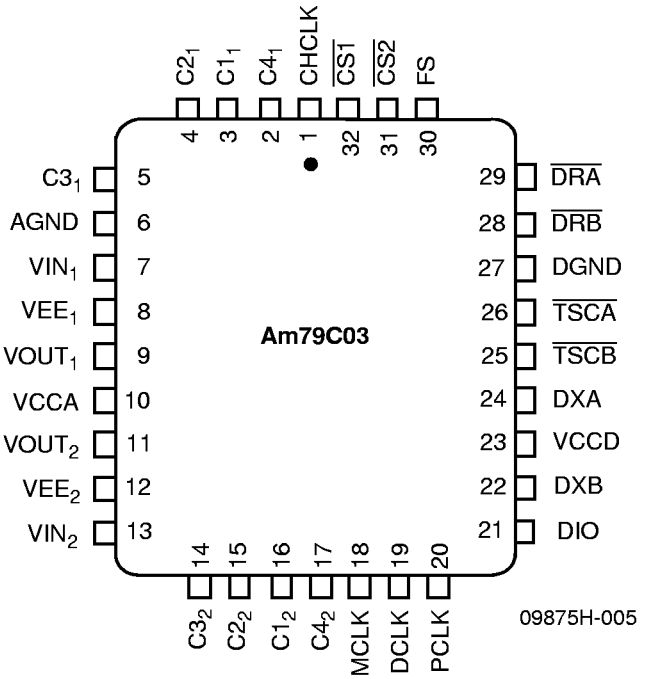
32-Pin PLCC



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Notes:

1. *Pin 1 is marked for orientation.*
2. *RSVD = Reserved pin; should not be connected externally to any signal or supply.*

PIN DESCRIPTIONS

$C1_1$–$C5_1$, $C1_2$–$C5_2$

Control Inputs/Outputs

The five SLIC control lines per channel are TTL compatible and bidirectional. They can be used to monitor or control the operation of a SLIC or any other device associated with the subscriber line. Lines C11–C51 are associated with Channel 1, and lines C12–C52 are associated with Channel 2. The C51 and C52 lines are available on the Am79C02(A) and Am79C031(A). C51 and C52 are output only on the Am79C031(A) and must be programmed as outputs.

CHCLK

SLIC Clock Output

This output provides a 256 kHz or 293 kHz, 50% duty cycle, TTL compatible clock for use by two SLICs. The CHCLK frequency is derived from MCLK and the phase relationship to MCLK is random. CHCLK is capable of driving two TTL inputs.

$\overline{CS2}$–$\overline{CS1}$

Chip Select Inputs

The Chip Select inputs (active Low) enable the device to read or write control data. $\overline{CS1}$ is for the Channel 1 microprocessor interface and $\overline{CS2}$ is for the Channel 2 microprocessor interface.

DCLK

Data Clock Input

The Data Clock input shifts data into and out of the microprocessor interface of the DSLAC device. The maximum clock rate is 4.096 MHz.

DIN

Data Input

Control data is serially written into the Am79C02(A) DSLAC device via the DIN pin with the most significant bit first. The Data Clock determines the data rate. DIN and DOUT may be strapped together to reduce the number of connections to the microprocessor.

DIO

Data Input/Output

Control data is serially written into and read out of the Am79C03(A) and Am79C031(A) DSLAC device via the DIO pin with the most significant bit first. The Data Clock determines the data rate. DIO is high impedance except when data is being transmitted from these DSLAC devices under control of $\overline{CS1}$ or $\overline{CS2}$. DIO replaces DIN and DOUT as found on the Am79C02(A).

DOUT

Data Output

Control data is serially read out of the Am79C02(A) DSLAC device via the DOUT pin with the most significant bit first. The Data Clock determines the data rate. DOUT is high impedance except when data is being transmitted from the DSLAC device under control of $\overline{CS1}$ or $\overline{CS2}$. DIN and DOUT may be strapped together to reduce the number of connections to the microprocessor.

DRA, DRB

PCM Inputs

The PCM data for Channels 1 and 2 is serially received on either the DRA or the DRB port during user programmed time slots. Eight bits are received with the most significant bit first. Data for each channel is received in 8-bit bursts every 125 µs at the PCLK rate.

DXA, DXB

PCM Outputs

The Transmit PCM data from Channels 1 and 2 is sent serially through either the DXA or DXB port during user programmed time slots. Eight bits are transmitted with the most significant bit first. The output is available every 125 µs and the data is shifted out in 8-bit bursts at the PCLK rate. DXA and DXB are high impedance between bursts and while the device is in the Inactive mode. DXB is not available on the 79C031(A).

FS

Frame Sync Input

The Frame Sync pulse is an 8 kHz signal that identifies the beginning of a system's PCM frame. The DSLAC device references individual time slots with respect to this input, which must be synchronized to PCLK.

MCLK

Master Clock Input

The Master Clock must be a 2.048 MHz or 4.096 MHz clock input for use by the digital signal processor. MCLK may be asynchronous to PCLK.

PCLK

PCM Clock Input

The PCM clock determines the rate at which PCM data is serially shifted into or out of the PCM ports. PCLK is an integer multiple of the frame sync frequency. The maximum clock frequency is 8.192 MHz and the minimum clock frequency is 128 kHz. The PCLK clock may be asynchronous to MCLK.

RST

Reset Input

A logic Low signal to this pin resets the DSLAC device to its default state. (Am79C02(A) only.)

$\overline{TSCA}$, $\overline{TSCB}$

Time Slot Control Outputs

The Time Slot Control outputs are open drain (requiring pull-up resistors) and are normally inactive (high impedance). $\overline{TSCA}$ is active (Low) when PCM data is output on the DXA pin and $\overline{TSCB}$ is active (Low) when PCM data is output on the DXB pin. ($\overline{TSCB}$ is available on the Am79C02 and Am79C03 only.)

VIN_1, VIN_2

Analog Inputs

The analog input is applied to the transmit path of the DSLAC device. The signal is sampled, digitally processed, and encoded for the PCM output. VIN_1 is the input for Channel 1 and VIN_2 is the input for Channel 2.

$VOUT_1$, $VOUT_2$

Analog Outputs

The received PCM data is digitally processed and converted to an analog signal at the VOUT pin. $VOUT_1$ is the output from Channel 1 and $VOUT_2$ is the output for Channel 2. These outputs can directly drive a transformer SLIC.

Power supply for the Am79C02:

$AGND_1$	Analog Ground (Channel 1)
$AGND_2$	Analog Ground (Channel 2)
$DGND_1$	Digital Ground (Channel 1)
$DGND_2$	Digital Ground (Channel 2)
PGND	PCM I/O Ground
$VCCA_1$	+5 V Analog Power Supply (Channel 1)
$VCCA_2$	+5 V Analog Power Supply (Channel 2)
$VCCD_1$	+5 V Digital Power Supply
	Internally connected to substrate
$VCCD_2$	+5 V Digital Power Supply
	Internally connected to substrate
VCCP	+5 V PCM I/O Power Supply
	Internally connected to substrate
VEE_1	–5 V Power Supply (Channel 1)
VEE_2	–5 V Power Supply (Channel 2)

Power supply for the Am79C03 and Am79C031:

AGND	Analog Ground
DGND	Digital Ground
VCCA	+5 V Analog Power Supply
VCCD	+5 V Digital Power Supply
	Internally connected to substrate
VEE_1	–5 V Power Supply (Channel 1)
VEE_2	–5 V Power Supply (Channel 2)

The many separate power supply inputs are intended to provide for good power supply decoupling techniques. Note that all of the +5 V inputs should be connected to the same source, all of the ground inputs should be connected to the same source, and both of the –5 V inputs should be connected to the same source.

FUNCTIONAL DESCRIPTION

The DSLAC device performs the codec/filter functions associated with the four-wire section of the subscriber line circuitry in a digital switch. These functions involve converting an analog voice signal into digital PCM samples and converting digital PCM samples back into an analog signal. During conversion, digital filters are used to bandlimit the voice signals.

Independent channels allow the DSLAC device to function as two SLAC™ devices. All of the digital filtering is performed in digital signal processors operating from either a 2.048 MHz or 4.096 MHz external clock. The A/D, D/A, and signal processing is separate for each channel and each channel has its own Chip Select ($\overline{CS1}$ and $\overline{CS2}$) to allow separate programming.

The user-programmable filters set the receive and transmit gain, perform the transhybrid balancing function, permit adjustment of the two-wire termination impedance, and provide equalization of the receive and transmit paths. All programmable digital filter coefficients can be calculated using the AmSLAC2 software. The PCM codes can be either 8-bit companded A-law or μ-law. The PCM data is read and written to the PCM highway in user-programmable time slots at rates of 128 kHz to 8.192 MHz. The output hold time and the transmit clock edge can be selected for compatibility with other devices that can be connected to the PCM highway.

Four configurations of the DSLAC device are offered with the PCM interface described above. The Am79C02(A), the original version of the DSLAC device, is available in the 44-pin PLCC package. The Am79C03(A) and Am79C031(A) are reduced pin count versions obtained by consolidating a number of ground and power supply buses on chip, and eliminating the hardware reset function. The Am79C03(A) is available in both 32-pin plastic DIP and 32-pin PLCC packages. The Am79C031(A) is available in a 32-pin PLCC package. The “A” version of both devices (e.g., Am79C02A) offers the adaptive transhybrid balance feature described in the Adaptive B Filter overview.

ABSOLUTE MAXIMUM RATINGS

Storage temperature . . . . . .–60°C≤ T_A ≤ +125°C

Ambient operating temperature . .–40°C≤ T_A ≤ +85°C

Ambient relative humidity . . . . . 5% to 100% (noncondensing)

V_{CCA} with respect to AGND . . . . . .–0.4 V to +7.0 V

V_{CCD} with respect to DGND. . . . . .–0.4 V to +7.0 V

V_{CCP} with respect to PGND . . . . . .–0.4 V to +7.0 V

V_{EE} with respect to AGND . . . . . .+0.4 V to –7.0 V

V_{IN} with respect to VCCA. . . . . .+0.4 V to –10.0 V (V_{EE} = –5 V)

V_{IN} with respect to V_{EE} . . . . . .–0.4 V to +10.0 V (V_{CCA} = +5 V)

Other pins with respect to $DGND_1$ . . . . .–0.4 V to V_{CC}

Total combined C1–C5 current per channel:

Source from VCC. . . . . 32 mA

Sink into DGND . . . . . 24 mA

Latch-up immunity (any pin). . . . . ±30 mA

Stresses above those listed under Absolute Maximum Ratings may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to Absolute Maximum Ratings for extended periods may affect device reliability.

OPERATING RANGES

Commercial (C) Devices

Analog supply . . . . . +5.0 V ±5%

$VCCA_1$, $VCCA_2$, or VCCA

Digital supply . . . . . +5.0 V ±5%

V_{CCP}, $VCCD_1$, $VCCD_2$, or VCCD

Analog supply VEE_1, VEE_2 . . . . . –5.0 V ±5%

PGND, $DGND_1$, $DGND_2$, or DGND . . . . . .0 V

$AGND_1$, $AGND_2$, or AGND . . . . . ±50 mV

Ambient temperature . . . . . .0°C≤ T_A ≤ +70°C*

Ambient relative humidity . . . . . .15% to 85%

Operating Ranges define those limits between which the functionality of the device is guaranteed.

** Functionality of the device from 0°C to +70°C is guaranteed by production testing. Performance from –40°C to +85°C is guaranteed by characterization and periodic sampling of production units.*

ELECTRICAL CHARACTERISTICS over operating range unless otherwise noted

Typical values are for T_A = 25°C and nominal supply voltages. Minimum and maximum specifications are over the temperature and supply voltage ranges shown in Operating Ranges.

Symbol	Parameter Descriptions	Min	Typ	Max	Unit	Note
V_{IL}	Input Low voltage	–0.5		0.8	V	
V_{IH}	Input High voltage	2.0		V_{CC}		
I_{IL}	Input leakage current			±10	µA	
V_{OL}	Output Low voltage				V	
	C1–C5 (I_{OL} = 6 mA)			0.4		2
	C1–C5 (I_{OL} = 15 mA)			1.0		2
	$\overline{TSCA}$, $\overline{TSCB}$ (I_{OL} = 14 mA)			0.4		—
	Other digital outputs (I_{OL} = 2 mA)			0.4		—
V_{OH}	Output High voltage					
	C1–C5 (I_{OH} = 4 mA)	V_{CC} – 0.4				2
	C1–C5 (I_{OH} = 10 mA)	V_{CC} – 1.0				2
	Other digital outputs (I_{OH} = 400 µA)	2.4				—
I_{OL}	Output leakage current (HI-Z State)			±10	µA	
V_{IR}	Analog input voltage range (AX = 0 dB)			±3.12	V	
	(AX = 6.02 dB)			±1.56		
V_{IOS}	Offset voltage allowed on V_{IN}			±160	mV	
I_{IL} (V_{IL})	Input leakage current on V_{IN}			±10	µA	
Z_{IN}	Analog input impedance 300 Hz to 3400 Hz	5			MΩ	
Z_{OUT}	V_{OUT} output impedance		1	10	Ω	
I_{OUT}	V_{OUT} output current (f < 3400 Hz)			±6.3	mA	1
V_{OR}	V_{OUT} voltage range (AR = 0 dB)			±3.12	V	
	(AR = 6.02 dB)			±1.56		
V_{OOS}	V_{OUT} offset voltage (AISN off)			±40	mV	
V_{OOSA}	V_{OUT} offset voltage (AISN on)			±80		3
LIN_{AISN}	Linearity of AISN circuity (input = 0 dBm0)			±¼	LSB	
PD	Power dissipation Both channels active		180	240	mW	—
	(MCLK, PCLK = 2.048 MHz) 1 channel active		120	160		—
	Both channels inactive		10	19		4
PD	Power dissipation Both channels active		190	270		—
	(MCLK, PCLK > 2.048 MHz) 1 channel active		130	175		—
	Both channels inactive		10	19		4
I_{CC}	Total +5 V current Both channels active		24.0		mA	—
	1 channel active		18.0			—
	Both channels inactive		2.5			4
I_{EE}	Total –5 V current Both channels active		10.0			—
	1 channel active		5.0			—
	Both channels inactive		0.05			4
C_I	Input capacitance (Digital)		15		pF	
C_O	Output capacitance (Digital)		15			
PSRR	Power supply rejection ratio (1.02 kHz, 100 mVrms, either supply or path, GX = GR = 0 dB)	40			dB	

Notes:

1. *When the DSLAC device is in the Inactive mode, the analog output presents a 0 V output level through a ~3 kΩ resistor.*
2. *The C1–C5 outputs are resistive for less than a 1 V drop. Total current must not exceed absolute maximum ratings.*
3. *If there is an external DC path from V_{OUT} to V_{IN} with a gain of GDC and the AISN has a gain of h_{AISN}, then the output offset is multiplied by 1/[1 – (h_{AISN} • GDC)].*
4. *Power Dissipation in the Inactive mode is measured with all digital inputs at $V_{IH} = V_{CC}$ and $V_{IL} = V_{SS}$ and with no load connected to $VOUT_1$ or $VOUT_2$.*

Transmission Characteristics

The gain of the receive path is defined to be 0 dB when a 0 dBm0, 1014 Hz PCM sine wave input results in a nominal 1.55 Vrms for µ-law or 1.56 Vrms for A-law analog output. The gain of the transmit path is 0 dB when a 1.55 Vrms for µ-law or 1.56 Vrms for A-law, 1014 Hz sine wave analog input results in a level of 0 dBm0 at the digital output.

When relative levels (dBm0) are used in any of the following transmission specifications, the specification holds for any setting of the AX + GX gain from 0 to 12 dB and the AR + GR loss from 0 to 12 dB. Performance specification for settings of the AX + GX gain from 12 to 18 dB and the AR + GR loss from 12 to 18 dB is determined as the device is characterized.

Description	Test Conditions		Min	Typ	Max	Unit	Note
Gain accuracy D to A or A to D	0 dBm0, 1014 Hz 0 dB < |path gain| < 6 dB	25°C to 85°C 0°C –40°C	–0.20 –0.25 –0.35		+0.20 +0.25 +0.35		
Gain accuracy D to A or A to D	0 dBm0, 1014 Hz 6 dB < |path gain| < 12 dB	70°C to 85°C 25°C 0°C –40°C	–0.20 –0.25 –0.30 –0.35		+0.20 +0.25 +0.30 +0.35		— 1 1 —
Gain accuracy analog to analog or digital to digital		25°C to 85°C 0°C –40°C	–0.20 –0.25 –0.35		+0.20 +0.25 +0.35	dB	
Attenuation distortion		300 Hz to 3400 Hz	–0.125		+0.125		2
Single frequency distortion, A to D					–46		3
Single frequency distortion, D to A	–6 dB < (GR + AR) < 0 dB –12 dB < (GR + AR) < –6 dB –12 dB < (GR + AR) < –6 dB –12 dB < (GR + AR) < –6 dB –12 dB < (GR + AR) < –6 dB	–40°C to 85°C 70°C to 85°C 25°C 0°C –40°C			–46 –46 –45 –43 –40		3 3 3, 4 3, 4 3, 4
Intermodulation distortion					–42 –56	dBr	5
Analog out Idle channel noise Digital out	digital looped back digital input = 0 analog V_{IN} = 0	weighted unweighted A-law µ-law A-law µ-law			–68 –55 –78 12 –68 19	dBm0p dBm0p dBm0p dBrnc0 dBm0p dBrnc0	6
Crosstalk same channel TX to RX RX to TX	0 dBm0	300 Hz to 3400 Hz			–75 –75		
Crosstalk between channels TX to TX TX to RX RX to TX RX to RX	0 dBm0	300 Hz to 3400 Hz			–76 –78 –76 –78		
Group delay PCLK ≥ 1.53 MHz PCLK ≤ 1.03 MHz	B, X, R, and Z filters disabled				630 695	µs	7

Notes:

1. *AMD guarantees less than 0.1% of units fall into the last 0.05 dB of these specification numbers.*
2. *See Figure 1.*
3. *With f swept between 0 to 300 Hz and 3400 to 12 kHz, any generated output signals other than f are less than –28 dBm0. This specification is valid for either transmission path.*
4. *AMD guarantees < 0.2% of units are above –46 dB. This relaxed specification applies to only the third harmonic.*
5. *Intermodulation distortion specification for two signals of same level in the range of –4 dBm0 to –21 dBm0 does not produce 2 • (f1 – f2) component above specified level. 50 Hz IMD specified with 50 Hz signal at –23 dBm0 and signal between 300 Hz to 3400 Hz at –9 dBm0.*
6. *No single frequency component in the range above 3800 Hz may exceed a level of –55 dBm0.*
7. *The Group Delay specification is defined as the sum of the minimum values of the group delays for the transmit and the receive paths when the transmit and receive time slots are identical and the B, X, R, and Z filters are disabled. For PCLK frequencies between 1.03 MHz and 1.53 MHz, the group delay may vary from one cycle to the next. See Figure 2.*

Attenuation Distortion

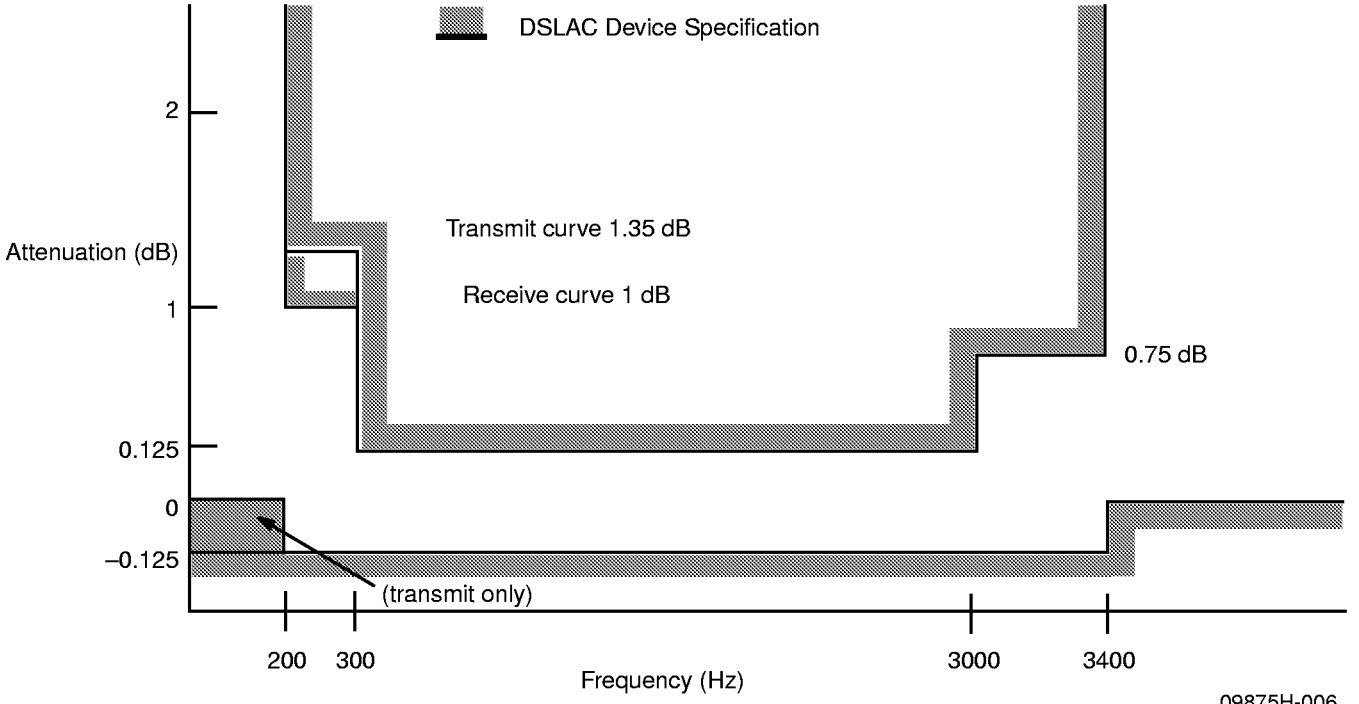


Figure 1. Attenuation Distortion (Single Ended)

Group Delay Distortion

For either transmission path, the group delay distortion is within the limits shown in Figure 2. The minimum value of the group delay is taken as the reference. The signal level should be 0 dBm0.

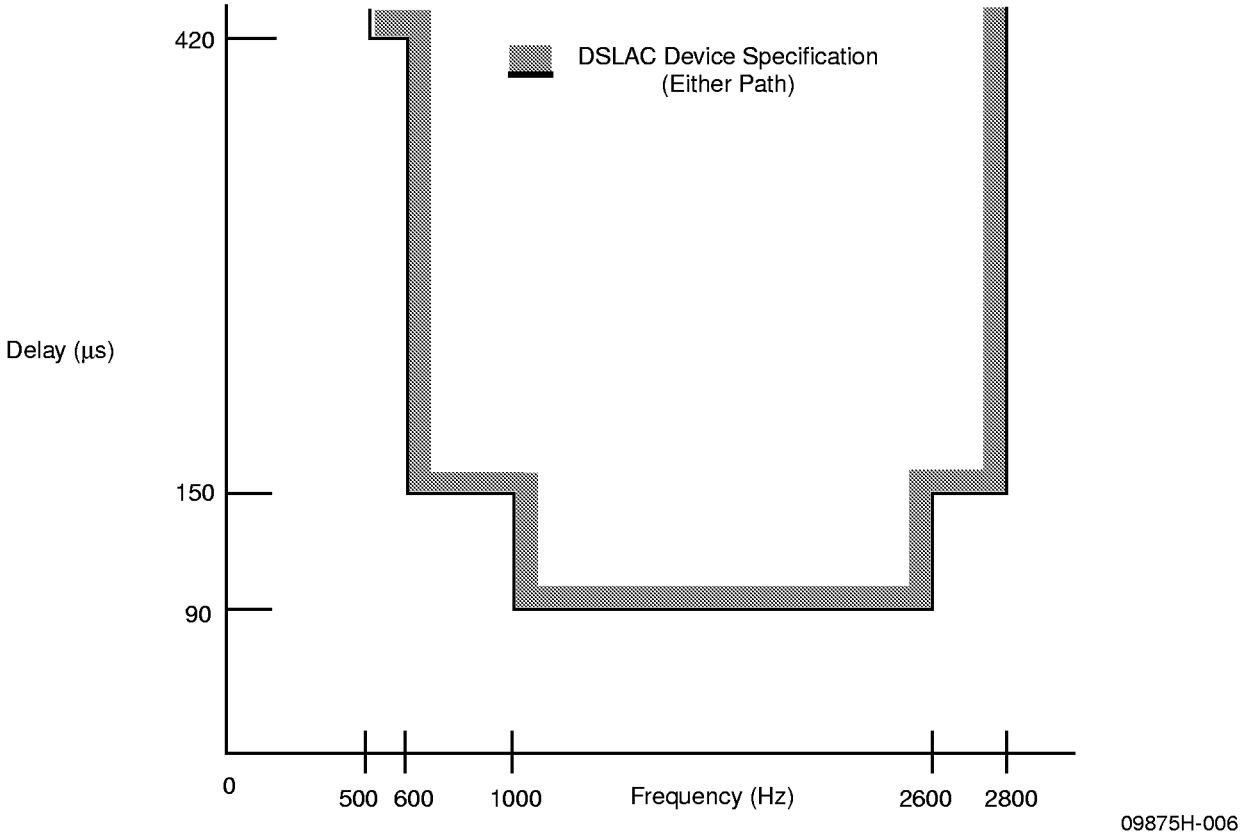


Figure 2. Group Delay Distortion

Variation of Gain with Input Level

The gain deviation relative to the gain at –10 dBm0 is within the limits shown if Figure 3 for either transmission path when the input is a sine wave signal of frequency 1014 Hz.

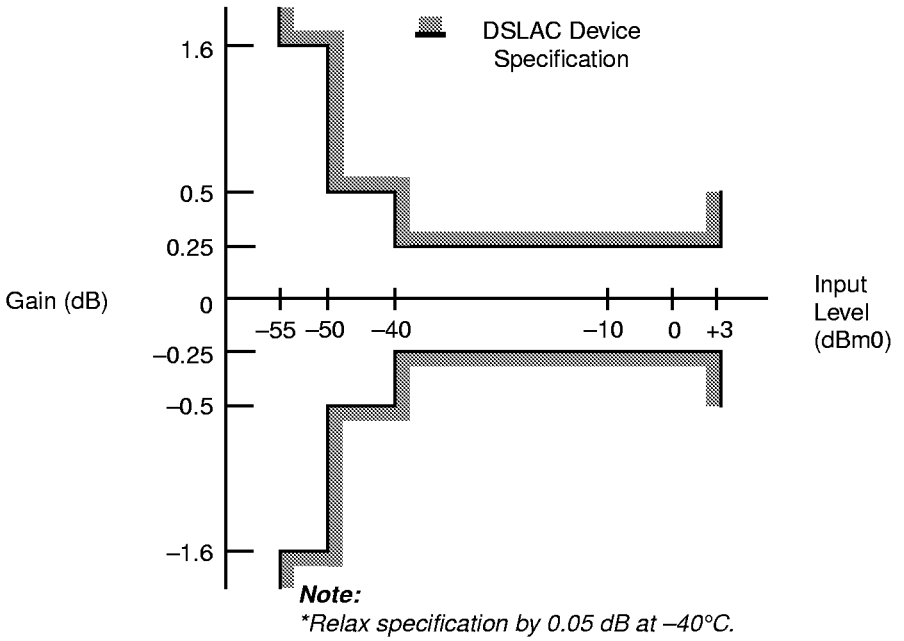


Figure 3. Gain Tracking with Tone Input*

Total Distortion, Including Quantizing Distortion

The signal-to-total distortion exceeds the limits shown in Figure 4 for either transmission path when the input is a sine wave signal of frequency 1014 Hz.

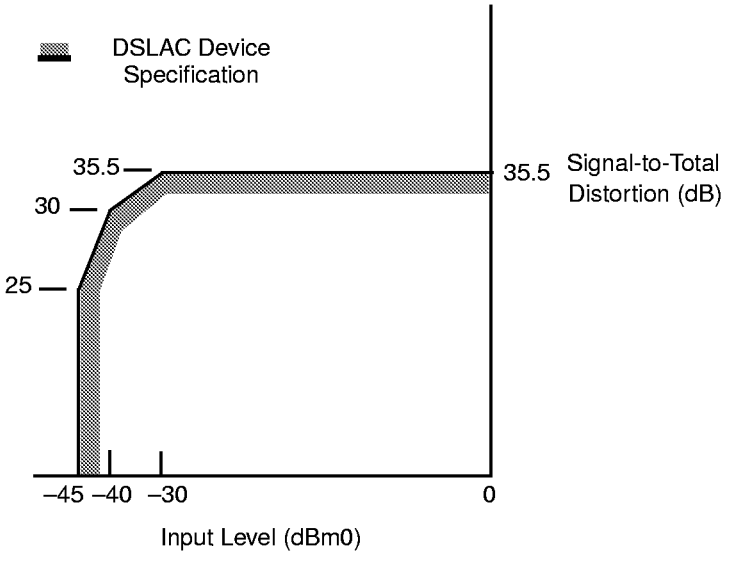
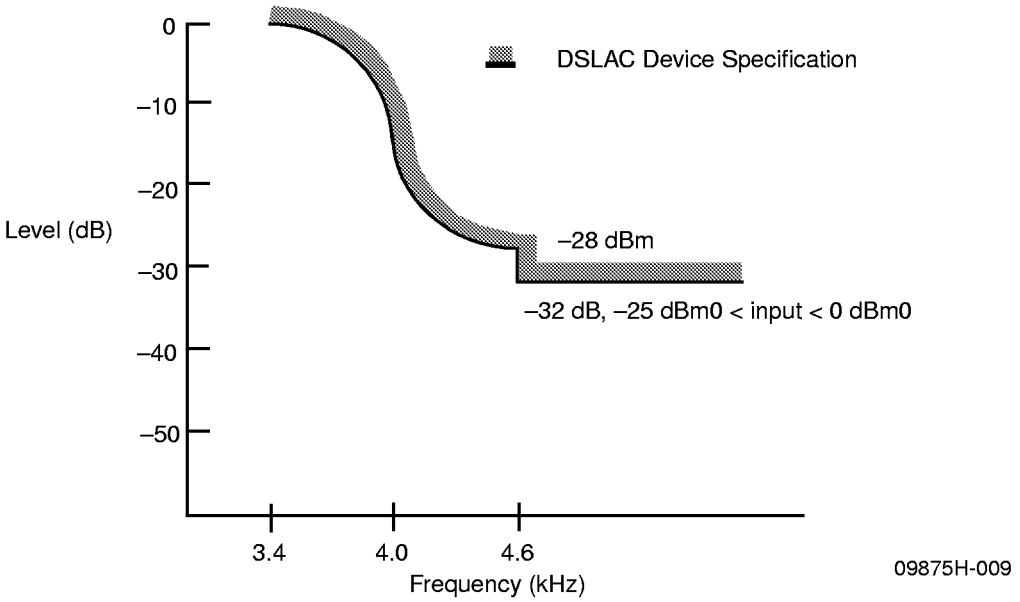


Figure 4. Total Distortion with Tone Input (Both Paths)

Discrimination against Out-of-Band Input Signals

When an out-of-band sine wave signal with frequency f and level A is applied to the analog input, there may be frequency components below 4 kHz at the digital output, caused by the out-of-band signal. These components are at least the specified dB level below the level of a signal at the same output originating from a 1014 Hz sine wave signal with a level of A dBm0 also applied to the analog input. The minimum specifications are shown in Figure 5.

Frequency of Out-of-Band Signal	Amplitude of Out-of-Band Signal	Level below A
16.6 Hz < f < 45 Hz	–25 dBm0 < A ≤ 0 dBm0	18 dB
45 Hz < f < 65 Hz	–25 dBm0 < A ≤ 0 dBm0	25 dB
65 Hz < f < 100 Hz	–25 dBm0 < A ≤ 0 dBm0	10 dB
3400 Hz < f < 4600 Hz	–25 dBm0 < A ≤ 0 dBm0	see Figure 5
4600 Hz < f < 100 kHz	–25 dBm0 < A ≤ 0 dBm0	32 dB



Note:
The attenuation of the waveform below amplitude A between 3400 Hz and 4600 Hz is given by the formula:

$$\text{Attenuation (dB)} = 14 - 14 \sin \frac{\pi(4000 - f)}{1200}$$

Figure 5. Discrimination against Out-of-Band Signals

Discrimination against 12 kHz and 16 kHz Metering Signals

If the DSLAC device is used in a metering application where 12 kHz or 16 kHz tone bursts are injected onto the telephone line toward the subscriber, a portion of those tones also may appear at the V_{IN} terminal. These out-of-band signals may cause frequency components to appear below 4 kHz at the digital output. For a 12 kHz tone, the frequency components below 4 kHz are reduced from the input by at least 48 dB, and for 16 kHz tones, the components are reduced by more than 70 dB.

To avoid degradation of in-band transmission performance, the input levels of these out-of-band tones must be limited. The maximum allowable level is 100 mVrms at 12 kHz, and is 500 mVrms at 16 kHz. An external notch filter at the VIN pin of the DSLAC device, incorporated with the metering injection design, is effective in reducing these tone levels.

Spurious Out-of-Band Signals at the Analog Output

With PCM code words representing a sine wave signal in the range of 300 Hz to 3400 Hz at a level of 0 dBm0 applied to the digital input, the level of the spurious out-of-band signals at the analog output is less than the limits shown in the following table.

Frequency	Level
4.6 kHz to 40 kHz	–32 dBm0
40 kHz to 240 kHz	–46 dBm0
240 kHz to 1 MHz	–36 dBm0

With code words representing any sine wave signal in the range 3.4 kHz to 4.0 kHz at a level of 0 dBm0 applied to the digital input, the level of the signals at the analog output are below the limits in Figure 6. The amplitude of the spurious out-of-band signals between 3400 Hz and 4600 Hz is given by the formula:

$$A = -14 - 14 \sin \frac{\pi(f - 4000)}{1200} \text{ dBm0}$$

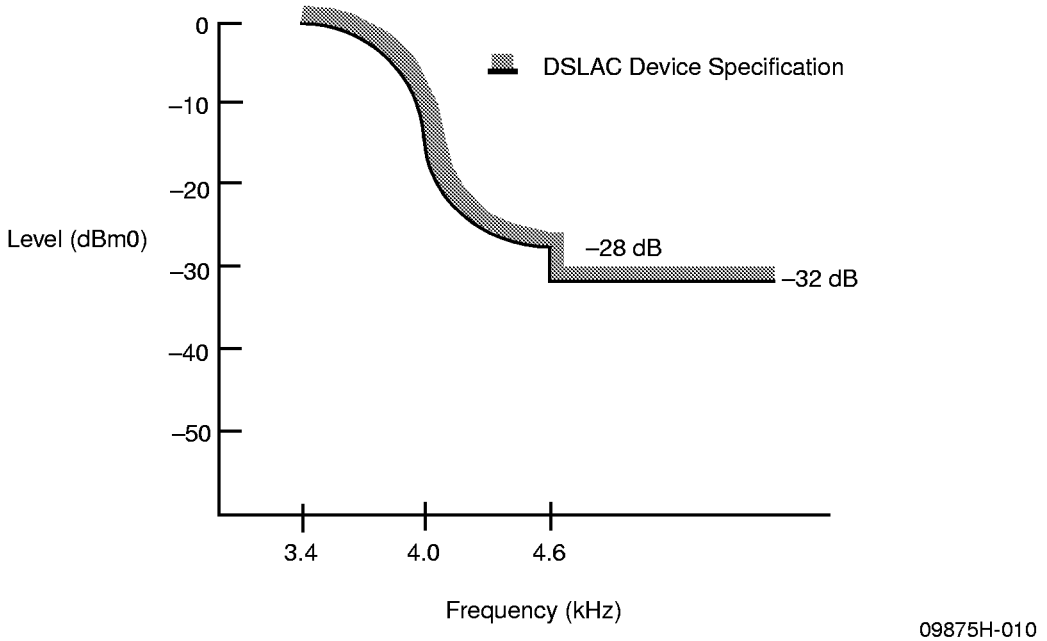


Figure 6. Spurious Out-of-Band Signals

Overload Compression

Figure 7 shows the acceptable region of operation for input signal levels above the reference input power (0 dBm0). The conditions for this figure are: (1) 1 dB < GX ≤ 12 dB; (2) –12 dB ≤ GR < –1 dB; (3) PCM output connected to PCM input; and (4) measurement analog-to-analog.

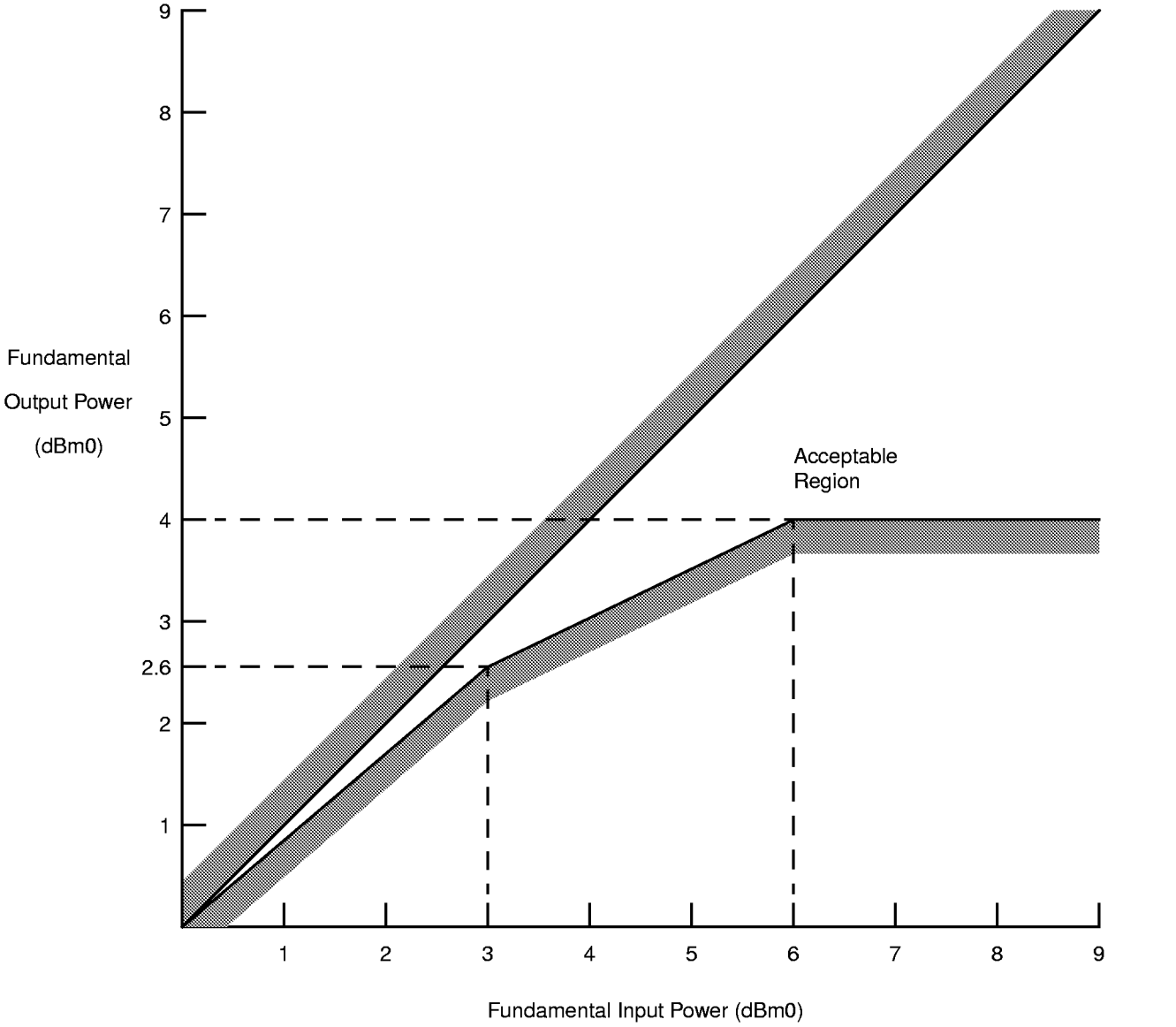


Figure 7. A/A Overload Compression

SWITCHING CHARACTERISTICS over operating range unless otherwise noted

Microprocessor Interface

Min and max values are valid for all digital outputs with a 150 pF load, except C1–C5 with a 30 pF load. Pull-up resistors of 360 Ω are attached to $\overline{TSCA}$ and $\overline{TSCB}$.

No.	Symbol	Parameter	Min	Typ	Max	Units
1	t_{DCY}	Data Clock Period	244			ns
2	t_{DCH}	Data Clock High Pulse Width (Note 1)	97			
3	t_{DCL}	Data Clock Low Pulse Width (Note 1)	97			
4	t_{DCR}	Rise Time of Clock			25	
5	t_{DCF}	Fall Time of Clock			25	
6	t_{ICSS}	Chip Select Setup Time, Input Mode	70		t_{DCY} – 10	
7	t_{ICSH}	Chip Select Hold Time, Input Mode	0		t_{DCH} – 20	
8	t_{ICSL}	Chip Select Pulse Width, Input Mode		$8t_{DCY}$		
9	t_{ICSO}	Chip Select Off Time, Input Mode (Note 7)		5		µs
10	t_{IDS}	Input Data Setup Time	30			ns
11	t_{IDH}	Input Data Hold Time	30			
12	t_{OLH}	SLIC Output Latch Valid	20		1000	
13	t_{OCSS}	Chip Select Setup Time, Output Mode	70		t_{DCY} – 10	
14	t_{OCSH}	Chip Select Hold Time, Output Mode	0		t_{DCH} – 20	
15	t_{OCSL}	Chip Select Pulse Width, Output Mode		$8t_{DCY}$		
16	t_{OCSO}	Chip Select Off Time, Output Mode (Note 7)		5		µs
17	t_{ODD}	Output Data Turn On Delay (Note 5)			50	ns
18	t_{ODH}	Output Data Hold Time	0			
19	t_{ODOF}	Output Data Turn Off Delay			50	
20	t_{ODC}	Output Data Valid	0		50	

PCM Interface

PCLK not to exceed 4.096 MHz when PCM delay is used.

No.	Symbol	Parameter	Min	Typ	Max	Units
21	t_{PCY}	PCM Clock Period (Note 2)	0.122		7.8125	µs
22	t_{PCH}	PCM Clock High Pulse Width	48		3890	ns
23	t_{PCL}	PCM Clock Low Pulse Width	48		3890	
24	t_{PCF}	Fall Time of Clock			15	
25	t_{PCR}	Rise Time of Clock			15	
26	t_{FSS}	FS Setup Time	25		t_{PCY} – 50	
27	t_{FSH}	FS Hold Time	50			
28	t_{TSD}	Delay to $\overline{TSC}$ Valid (with Programmable Delay) (Note 3)	5 30		80 150	
29	t_{TSO}	Delay to $\overline{TSC}$ Off (with Programmable Delay) (Note 6)	5 30		80 150	
30	t_{DXD}	PCM Data Output Delay (with Programmable Delay) (Note 4)	3 30		80 150	
31	t_{DXH}	PCM Data Output Hold Time (with Programmable Delay) (Note 4)	5 30		80 150	
32	t_{DXZ}	PCM Data Output Delay to HI-Z (with Programmable Delay) (Note 4)	5 30		80 150	
33	t_{DRS}	PCM Data Input Setup Time	25			
34	t_{DRH}	PCM Data Input Hold Time	5			

Master Clock

For 2.048 MHz ±100 ppm or 4.096 MHz ±100 ppm operation:

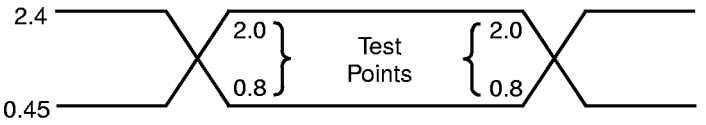
No.	Symbol	Parameter	Min	Typ	Max	Units
35	t_{MCY}	Master Clock Period (2.048 MHz)	488.23	488.28	488.33	ns
		Master Clock Period (4.096 MHz)	244.11	244.14	244.17	
36	t_{MCR}	Rise Time of Clock		15		
37	t_{MCF}	Fall Time of Clock			15	
38	t_{MCH}	MCLK High Pulse Width (2.048 MHz)	200			
		MCLK High Pulse Width (4.096 MHz)	80			
39	t_{MCL}	MCLK Low Pulse Width (2.048 MHz)	200			
		MCLK Low Pulse Width (4.096 MHz)	80			

Notes:

1. *DCLK may be stopped in the High or Low state indefinitely without loss of information. If $\overline{CS}$ makes a transition to the Low state, the last byte received is interpreted by the Microprocessor Interface logic.*
2. *The PCM clock (PCLK) frequency must be an integer multiple of the frame sync (FS) frequency with an accuracy of 800 ppm relative to the MCLK frequency. This allowance includes any jitter that may occur between the PCM signals (FS, PCLK) and MCLK. The actual PCLK rate is dependent on the number of channels allocated within a frame. The DSLAC supports 2–128 channels. A PCLK of 1.544 MHz can be used for standard US transmission systems. The minimum clock frequency is 128 kHz.*
3. *$\overline{TSC}$ is delayed from FS by a typical value of N • t_{PCY}, where N is the value stored in the time/clock-slot register.*
4. *There is a special conflict detection circuitry that prevents high-power dissipation from occurring when the DXA or DXB pins of two DSLAC devices are tied together and one DSLAC device starts to transmit before the other has gone into a high-impedance state.*
5. *The first data bit is enabled on the falling edge of $\overline{CS}$ or on the falling edge of DCLK, whichever occurs last.*
6. *t_{TSO} is defined as the time at which the output achieves the open circuit condition.*
7. *The DSLAC device requires 40 cycles of the 8 MHz internal clock (5 µs) between SIO operations. If the MPI is being accessed while the MCLK input is not active, a Chip Select Off time of 20 µs is required.*

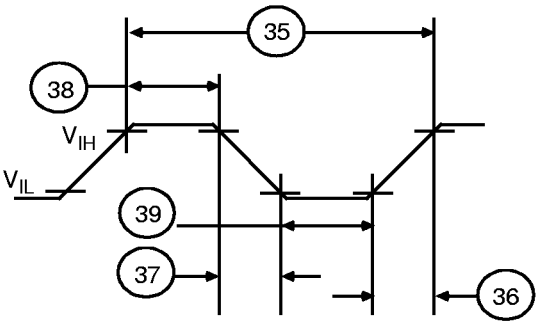
SWITCHING WAVEFORMS

Input and Output Waveforms for AC Tests



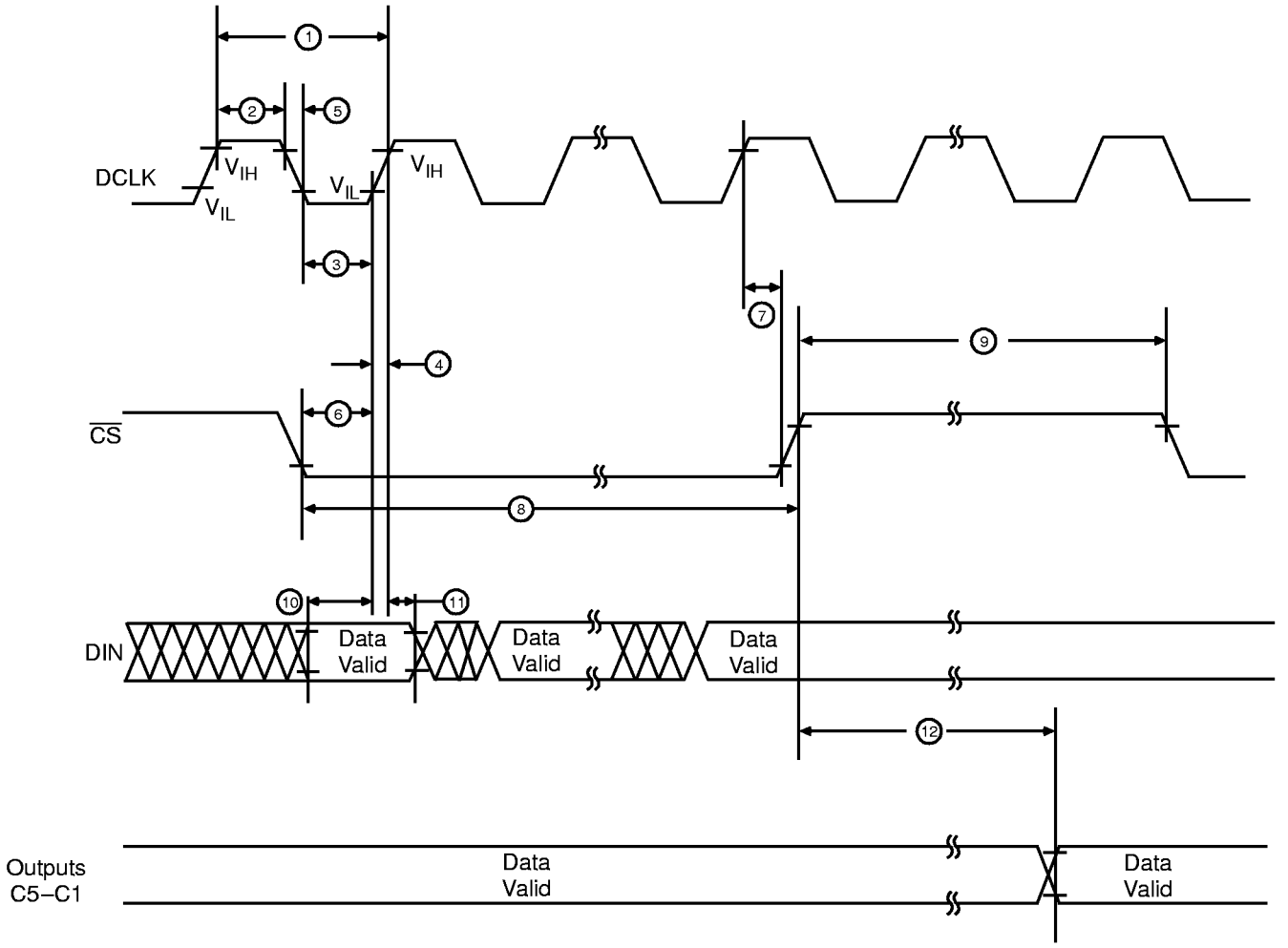
09875H-012

Master Clock Timing



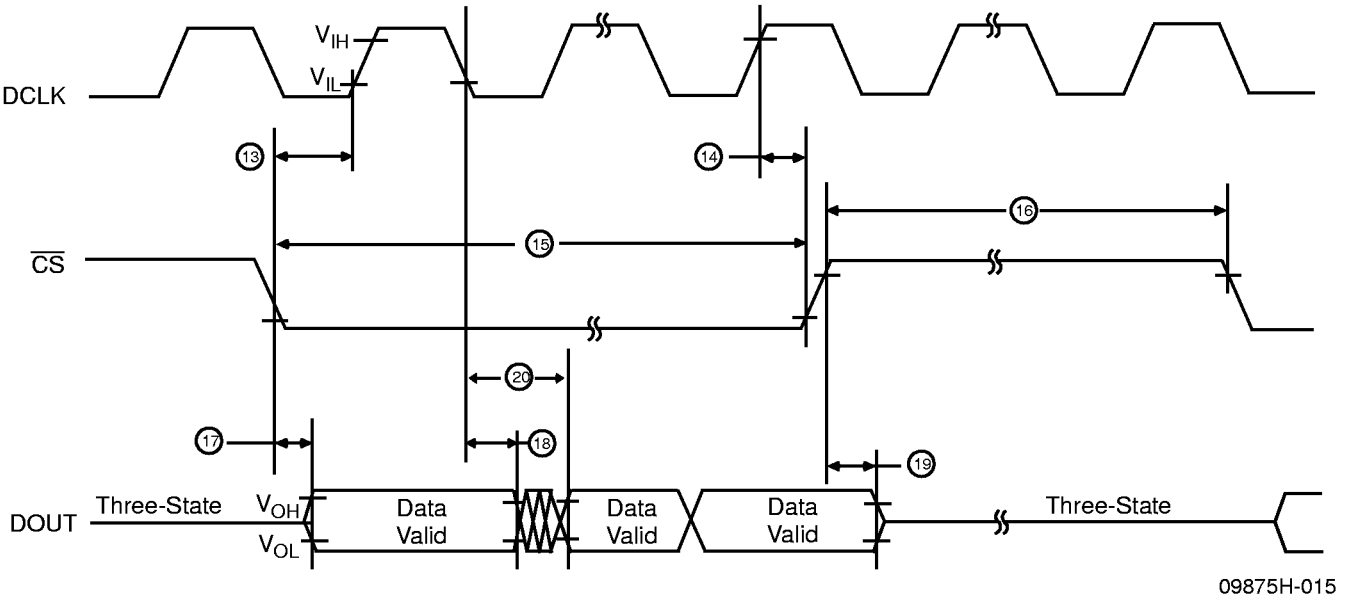
09875H-013

Microprocessor Interface (Input Mode)



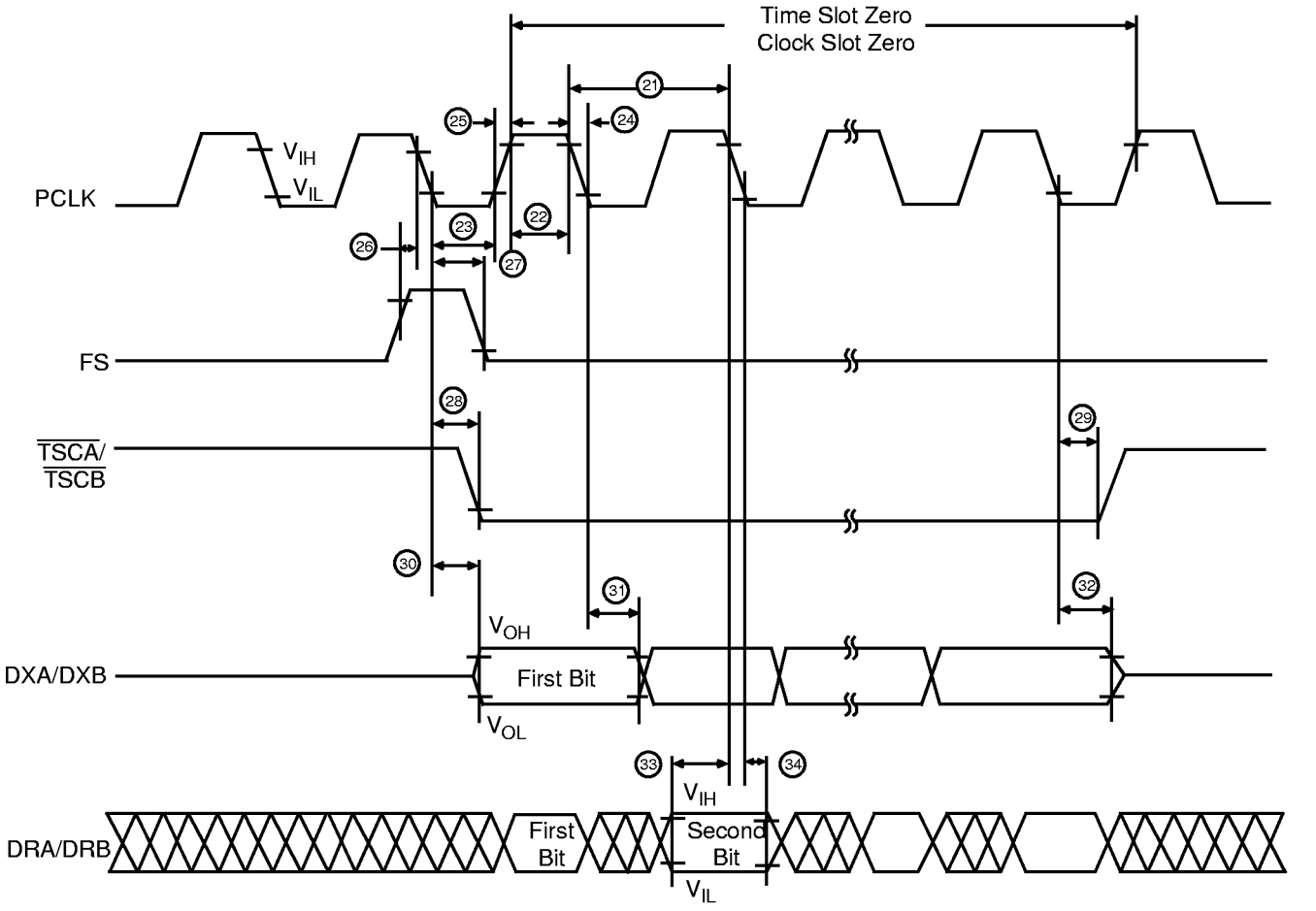
09875H-014

Microprocessor Interface (Output Mode)



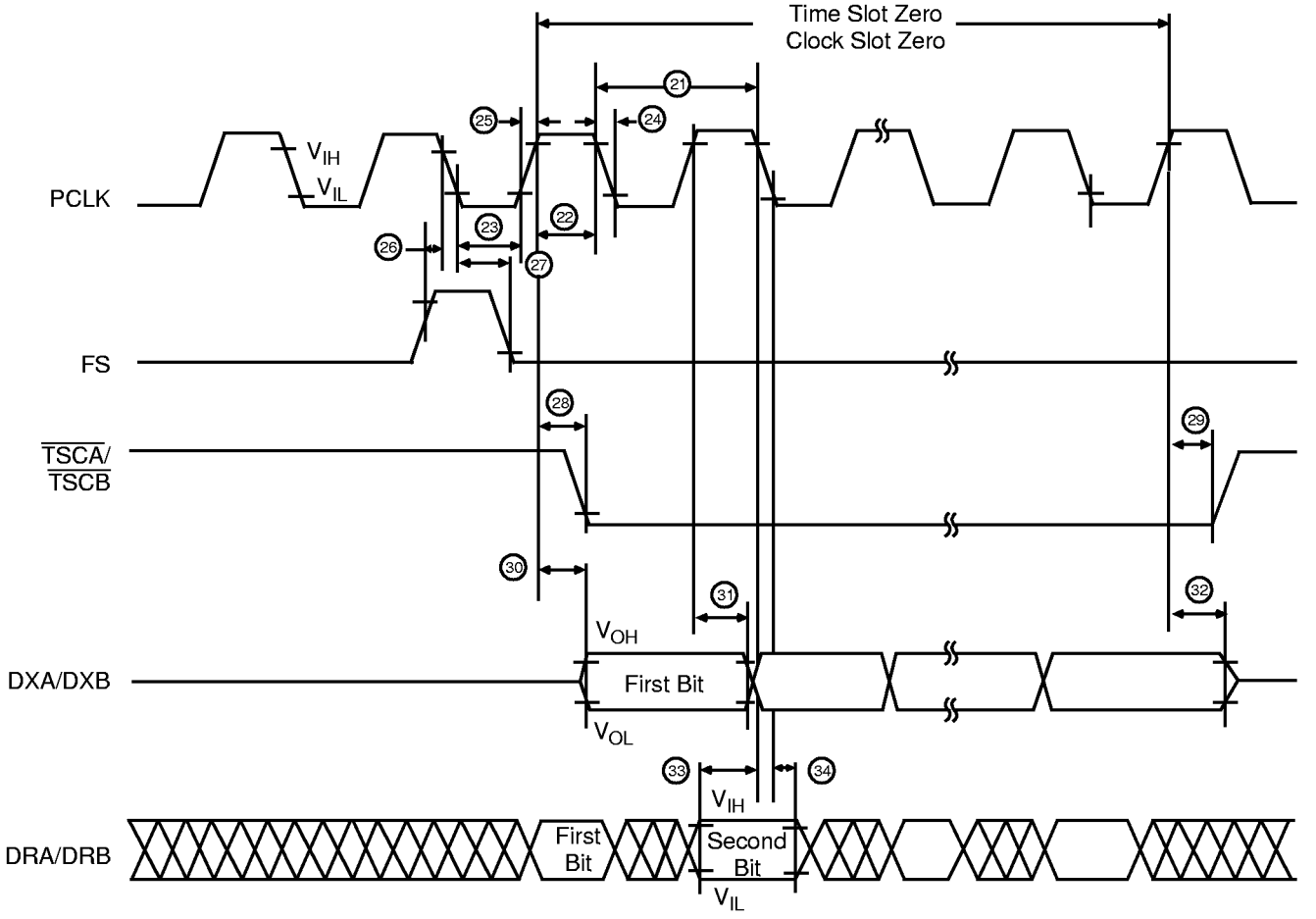
09875H-015

PCM Highway Timing for XE = 0 (Transmit on Negative PCLK Edge)



09875H-016

PCM Highway Timing for XE = 1 (Transmit on Positive PCLK Edge)



09875H-017

Note:
In this mode, the PCM transmit timing is compatible with other CODEC IC's.

Operating the DSLAC Device

The following describes the operation of either channel of the DSLAC device. The description is valid for either Channel 1 or 2. VIN in this data sheet refers to either VIN_1 or VIN_2, VOUT refers to either $VOUT_1$ or $VOUT_2$, and $\overline{CS}$ refers to either $\overline{CS1}$ or $\overline{CS2}$.

Power-Up Sequence from V_{CC} = 0 V

The recommended power-up sequence is to apply:

1. Power supply grounds
2. V_{CC}/V_{EE}
3. Signal connections
4. Hardware Reset (02 only)

The software initialization should then include:

1. Select MCLK (Command 6)
2. Software Reset (Command 2)
3. Program filter coefficients and other parameters
4. Activate (Command 5)

Software initialization of the DSLAC device should always follow any power-up or hardware reset.

Upon initial application of power, a minimum of 1 ms is needed before $\overline{CS1}$ or $\overline{CS2}$ may go Low and an MPI command initiated. If the power supply ($VCCD_1$ or $VCCD_2$) falls below approximately 2.0 V, the device is reset and requires complete reprogramming with the above sequence. Bit 7 of the SLIC Direction Register reads back as a logical 1 to indicate that a power interruption has been detected. This bit is cleared when a software reset command is sent to the DSLAC device. The RST pin may be tied to +5 V if it is not needed in the system (Am79C02 only).

Active Mode

Each channel of the DSLAC device can operate in either the Active (operational) or Inactive (standby) mode. In the Active mode, the DSLAC device is able to transmit and receive PCM and analog information. This is the normal operating mode when a telephone call is in progress. The Activate command, Microprocessor Interface (MPI) Command 5, puts the device into this state. Bringing the DSLAC device into the Active mode is possible only through the MPI.

Inactive Mode

The DSLAC device is forced into the Inactive (standby) mode after a powerup, hardware or software reset, or is programmed into this mode by the Deactivate command (Command 1). Power is switched off from all nonessential circuitry, though the MPI remains active to receive new commands. The analog output is tied to ground through an approximate 3 kΩ resistor. All circuits, which contain programmed information, retain their data in the Inactive mode.

Reset State

An active Low, hardware Reset pin ($\overline{RST}$) is available on the Am79C02, which resets the device to the following default state. (For the Am79C02, Am79C03, and Am79C031, when power is first applied, an internal power-up reset puts the device into the following default state.)

1. A-law is selected
2. B, X, R, and Z filters disabled; AISN gain is zero.
3. Digital (GX and GR) gain blocks are disabled, resulting in unity gain, and analog (AX and AR) gains are set to unity.
4. SLIC input/output direction is set to the Input mode.
5. Normal conditions are selected (see Command 4).
6. The B-filter Adaptive mode is turned off.
7. Both channels placed in Inactive (standby) mode.
8. Transmit time, receive time, and clock slots are set to zero.
9. DXA/DRA ports are selected for Channel 1.
10. DXB/DRB ports are selected for Channel 2.

    Note: *Must be reassigned to DXA/DRA for Am79C031.*
11. MCLK is selected to be 4.096 MHz.
12. Transmit on the negative edge of PCLK. (XE = 0)
13. PCM Delay is inserted.

Reset states 1 to 7 are identical to those of the software reset (Command 2). The software reset command affects only those channels that have their CS asserted.

Signal Processing

Overview of Digital Filters

Several of the blocks in the signal processing section are user programmable. These allow the user to optimize the performance of the DSLAC device for the system. Figure 8 shows the DSLAC device signal processing and indicates the programmable blocks.

The advantages of digital filters are:

- High reliability
- No drift with time or temperature
- Unit-to-unit repeatability
- Superior transmission performance

Two-Wire Impedance Matching

Two feedback paths on the DSLAC device modify the effective two-wire input impedance of the SLIC by providing programmable feedback from V_{IN} to V_{OUT}. The Analog Impedance Scaling Network (AISN) is a programmable analog gain of –0.9375 to +0.935 from V_{IN} to V_{OUT}. The Z filter is a programmable digital filter, also connecting V_{IN} to V_{OUT}.

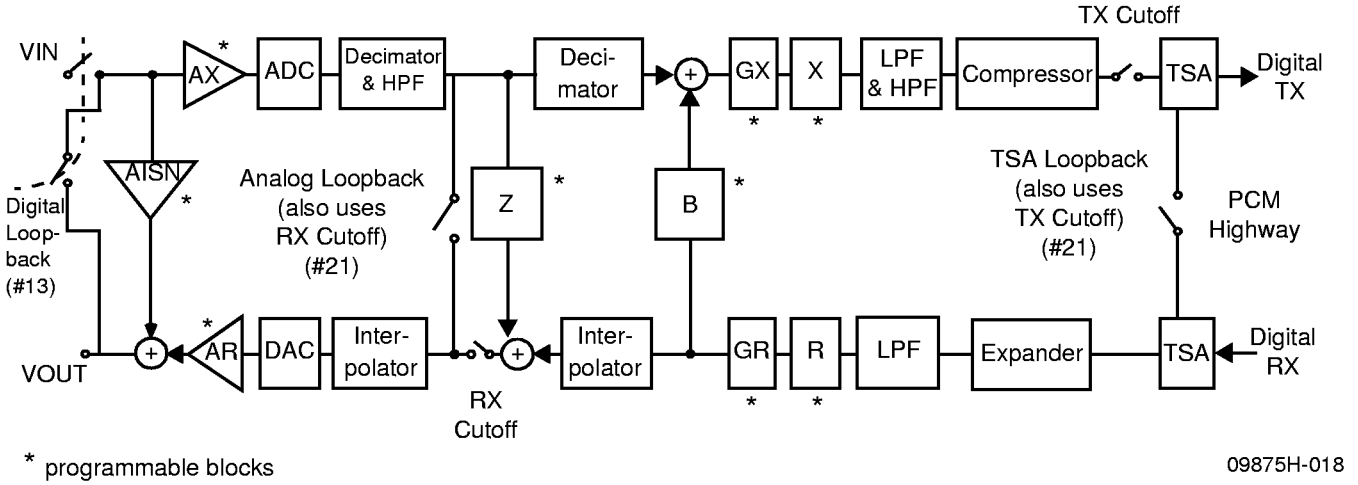


Figure 8. DSLAC Block Diagram

Distortion Correction and Equalization

The DSLAC device contains programmable filters in the receive (R) and transmit (X) directions that may be programmed for line equalization and to correct any attenuation distortion caused by the Z filter.

Transhybrid Balancing

The DSLAC device's programmable B filter is used to adjust transhybrid balance. The filter has a single pole IIR section (BIIR) and an eight tap FIR section (BFIR), both operating at 16 kHz. The DSLAC device has an optional Adaptive mode for the B filter, which may be used to achieve optimum performance. The Echo Path Gain (EPG) and Error Level Threshold (ELT) registers contain values that determine the Adaptive mode performance.

Gain Adjustment

The DSLAC device's transmit path has two programmable gain blocks. Gain block AX is an analog gain of 0 dB or 6.02 dB, located immediately before the A/D converter. Gain block GX is a digital gain that is programmable to any gain from 0 dB to 12 dB with a worst-case step size of 0.3 dB for gain settings above 10 dB. The filters provide a net gain in the range of 0 dB to 18 dB.

The DSLAC device receive path has two programmable loss blocks. Loss block GR is a digital loss that is programmable from 0 dB to 12 dB with a worst-case step size of 0.1 dB. Loss block AR is an analog loss of 0 dB or 6.02 dB, located immediately after the D/A converter. This provides a net loss in the range of 0 dB to 18 dB.

Transmit Signal Processing

In the transmit path, the analog input signal is A/D converted, filtered, companded (A-law or µ-law), and made available for output to the PCM highway. The signal processor contains an ALU, RAM, ROM, and control logic to implement the filter sections. The B, X, and GX blocks are user-programmable digital filter sections with coefficients stored in the coefficient RAM while AX is an analog amplifier that can be programmed for 0 dB or 6.02 dB gain. The filters may be made transparent when not required in a system.

The decimator reduces the high input sampling rate to 16 kHz for input to the B, GX, and X filters. The X filter is a six tap FIR section, which is part of the frequency response correction network. The B filter operates on samples from the receive signal path in order to provide transhybrid balancing in the loop. The high-pass filter rejects low frequencies such as 50 or 60 Hz and may be disabled.

Transmit PCM Interface

The transmit PCM interface receives an 8-bit compressed code from the digital A-law/µ-law compressor. Transmit logic controls the transmission of data onto the PCM highway through output port selection and time/clock slot control circuitry.

The frame sync (FS) pulse identifies the beginning of a transmit frame and all channels (time slots) are referenced to it. The logic contains user programmable Transmit Time Slot and Transmit Clock Slot registers.

The Time Slot register is 7 bits wide and allows up to 128 8-bit channels (using a PCLK of 8.192 MHz) in each frame. This feature allows any clock frequency between 128 kHz and 8.192 MHz (2 to 128 channels) in a system. The Clock Slot register is 3 bits wide and may be programmed to offset the time slot assignment by 0 to 7 PCLK periods to eliminate any clock skew in the system. The data is transmitted in bytes with the most significant bit first.

An exception occurs when division of the PCLK frequency by 64 kHz produces a nonzero remainder, R ($R = f_{PCLK}$ modulo 64 kHz, $R > 0$), and when the transmit clock slot is greater than R. In that case, the R-bit

fractional time slot after the last full time slot in the frame contains random information and has the TSC output turned on. For example, if the PCLK frequency is 1.544 MHz (R = 1) and the transmit clock slot is greater than 1, the 1-bit fractional time slot after the last full time slot in the frame contains random information, and the TSC output remains active during the fractional time slot. The data is transmitted in bytes, with the most significant bit first.

The PCM data may be user programmed for output onto either the DXA or DXB port. Correspondingly, either TSCA or TSCB is Low during transmission.

The DXA/DXB and TSCA/TSCB outputs can be programmed to change either on the negative or positive edge of PCLK. In the first case, an extra delay (PCM delay) in the timing of the DXA and DXB signals may be programmed to allow timing compatibility with other devices on the PCM highway.

Receive Signal Processing

In the receive path, the digital signal is expanded, filtered, converted to analog, and passed to the VOUT pin. The signal processor contains an ALU, RAM, ROM, and control logic to implement the filter sections. The Z, R, and GR blocks are user-programmable filter sections with their coefficients stored in the coefficient RAM, while AR is an analog amplifier that can be programmed for a 0 dB or 6.02 dB loss. The filters may be made transparent when not required in a system.

The low-pass filter band limits the signal. The R filter is a six tap FIR section operating at a 16 kHz sampling rate and is part of the frequency response correction network. The Analog Impedance Scaling Network (AISN) is a user-programmable gain block providing feedback from V_{IN} to V_{OUT} to emulate different ZSLIC impedances from a single external ZSLIC impedance. The Z filter provides feedback from the transmit signal path to the receive path and is used to modify the effective input impedance to the system. The interpolator increases the sampling rate prior to D/A conversion.

Receive PCM Interface

The receive PCM interface logic controls the reception of data bytes from the PCM highway, transfers the data to the A-law/µ-law expansion logic, and then passes the data to the receive path of the signal processor. The frame sync (FS) pulse identifies the beginning of a receive frame, and all channels (time slots) are referenced to it.

The logic contains user-programmable Receive Time Slot and Receive Clock Slot registers. The Time Slot register is 7 bits wide and allows up to 128 8-bit channels (using a PCLK of 8.192 MHz) in each frame. This feature allows any clock frequency between 128 kHz and 8.192 MHz (2 to 128 channels) in a system. The Clock Slot register is 3 bits wide and may be programmed to offset the time slot assignment by 0 to 7 PCLK periods to eliminate any clock skews in the system. An exception occurs when division of the PCLK frequency by 64 kHz produces a nonzero remainder, R ($R = f_{PCLK}$ modulo 64 kHz, $R > 0$) and when the receive clock slot is greater than R. In that case, the last receive time slot in the frame is not usable. For example, if the PCLK frequency is 1.544 MHz (R = 1), the receive clock slot can be only 0 or 1 if the last time slot is to be used. The PCM data may be user programmed for input from either the DRA or DRB port.

Analog Impedance Scaling Network (AISN)

The AISN is incorporated in the DSLAC device to scale the value of the external ZSLIC impedance. Scaling this external impedance with the AISN (along with the Z filter) allows matching of many different line conditions using a single impedance value. Linecards may be designed for many different specifications without any hardware changes.

The AISN is a programmable gain that is connected across the DSLAC device input from V_{IN} to V_{OUT}. The gain can be varied from –0.9375 to +0.9375 in 31 steps of 0.0625. The AISN gain is given by the following equation:

$$h_{AISN} = 0.0625[(A2^4 + B2^3 + C2^2 + D2^1 + E2^0) - 16]$$

where A, B, C, D, and E = 1 or 0.

The AISN gain is used to alter the input impedance of the DSLAC device from the SLIC as given by:

$$Z_{IN} = Z_{SL} \frac{(1 - G_{44}h_{AISN})}{(1 - G_{440}h_{AISN})}$$

where G_{440} (defined as $G_{24}\ G_{42} + G_{44}$) is the echo gain into an open circuit and G_{44} is the echo gain into a short circuit.

There are two special cases to the formula for h_{AISN}: 1) value of ABCDE = 00000 specifies a gain of 0 (or cutoff), and 2) a value of ABCDE = 10000 is a special case where the AISN circuitry is disabled and the V_{OUT} pad is connected internally to V_{IN} with a gain of 0 dB. This allows a digital-to-digital Loopback mode wherein a digital PCM input signal is completely processed through the receive section all the way to the VOUT pin. The signal then is connected internally to V_{IN} where it is processed through the transmit section and output as digital PCM data.

Speech Coding

The A/D and D/A conversion follows either the A-law or the µ-law as they are defined in CCITT Rec. G.711. A-law or µ-law operation is programmed using MPI Command 19. Alternate bit inversion is performed as part of the A-law coding.

Command Description and Formats

Microprocessor Interface Description

A microprocessor may be used to program the DSLAC device and control its operation using the Microprocessor Interface (MPI). Data programmed previously may be read out for verification. For each channel, commands are provided to assign values to the following parameters.

– Transmit time slot

– Receive time slot

– Transmit clock slot

– Receive clock slot

– Transmit gain

– Receive loss

– B-filter coefficients

– X-filter coefficients

– R-filter coefficients

– Z-filter coefficients

– Adaptive B filter parameters

– AISN coefficient

– Read/Write SLIC Input/Output

– Select A-law or µ-law code

– Select Transmit PCM Port A or B

– Select Transmit PCM clock edge

– Select Transmit PCM delay

– Select Receive PCM Port A or B

– Enable/disable B filter

– Enable/disable Z filter

– Enable/disable X filter

– Enable/disable R filter

– Enable/disable GX filter

– Enable/disable GR filter

– Enable/disable AX amplifier

– Enable/disable AR amplifier

– Enable/disable adaptive B filter

– Select test modes

– Select Active or Inactive (standby) mode

The following description of the MPI is valid for either Channel 1 or 2. Whenever $\overline{CS}$ is specified, it refers to either $\overline{CS1}$ or $\overline{CS2}$. If desired, both channels may be programmed simultaneously with identical information by activating $\overline{CS1}$ and $\overline{CS2}$ at the same time. Commands that affect both channels simultaneously are noted as such.

The MPI consists of serial data input (DIN or DIO), output (DOUT or DIO), data clock (DCLK), and a separate chip select ($\overline{CS1}$ and $\overline{CS2}$) input for each channel. The serial input consists of 8-bit command words that may be followed with additional bytes of input data or may be followed by the DSLAC device sending out bytes of data. All data input and output is MSB (D7) first and LSB (D0) last. All data bytes are read or written one at a time, with $\overline{CS}$ going High for at least the minimum off period before the next byte is read or written.

All commands that require additional input data to the device must have the input data as the next N words written into the device (for example, framed by the next N transitions of $\overline{CS}$). All commands that are followed by output data causes the device to output data for the next N transitions of $\overline{CS}$ going Low. The DSLAC device does not accept any input commands until all the data is shifted out. Unused bits in the data bytes are read out as zeros.

A command sequence to one channel must be finished before a command can be sent to the channel. The NOP Command 2 is recommended to follow any set of commands to the DSLAC device. The NOP is executed in the event of any anamolous $\overline{CS}$ assertion.

An MPI cycle is defined by transitions of $\overline{CS}$ and DCLK. If the $\overline{CS}$ lines are held in the High state between accesses, the DCLK may run continuously with no change to the internal control data. Using this method, the same DCLK may be run to a number of DSLAC devices and the individual $\overline{CS}$ lines selects the appropriate device to access. Between command sequences, DCLK can stay in the High state indefinitely with no loss of internal control information regardless of any transitions on the $\overline{CS}$ lines. Between bytes of a multibyte read or write command sequence, DCLK also can stay in the High state indefinitely; however, each low-going transition of the $\overline{CS}$ line still advances the byte counter. DCLK can stay in the Low state indefinitely with no loss of internal control information, provided the $\overline{CS}$ lines remain at a high level.

Summary of MPI Commands**

C#	Hex	Description
1.	00	Deactivate (Standby mode)
2.	02	Reset
3.	06	No Operation
4.	08	Reset to Normal Conditions
5.	0E	Activate
6.	1*	MCLK Selection
7.	40	Write TX Time Slot & PCM Highway
8.	41	Read TX Time Slot & PCM Highway
9.	42	Write RX Time Slot & PCM Highway
10.	43	Read RX Time Slot & PCM Highway
11.	44	Write RX & TX Clock Slot and TX Edge
12.	45	Read RX & TX Clock Slot and TX Edge
13.	50	Write AISN, PCM delay, Analog Gains
14.	51	Read AISN, PCM delay, Analog Gains
15.	52	Write SLIC Input/Output Register
16.	53	Read SLIC Input/Output Register
17.	54	Write SLIC Input/Output Direction
18.	55	Read SLIC I/O Direction, Power Interrupt Bit, and Channel Status Bit
19.	60	Write Operating Functions
20.	61	Read Operating Functions
21.	70	Write Operating Conditions
22.	71	Read Operating Conditions
23.	73	Read Revision Code Number

C#	Hex	Description
24.	80	Write GX Filter Coefficients
25.	81	Read GX Filter Coefficients
26.	82	Write GR Filter Coefficients
27.	83	Read GR Filter Coefficients
28.	84	Write Z Filter Coefficients
29.	85	Read Z Filter Coefficients
30.	86	Write B Filter Coefficients
31.	87	Read B Filter Coefficients
32.	88	Write X Filter Coefficients
33.	89	Read X Filter Coefficients
34.	8A	Write R Filter Coefficients
35.	8B	Read R Filter Coefficients
36.	8C	Write Echo Path Gain
37.	8D	Read Echo Path Gain
38.	8E	Write Error Level Threshold
39.	8F	Read Error Level Threshold
40.	92	Write GZ Filter Coefficient
41.	93	Read GZ Filter Coefficient
42.	90	Write Adaptive B Filter Control
43.	91	Read Adaptive B Filter Control
44.	64	Write Operating Functions II
45.	65	Read Operating Functions II

Notes:

1. **Code changes with function.*
2. ***All codes not listed are reserved by AMD and should not be used.*

COMMAND STRUCTURE

This section describes in detail each of the MPI commands. Each of the commands is shown along with the format of any additional data bytes that follow. For details of the filter coefficients of the for $C_{xy}m_{xy}$, please refer to the *Description of Coefficients* section.

1. Deactivate (Standby State)

(00h)

	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
Command	0	0	0	0	0	0	0	0

During the Inactive state (of one or more channels):

a) All of the programmed information is retained.
b) The Microprocessor Interface (MPI) remains active.
c) The PCM outputs are in high impedance and the PCM inputs are disabled.
d) The analog output is tied to 2.1 V through an internal resistor (~3 kΩ).

2. Software Reset

(02h)

	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
Command	0	0	0	0	0	0	1	0

The software reset state of the device is:

a) The channel is placed in the Inactive (standby) mode.
b) GX, GR, X, R, B, and Z filters are disabled with coefficients retained.
c) AX and AR are set to unity and AISN gain is set to 0.
d) The Adaptive B feature is disabled.
e) A-law is selected.
f) All SLIC I/O lines are configured as inputs.
g) Normal conditions are selected (see Command 4).

3. No Operation

(06h)

	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
Command	0	0	0	0	0	1	1	0

4. Reset to Normal Conditions

(08h)

	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
Command	0	0	0	0	1	0	0	0

Reset to Normal Conditions performs the following operations:

a) Does not insert 6 dB loss in receive path.
b) Receive and transmit paths are not cutoff.
c) High-pass filter is enabled.
d) Test modes are turned off.

5. Activate (Operational State)

(0Eh)

	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
Command	0	0	0	0	1	1	1	0

This command places the device in the Active mode. No valid PCM data is transmitted until after the second FS pulse is received following the execution of the Activate command.

6. MCLK Selection

(10h/12h)

	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
Command	0	0	0	1	0	0	A	0

MCLK may be selected to operate from a 2.048 MHz or 4.096 MHz external clock. MCLK selection on either channel affects both channels.

A = 0: 2.048 MHz
A = 1: 4.096 MHz

7. Write Transmit Time Slot and PCM Highway Selection

(40h)

	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
Command	0	1	0	0	0	0	0	0
Output Data	PCM	TS	TS	TS	TS	TS	TS	TS

PCM = 0: Highway A
PCM = 1: Highway B
TS: Time slot number 0 to 127

The PCM Highway B is not available on the Am79C031(A). The Transmit section of both channels must not be set to the same time slot on the same output port simultaneously.

8. Read Transmit Time Slot and PCM Highway Selection

(41h)

	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
Command	0	1	0	0	0	0	0	1
Output Data	PCM	TS	TS	TS	TS	TS	TS	TS

9. Write Receive Time Slot and PCM Highway Selection

(42h)

	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
Command	0	1	0	0	0	0	1	0
Output Data	PCM	TS	TS	TS	TS	TS	TS	TS

PCM = 0: Highway A
PCM = 1: Highway B
TS: Time slot number 0 to 127

The PCM Highway B is not available on the Am79C031(A).

10. Read Receive Time Slot and PCM Highway Selection

(43h)

	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
Command	0	1	0	0	0	0	1	1
Output Data	PCM	TS	TS	TS	TS	TS	TS	TS

11. Write Transmit Clock Slot, Receive Clock Slot, and Transmit Clock Edge (44h)

	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
Command	0	1	0	0	0	1	0	0
Input Data	RSVD	XE	RCS	RCS	RCS	TCS	TCS	TCS

TCS: Transmit Clock Slot number 0–7

RCS: Receive Clock Slot number 0–7

XE=0 Transmit on negative edge of PCLK

XE = 1 Transmit on positive edge of PCLK

RSVD: Reserved. Always write as 0, but 0 is not guaranteed when read.

Note: *XE = 1 should not be programmed unless the PCM delay is removed (i.e., PCD = 1). The XE bit is set for both channels when written to either channel. If XE = 1, the maximum PCM clock rate becomes 4.096 MHz.*

12. Read Transmit Clock Slot, Receive Clock Slot, and Transmit Clock Edge (45h)

	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
Command	0	1	0	0	0	1	0	1
Output Data	RSVD	XE	RCS	RCS	RCS	TCS	TCS	TCS

RSVD: Reserved. Always write as 0, but 0 is not guaranteed when read.

13. Write AISN, PCM Delay, and Analog Gains (50h)

	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
Command	0	1	0	1	0	0	0	0
Input Data	PCD	AX	AR	A	B	C	D	E

PCM Delay:

PCD = 0* Delay inserted (SLAC device compatible)
PCD = 1 Delay removed (high speed)

Transmit Analog Gain:

AX = 0* 0 dB gain
AX = 1 6.02 dB gain

Receive Analog Loss:

AR = 0* 0 dB loss
AR = 1 6.02 dB loss

AISN coefficient: A, B, C, D, E

The Analog Impedance Scaling Network (AISN) gain can be varied from –0.9375 to 0.9375 in multiples of 0.0625. The gain coefficient is decoded using the following equation:

$$h_{AISN} = 0.0625[(A \bullet 2^4 + B \bullet 2^3 + C \bullet 2^2 + D \bullet 2^1 + E \bullet 2^0) - 16]$$

where h_{AISN} is the gain of the AISN and A, B, C, D, and E = 0 or 1. A value of ABCDE = 10000 implements a special digital Loopback mode, and a value of ABCDE = 00000 indicates a gain of 0 (cutoff).

* Power-up default value.

Note: *Maximum PCLK frequency with PCM delay inserted (PCD = 0) is: 4.096 MHz.*

14. Read AISN, PCM Delay, and Analog Gains

(51h)

	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
Command	0	1	0	1	0	0	0	1
Output Data	PCD	AX	AR	A	B	C	D	E

15. Write SLIC Output Register

(52h)

	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
Command	0	1	0	1	0	0	1	0
Input Data	RSVD	RSVD	RSVD	C5	C4	C3	C2	C1

C1 through C5 are set to 1 or 0. The data appears latched on the C1 through C5 SLIC I/O pins, provided they are set in the Output mode (see Command 17). The data sent to any of the pins set to the Input mode are latched, but do not appear at the pins.

RSVD Reserved. Always write as 0, but 0 is not guaranteed when read.

16. Read SLIC Pins

(53h)

	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
Command	0	1	0	1	0	0	1	1
Output Data	RSVD	RSVD	RSVD	C5	C4	C3	C2	C1

The logic state of pins C1 through C5 is read regardless of the direction programmed into the Input/Output register.

17. Write SLIC Input/Output Direction

(54h)

	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
Command	0	1	0	1	0	1	0	0
Input Data	RSVD	RSVD	RSVD	C5	C4	C3	C2	C1

Pins C1x through C5x are set to input or output modes individually. Pins C51 and C52 are not available on the Am79C03(A). C51 and C52 pins are output only on the Am79C031(A) and must be programmed as outputs with this command. All unused SLIC I/O pins should be programmed as outputs to reduce power consumption.

Data bit A sets pins C51 or C52.
Data bit B sets pins C41 or C42.
Data bit C sets pins C31 or C32.
Data bit D sets pins C21 or C22.
Data bit E sets pins C11 or C12.
Data bit = 0; Pin mode = Input.*
Data bit = 1; Pin mode = Output.

RSVD Reserved. Always write as 0, but 0 is not guaranteed when read.

* Power up default value

18. Read SLIC Input/Output Direction, Channel Status Bit, and Power Interrupt Bit (55h)

	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
Command	0	1	0	1	0	1	0	1
Output Data	PI	CSTAT	RSVD	A	B	C	D	E

Power Interruption

PI = 0 — There has not been a power interruption since the last software reset command.

PI = 1 — A power interruption has been previously detected requiring the DSLAC device to be completely reprogrammed. This bit is cleared by issuing a software reset command.

Channel Status

CSTAT = 0 — Channel is inactive (Standby mode).

CSTAT = 1 — Channel is active.

19. Write Operating Functions

(60h)

	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
Command	0	1	1	0	0	0	0	0
Input Data	ABF	A/μ	EGR	EGX	EX	ER	EZ	EB

Adaptive B Filter

ABF = 0* B filter Nonadaptive mode
PCD = 1 B filter Adaptive mode

A-law/μ-law

A/m = 0* A-law coding
A/m = 1 μ-law coding

GR Filter

EGR = 0* GR filter disabled
EGR = 1 GR filter enabled

GX Filter

EGX = 0* GX filter disabled
EGX = 1 GX filter enabled

X Filter

EX = 0* X filter disabled
EX = 1 X filter enabled

R Filter

ER = 0* R filter disabled
ER = 1 R filter enabled

Z Filter

EZ = 0* Z filter disabled
EZ = 1 Z filter enabled

B Filter

EB = 0* B filter disabled
EB = 1 B filter enabled

* Power up default value.

Note: *The enable adaptive B filter command only is effective when used with the enable B filter command.*

20. Read Operating Functions

(61h)

	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
Command	0	1	1	0	0	0	0	1
Input Data	ABF	A/μ	EGR	EGX	EX	ER	EZ	EB

21. Write Operating Conditions

(70h)

	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
Command	0	1	1	1	0	0	0	0
Input Data	CTP	CRP	HPF	RG	ALB	TLB	RSVD	RSVD

Cut off Transmit Path

CTP = 0* Transmit path connected
CTP = 1 Transmit path cut off (see note)

Cut off Receive Path

CRP = 0* Receive path connected
CRP = 1 Receive path cut off

High-Pass Filter

HPF = 0* High-pass filter enabled
HPF = 1 High-pass filter disabled

Receive Path Gain

RG = 0* 6 dB loss not inserted
RG = 1 6 dB loss inserted

Analog Loopback

ALB = 0* Analog loopback disabled
ALB = 1 Analog loopback enabled

TSA Loopback

TLB = 0* TSA loopback disabled
TLB = 1 TSA loopback enabled

RSVD = Reserved. Always write as 0, but 0 is not guaranteed when read.

* Power up default value.

Note: *The B Filter still is connected across the PCM highway during Receive Cut off. Accompany Receive Cut off with a B Filter disable command.*

22. Read Operating Conditions

(71h)

	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
Command	0	1	1	1	0	0	0	1
Output Data	CTP	CRP	HPF	RG	ALB	TLB	RSVD	RSVD

23. Read Revision Code Number

(73h)

	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
Command	0	1	1	1	0	0	1	1
Output Data	#	#	#	#	#	#	#	#

This command returns an 8-bit number describing the revision number of the DSLAC device. It can be read on either channel.

24. Write GX Filter Coefficients

(80h)

	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
Command	1	0	0	0	0	0	0	0
Input Data Byte 1	C40	m40			C30	m30		
Input Data Byte 2	C20	m20			C10	m10		

The coefficient for the GX filter is defined as:

$$H_{GX} = 1 + (C10 \bullet 2^{-m10}\{1 + C20 \bullet 2^{-m20}[1 + C30 \bullet 2^{-m30}(1 + C40 \bullet 2^{-m40})]\})$$

25. Read GX Filter Coefficients

(81h)

	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
Command	1	0	0	0	0	0	0	1
Output Data Byte 1	C40	m40			C30	m30		
Output Data Byte 2	C20	m20			C10	m10		

26. Write GR Filter Coefficients

(82h)

	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
Command	1	0	0	0	0	0	1	0
Input Data Byte 1	C40	m40			C30	m30		
Input Data Byte 2	C20	m20			C10	m10		

The coefficient for the GR filter is defined as:

$$H_{GR} = C10 \bullet 2^{-m10}\{1 + C20 \bullet 2^{-m20}[1 + C30 \bullet 2^{-m30}(1 + C40 \bullet 2^{-m40})]\}$$

27. Read GR Filter Coefficients

(83h)

	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
Command	1	0	0	0	0	0	1	1
Output Data Byte 1	C40	m40			C30	m30		
Output Data Byte 2	C20	m20			C10	m10		

28. Write Z Filter Coefficients

(84h)

	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
Command	1	0	0	0	0	1	0	0
Input Data Byte 1	C45	m45			C35	m35		
Input Data Byte 2	C25	m25			C15	m15		
Input Data Byte 3	C40	m40			C30	m30		
Input Data Byte 4	C20	m20			C10	m10		
Input Data Byte 5	C41	m41			C31	m31		
Input Data Byte 6	C21	m21			C11	m11		
Input Data Byte 7	C42	m42			C32	m32		
Input Data Byte 8	C22	m22			C12	m12		
Input Data Byte 9	C43	m43			C33	m33		
Input Data Byte 10	C23	m23			C13	m13		
Input Data Byte 11	C44	m44			C34	m34		
Input Data Byte 12	C24	m24			C14	m14		
Input Data Byte 13	C46	m46			C36	m36		
Input Data Byte 14	C26	m26			C16	m16		

The Z-transform equation for the Z filter is defined as:

$$H_z(z) = Z_0 + Z_1 z^{-1} + Z_2 z^{-2} + Z_3 z^{-3} + Z_4 z^{-4} + \frac{Z_5}{1 - Z_6 z^{-1}}$$

The coefficients are defined as:

$$Z_i = Cli \bullet 2^{-m1i}\{1 + C2i \bullet 2^{-m2i}[1 + C3i \bullet 2^{-m3i}(1 + C4i \bullet 2^{-m4i})]\}$$

for i = 0, 1, 2, 3, 4, 5, 6.

29. Read Z Filter Coefficients

(85h)

	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
Command	1	0	0	0	0	1	0	1
Output Data Byte 1	C45	m45			C35	m35		
Output Data Byte 2	C25	m25			C15	m15		
Output Data Byte 3	C40	m40			C30	m30		
Output Data Byte 4	C20	m20			C10	m10		
Output Data Byte 5	C41	m41			C31	m31		
Output Data Byte 6	C21	m21			C11	m11		
Output Data Byte 7	C42	m42			C32	m32		
Output Data Byte 8	C22	m22			C12	m12		
Output Data Byte 9	C43	m43			C33	m33		
Output Data Byte 10	C23	m23			C13	m13		
Output Data Byte 11	C44	m44			C34	m34		
Output Data Byte 12	C24	m24			C14	m14		
Output Data Byte 13	C46	m46			C36	m36		
Output Data Byte 14	C26	m26			C16	m16		

30. Write B Filter Coefficients

(86h)

	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
Command	1	0	0	0	0	1	1	0
Input Data Byte 1	C30	m30			C20	m20		
Input Data Byte 2	C10	m10			C31	m31		
Input Data Byte 3	C21	m21			C11	m11		
Input Data Byte 4	C32	m32			C22	m22		
Input Data Byte 5	C12	m12			C33	m33		
Input Data Byte 6	C23	m23			C13	m13		
Input Data Byte 7	C34	m34			C24	m24		
Input Data Byte 8	C14	m14			C35	m35		
Input Data Byte 9	C25	m25			C15	m15		
Input Data Byte 10	C36	m36			C26	m26		
Input Data Byte 11	C16	m16			C37	m37		
Input Data Byte 12	C27	m27			C17	m17		
Input Data Byte 13	C48	m48			C38	m38		
Input Data Byte 14	C28	m28			C18	m18		

The Z-transform equation for the B filter is defined as:

$$H_B(z) = B_0 + B_1 z^{-1} + B_2 z^{-2} + B_3 z^{-3} + B_4 z^{-4} + B_5 z^{-5} + B_6 z^{-6} + \frac{B_7 z^{-7}}{1 - B_8 z^{-1}}$$

The coefficients for the FIR B section and the gain of the IIR B section are defined as:

$$B_i = Cli \bullet 2^{-m1i}[1 + C2i \bullet 2^{-m2i}(1 + C3i \bullet 2^{-m3i})]$$

The feedback coefficient of the IIR B section is defined as:

$$B_8 = C18 \bullet 2^{-m18}\{1 + C28 \bullet 2^{-m28}[1 + C38 \bullet 2^{-m38}(1 + C48 \bullet 2^{-m48})]\}$$

Warning: *Not all B filter coefficients are "valid" to initiate adaptive balance. One valid coefficient is set as: 2A F2 AF 2A F2 AF 2A F2 AF 2A F2 AF 0A 80, which corresponds to all FIR coefficients (B0–B7) equal to zero, and the IIR denomination coefficient (B8) equal to 1/2. Other valid coefficients that may reduce the time to convergence of the algorithm may be obtained by reading back the registers after adaptive balance has been run (see Command 31).*

31. Read B Filter Coefficients

(87h)

	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
Command	1	0	0	0	0	1	1	1
Output Data Byte 1	C30	m30			C20	m20		
Output Data Byte 2	C10	m10			C31	m31		
Output Data Byte 3	C21	m21			C11	m11		
Output Data Byte 4	C32	m32			C22	m22		
Output Data Byte 5	C12	m12			C33	m33		
Output Data Byte 6	C23	m23			C13	m13		
Output Data Byte 7	C34	m34			C24	m24		
Output Data Byte 8	C14	m14			C35	m35		
Output Data Byte 9	C25	m25			C15	m15		
Output Data Byte 10	C36	m36			C26	m26		
Output Data Byte 11	C16	m16			C37	m37		
Output Data Byte 12	C27	m27			C17	m17		
Output Data Byte 13	C48	m48			C38	m38		
Output Data Byte 14	C28	m28			C18	m18		

32. Write X Filter Coefficients

(88h)

	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
Command	1	0	0	0	1	0	0	0
Input Data Byte 1	C40	m40			C30	m30		
Input Data Byte 2	C20	m20			C10	m10		
Input Data Byte 3	C41	m41			C31	m31		
Input Data Byte 4	C21	m21			C11	m11		
Input Data Byte 5	C42	m42			C32	m32		
Input Data Byte 6	C22	m22			C12	m12		
Input Data Byte 7	C43	m43			C33	m33		
Input Data Byte 8	C23	m23			C13	m13		
Input Data Byte 9	C44	m44			C34	m34		
Input Data Byte 10	C24	m24			C14	m14		
Input Data Byte 11	C45	m45			C35	m35		
Input Data Byte 12	C25	m25			C15	m15		

The Z-transform equation for the X filter is defined as:

$$H_x(z) = X_0 + X_1 z^{-1} + X_2 z^{-2} + X_3 z^{-3} + X_4 z^{-4} + X_5 z^{-5}$$

The coefficients for the X filter are defined as:

$$X_i = C1i \bullet 2^{-m1i}\{1 + C2i \bullet 2^{-m2i}[1 + C3i \bullet 2^{-m3i}(1 + C4i \bullet 2^{-m4i})]\}$$

33. Read X Filter Coefficients

(89h)

	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
Command	1	0	0	0	1	0	0	1
Output Data Byte 1	C40	m40			C30	m30		
Output Data Byte 2	C20	m20			C10	m10		
Output Data Byte 3	C41	m41			C31	m31		
Output Data Byte 4	C21	m21			C11	m11		
Output Data Byte 5	C42	m42			C32	m32		
Output Data Byte 6	C22	m22			C12	m12		
Output Data Byte 7	C43	m43			C33	m33		
Output Data Byte 8	C23	m23			C13	m13		
Output Data Byte 9	C44	m44			C34	m34		
Output Data Byte 10	C24	m24			C14	m14		
Output Data Byte 11	C45	m45			C35	m35		
Output Data Byte 12	C25	m25			C15	m15		

34. Write R Filter Coefficients

(8Ah)

	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
Command	1	0	0	0	1	0	1	0
Input Data Byte 1	C40	m40			C30	m30		
Input Data Byte 2	C20	m20			C10	m10		
Input Data Byte 3	C41	m41			C31	m31		
Input Data Byte 4	C21	m21			C11	m11		
Input Data Byte 5	C42	m42			C32	m32		
Input Data Byte 6	C22	m22			C12	m12		
Input Data Byte 7	C43	m43			C33	m33		
Input Data Byte 8	C23	m23			C13	m13		
Input Data Byte 9	C44	m44			C34	m34		
Input Data Byte 10	C24	m24			C14	m14		
Input Data Byte 11	C45	m45			C35	m35		
Input Data Byte 12	C25	m25			C15	m15		

The Z-transform equation for the R filter is defined as:

$$H_R(z) = R_0 + R_1 z^{-1} + R_2 z^{-2} + R_3 z^{-3} + R_4 z^{-4} + R_5 z^{-5}$$

The coefficients for the R filter are defined as:

$$R_i = Cli \bullet 2^{-m1i}\{1 + C2i \bullet 2^{-m2i}[1 + C3i \bullet 2^{-m3i}(1 + C4i \bullet 2^{-m4i})]\}$$

35. Read R Filter Coefficients
(8Bh)

	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
Command	1	0	0	0	1	0	1	1
Output Data Byte 1	C40	m40			C30	m30		
Output Data Byte 2	C20	m20			C10	m10		
Output Data Byte 3	C41	m41			C31	m31		
Output Data Byte 4	C21	m21			C11	m11		
Output Data Byte 5	C42	m42			C32	m32		
Output Data Byte 6	C22	m22			C12	m12		
Output Data Byte 7	C43	m43			C33	m33		
Output Data Byte 8	C23	m23			C13	m13		
Output Data Byte 9	C44	m44			C34	m34		
Output Data Byte 10	C24	m24			C14	m14		
Output Data Byte 11	C45	m45			C35	m35		
Output Data Byte 12	C25	m25			C15	m15		

36. Write Echo Path Gain
(8Ch)

	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
Command	1	0	0	0	1	1	0	0
Input Data Byte 1	C80	m80			C70	m70		
Input Data Byte 2	C60	m60			C50	m50		
Input Data Byte 3	0	0	0	0	0	0	0	0
Input Data Byte 4	0	0	0	0	0	0	1	1

The equation for the Echo Path Gain is defined as:

$$EPG = 1 + C50 \bullet 2^{-m50}\{1 + C60 \bullet 2^{-m60}[1 + C70 \bullet 2^{-m70}(1 + C80 \bullet 2^{-m80})]\}$$

37. Read Echo Path Gain
(8Dh)

	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
Command	1	0	0	0	1	1	0	1
Output Data Byte 1	C80	m80			C70	m70		
Output Data Byte 2	C60	m60			C50	m50		
Output Data Byte 3	0	0	0	0	0	0	0	0
Output Data Byte 4	0	0	0	0	0	0	1	1

38. Write Error Level Threshold
(8Eh)

	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
Command	1	0	0	0	1	1	1	0
Input Data Byte 1	C20	m20			C10	m10		

The equation for the Error Level Threshold is defined as:

$$ELT = C10 \bullet 2^{-m10}(1 + C20 \bullet 2^{-m20})$$

39. Read Error Level Threshold

(8Fh)

	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
Command	1	0	0	0	1	1	1	1
Output Data Byte 1	C20	m20			C10	m10		

40. Write GZ Filter Coefficient

(92h)

	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
Command	1	0	0	1	0	0	1	0
Input Data	C10	m10			RSVD	RSVD	RSVD	RSVD

RSVD Reserved. Always write as 0, but 0 is not guaranteed when read.

The coefficient, GZ, is defined as:

$$GZ = C10 \bullet 2^{-m10}$$

The default value after any reset is GZ = 0 hex for a gain of 1.

41. Read GZ Filter Coefficient

(93h)

	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
Command	1	0	0	1	0	0	1	1
Output Data	C10	m10			RSVD	RSVD	RSVD	RSVD

42. Write Adaptive B Filter Control Coefficients

(90h)

New to Revision E	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
Command	1	0	0	1	0	0	0	0
Input Data	C20	m20			C10	m10		
Input Data	C21	m21			C11	m11		
Input Data	C32	m32			C22	m22		
Input Data	C12	m12			C33	m33		
Input Data	C23	m23			C13	m13		

The equations for the decorrelation threshold coefficients are:

$$DCR1 = C10 \bullet 2^{-m10}(1 + C20 \bullet 2^{-m20})$$

$$DCR2 = C11 \bullet 2^{-m11}(1 + C21 \bullet 2^{-m21})$$

The equation for the low level signal threshold coefficient is:

$$LST = C12 \bullet 2^{-m12}(1 + C22 \bullet 2^{-m22}[1 + C32 \bullet 2^{-m32}])$$

The equation for the digital prebalance threshold coefficient is:

$$DPB = C13 \bullet 2^{-m13}(1 + C23 \bullet 2^{-m23}[1 + C33 \bullet 2^{-m33}])$$

43. Read Adaptive B Filter Coefficients

(91h)

New to Revision E	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
Command	1	0	0	1	0	0	0	1
Output data	C20	m20			C10	m10		
Output data	C21	m21			C11	m11		
Output data	C32	m32			C22	m22		
Output data	C12	m12			C33	m33		
Output data	C23	m23			C13	m13		

44. Write Operating Functions 2

(64h)

New to Revision E	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
Command	0	1	1	0	0	1	0	0
Input data	RSVD	RSVD	RSVD	RSVD	RSVD	CHP	EAC	EPB

Chopper Clock Control

CHP = 0 Chopper Clock is 256 kHz
CHP = 1 Chopper Clock is 292.571 kHz

Adaptation Control

EAC = 0 LST, DCR1, and DCR2 are disabled
EAC = 1 LST, DCR1, and DCR2 are enabled
EPB = 0 DPB is disabled
EPB = 1 DPB is enabled

45. Read Operating Functions 2

(65h)

New to Revision E	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
Command	0	1	1	0	0	1	0	1
Output data	RSVD	RSVD	RSVD	RSVD	RSVD	CHP	EAC	EPB

RSVD Reserved. Always write as 0, but 0 is not guaranteed when read.

Programmable Filters

General Description of CSD Coefficients

The filter functions are performed by a series of multiplications and accumulations. A multiplication is accomplished by repeatedly shifting the multiplicand and summing the result with the previous value at that summation node. The method used in the DSLAC device is known as Canonic Signed Digit (CSD) multiplication and splits each coefficient into a series of CSD coefficients.

Each programmable FIR filter section has the following general transfer function:

$$HF(z) = h_0 + h_1 z^{-1} + h_2 z^{-2} + \ldots + h_n z^{-n} \qquad \text{Eq. (1)}$$

where the number of taps in the filter = n + 1.

The transfer function for IIR part of Z and B filters is:

$$HI(z) = \frac{1}{1 - h_{(n+1)} z^{-1}} \qquad \text{Eq. (2)}$$

The values of the user-defined coefficients (hi) are assigned via the MPI. Each of the coefficients (hi) is defined in the following general equation:

$$hi = B_1 2^{-M1} + B_2 2^{-M2} + \ldots + B_N 2^{-MN} \qquad \text{Eq. (3)}$$

where:

M_i = the number of shifts $\leq M_i + 1$

B_i = sign = ±1

N = number of CSD coefficients

The value of h_i in Equation 3 represents a decimal number that is broken down into a sum of successive values of:

±1.0 multiplied by 2^{-0}, or 2^{-1}, or $2^{-2}...2^{-7}...$

or

±1.0 multiplied by 1, or 1/2, or 1/4...1/128...

The limit on the negative powers of 2 is determined by the length of the registers in the ALU.

The coefficient h_i in Equation 3 can be considered to be a value made up of N binary 1s in a binary register where the leftmost part represents whole numbers, the rightmost part represents decimal fractions, and a decimal point separates them. The first binary 1 is shifted M1 bits to the right of the decimal point, the second binary 1 is shifted M2 bits to the right of the decimal point, the third binary 1 is shifted M3 bits to the right of the decimal point, and so on.

Note that when M1 is 0, the resulting value is a binary 1 in front of the decimal point, that is, no shift. If M2 also is 0, the result is another binary 1 in front of the decimal point, giving a total value of binary 10 in front of the decimal point (i.e., a decimal value of 2.0). The value of N, therefore, determines the range of values the coefficient h_i can take (e.g., if N = 3, the maximum and minimum values are ±3, and if N = 4, the values are between ±4).

Detailed Description of DSLAC Device Coefficients

The CSD coding scheme in the DSLAC device uses a value called mi, where m1 represents the distance shifted right of the decimal point for the first binary 1. m2 represents the distance shifted to the right of the previous binary 1, and m3 represents the number of shifts to the right of the second binary 1. Note that the range of values determined by N is unchanged. Equation 3 now is modified (in the case of N = 4) to:

$$h_i = B_1 2^{-M1} + B_2 2^{-M2} + B_3 2^{-M3} + B_4 2^{-M4} \qquad \text{Eq. (4)}$$

$$h_i = C_1 2^{-m1} + C_1 C_2 2^{-(m1+m2)} + C_1 C_2 C_3 2^{-(m1+m2+m3)} + C_1 C_2 C_3 C_4 2^{-(m1+m2+m3+m4)} \qquad \text{Eq. (5)}$$

$$h_i = C_1 2^{-m1} \bullet \{1 + C_2 2^{-m2} \bullet [1 + C_3 2^{-m3} \bullet (1 + C_4 2^{-m4})]\} \qquad \text{Eq. (6)}$$

where:

$$M_1 = m_1 \qquad B_1 = C_1$$
$$M_2 = m_1 + m_2 \quad \text{and} \quad B_2 = C_1 \bullet C_2$$
$$M_3 = m_1 + m_2 + m_3 \qquad B_3 = C_1 \bullet C_2 \bullet C_3$$
$$M_4 = m_1 + m_2 + m_3 + m_4 \qquad B_4 = C_1 \bullet C_2 \bullet C_3 \bullet C_4$$

In the DSLAC device, a coefficient, h_i, consists of N CSD coefficients, each being made up of 4 bits and formatted as Cxymxy, where Cxy is one bit (MSB) and mxy is 3 bits. Each CSD coefficient is broken down as follows:

Cxy is the sign bit (0 = positive, 1 = negative).

mxy is the 3-bit shift code. It is encoded as a binary number as follows:

000:	0 shifts
001:	1 shifts
010:	2 shifts
011:	3 shifts
100:	4 shifts
101:	5 shifts
110:	6 shifts
111:	7 shifts

y is the coefficient number (the i in h_i).

x is the position of this CSD coefficient position of the binary 1 represented by this CSD coefficient within the h_i coefficient. The most significant binary 1 is represented by x = 1. The next most significant binary 1 is represented by x = 2, and so on.

Thus, C13m13 represents the sign and the relative shift position for the first (most significant) binary 1 in the 4th (h3) coefficient.

The number of CSD coefficients, N, is limited to 4 in the GR, GX, R, X, Z, and the IIR part of the B filter, and 3 for the FIR part of the B filter. Note also that the GX filter coefficient equation is slightly different from that of the other filters.

$$h_{iGX} = 1 + h_i \qquad \text{Eq. (7)}$$

Please refer to the section detailing the commands for complete details on the programming of the coefficients.

Adaptive B Filter Overview

The DSLAC device B filter is designed to work with preprogrammed coefficients or with coefficients determined by an adaptive algorithm (Note: The adaptive transhybrid balance feature is guaranteed only on the Am79C02A/03A/031A versions). The adaptive algorithm can be operated in a mode where it continuously adapts or where it adapts for a short period, and then holds its value.

Operation with preprogrammed coefficients requires only the use of MPI Command 30 to feed in the coefficients. The Adaptive mode uses some preprogrammed coefficients and generates new ones using an algorithm, which by a series of iterations, minimizes the receive signal that is echoed in the transmit signal (due to mismatches in the SLIC, hybrid, and line). Adaptation applies to the FIR part of the filter only. Preprogrammed coefficients used to initiate the adaptive algorithm must be "valid" (shown under Command 30). Other valid coefficients may be obtained by using this coefficient, running adaptive balance, and then reading back the registers (refer to #30 in command structure).

In the continuous Adaptation mode, the algorithm is switched on (via MPI Command 19) after a call is connected and remains on until the call ends. In this way, the B filter is continually being optimized to the received signal.

In the Adapt and Freeze modes, the algorithm is used only when a line is brought into service and the DSLAC device is activated. The algorithm is switched on and is allowed to converge with the received signal, which is a bandlimited white noise signal generated in the exchange for this purpose. The noise signal need only be injected for less than a second to yield converged coefficients. The Adaptive mode then is switched off (via Command 19).

The converged coefficients may be read out of the DSLAC device (using MPI Command 31) and stored for future reference. The DSLAC device is now optimized for general input signals.

Adaptive Filter Programming

The purpose of the B filter is to cancel the received signal that leaks across the hybrid into the transmit path. The B filter transfer function must match (as closely as possible) the transfer function of the echo path.

There are two programmable registers associated with the adaptive B filtering. The Echo Path Gain (EPG) is a programmable value that predicts the amount of the receive signal leaking across the hybrid to the transmit path. The EPG is used as part of an algorithm, which stops the adaptive filter from iterating in the presence of signals from the subscriber line (nearend talker).

The Error Level Threshold (ELT) is a programmable value that determines the transhybrid loss the adaptive filter attempts to meet. The adaptive algorithm continues to iterate until it meets the loss requirement specified by the ELT. Both the EPG and ELT values are generated by the WinSLAC™ software program (formerly AmSLAC2™ software). Please refer to the software technical documentation.

User Test Modes

The DSLAC device supports testing by providing both digital and analog loopback paths as shown in Figure 8. In the TSA Loopback mode, the DR input is connected to the DX output in the Time Slot Assigner circuitry. The TSA Loopback mode is programmed via Command 21.

A different type of digital loopback is provided when the AISN register is programmed with a value of 10000. In this case, the AISN circuitry is disabled and the VOUT pad is connected internally to VIN. This allows the D/A and A/D converters to be included in the digital loopback test. This mode is programmed via Command 13. Note that the signal, which is connected internally from VOUT to VIN, also is present on the VOUT pin.

The VIN input can be connected to the VOUT output through the Z filter for analog loopback. The response of the line to low frequencies can be tested by disabling the high-pass filter. Additionally, the receive and transmit paths may be cut off.

A-Law and μ-Law Companding

Table 1 and Table 2 show the companding definitions used for A-law and μ-law PCM encoding.

Table 1. A-Law: Positive Input Values

1	2	3	4	5	6	7	8
Segment Number	# Intervals x Interval Size	Value at Segment End Points	Decision Value Number *n*	Decision Value x_n (*See Note 1*)	Character Signal pre Inversion of Even Bits Bit No. 1 2 3 4 5 6 7 8	Quantized Value (at Decoder Output) y_n	Decoder Output Value No.
		4096	(128)	(4096)			
7	16 x 128		127	3968	11111111	4032	128
			⋮	⋮	*See Note 2*	⋮	⋮
			113	2176			
		2048	112	2048	11110000	2112	113
6	16 x 64		⋮	⋮	*See Note 2*	⋮	⋮
			97	1088			
		1024	96	1024	11100000	1056	97
5	16 x 32		⋮	⋮	*See Note 2*	⋮	⋮
			81	544			
		512	80	512	11010000	528	81
4	16 x 16		⋮	⋮	*See Note 2*	⋮	⋮
			65	272			
		256	64	256	11000000	264	65
3	16 x 8		⋮	⋮	*See Note 2*	⋮	⋮
			49	136			
		128	48	128	10110000	132	49
2	16 x 4		⋮	⋮	*See Note 2*	⋮	⋮
			33	68			
		64	32	64	10100000	66	33
1	32 x 2		⋮	⋮	*See Note 2*	⋮	⋮
			1	2			
↓			0	0	10000000	1	1

Notes:

1. *4096 normalized value units correspond to TMAX = 3.14 dBm0.*
2. *The character signals are obtained by inverting the even bits of the signals of column 6. Before this inversion, the character signal corresponding to positive input values between two successive decision values numbered n and n+1 (see column 4) is 128+n, expressed as a binary number.*
3. *The value at the decoder output is* $y_n = \frac{x_{n-1} + x_n}{2}$ *, for n = 1,...127, 128.*
4. *x_{128} is a virtual decision value.*
5. *Bit 1 is a 0 for negative input values.*

Table 2. μ-Law: Positive Input Values

1	2	3	4	5	6	7	8
Segment Number	# Intervals x Interval Size	Value at Segment End Points	Decision Value Number *n*	Decision Value x_n (*See Note 1*)	Character Signal pre Inversion of Even Bits Bit No. 1 2 3 4 5 6 7 8	Quantized Value (at Decoder Output) y_n	Decoder Output Value No.
		8159	(128)	(8159)			
8	16 x 256		127	7903	10000000	8031	127
			⋮	⋮	*See Note 2*	⋮	⋮
			113	4319			
		4063	112	4063	10001111	2112	112
7	16 x 128		⋮	⋮	*See Note 2*	⋮	⋮
			97	2143			
		2015	96	2015	10011111	1056	96
6	16 x 64		⋮	⋮	*See Note 2*	⋮	⋮
			81	1055			
		991	80	991	10101111	528	80
5	16 x 32		⋮	⋮	*See Note 2*	⋮	⋮
			65	511			
		479	64	479	10111111	264	64
4	16 x 16		⋮	⋮	*See Note 2*	⋮	⋮
			49	239			
		223	48	223	11001111	132	48
3	16 x 8		⋮	⋮	*See Note 2*	⋮	⋮
			33	103			
		95	32	95	11011111	99	32
2	16 x 4		⋮	⋮	*See Note 2*	⋮	⋮
			17	35			
		31	16	31	11101111	33	16
1	15 x 2		⋮	⋮	*See Note 2*	⋮	⋮
			2	3			
↓			1	1	11111110	2	1
	1 x 1				11111111	0	0
			0	0			

Notes:

1. *8159 normalized value units correspond to TMAX = 3.17 dBm0.*
2. *The character signal corresponding to positive input values between two successive decision values numbered n and n+1 (see column 4) is 255-n, expressed as a binary number.*
3. *The value at the decoder is $y_0 = x_0 = 0$ for n = 0, and $y_n = \frac{x_{n+1} + x_n}{2}$, for n = 1, 2,...127.*
4. *x_{128} is a virtual decision value.*
5. *Bit 1 is a 0 for negative input values.*

APPLICATIONS

The DSLAC device performs a programmable codec/filter function for two telephone lines. It interfaces to the telephone lines through either a transformer or an electronic SLIC, such as the AMD SLIC devices. The DSLAC device provides latched digital I/O to control and monitor two SLICs and has a selectable clock output to operate the switched mode regulator in an Am795XX family SLIC. When several line conditions must be matched, a single SLIC design can be used. The line characteristics (such as apparent impedance, attenuation, and hybrid balance) can be modified by programming each DSLAC channel's coefficients to meet desired performance. The DSLAC device can drive a transformer SLIC device without a buffer.

Connection to a PCM highway backplane is implemented by means of a simple buffer chip. Several DSLAC devices can be bused together into one bus interface buffer. An intelligent bus interface chip is not required because each DSLAC device provides its own buffer control. The DSLAC device can be controlled through the Microprocessor Interface, either by a microprocessor on the linecard or by a central processor.

Controlling the SLIC

SLIC Chopper Clock

The CHCLK output pin on the DSLAC device drives the CHCLK inputs for AMD switcher type SLICs. The CHCLK output is a 256 kHz or 293 kHz, TTL compatible signal that can drive two SLICs. It is active only when one or both channels are activated; otherwise, it is held high internally.

SLIC Input/Output

The Am79C02(A) and Am79C031(A) DSLAC device have five TTL compatible I/O pins (C1 to C5) for each channel. The Am79C03(A) DSLAC device has only C1 through C4 available. The outputs are programmed using Command 15 and the status is read back using Command 16. The direction of the pins (input or output) is specified by programming the SLIC I/O direction register (Command 17). The C5 pins of the Am79C031(A) are output only and must be programmed as outputs to be used.

Calculating Coefficients with WinSLAC Software

The WinSLAC software is a program that models the DSLAC device, the line conditions, the SLIC, and the linecard components to obtain the coefficients of the programmable filters of the DSLAC device and some of the transmission performance plots.

The following parameters relating to the desired line conditions and the components/circuits used in the linecard are to be provided as input to the program:

1. Line impedance or the balance impedance of the line is specified by the local PTT.
2. Desired two-wire impedance that is to appear at the linecard terminals of the exchange.
3. Tabular data for templates describing the frequency response and attenuation distortion of the design.
4. Relative analog signal levels for both the transmit and receive two-wire signals.
5. Component values and SLIC device selection for the analog portion of the line circuits.
6. Two-wire return loss template is usually specified by the local PTT.
7. Four-wire return loss template is usually specified by the local PTT.

The output from the WinSLAC program includes the coefficients of the GR, GX, Z, R, X, B, and EPG filters as well as transmission performance plots of two-wire return loss, receive and transmit path frequency response, and four-wire return loss.

The software supports the use of the AMD SLICs or allows entry of a SPICE netlist describing the behavior of any type of SLIC circuit.

Count Registers

Each of the three timers has a 16-bit count register. The contents of this register may be read or written by the processor at any time. If the register is written into while the timer is counting, the new value will take effect in the current count cycle.

The count registers should be programmed before attempting to use the timers, since they are not automatically initialized to zero.

Max Count Registers

Timers 0 and 1 have two MAX COUNT registers, while Timer 2 has a single MAX COUNT register. These contain the number of events the timer will count. In timers 0 and 1, the MAX COUNT register used can alternate between the two MAX COUNT values whenever the current maximum count is reached. A timer resets when the timer count register equals the MAX COUNT value being used. If the timer count register or the MAX COUNT register is changed so that the MAX COUNT is less than the timer count the timer does not immediately reset. Instead, the timer counts up to 0FFFFH, "wraps around" to zero, counts up to the MAX COUNT value, and then resets.

Timers and Reset

Upon RESET, the Timers will perform the following actions:

- All EN (Enable) bits are reset preventing timer counting.
- For Timers 0 and 1, the RIU bits are reset to zero and the ALT bits are set to one. This results in the Timer Out pins going High.
- The contents of the count registers are indeterminate.

INTERRUPT CONTROLLER

The 80C186 can receive interrupts from a number of sources, both internal and external. The internal interrupt controller serves to merge these requests on a priority basis, for individual service by the CPU.

Internal interrupt sources (Timers and DMA channels) can be disabled by their own control registers or by mask bits within the interrupt controller. The 80C186 interrupt controller has its own control register that sets the mode of operation for the controller.

The interrupt controller will resolve priority among requests that are pending simultaneously. Nesting is provided so interrupt service routines for lower priority interrupts may themselves be interrupted by higher priority interrupts. A block diagram of the interrupt controller is shown in Figure 19.

The 80C186 has a special slave mode in which the internal interrupt controller acts as a slave to an external master. The controller is programmed into this mode by setting bit 14 in the peripheral control block relocation register (see Slave Mode section).

MASTER MODE OPERATION

Interrupt Controller External Interface

Five pins are provided for external interrupt sources. One of these pins is NMI, the non-maskable interrupt. NMI is generally used for unusual events such as power-fail interrupts. The other four pins may be configured in any of the following ways:

- As four interrupt lines with internally generated interrupt vectors.
- As an interrupt line and interrupt acknowledge line pair (cascade mode) with externally generated interrupt vectors plus two interrupt input lines with internally generated vectors.
- As two pairs of interrupt/interrupt acknowledge lines (cascade mode) with externally generated interrupt vectors.

External sources in the cascade mode use externally generated interrupt vectors. When an interrupt is acknowledged, two $\overline{\text{INTA}}$ cycles are initiated and the vector is read into the 80C186 on the second cycle. The capability to interface to external 82C59A programmable interrupt controllers is provided when the inputs are configured in cascade mode.

Interrupt Controller Modes of Operation

The basic modes of operation of the interrupt controller in master mode are similar to the 82C59A. The interrupt controller responds identically to internal interrupts in all three modes; the difference is only in the interpretation of function of the four external interrupt pins. The interrupt controller is set into one of these three modes by programming the correct bits in the INT0 and INT1 control registers. The modes of interrupt controller operation are as follows:

Fully Nested Mode

When in the fully nested mode four pins are used as direct interrupt requests as in Figure 20. The vectors for these four inputs are generated internally. An in-service bit is provided for every interrupt source. If a lower-priority device requests an interrupt while the in-service bit (IS) is set, no interrupt will be generated by the interrupt controller. In addition, if another interrupt request occurs from the same interrupt source while the in-service bit is set, no interrupt will be generated by the interrupt controller. This allows interrupt service routines to operate

with interrupts enabled, yet be suspended only by interrupts of higher priority than the in-service interrupt.

When a service routine is completed, the proper IS bit must be reset by writing the proper pattern to the EOI register. This is required to allow subsequent interrupts from this interrupt source and to allow servicing of lower-priority interrupts. An EOI command is executed at the end of the service routine just before the return from interrupt instruction. If the fully nested structure has been upheld, the next highest-priority source with its IS bit set is then serviced.

Cascade Mode

The 80C186 has four interrupt pins and two of them have dual functions. In the fully nested mode, the four pins are used as direct interrupt inputs and the corresponding vectors are generated internally. In the cascade mode, the four pins are configured into interrupt input-dedicated acknowledge signal pairs. The interconnection is shown in Figure 21. INT0 is an interrupt input interfaced to an 82C59A, while INT2/$\overline{\text{INTA0}}$ serves as the dedicated interrupt acknowledge signal to that peripheral. The same is true for INT1 and INT3/$\overline{\text{INTA1}}$. Each pair can selectively be placed in the cascade or non-cascade mode by programming the proper value into INT0 and INT1 control registers. The use of the dedicated acknowledge signals eliminates the need for the use of external logic to generate $\overline{\text{INTA}}$ and device select signals.

The primary cascade mode allows the capability to serve up to 128 external interrupt sources through the use of external master and slave 82C59As. Three levels of priority are created, requiring priority resolution in the 80C186 interrupt controller, the master 82C59As, and the slave 82C59As. If an external interrupt is serviced, one IS bit is set at each of these levels. When the interrupt service routine is completed, up to three end-of-interrupt commands must be issued by the programmer.

Special Fully Nested Mode

This mode is entered by setting the SFNM bit in INT0 or INT1 control register. It enables complete nestability with external 82C59A masters. Normally, an interrupt request from an interrupt source will not be recognized unless the in-service bit for that source is reset. If more than one interrupt source is connected to an external interrupt controller, all of the interrupts will be funneled through the same 80C186 interrupt request pin. As a result, if the external interrupt controller receives a higher-priority interrupt, its interrupt will not be recognized by the 80C186 controller until the 80C186 in-service bit is reset. In special fully nested mode, the 80C186 interrupt controller will allow interrupts from an external pin, regardless of the state of the in-service bit for an interrupt source, in order to allow multiple interrupts from a single pin. An in-service bit will continue to be set, however, to inhibit interrupts from other lower-priority 80C186 interrupt sources.

Special procedures should be followed when resetting IS bits at the end of interrupt service routines. Software polling of the IS register in the external master 82C59A is required to determine if there is more than one bit set. If so, the IS bit in the 80C186 remains active and the next interrupt service routine is entered.

Operation in a Polled Environment

The controller may be used in a polled mode if interrupts are undesirable. When polling, the processor disables interrupts and then polls the interrupt controller whenever it is convenient. Polling the interrupt controller is accomplished by reading the Poll Word (Figure 30). Bit 15 in the poll word indicates to the processor that an interrupt of high enough priority is requesting service. Bits 4–0 indicate to the processor the type vector of the highest-priority source requesting service. Reading the Poll Word causes the in-service bit of the highest-priority source to be set.

It is desirable to be able to read the Poll Word information without guaranteeing service of any pending interrupt, that is, not set the indicated in-service bit. The 80C186 provides a Poll Status Word, in addition to the conventional Poll Word, to allow this to be done. Poll Word information is duplicated in the Poll Status Word, but reading the Poll Status Word does not set the associated in-service bit. These words are located in two adjacent memory locations in the register file.

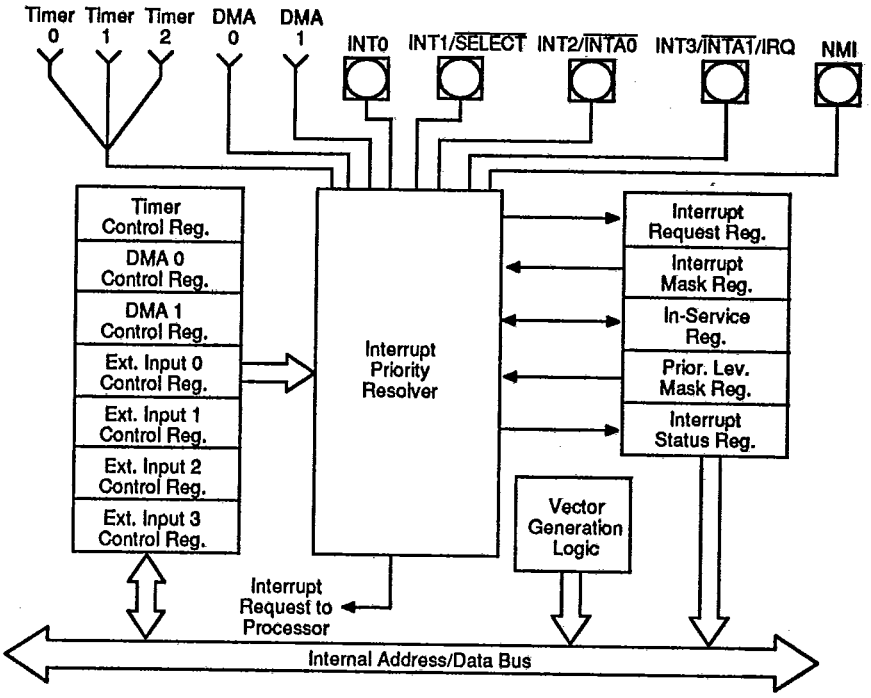


Figure 19. Interrupt Controller Block Diagram

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Master Mode Features

Programmable Priority

The user can program the interrupt sources into any of eight different priority levels. The programming is done by placing a 3-bit priority level (0–7) in the control register of each interrupt source. (A source with a priority level of 4 has higher priority over all priority levels from 5 to 7. Priority registers containing values lower than 4 have greater priority.) All interrupt sources have preprogrammed default priority levels (see Table 3).

If two requests with the same programmed priority level are pending at once, the priority ordering scheme shown in Table 3 is used. If the serviced interrupt routine reenables interrupts, it allows other interrupt requests to be serviced.

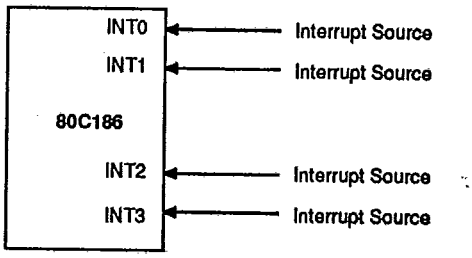

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Figure 20. Fully Nested (Direct) Mode Interrupt Controller Connections