PRELIMINARY

Am79C04(A)

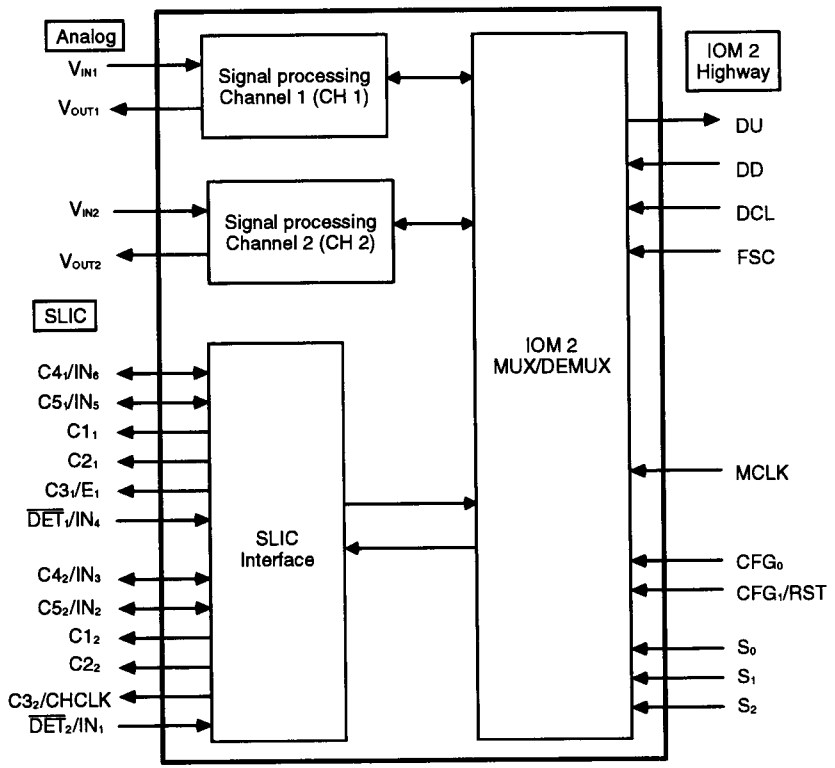
Dual Subscriber Line Audio-Processing Circuit (DSLAC™ Device)

Advanced Micro Devices

DISTINCTIVE CHARACTERISTICS

- **IOM 2 Interface**
  - —Control and PCM on one bus
  - —Data rate up to 4.096-MHz independent of master clock
- **Two independent channels**
- **Software programmable**
  - —SLIC impedance
  - —Trans-hybrid balance
  - —Transmit and receive gains
  - —Equalization
  - —Digital I/O pins with input debouncing
- **A-law or μ-law coding**
- **Adaptive trans-hybrid balance function (Am79C04/A only)**
- **2.048- or 4.096-MHz master clock**
- **Simple interface to Am795XX series SLICs**
- **Direct transformer drive**
- **Built-in test modes**
- **Low-power CMOS**
- **Mixed mode (analog and digital) impedance scaling**
- **Performance characteristics guaranteed over 12-dB gain range**

BLOCK DIAGRAM



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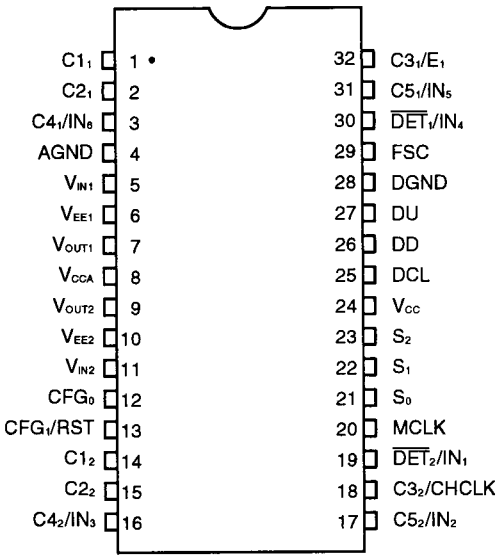
GENERAL DESCRIPTION

The DSLAC IC is designed to be used in telecommunication linecards for both PBX and central office telephone exchanges. It converts the analog signal from the subscriber to digital PCM-encoded signals for transmission on the IOM 2 highway and converts a PCM-encoded signal received from an IOM 2 highway to an analog signal to be sent to the subscribers. The advanced architecture of the DSLAC device implements two independent channels and employs digital filters to allow software control of transmission parameters.

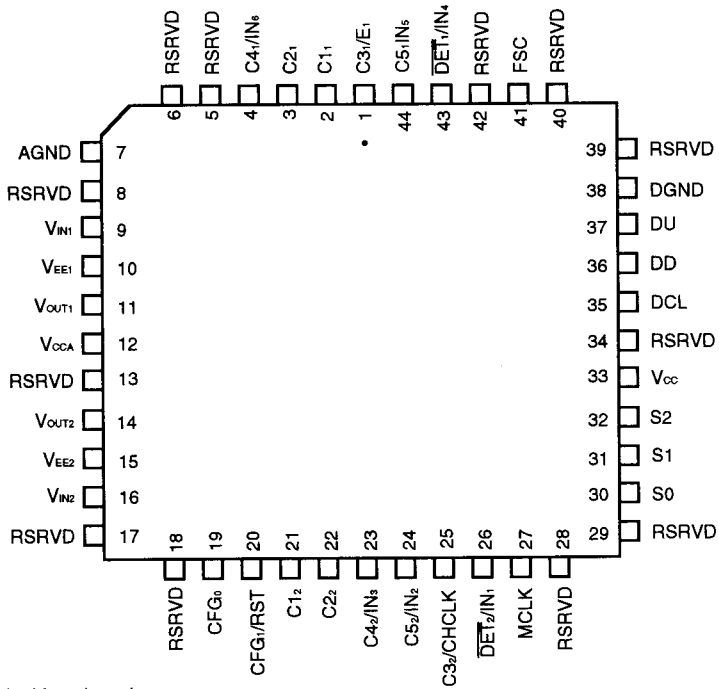
Advanced CMOS technology gives the economical DSLAC device both the functions and the low-power consumption needed by linecard designers to maximize linecard density at minimum cost. When used with two SLICs, the DSLAC device provides a complete dual-channel, software-configurable solution to the BORSCHT (Battery feed, Overvoltage protection, Ringing, Supervision, coding, Hybrid and Test) function.

CONNECTION DIAGRAMS
Top View

32-Pin DIP



44-Pin PLCC

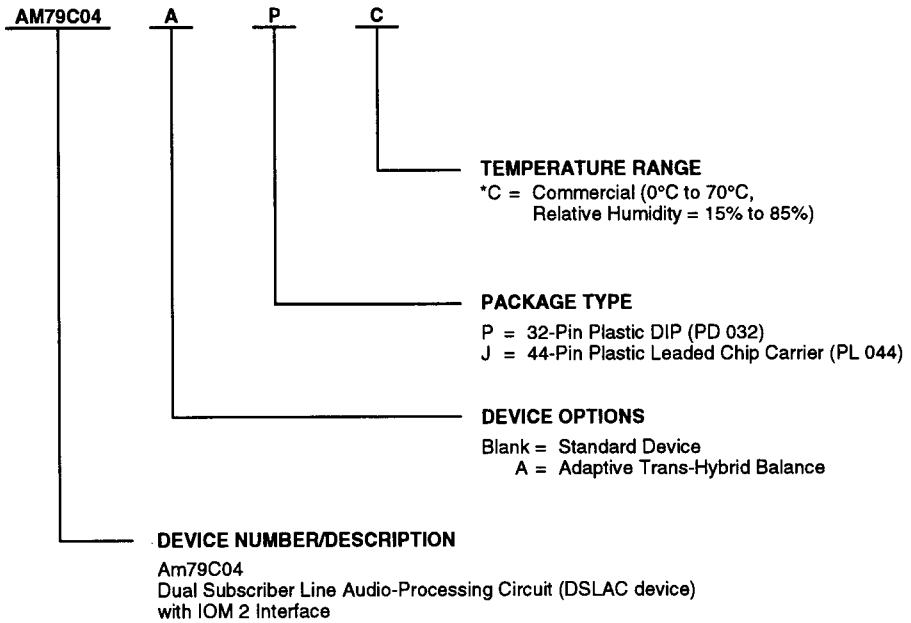


Note: 1. Pin 1 is marked for orientation purposes.
2. RSRVD = Reserved pin, should not be connected externally to any signal or supply.

ORDERING INFORMATION

Standard Products

AMD® standard products are available in several packages and operating ranges. The order number (Valid Combination) is formed by a combination of the elements below.



Valid Combinations	
AM79C04	AJC, APC, JC, PC

Valid Combinations

Valid Combinations lists configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations, to check on newly released combinations, and to obtain additional data on the AMD standard military grade products.

* The performance specifications contained in this data sheet are valid for the commercial temperature range only. See the DSLAC Extended Temperature Supplement for information on industrial temperature range (–40°C to +85°C) specifications.

PIN DESCRIPTION

AGND

Analog Ground

$C1_1$, $C2_1$, $C3_1/E_1$, $C1_2$, $C2_2$, $C3_2$/CHCLK

SLIC Outputs

These latched outputs are TTL compatible and may be used to control the operation of a SLIC or any other device associated with the subscriber line. $C1_1$, $C2_1$, and $C3_1/E_1$ are associated with Channel 1 and $C1_2$, $C2_2$, and $C3_2$/CHCLK are associated with Channel 2. The outputs are set to a Low level when the device is powered up. The C/I (Command/Indicate) channel is then used to write data to these pins.

In the Multiplexed mode, the $C3_2$/CHCLK output provides a 256-kHz or 273-kHz, 50% duty-cycle clock for use by two SLICs. The CHCLK frequency is synchronous to MCLK, but the phase relationship to MCLK is random. It is capable of driving two TTL inputs. As CHCLK, this output is only active when one or both channels are in the active state; otherwise it is held High. In the Multiplexed mode, the $C3_1/E_1$ output is used to control the $\overline{DET}$ output from an Am795XX series SLIC. A High level allows the SLIC to output its ground-key detect status while a Low level allows the SLIC to output the status of its off-hook detector. $C3_1/E_1$ can be programmed to go to a High level for approximately 16 µs every 1 to 15 ms to demultiplex the $\overline{DET}$ inputs.

$C5_1/IN_5$, $C5_2/IN_2$, $C4_1/IN_6$, $C4_2/IN_3$

SLIC Inputs/Outputs

Each pin may be programmed to be an input or output. $C4_1/IN_6$ and $C5_1/IN_5$ are associated with Channel 1 and $C4_2/IN_3$ and $C5_2/IN_2$ are associated with Channel 2. All pins are set to the Input mode when the device is powered up. If these pins are programmed to be outputs, they are written via the C/I channel. These lines are TTL compatible with latched outputs and may be used to control the operation of a SLIC or any other device associated with the subscriber line. If the pins are programmed to be inputs, $C4_1/IN_6$ will appear as C/I upstream bit 6, $C5_1/IN_5$ will appear as C/I upstream bit 5, $C4_2/IN_3$ will appear as C/I upstream bit 3, and $C5_2/IN_2$ will appear as C/I upstream bit 2. The Monitor Channel may be used to read the data on these pins.

CFG_1/RST, CFG_0

Configuration Number Assignment

These inputs allow a configuration number assignment from 0 to 5 by connecting them to either –5 V, ground, or +5 V. A voltage of greater than +2 V applied to the CFG_1/RST input causes the device to perform a hardware reset. For proper operation, CFG_0 should be hardwired to one of the DSLAC device's power supplies.

DCL

IOM 2 Clock

The IOM 2 clock determines the rate at which IOM 2 data is serially shifted into or out of the IOM 2 ports. This rate is twice the desired bit rate. The maximum clock frequency is 8.192 MHz and the minimum clock frequency is 512 kHz. The IOM 2 clock may be asynchronous to MCLK.

DD

IOM 2 Downstream Input

Downstream data is received serially on the DD port every 125 µs at half the DCL rate.

$\overline{DET_1}/IN_4$, $\overline{DET_2}/IN_1$

Loop Status Detector Inputs

In the Multiplexed mode, the $\overline{DET_1}/IN_4$ and $\overline{DET_2}/IN_1$ inputs are intended to monitor outputs from a Subscriber Line Interface Circuit (SLIC), providing off-hook and ground-key sensing on the same signal. When the E_1 output is Low, the IOM 2 DSLAC device interprets $\overline{DET_1}/IN_4$ or $\overline{DET_2}/IN_1$ as off-hook detector inputs. When E_1 is High, the DSLAC device interprets these pins as ground-key detector inputs. These pins may also be used in a non-Multiplexed mode, whereby the $\overline{DET_1}/IN_4$ input is routed to the C/I upstream bit 4 and the $\overline{DET_2}/IN_1$ input is routed to the C/I upstream bit 1. These inputs are TTL compatible.

DGND

Digital Ground

DU

IOM 2 Upstream Output

Upstream data is output serially on the DU pin every 125 µs at half the DCL rate. DU is high impedance between bursts. This pin is an open-drain output.

FSC

Frame Sync

The Frame Sync pulse is an 8-kHz signal which identifies the beginning of a frame. The IOM 2 DSLAC device references individual time slots with respect to the Frame Sync pulse. FSC is synchronized to DCL.

MCLK

Master Clock

The Master Clock is a 2.048- or 4.096-MHz clock input for use by the digital signal processor. DCL may be asynchronous to MCLK.

S_2–S_0

Time Slot Number Assignment

These inputs are used for a time slot number assignment from 0 to 7. They direct the DSLAC device to input and output PCM and programming information on one of eight time slots.

V_{CC}

Digital Power Supply

+5-V digital power supply.

V_{CCA}

Analog Power Supply

+5-V analog power supply must be connected to the +5-V digital power supply.

V_{EE1}

–5-V power supply—Channel 1.

V_{EE2}

–5-V power supply—Channel 2.

V_{IN1},V_{IN2}

Analog Inputs

The analog input is applied to the transmit path of the IOM 2 DSLAC device. The signal is sampled, digitally processed, and encoded for the IOM 2 PCM output. V_{IN1} is for Channel 1 and V_{IN2} is for Channel 2.

V_{OUT1},V_{OUT2}

Analog Outputs

The received PCM data is digitally processed and converted to an analog signal at the V_{OUT} pin. V_{OUT1} is for Channel 1 and V_{OUT2} is for Channel 2. These outputs may be used to drive a transformer SLIC directly.

FUNCTIONAL DESCRIPTION

The DSLAC device performs the Codec/filter functions associated with the four-wire section of the subscriber line circuitry in a digital switch. These functions involve converting an analog voice signal into digital PCM samples and converting digital PCM samples back into an analog signal. The PCM codes are 8-bit and are programmed to be either A-law or μ-law companded. During conversion, digital filters are used to band-limit the voice signals.

The user-programmable filters set the receive and transmit gain, perform the trans-hybrid balancing function, permit adjustment of the two-wire termination impedance, and provide frequency attenuation adjustment (equalization) of the receive and transmit paths. Adaptive trans-hybrid balancing is a feature of the Am79C04A. All programmable digital filter coefficients can be calculated using AmSLAC2™ software.

The independent channels allow the DSLAC device to function as two SLAC™ devices. All of the digital filtering is performed in digital signal processors operating from either a 2.048-MHz or 4.096-MHz external clock. The A/D, D/A, and signal processing are separate for each channel. The IOM 2 DSLAC device is available in a 32-pin DIP or a 44-pin PLCC.

This section describes the operation of the IOM 2 interface portion of the Am79C04 DSLAC device. The operational and signal processing features of the Am79C04 DSLAC device are identical to the Am79C02. A full description of these features can be found in the Am79C02 data sheet.

Operational Modes

See the Am79C02/3(A) Data Sheet.

Signal Processing

See the Am79C02/3(A) Data Sheet.

IOM 2 Interface

The IOM 2 Interface allows communication of both control and voice data between the IOM 2 highway and subscriber line circuits over a single pair of pins on the DSLAC device.

Upstream IOM 2 Interface

The upstream IOM 2 Interface logic (Figure 1) receives an 8-bit compressed voice code from each subscriber channel signal processor. Also input to the multiplexer are a Status and Control (SC) byte containing subscriber line status information and a Monitor (M) byte containing processor status information. These four inputs are formed into a 4-byte time slot by the upstream multiplexer and sent upstream via the DU pin on the DSLAC device. The frame sync (FSC) pulse identifies the beginning of a frame and all time slots are referenced to it.

The time slot is determined by the code appearing on the Time Slot Assignment pins, S_2–S_0. This allows up to eight 4-byte time slots (using a DCL of 4.096 MHz) in each frame. This feature allows any clock frequency between 512 kHz and 4.096 MHz (1 to 8 time slots) in a system. Frequencies between 4.096 MHz and 8.192 MHz are allowed, but only the first eight time slots are used.

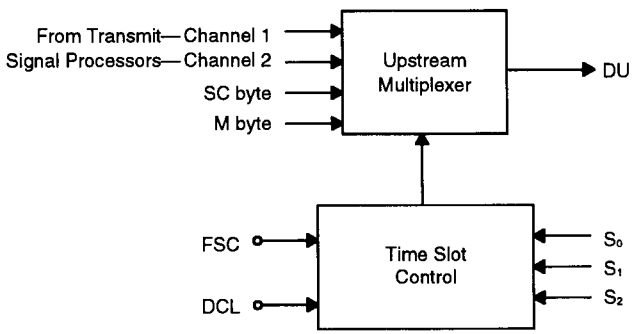


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Figure 1. Transmit (Upstream) IOM 2 Interface

Downstream IOM 2 Interface

The downstream IOM 2 Interface logic (Figure 2) demultiplexes a time slot (determined by the code on pins S_2–S_0) from the downstream data on input DD of the DSLAC device. The time slot contains voice data destined for each of the subscriber line signal processors. Also obtained from the time slot are an SC byte used for SLIC I/O programming and an M byte used for signal processor programming.

As in the upstream interface, one to eight 4-byte time slots are allowed in each frame (using a DCL frequency of 512 kHz to 4.096 MHz).

IOM 2 FORMAT AND COMMAND STRUCTURE

IOM 2 Format

A complete IOM 2 frame is sent upstream on the DU pin and received downstream on the DD pin every 125 µs. Each frame consists of up to eight 4-byte time slots. The overall structure of the IOM 2 frame is shown in Figures 3 and 4. Figure 3 shows the pattern when only a single IOM 2 time slot is used with a 256 kb/s bit rate. In this case the same 32-bit time slot is sent for every frame. Figure 4 shows the pattern when the maximum capacity of eight IOM 2 time slots is used. In this case, a bit rate of 2048 kb/s is needed. Any number of time slots between 1 and 8 can be used, provided the bit rate is adjusted such that a complete frame of time slots can occur every 125 µs. Note that the DCL clock input must be set at a frequency of twice the desired bit rate.

An individual 4-byte IOM 2 time slot contains the following:

- Two bytes, B1 and B2, containing voice data for two separate channels. One IOM 2 time slot can serve two analog subscriber lines.
- One Monitor (M) byte for reading and writing control data and DSP coefficients.
- One Signaling and Control (SC) byte containing a 6-bit Command/Indicate (C/I) field for control information and a 2-bit field with Monitor Receive and Monitor Transmit (MR and MX) bits for handshaking functions. All principal signaling information is carried on the C/I channel.

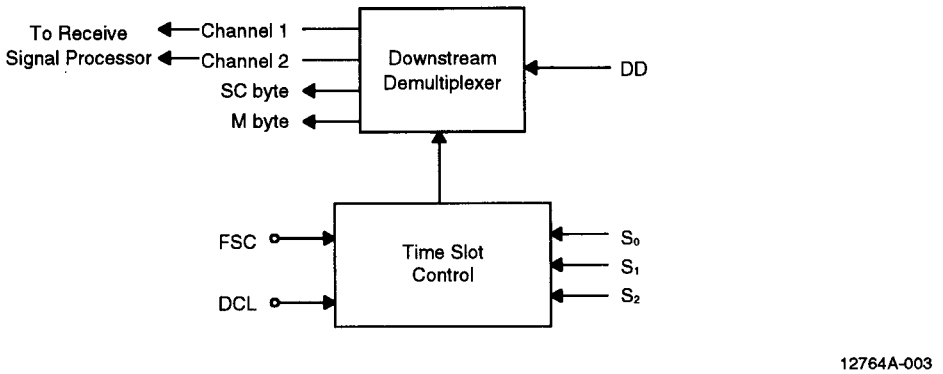


Figure 2. Receive (Downstream) IOM 2 Interface

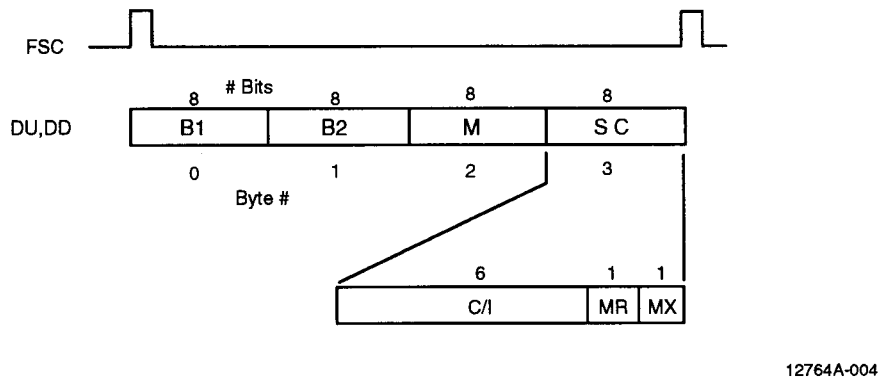


Figure 3. IOM 2 Time Slot Structure (256 kb/s)

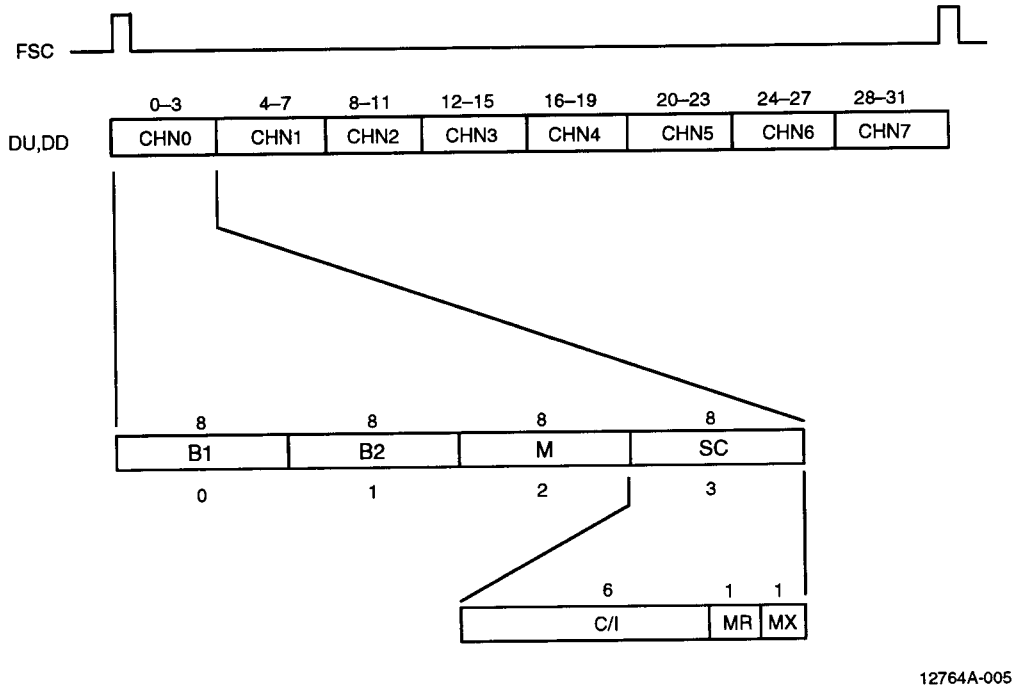


Figure 4. Multiplexed IOM 2 Time Slot Structure (2048 kb/s)

Programming the DSLAC device is accomplished by using the Signaling and Control (SC) and Monitor (M) bytes of the downstream IOM 2 channel. Additionally, data programmed previously may be read out for verification via the upstream IOM 2 channel M and SC bytes. For each subscriber channel, commands are provided to assign values to the following parameters:

Transmit gain

Receive loss

B-filter coefficients

X-filter coefficients

R-filter coefficients

Z-filter coefficients

Adaptive B-filter parameters

AISN coefficient

Switch-hook/ground-key sampling interval

Debounce time for SLIC input port

Read/Write SLIC input/output

Enable/disable GX filter

Enable/disable GR filter

Enable/disable B filter

Enable/disable X filter

Enable/disable R filter

Enable/disable Z filter

Enable/disable adaptive B filter

Enable/disable AX amplifier

Enable/disable AR amplifier

Selection of A-law or μ-law code

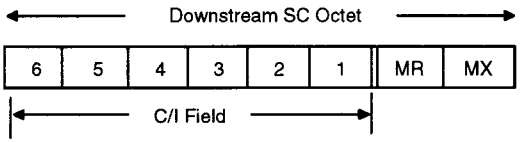
Selection of test modes

Selection of active or standby mode

The SC Channel Command Structure

Downstream C/I Channel

C/I bit 6, the first bit received of the SC octet, is the address bit and selects whether the data in C/I bits 5 through 1 is intended for Channel 1 or Channel 2. C/I bits 5 through 1 are directed to C_5 through C_1, provided these SLIC I/O bits are programmed to be outputs. Any data directed to a SLIC line programmed to be an input would be ignored.



Downstream Bit Definitions of C/I field:

Bit 6— Address bit. A0 selects Channel 1. A1 selects Channel 2

Bit 5—Data to C5 (if configured to be an output)

Bit 4—Data to C4 (if configured to be an output)

Bit 3—Data to C3 (in non-Multiplexed mode)

Bit 2—Data to C2

Bit 1—Data to C1

Figure 5 shows a flow chart describing the maximum security protocol. Whenever the received pattern of C/I bits 6 through 1 is different from the pattern currently in the C/I input register, the new pattern is loaded into a secondary C/I register. When the next pattern is received (in the following cycle), the following rules apply:

1. If the channel is addressed in the following frame and the received pattern corresponds to the pattern in the secondary register, then the new pattern is loaded into the C/I register.
2. If the channel is not addressed in the following frame, the newly received pattern is loaded into the secondary C/I and the content of the C/I register is unchanged.
3. If the channel is addressed in the following frame but the received pattern is different from the pattern in the secondary register and different from the pattern currently in the C/I register, the newly received pattern is loaded into the secondary C/I register.
4. If the channel is addressed in the following frame but the received pattern is the same as the pattern currently in the C/I register, the C/I register is unchanged. The result is the C/I field (6–1) must be the same for two consecutive frames before it is latched internally.

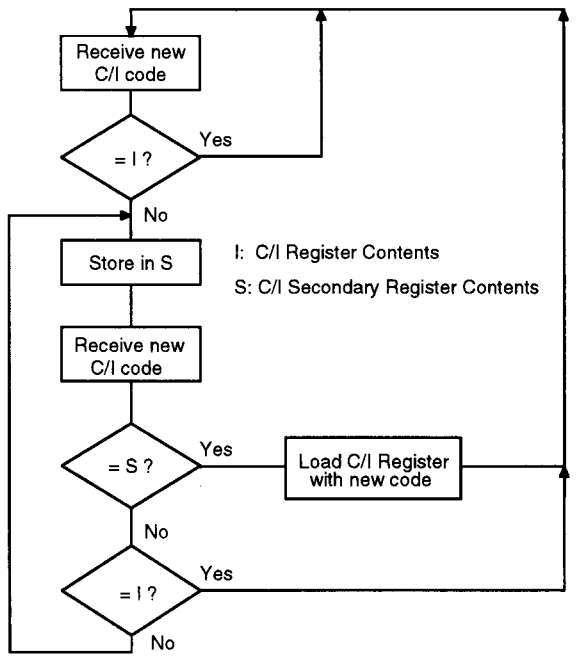


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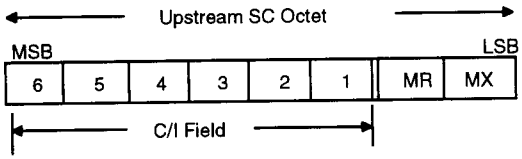
Figure 5. Security Procedure for C/I Downstream Byte

Upstream C/I Channel

There are three upstream C/I bits for each of the two analog lines. C/I bits 4, 5, and 6 are used for Channel 1, while C/I bits 1, 2, and 3 are used for Channel 2. Since the upstream receiving device will also be applying a last look security protocol to the complete 6-bit C/I field, and since changes to the C/I pattern will not be synchronized between two independent source devices, each new 3-bit pattern must be present in at least three consecutive 125-µs frames to ensure transfer.



Upstream Bit Definitions of C/I field:

Bit 6— $C4_1/IN_6$, if $C4_1/IN_6$ is programmed to be an input, High otherwise

***Bit 5**—Ground-key detect, Channel 1 (Multiplexed mode), or $C5_1/IN_5$ (non-Multiplexed mode if pin is programmed to be an input), or logic 1 (if pin is programmed to be an output)

***Bit 4**—Switch-hook detect, Channel 1 (Multiplexed mode), or $\overline{DET}_1/IN_4$ (non-Multiplexed mode)

Bit 3— $C4_2/IN_3$, if $C4_2/IN_3$ is programmed to be an input, High otherwise

***Bit 2**—Ground-key detect, Channel 2 (Multiplexed mode), or $C5_2/IN_2$ (non-Multiplexed mode if pin is programmed to be an input), or logic 1 (if pin is programmed to be an output)

***Bit 1**—Switch-hook detect, Channel 2 (Multiplexed mode), or $\overline{DET}_2/IN_1$ (non-Multiplexed mode)

*The data sent from the DSLAC device on bits 5, 4, 2, and 1 reflect the output from the corresponding debounce circuit, if enabled.

The Monitor Channel

Monitor Channel Protocol

The Monitor Channel is used to load internal device registers, to read the status of the device and the contents of the internal registers, and to provide supplementary signaling. Information is transferred on the Monitor Channel using the MR and MX bits of the fourth (SC) octet to provide a reliable method of handshaking.*

Monitor byte information is transferred via the IOM 2 Interface between read/write registers in the DSLAC device and upstream devices using the following procedure (refer to Figures 6 through 9). Note that the active state of the MX and MR bits is Low.

1. The MX bit remains in the inactive state for two or more consecutive frames to indicate an idle state or an end of transmission on the Monitor channel.
2. A start-of-message is initiated by the sender by a transition of the MX bit from the inactive state to the active state together with the first byte transmitted in the monitor data octet of the same frame. The transmission may start only if the MR bit received by the transmitter has previously been in the inactive state for at least two frames. The receiver acknowledges start-of-messages by a transition of its MR bit to the active state and confirms receipt of the first byte by holding the MR bit in the active state for a second frame.
3. The transition of the MX bit from the active to the inactive state indicates the transmission of a new byte. The transition of the MX bit from the inactive state to the active state in the following frame indicates a repeat of the new data byte.
4. The transition of the MX bit from the active to the inactive state, followed by a repeat of the inactive state for at least one or more frames, indicates end-of-message and that the content of the monitor data field is invalid.
5. The transition of the MR bit from the active to the inactive state acknowledges receipt of the first transmission of a new byte. The transition of the MR bit from the inactive to the active state in the following frame confirms the new byte has been correctly received.
6. The transition of the MR bit from the active to the inactive state, followed by a repeat of the inactive state for at least one more frame, acknowledges the receipt of end-of-message or, if received before end-of-message has been transmitted, requests to abort the message and repeat.
7. The active state of the MX bit, accompanied by further transmissions of the current data byte, may continue indefinitely (subject to a time out) for the purpose of flow control.
8. The active state of the MR bit may continue indefinitely (subject to a time out) for the purpose of flow control.

Each data byte is repeated until the transmission of a new byte, an end-of-message, or an abort.

*The IOM 2 DSLAC device will acknowledge receipt of a Monitor byte only if it is identical to the Monitor byte of the previous Frame. [This is the same security protocol used for the C/I bits (6–1).]

The circled numbers in Figures 6 through 9 refer to the sequence numbers listed previously:

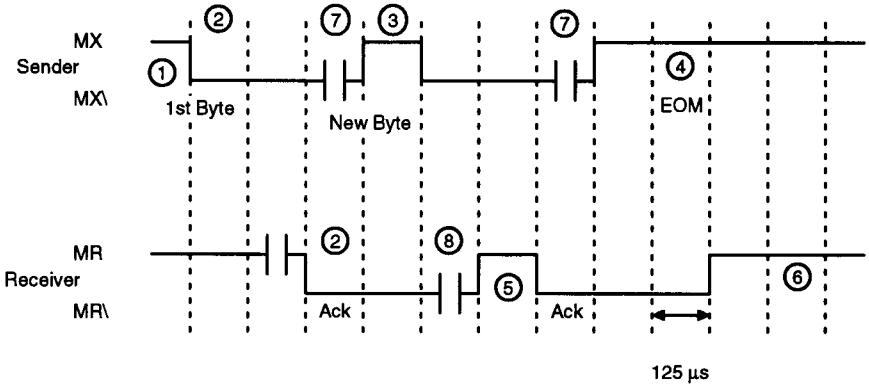


Figure 6. General Case of Multiple Byte Message Transfer

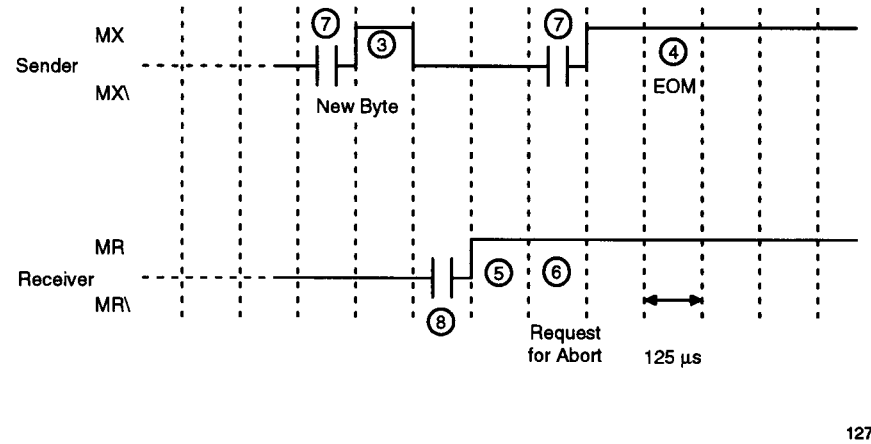


Figure 7. Abort Request on Multiple Byte Message Transfer

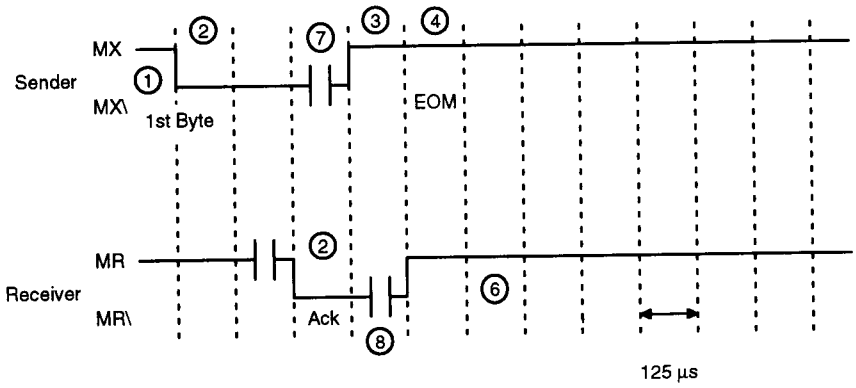


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Figure 8. Single Byte Message Transfer

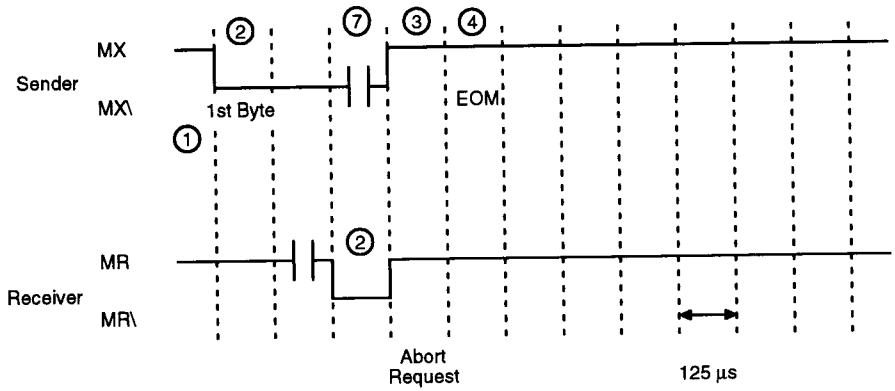

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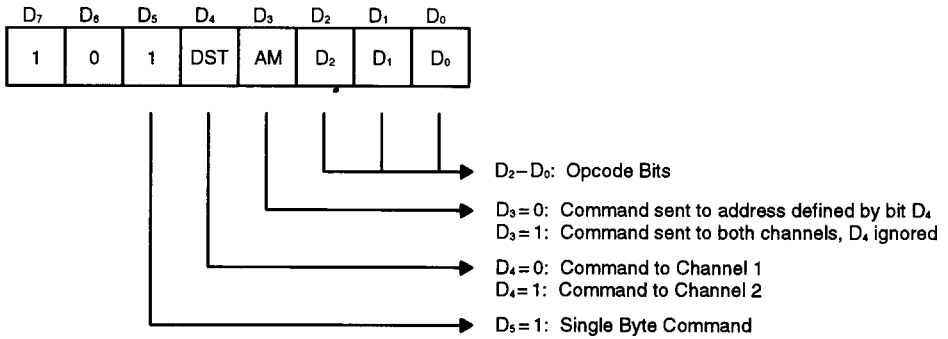
Figure 9. Abort Request on Single Byte Message Transfer

Monitor Channel Command Structure

The Monitor byte is the third byte in the 4-byte frame sent and received every 125 µs over the DU or DD pins. A Monitor command consists of one or more command bytes which may be followed with additional bytes of input data or may be followed by the DSLAC device sending out bytes of data over the DU pin. The first byte sent in a monitor channel message contains address, command, and read/write information conforming to the format in the diagrams below. Commands #25 through #40 are used to program the internal filters of the DSLAC device. Please refer to the Am79C02/3(A) DSLAC Preliminary Data Sheet for a complete description of the filter transfer functions and the coefficient structure.



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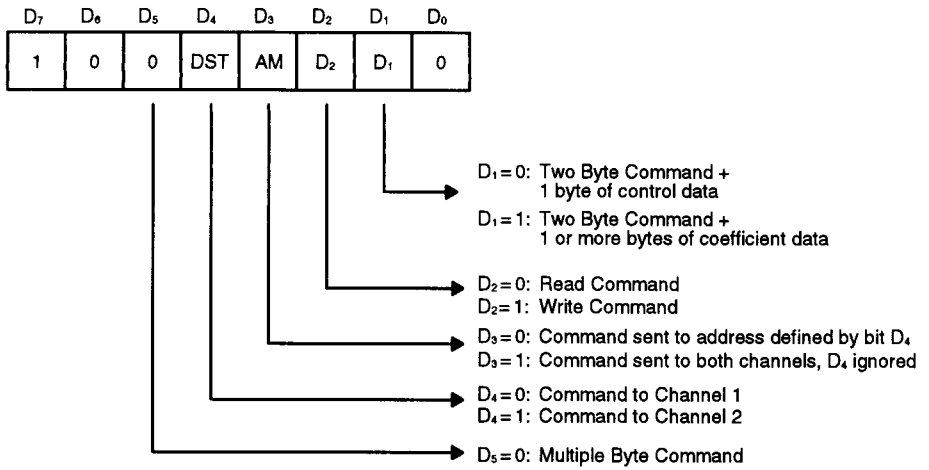

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Summary of Monitor Channel Commands

#	Byte 1	Byte 2	
1	101AB000		Inactivate (Standby mode)
2	101AB001		Reset
3	101AB010		No Operation
4	101AB011		Reset to Normal Conditions
5	101AB100		Activate
6	101AB110		MCLK = 2.048 MHz
7	101AB111		MCLK = 4.096 MHz
8	100A0000	00000000	Read Channel ID Information
9	100AB100	00000001	Write AISN & Analog Gains
10	100A0000	00000001	Read AISN & Analog Gains
11	100AB100	00000011	Write SLIC Input/Output Direction
12	100A0000	00000011	Read SLIC Input/Output Direction and Power Status
13	100A0000	00000100	Read SLIC Input/Output Registers
14	100AB100	00000101	Write Operating Functions
15	100A0000	00000101	Read Operating Functions
16	100AB100	00000110	AMD Internal Use Only
17	100A0000	00000110	AMD Internal Use Only
18	100AB100	00000111	Write Operating Conditions
19	100A0000	00000111	Read Operating Conditions
20	100A0000	00001000	Read Revision Code Number
21	100AB100	00001001	Write Ground-Key Sampling Interval
22	100A0000	00001001	Read Ground-Key Sampling Interval
23	100AB100	00001010	Write SLIC Upstream Input Debounce Time
24	100A0000	00001010	Read SLIC Upstream Input Debounce Time
25	100AB110	00000000	Write GX-Filter Coefficients
26	100A0010	00000000	Read GX-Filter Coefficients
27	100AB110	00000001	Write GR-Filter Coefficients
28	100A0010	00000001	Read GR-Filter Coefficients
29	100AB110	00000010	Write Z-Filter Coefficients
30	100A0010	00000010	Read Z-Filter Coefficients
31	100AB110	00000011	Write B-Filter Coefficients
32	100A0010	00000011	Read B-Filter Coefficients
33	100AB110	00000100	Write X-Filter Coefficients
34	100A0010	00000100	Read X-Filter Coefficients
35	100AB110	00000101	Write R-Filter Coefficients
36	100A0010	00000101	Read R-Filter Coefficients
37	100AB110	00000110	Write Echo Path Gain
38	100A0010	00000110	Read Echo Path Gain
39	100AB110	00000111	Write Error Level Threshold
40	100A0010	00000111	Read Error Level Threshold

A is referred to as DST in the following section.

A: 0 = Destination is Channel 1
1 = Destination is Channel 2

B is referred to as AM in the following section.

B: 0 = Command to channel defined by A bit
1 = Command to both channels, A bit ignored

DETAILED MONITOR COMMAND DEFINITIONS

Inactivate (Standby mode)

	MSB							LSB
Format:	1	0	1	DST	AM	0	0	0

Bit Name	Description
	During Inactive mode (of one or both channels), none of the programmed information is changed and the analog output is set to 0 V.

Reset

	MSB							LSB
Format:	1	0	1	DST	AM	0	0	1

Bit Name	Description
	The Reset state of the device is: a. A-law is selected. b. B, X, R, and Z filters are disabled and AISN gain is zero. c. Transmit (GX and AX) and Receive (GR and AR) gains are set to unity. d. SLIC Input/Output is set to the Read mode. e. Normal conditions are selected (see Command 4). f. The Adaptive mode and Error Level Threshold are reset. g. The SLIC interface is set to the non-Multiplexed mode. h. Both channels are placed in the Inactive (Standby) mode.

Reset to Normal Conditions

	MSB							LSB
Format:	1	0	1	DST	AM	0	1	1

Bit Name	Description
	Normal conditions are: a. 6 dB loss in receive path not inserted. b. Receive path not cut off. c. High-pass filter enabled. d. Test modes are turned off.

Activate (Operational Mode)

	MSB							LSB
Format:	1	0	1	DST	AM	1	0	0

Bit Name	Description
	Valid IOM 2 data is not transmitted until after the second FSC pulse is received following the execution of the Activate command.

Set MCLK to 2.048 MHz

	MSB							LSB
Format:	1	0	1	DST	AM	1	1	0

Set MCLK to 4.096 MHz

	MSB							LSB
Format:	1	0	1	DST	AM	1	1	1

Read Channel Identification Information

Command

	MSB							LSB
Format:	1	0	0	DST	0	0	0	0
	0	0	0	0	0	0	0	0

Output Data

1	0	0	SRC	0	C	C	C
T	T	L	L	L	L	L	L

Bit Name	Description
SRC	Source 0 = Source is Channel 1. 1 = Source is Channel 2.
C	Configuration This field reflects the state of the configuration inputs.
T	Device Type These 2 bits always have a value of 10.
L	Design Level This 6-bit field is used to differentiate between different implementations of the same device type. The IOM 2 DSLAC device is assigned the number 000100.

Write AISN and Analog Gains

Command (2 Bytes)

	MSB							LSB
Format:	1	0	0	DST	AM	1	0	0
	0	0	0	0	0	0	0	1

Input Data

—	AX	AR	A	B	C	D	E

Bit Name	Description
AX	Transmit Analog Gain AX = 0 0 dB gain AX = 1 6 dB gain
AR	Receive Analog Loss AR = 0 0 dB loss AR = 1 6 dB loss
A, B, C, D, E	AISN coefficients The Analog Impedance Scaling Network (AISN) gain can be varied from –0.9375 to 0.9375 in increments of 0.0625. The gain coefficient is encoded and decoded using the following equation: $h_{AISN} = 0.0625\ ((A2^4 + B2^3 + C2^2 + D2^1 + E2^0) - 16)$ where h_{AISN} is the gain of the AISN and A, B, C, D, and E = 0 or 1. A value of ABCDE = 10000 implements a special digital loop-back mode and a value of ABCDE = 00000 indicates a gain of 0 (cut off).

Read AISN and Analog Gains

Command (2 Bytes)

	MSB							LSB
Format:	1	0	0	DST	0	0	0	0
	0	0	0	0	0	0	0	1

Output Data

—	AX	AR	A	B	C	D	E

Write SLIC Input/Output Direction

Command (2 Bytes)

Format:

	MSB							LSB
	1	0	0	DST	AM	1	0	0
	0	0	0	0	0	0	1	1

Input Data

—	—	—	A	B	—	—	—

Bit Name	Description
	Pins $C5_1/IN_5$, $C5_2/IN_2$, $C4_1/IN_6$, and $C4_2/IN_3$ are set to Input or Output modes individually. The Input mode is set when the appropriate data bit is set to 0, and the Output mode is set when the data bit is set to 1. Data bit A sets pins $C5_1/IN_5$ or $C5_2/IN_2$ Data bit B set pins $C4_1/IN_6$, or $C4_2/IN_3$

Read SLIC Input/Output Direction and Power Status

Command (2 Bytes)

Format:

	MSB							LSB
	1	0	0	DST	0	0	0	0
	0	0	0	0	0	0	1	1

Output Data

PI	CS	—	A	B	—	—	—

Bit Name	Description
PI	Power Interrupt Bit PI = 0 There has not been a power interruption since the last software reset command. PI = 1 A power interruption has been previously detected requiring the DSLAC device to be completely reprogrammed. This bit is cleared by issuing a software reset command. THE DSLAC DEVICE CANNOT BE ACTIVATED UNTIL THIS BIT IS CLEAR.
CS	Channel Status Bit CS = 0 The status of the channel is inactive (Standby mode). CS = 1 The status of the channel is active (Operational mode).

Read SLIC Input/Output Registers

Command (2 Bytes)

	MSB							LSB
Format:	1	0	0	DST	0	0	0	0
	0	0	0	0	0	1	0	0

Output Data

—	—	DET	C5	C4	C3	C2	C1

Bit Name	Description
C5	Refers to $C5_1$ or $C5_2$ if they are used as outputs. Refers to IN_5 or IN_2 if they are used as inputs.
C4	Refers to $C4_1$ or $C4_2$ if they are used as outputs. Refers to IN_6 or IN_3 if they are used as inputs.

Write Operating Functions

Command (2 Bytes)

	MSB							LSB
Format:	1	0	0	DST	AM	1	0	0
	0	0	0	0	0	1	0	1

Input Data

ABF	A/U	EGR	EGX	EX	ER	EZ	EB

Bit Name	Description
ABF	Adaptive B Filter ABF = 0 non-Adaptive mode ABF = 1 Adaptive mode
A/U	A-law/μ-law A/U = 0 A-law coding A/U = 1 μ-law coding
EGR	GR Filter EGR = 0 GR filter disabled EGR = 1 GR filter enabled
EGX	GX Filter EGX = 0 GX filter disabled EGX = 1 GX filter enabled
EX	X Filter EX = 0 X filter disabled EX = 1 X filter enabled

Write Operating Functions—(continued)

Bit Name	Description
ER	R Filter
	ER = 0 R filter disabled
	ER = 1 R filter enabled
EZ	Z Filter
	EZ = 0 Z filter disabled
	EZ = 1 Z filter enabled
EB	B Filter
	EB = 0 B filter disabled
	EB = 1 B filter enabled

Read Operating Functions

Command (2 Bytes)

Format:

MSB							LSB
1	0	0	DST	0	0	0	0
0	0	0	0	0	1	0	1

Output Data

ABF	A/μ	EGR	EGX	EX	ER	EZ	EB

Write Operating Conditions

Command (2 Bytes)

Format:

MSB							LSB
1	0	0	DST	AM	1	0	0
0	0	0	0	0	1	1	1

Input Data

—	CRP	HPF	RG	ALB	DLB	—	—

Bit Name	Description
CRP	Cutoff Receive Path
	CRP = 0 Receive path connected
	CRP = 1 Receive path cutoff
HPF	High-Pass Filter
	HPF = 0 High-pass filter enabled
	HPF = 1 High-pass filter disabled
RG	Receive Path Gain
	RG = 0 6 dB loss not inserted
	RG = 1 6 dB loss inserted

Write Operating Conditions—(continued)

Bit Name	Description
ALB	Analog Loop-Back ALB = 0 Analog loop-back disabled ALB = 1 Analog loop-back enabled
DLB	Digital Loop-Back DLB = 0 Digital loop-back disabled DLB = 1 Digital loop-back enabled

Note: Analog and Digital loop-backs must not be programmed at the same time.

Read Operating Conditions

Command (2 Bytes)

	MSB							LSB
Format:	1	0	0	DST	0	0	0	0
	0	0	0	0	0	1	1	1

Output Data

—	CRP	HPF	RG	ALB	DLB	—	—

Read Revision Code Number

Command (2 Bytes)

	MSB							LSB
Format:	1	0	0	DST	0	0	0	0
	0	0	0	0	1	0	0	0

Input Data

#	#	#	#	#	#	#	#

Bit Name	Description
DST	Don't care

Write Ground-Key Sampling Interval

Command (2 Bytes)

Format:

MSB							LSB
1	0	0	DST	AM	1	0	0
0	0	0	0	1	0	0	1

Input Data

—	—	CHF*	MUX	Gk3	Gk2	Gk1	Gk0

Bit Name	Description
MUX	Multiplexed mode MUX = 0 non-Multiplexed mode MUX = 1 Multiplexed mode The device may be configured to operate in the Multiplexed mode (MUX) where the off-hook status and the ground-key status are multiplexed onto the same line. Note that there is only one Ground-Key Sampling Interval register and one MUX bit per IOM 2 DSLAC device (not per channel). Thus, the DST and the AM fields are not decoded and a command to either channel will write into the Ground-Key register and the MUX bit.
Gk3–Gk0	Sampling Interval 1 to 15 ms in 1 ms steps. If the Gk3–Gk0 field is set to 0000 there is no debounce performed. If, additionally, the MUX bit is set to a 0 or if the Gk3–Gk0 field is set to 0000, the $C3_I/E_1$ output is controlled by writing a 0 or a 1 into the output latch via the C/I downstream byte.

Read Ground-Key Sampling Interval

Command (2 Bytes)

Format:

MSB							LSB
1	0	0	DST	0	0	0	0
0	0	0	0	1	0	0	1

Output Data

—	—	CHF*	MUX	Gk3	Gk2	Gk1	Gk0

*CHF— Chopper Clock Frequency (this bit sets the chopper clock frequency when the IOM 2 DSLAC device is operating in multiplexed mode).
CHF = 0 256 kHz (default)
CHF = 1 273 kHz

Write SLIC Detect Inputs Debounce Time

Command (2 Bytes)

	MSB							LSB
Format:	1	0	0	DST	AM	1	0	0
	0	0	0	0	1	0	1	0

Input Data

	—	—	—	—	Db3	Db2	Db1	Db0

Bit Name	Description
Db3–Db0	Debounce Interval Sets the debounce time from 0 to 15 ms in steps of 1 ms. This command sets the debounce interval for the input signals at $\overline{DET}_1$ and $\overline{DET}_2$. Note that there is only one Detect Input Debounce register per IOM 2 DSLAC device (not per channel). Thus, the DST and the AM fields are unused and a command to either channel will write into the Debounce register. If the Db3–Db0 field is set to 0000, there is no debounce performed.

Read SLIC Upstream Inputs Debounce Time

Command (2 Bytes)

	MSB							LSB
Format:	1	0	0	DST	0	0	0	0
	0	0	0	0	1	0	1	0

Output Data

	—	—	—	—	Db3	Db2	Db1	Db0

Write GX-Filter Coefficients

Command (2 Bytes)

	MSB							LSB
Format:	1	0	0	DST	AM	1	1	0
	0	0	0	0	0	0	0	0

Input Data

C_{40}	m_{40}	C_{30}	m_{30}	Byte 1
C_{20}	m_{20}	C_{10}	m_{10}	Byte 2

Read GX-Filter Coefficients

Command (2 Bytes)

Format:

MSB							LSB
1	0	0	DST	0	0	1	0
0	0	0	0	0	0	0	0

Output Data

C_{40}	m_{40}	C_{30}	m_{30}	Byte 1
C_{20}	m_{20}	C_{10}	m_{10}	Byte 2

Write GR-Filter Coefficients

Command (2 Bytes)

Format:

MSB							LSB
1	0	0	DST	AM	1	1	0
0	0	0	0	0	0	0	1

Input Data

C_{40}	m_{40}	C_{30}	m_{30}	Byte 1
C_{20}	m_{20}	C_{10}	m_{10}	Byte 2

Read GR-Filter Coefficients

Command (2 Bytes)

Format:

MSB							LSB
1	0	0	DST	0	0	1	0
0	0	0	0	0	0	0	1

Output Data

C_{40}	m_{40}	C_{30}	m_{30}	Byte 1
C_{20}	m_{20}	C_{10}	m_{10}	Byte 2

Write Z-Filter Coefficients

Command (2 Bytes)

	MSB							LSB
Format:	1	0	0	DST	AM	1	1	0
	0	0	0	0	0	0	1	0

Input Data

C_{45}	m_{45}	C_{35}	m_{35}	Byte 1
C_{25}	m_{25}	C_{15}	m_{15}	Byte 2
C_{40}	m_{40}	C_{30}	m_{30}	Byte 3
C_{20}	m_{20}	C_{10}	m_{10}	Byte 4
C_{41}	m_{41}	C_{31}	m_{31}	Byte 5
C_{21}	m_{21}	C_{11}	m_{11}	Byte 6
C_{42}	m_{42}	C_{32}	m_{32}	Byte 7
C_{22}	m_{22}	C_{12}	m_{12}	Byte 8
C_{43}	m_{43}	C_{33}	m_{33}	Byte 9
C_{23}	m_{23}	C_{13}	m_{13}	Byte 10
C_{44}	m_{44}	C_{34}	m_{34}	Byte 11
C_{24}	m_{24}	C_{14}	m_{14}	Byte 12
C_{46}	m_{46}	C_{36}	m_{36}	Byte 13
C_{26}	m_{26}	C_{16}	m_{16}	Byte 14

Read Z-Filter Coefficients

Command (2 Bytes)

	MSB							LSB
Format:	1	0	0	DST	0	0	1	0
	0	0	0	0	0	0	1	0

Output Data

C_{45}	m_{45}	C_{35}	m_{35}	Byte 1
C_{25}	m_{25}	C_{15}	m_{15}	Byte 2
C_{40}	m_{40}	C_{30}	m_{30}	Byte 3
C_{20}	m_{20}	C_{10}	m_{10}	Byte 4
C_{41}	m_{41}	C_{31}	m_{31}	Byte 5
C_{21}	m_{21}	C_{11}	m_{11}	Byte 6
C_{42}	m_{42}	C_{32}	m_{32}	Byte 7
C_{22}	m_{22}	C_{12}	m_{12}	Byte 8
C_{43}	m_{43}	C_{33}	m_{33}	Byte 9
C_{23}	m_{23}	C_{13}	m_{13}	Byte 10
C_{44}	m_{44}	C_{34}	m_{34}	Byte 11
C_{24}	m_{24}	C_{14}	m_{14}	Byte 12
C_{46}	m_{46}	C_{36}	m_{36}	Byte 13
C_{26}	m_{26}	C_{16}	m_{16}	Byte 14

Write B-Filter Coefficients

Command (2 Bytes)

Format:

MSB							LSB
1	0	0	DST	AM	1	1	0
0	0	0	0	0	0	1	1

Input Data

C_{30}	m_{30}	C_{20}	m_{20}	Byte 1
C_{10}	m_{10}	C_{31}	m_{31}	Byte 2
C_{21}	m_{21}	C_{11}	m_{11}	Byte 3
C_{32}	m_{32}	C_{22}	m_{22}	Byte 4
C_{12}	m_{12}	C_{33}	m_{33}	Byte 5
C_{23}	m_{23}	C_{13}	m_{13}	Byte 6
C_{34}	m_{34}	C_{24}	m_{24}	Byte 7
C_{14}	m_{14}	C_{35}	m_{35}	Byte 8
C_{25}	m_{25}	C_{15}	m_{15}	Byte 9
C_{36}	m_{36}	C_{26}	m_{26}	Byte 10
C_{16}	m_{16}	C_{37}	m_{37}	Byte 11
C_{27}	m_{27}	C_{17}	m_{17}	Byte 12
C_{48}	m_{48}	C_{38}	m_{38}	Byte 13
C_{28}	m_{28}	C_{18}	m_{18}	Byte 14

Read B-Filter Coefficients

Command (2 Bytes)

Format:

MSB							LSB
1	0	0	DST	0	0	1	0
0	0	0	0	0	0	1	1

Output Data

C_{30}	m_{30}	C_{20}	m_{20}	Byte 1
C_{10}	m_{10}	C_{31}	m_{31}	Byte 2
C_{21}	m_{21}	C_{11}	m_{11}	Byte 3
C_{32}	m_{32}	C_{22}	m_{22}	Byte 4
C_{12}	m_{12}	C_{33}	m_{33}	Byte 5
C_{23}	m_{23}	C_{13}	m_{13}	Byte 6
C_{34}	m_{34}	C_{24}	m_{24}	Byte 7
C_{14}	m_{14}	C_{35}	m_{35}	Byte 8
C_{25}	m_{25}	C_{15}	m_{15}	Byte 9
C_{36}	m_{36}	C_{26}	m_{26}	Byte 10
C_{16}	m_{16}	C_{37}	m_{37}	Byte 11
C_{27}	m_{27}	C_{17}	m_{17}	Byte 12
C_{48}	m_{48}	C_{38}	m_{38}	Byte 13
C_{28}	m_{28}	C_{18}	m_{18}	Byte 14

Write X-Filter Coefficients

Command (2 Bytes)

Format:

MSB							LSB
1	0	0	DST	AM	1	1	0
0	0	0	0	0	1	0	0

Input Data

C_{40}	m_{40}	C_{30}	m_{30}	Byte 1
C_{20}	m_{20}	C_{10}	m_{10}	Byte 2
C_{41}	m_{41}	C_{31}	m_{31}	Byte 3
C_{21}	m_{21}	C_{11}	m_{11}	Byte 4
C_{42}	m_{42}	C_{32}	m_{32}	Byte 5
C_{22}	m_{22}	C_{12}	m_{12}	Byte 6
C_{43}	m_{43}	C_{33}	m_{33}	Byte 7
C_{23}	m_{23}	C_{13}	m_{13}	Byte 8
C_{44}	m_{44}	C_{34}	m_{34}	Byte 9
C_{24}	m_{24}	C_{14}	m_{14}	Byte 10
C_{45}	m_{45}	C_{35}	m_{35}	Byte 11
C_{25}	m_{25}	C_{15}	m_{15}	Byte 12

Read X-Filter Coefficients

Command (2 Bytes)

Format:

MSB							LSB
1	0	0	DST	0	0	1	0
0	0	0	0	0	1	0	0

Output Data

C_{40}	m_{40}	C_{30}	m_{30}	Byte 1
C_{20}	m_{20}	C_{10}	m_{10}	Byte 2
C_{41}	m_{41}	C_{31}	m_{31}	Byte 3
C_{21}	m_{21}	C_{11}	m_{11}	Byte 4
C_{42}	m_{42}	C_{32}	m_{32}	Byte 5
C_{22}	m_{22}	C_{12}	m_{12}	Byte 6
C_{43}	m_{43}	C_{33}	m_{33}	Byte 7
C_{23}	m_{23}	C_{13}	m_{13}	Byte 8
C_{44}	m_{44}	C_{34}	m_{34}	Byte 9
C_{24}	m_{24}	C_{14}	m_{14}	Byte 10
C_{45}	m_{45}	C_{35}	m_{35}	Byte 11
C_{25}	m_{25}	C_{15}	m_{15}	Byte 12

Write R-Filter Coefficients

Command (2 Bytes)

Format:

MSB							LSB
1	0	0	DST	AM	1	1	0
0	0	0	0	0	1	0	1

Input Data

C_{40}	m_{40}	C_{30}	m_{30}	Byte 1
C_{20}	m_{20}	C_{10}	m_{10}	Byte 2
C_{41}	m_{41}	C_{31}	m_{31}	Byte 3
C_{21}	m_{21}	C_{11}	m_{11}	Byte 4
C_{42}	m_{42}	C_{32}	m_{32}	Byte 5
C_{22}	m_{22}	C_{12}	m_{12}	Byte 6
C_{43}	m_{43}	C_{33}	m_{33}	Byte 7
C_{23}	m_{23}	C_{13}	m_{13}	Byte 8
C_{44}	m_{44}	C_{34}	m_{34}	Byte 9
C_{24}	m_{24}	C_{14}	m_{14}	Byte 10
C_{45}	m_{45}	C_{35}	m_{35}	Byte 11
C_{25}	m_{25}	C_{15}	m_{15}	Byte 12

Read R-Filter Coefficients

Command (2 Bytes)

Format:

MSB							LSB
1	0	0	DST	0	0	1	0
0	0	0	0	0	1	0	1

Output Data

C_{40}	m_{40}	C_{30}	m_{30}	Byte 1
C_{20}	m_{20}	C_{10}	m_{10}	Byte 2
C_{41}	m_{41}	C_{31}	m_{31}	Byte 3
C_{21}	m_{21}	C_{11}	m_{11}	Byte 4
C_{42}	m_{42}	C_{32}	m_{32}	Byte 5
C_{22}	m_{22}	C_{12}	m_{12}	Byte 6
C_{43}	m_{43}	C_{33}	m_{33}	Byte 7
C_{23}	m_{23}	C_{13}	m_{13}	Byte 8
C_{44}	m_{44}	C_{34}	m_{34}	Byte 9
C_{24}	m_{24}	C_{14}	m_{14}	Byte 10
C_{45}	m_{45}	C_{35}	m_{35}	Byte 11
C_{25}	m_{25}	C_{15}	m_{15}	Byte 12

Write Echo Path Gain

Command (2 Bytes)

Format:

MSB							LSB
1	0	0	DST	AM	1	1	0
0	0	0	0	0	1	1	0

Input Data

C_{80}	m_{80}	C_{70}	m_{70}	Byte 1
C_{60}	m_{60}	C_{50}	m_{50}	Byte 2
C_{40}	m_{40}	C_{30}	m_{30}	Byte 3
C_{20}	m_{20}	C_{10}	m_{10}	Byte 4

Read Echo Path Gain

Command (2 Bytes)

Format:

MSB							LSB
1	0	0	DST	0	0	1	0
0	0	0	0	0	1	1	0

Output Data

C_{80}	m_{80}	C_{70}	m_{70}	Byte 1
C_{60}	m_{60}	C_{50}	m_{50}	Byte 2
C_{40}	m_{40}	C_{30}	m_{30}	Byte 3
C_{20}	m_{20}	C_{10}	m_{10}	Byte 4

Write Error Level Threshold

Command (2 Bytes)

Format:

MSB							LSB
1	0	0	DST	AM	1	1	0
0	0	0	0	0	1	1	1

Input Data

C_{20}	m_{10}	C_{20}	m_{10}	Byte 1

Read Error Level Threshold

Command (2 Bytes)

Format:

MSB							LSB
1	0	0	DST	0	0	1	0
0	0	0	0	0	1	1	1

Output Data

C_{20}	m_{20}	C_{10}	m_{10}	Byte 1

SLIC INTERFACE

General Description

Each channel of the DSLAC device has I/O pins for interfacing with a SLIC or other line circuit device. The I/O pins on port 1 are labeled $C5_1/IN_5$, $C4_1/IN_6$, $C3_1/E_1$, $C2_1$, and $C1_1$. The I/O pins on port 2 are labeled $C5_2/IN_2$, $C4_2/IN_3$, $C3_2$/CHCLK, $C2_2$, and $C1_2$. One input-only pin for each channel ($\overline{DET}_1/IN_4$ for Channel 1 and $\overline{DET}_2/IN_1$ for Channel 2) is also available. When used with an Am795XX series SLIC, C_4, C_2, and C_1 can be used as outputs to set the Operating mode of the SLIC while C_5 would typically be used to control a test relay driver on the SLIC. $C3_1/E_1$ is used (in the Multiplexed mode) to control the function of the SLIC line monitor output, $\overline{DET}$. C_5 and C_4 of each channel can be programmed to be an input or an output via a Monitor channel command.

Data can be sent to any of the I/O pins configured as outputs via the six C/I bits of the downstream SC byte. All of the I/O pins configured as inputs may be read via a Monitor channel command. Additionally, three input signals from each channel are taken to form the six C/I bits of the upstream SC byte.

Ground-Key/Switch-Hook Detector Multiplexing

The $\overline{DET}$ input for each channel can be programmed to operate in the Multiplexed mode to interface with the Am795XX series SLIC devices. In this mode, the interpretation of the signal on the $\overline{DET}$ input is controlled by the $C3_1/E_1$ output. When E_1 is Low, $\overline{DET}$ is interpreted as switch-hook detect. When E_1 is High, $\overline{DET}$ is interpreted as ground-key detect. Input debouncing may be selected for both the switch-hook and ground-key functions. Note that in the Multiplexed mode, the ground-key detect status and not the $C5_1/IN_5$ and the $C5_2/IN_2$ inputs are part of the upstream SC byte.

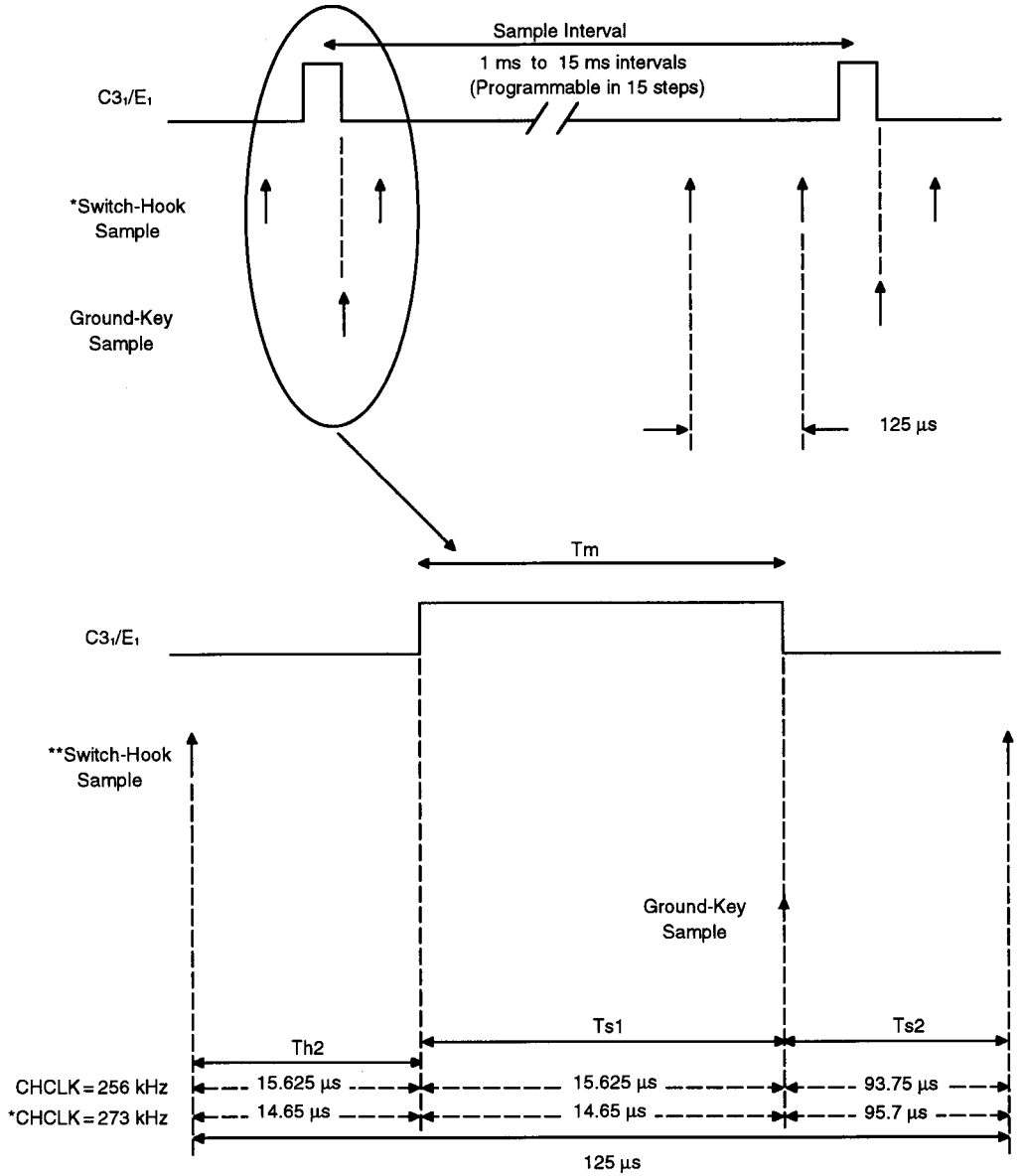
The state of E_1 can be controlled directly via a Monitor channel command or by the internal ground-key (Gk) timer which allows it to go High for approximately 16 µs every 1 to 15 ms. In this way, the DSLAC device can automatically de-multiplex the switch-hook and ground-key detector. Figure 10 shows the details of ground-key/switch-hook multiplexer timing.

Input Debouncing for Switch-Hook and Ground-Key Detect Inputs

There are two input debounce circuits associated with each channel of the DSLAC device. The first is used to debounce the $\overline{DET}$ input. The circuitry requires the signal on the $\overline{DET}$ input to be stable for two of the debounce intervals defined by the state of the Db timer (1 to 15 ms set by monitor command #23) in order for the upstream C/I byte to reflect the change.

A second debounce circuit per channel is available which would typically be used for the ground-key input. The input to this debounce circuit can come from $C5_1/IN_5$ and $C5_2/IN_2$ (in the non-Multiplexed mode), or the $\overline{DET}_1$ and $\overline{DET}_2$ inputs (in the Multiplexed mode). This circuit operates as a duty-cycle detector and consists of an up/down counter which can range between 0 and 6. The counter is clocked by the Gk timer which is set by monitor command #21 to a value between 1 to 15 ms. When the sampled value of the ground-key input is High, the counter is incremented. When the sampled value is a Low, the counter is decremented. If the counter increments to its maximum value of 6, it sets a latch whose output is the corresponding upstream C/I bit. If the counter decrements to its minimum value of 0, the latch is cleared. The following truth table shows the functioning of the ground key debounce circuit at every Gk clock.

Ground-Key Input	Current State	Next State	Action On C/I Bit Latch
0	State 0	State 0	Force Low
0	State 1	State 0	Force Low
0	State 2	State 1	No change
0	State 3	State 2	No change
0	State 4	State 3	No change
0	State 5	State 4	No change
0	State 6	State 5	No change
1	State 0	State 1	No change
1	State 1	State 2	No change
1	State 2	State 3	No change
1	State 3	State 4	No change
1	State 4	State 5	No change
1	State 5	State 6	Force High
1	State 6	State 6	Force High



*Programmed through CHF bit in Ground-Key Sampling Internal Register.
**Switch-hook samples occur at the beginning of selected time slot.

12764A–013

Figure 10. Switch-Hook/Ground-Key Multiplex Timing

The following table describes the various operating modes depending on the state of the MUX bit and the Ground Key (Gk) and the Debounce (Db) timers. A diagram of the SLIC I/O architecture is shown in Figure 11.

MUX	Gk3–Gk0	Db3–Db0	Operating Mode
0	0000	0000	1. **Non-Multiplexed mode.** The $\overline{DET_1}$ input is sampled every cycle and appears on C/I bit 4. The $\overline{DET_2}$ input is sampled every cycle and appears on C/I bit 1. Since the Db3–Db0 field is set to all 0s, there is no input debouncing. The $C5_1/IN_5$ input is sampled every frame and appears on C/I bit 5. The $C5_2/IN_2$ input is sampled every frame and appears on C/I bit 2. Since the Gk3–Gk0 field is set to all 0s, there is no input debouncing on C/I bit 5 or C/I bit 2.
0	1–15	1–15	2. **Same as 1**, except the $\overline{DET}$ inputs must be stable for two of the clock cycles defined by the state of the Db timer (1 to 15 ms) for the upstream C/I byte to reflect the change. The $C5_1/IN_5$ and the $C5_2/IN_2$ inputs are passed through the ground-key debounce circuit at a clock rate defined by the state of the Gk timer (1 to 15 ms).
1	1–15	0–15	3. **Multiplexed mode.** The $C3_1/E_1$ output will pulse High for one frame at a rate set by the Gk timer (1 to 15 ms). Thus, the state of the ground-key detector will be sampled at the Gk rate and passed to the ground-key debounce circuit. The ground-key status bits, C/I bit 2 and C/I bit 5, will reflect the output of the debounce circuit. If the Db3–Db0 field is set to 0000, C/I bit 1 and C/I bit 4 will be updated every frame except when the ground-key is being sampled. Otherwise, the switch-hook detect is sampled at the Db-clock rate and C/I bit 1 and C/I bit 4 will be updated when the sampled value has been stable for 2 Db-clock cycles.
1	0000	0–15	4. **Same as 3**, except the $C3_1/E_1$ pin is controlled by the downstream C/I channel and not by the Gk timer. Thus, the multiplexer can be manually set to interpret the $\overline{DET}$ input as either switch-hook status or ground-key status. When the E_1 signal is Low (selecting switch-hook status), C/I bits 5 and 2 (the ground-key detect bits) will not change states. Conversely, when the E_1 signal is High, C/I bits 4 and 1 will not change states.

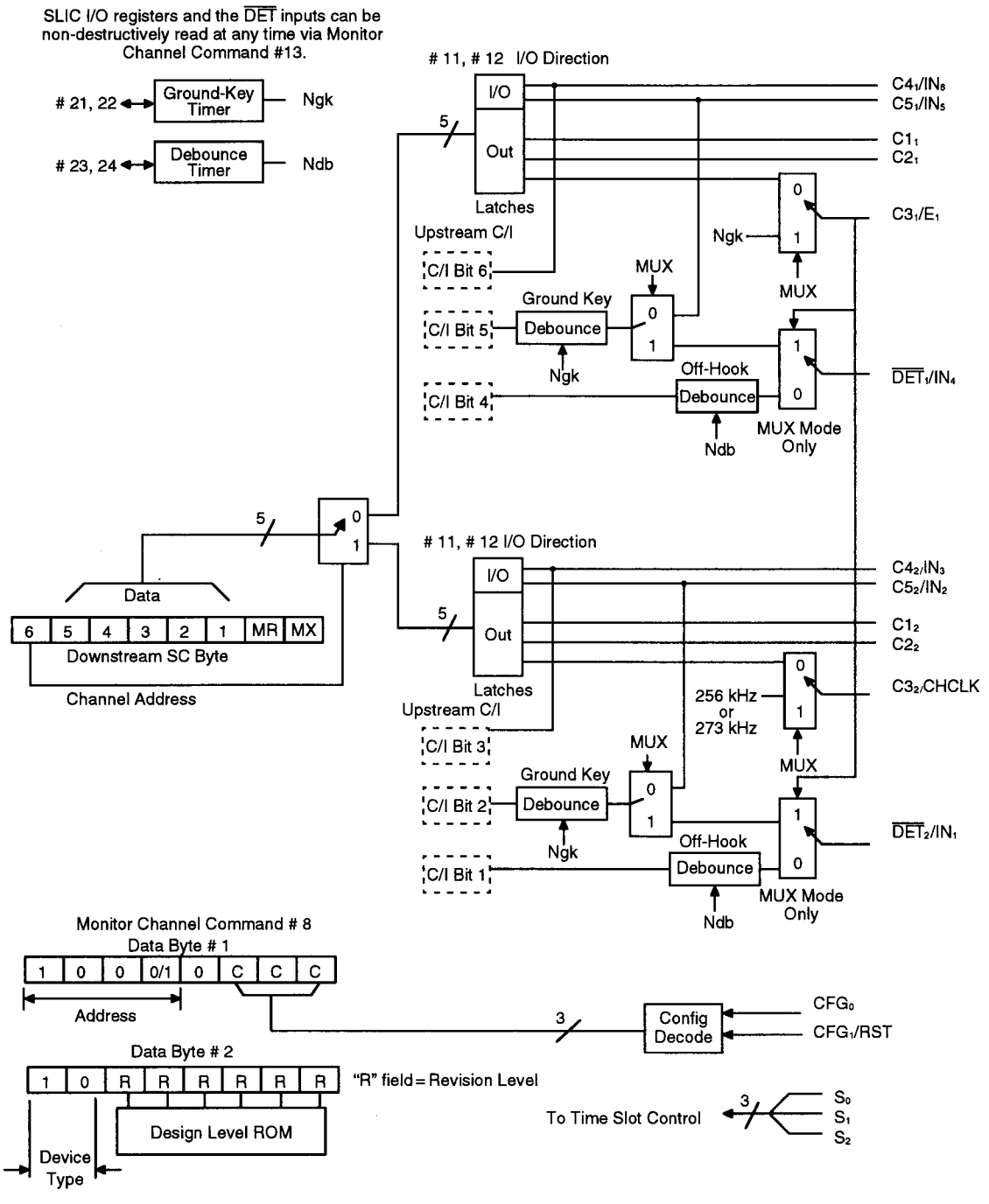


Figure 11. SLIC I/O Architecture

CONFIGURATION INPUTS

A method of identifying the configuration of the line circuit in which the DSLAC device is used is provided by strapping configuration inputs CFG_0 and CFG_1/RST. There are six possible configuration states which can be set via these two inputs. This data is sent upstream over the Monitor channel using command #8. The CFG_0 and CFG_1/RST inputs are decoded in the following table. A possible circuit for the CFG_1/RST pin is shown in Figure 12.

CFG_1	CFG_0	Configuration Number
+5 V	X	Hardware Reset
GND	–5 V	000
GND	GND	001
GND	+5 V	010
–5 V	–5 V	011
–5 V	GND	100
–5 V	+5 V	101

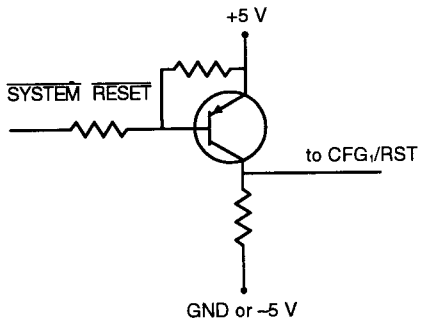


Figure 12. Circuit Schematic for the CFG_1, RST Input

TIME SLOT ASSIGNMENT INPUTS

In the time slot control block (shown in Figure 13), the Frame Sync (FSC) pulse identifies the beginning of a Transmit frame and all IOM 2 time slots are referenced to it. The time slot number is read from the external time slot identification pins, S_2–S_0. The table below shows the decoding on the time slot assignment inputs.

S_2	S_1	S_0	Time Slot Number	Byte number
0	0	0	0	0–3
0	0	1	1	4–7
0	1	0	2	8–11
0	1	1	3	12–15
1	0	0	4	16–19
1	0	1	5	20–23
1	1	0	6	24–27
1	1	1	7	28–31

The time slot number information is sent to the Transmit multiplexer where the code is shifted out during the appropriate time slot. From one to eight IOM 2 time slots per frame are allowed. The bit rate must be at least 256K times the number of IOM 2 time slots to be compatible with the number of time slots used. For example, since the DCL clock is twice the bit rate, DCL is at least 512 kHz for one time slot and 4.096 MHz for the full eight time slots.

The DSLAC device is capable of operation at a bit rate up to 4096 kb/s (DCL = 8.192 MHz). If the clock frequency exceeds the minimum for the given number of time slots on the IOM 2 line, there will be some time slots or surplus bits at the end of each frame which are ignored.

The receive side uses the same time slot control block information to de-multiplex the incoming IOM 2 data stream and load each byte into the input register. The input register feeds these bytes into the A-/μ-law expander for further signal processing.

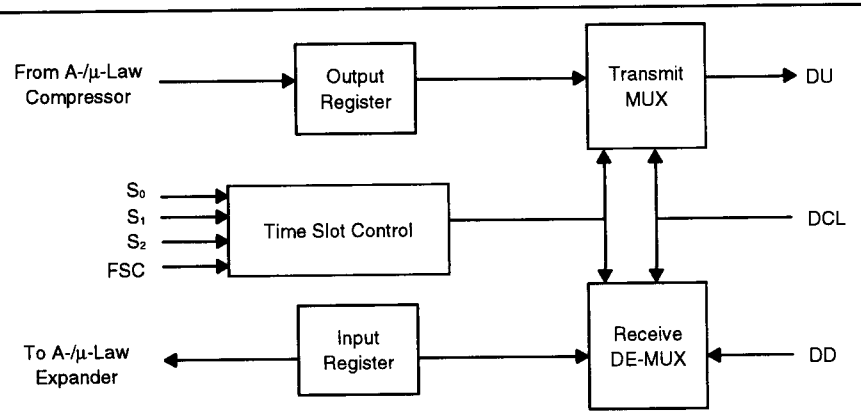


Figure 13. Time Slot Control and IOM 2 Interface

ABSOLUTE MAXIMUM RATINGS

Storage Temperature ..... $-60°C \le T_A \le +125°C$
Ambient Temperature, under Bias ..... $-40°C \le T_A \le 85°C$
Ambient Relative Humidity (non-condensing) ..... 5 to 100%
V_{CCA} with respect to AGND ..... –0.4 V to +7.0 V
V_{CC} with respect to DGND ..... –0.4 V to +7.0 V
V_{EE1} with respect to AGND ..... +0.4 V to –7.0 V
V_{EE2} with respect to AGND ..... +0.4 V to –7.0 V
V_{IN} with respect to V_{CCA} (V_{EE} = –5 V) ..... +0.4 V to –10.0 V
V_{IN} with respect to V_{EE} (V_{CCA} = +5 V) ..... –0.4 V to +10.0 V
Any other pin with respect to DGND ... –0.4 V to V_{CC}

Stresses above those listed under Absolute Maximum Ratings may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to Absolute Maximum Ratings for extended periods may affect device reliability.

OPERATING RANGES

Analog Supply V_{CCA} ..... +5.0 V ±5%
Digital Supply V_{CC} ..... +5.0 V ±5%
Analog Supply V_{EE1}, V_{EE2} ..... –5.0 V ±5%
DGND ..... 0 V
AGND ..... DGND ±50 mV
Ambient Temperature ..... $0°C \le T_A \le +70°C$
Ambient Relative Humidity ..... 15% to 85%

Operating ranges define those limits between which the functionality of the device is guaranteed.

DISTINCTIVE CHARACTERISTICS

Symbol	Parameter		Preliminary Min	Typ	Max	Units
V_{IL}	Input Low Voltage		−0.5		0.8	V
V_{IH}	Input High Voltage		2.0		V_{CC}	V
I_{IL}	Input Leakage Current				±10	µA
V_{OL}	Output Low Voltage (I_{OL} = −2 mA)				0.4	V
V_{OH}	Output High Voltage (I_{OH} = 400 µA)		2.4			V
I_{OL}	Output Leakage Current (Hi-Z state)				±10	µA
V_{IR}	Analog Input Voltage Range (AX = 0 dB) (AX = 6.02 dB)				±3.24 ±1.62	V V
V_{IOS}	Offset Voltage allowed on V_{IN}				±160	mV
I_{IL} (V_{IN})	Input Leakage Current on V_{IN}				±10	µA
Z_{OUT}	V_{OUT} Output Impedance			1	10	ohms
I_{OUT}	V_{OUT} Output Current (f < 3400 Hz) (Note 1)				±6.3	mA
V_{OR}	V_{OUT} Voltage Range (AR = 0 dB) (AR = 6.02 dB)				±3.24 ±1.62	V V
V_{OOS}	V_{OUT} Offset Voltage (AISN off)				±40	mV
V_{OOSA}	V_{OUT} Offset Voltage (AISN on)				±80	mV
LIN_{AISN}	Linearity of AISN Circuitry (Input = 0 dBm0)				±1/4	LSB
PD	Power Dissipation (Note 2) (MCLK, PCLK = 2.048 MHz)	Both Channels Active 1 Channel Active Both Channels Inactive (Note 3)		180 120 10	240 160 19	mW mW mW
PD	Power Dissipation (Note 2) (MCLK, PCLK > 2.048 MHz)	Both Channels Active 1 Channel Active Both Channels Inactive (Note 3)		190 130 10	270 175 19	mW mW mW
I_{CC}	Total +5-V Current (Note 2)	Both Channels Active 1 Channel Active Both Channels Inactive (Note 3)		24.0 18.0 2.5		mA mA mA
I_{EE}	Total −5-V Current (Note 2)	Both Channels Active 1 Channel Active Both Channels Inactive (Note 3)		10.0 5.0 0.05		mA mA mA
C_I	Input Capacitance (Digital)			15		pF
C_O	Output Capacitance (Digital)			15		pF
C_{DU}	Output Load Capacitance (DU pin only)				150	pF

Notes: 1. When the DSLAC device is in the Power Down mode, the analog output will present a 0-V output level through a ≈3K resistor.

2. V_{OUT1} and V_{OUT2} have no load.

3. Power Dissipation in the inactive mode is measured with all digital inputs at $V_{ih} = V_{CC}$ and $V_{il} = V_{SS}$ and with no load connected to V_{OUT1} or V_{OUT2}.

SWITCHING CHARACTERISTICS

V_{CC} = 5 V ±5%, AGND = DGND = 0 V, V_{EE} = –5 V ±5%. C_{DU} = 150 pF (Note 2)

IOM 2 Interface

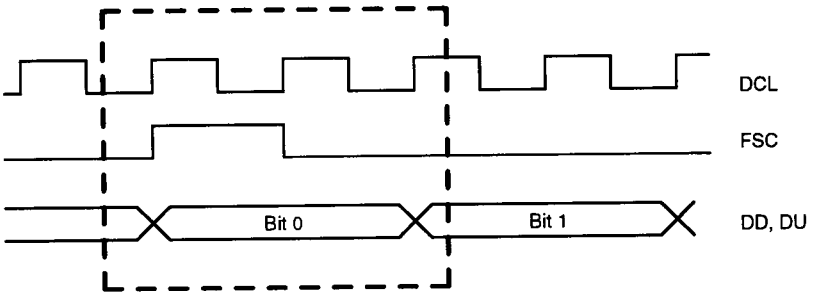
Symbol	Signal	Parameter	Preliminary			Units
			Min	Typ	Max	
t_r, t_f	DCL[1]	Rise/Fall Time (Note 1)			60	ns
t_{DCL}	DCL	Period	110			ns
t_{WH}, t_{WL}	DCL	Pulse Width	53			ns
t_r, t_f	FSC	Rise/Fall Time			60	ns
t_{sF}	FSC	Setup Time	70			ns
t_{hF}	FSC	Hold Time	50			ns
t_{WFH}	FSC	High Pulse Width	130			ns
t_{dDC}	DU[2]	Delay from DCL edge			100	ns
t_{dDF}	DU	Delay from FSC edge			150	ns
t_{sD}	DD	Data Setup	t_{WH} + 20			ns
t_{hD}	DD	Hold Setup	50			ns

MCLK, for 2.048 MHz + 100 ppm or 4.096 MHz + 100 ppm

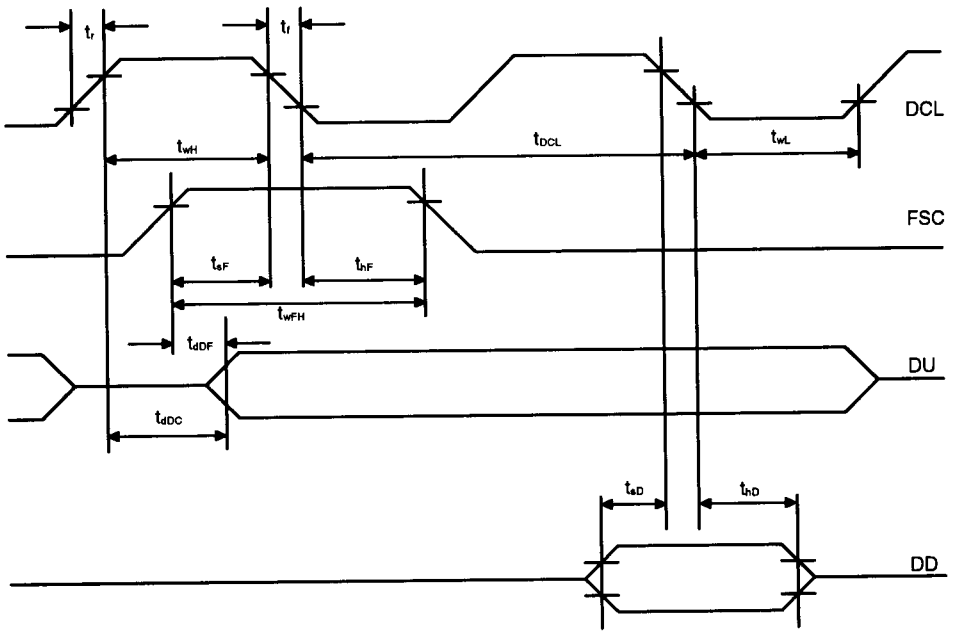
Symbol	Signal	Parameter	Preliminary			Units
			Min	Typ	Max	
t_{MCR}, t_{MCF}	MCLK	Rise/Fall Time			10	ns
t_{MCY}	MCLK	Period, 2.048 MHz Peroid, 4.096 MHz	488.23 244.11	488.28 244.14	488.33 244.17	ns ns
t_{MCH}, t_{MCL}	MCLK	High/Low Pulse Width	80			ns

Notes: 1. The IOM 2 clock may be stopped in the High or Low state without loss of information.
2. The drive capacity of the IOM 2 Interface allows eight DSLAC devices per linecard (16 subscriber lines) without using external buffers.

IOM 2 Switching Characteristics



Detail A



Detail A

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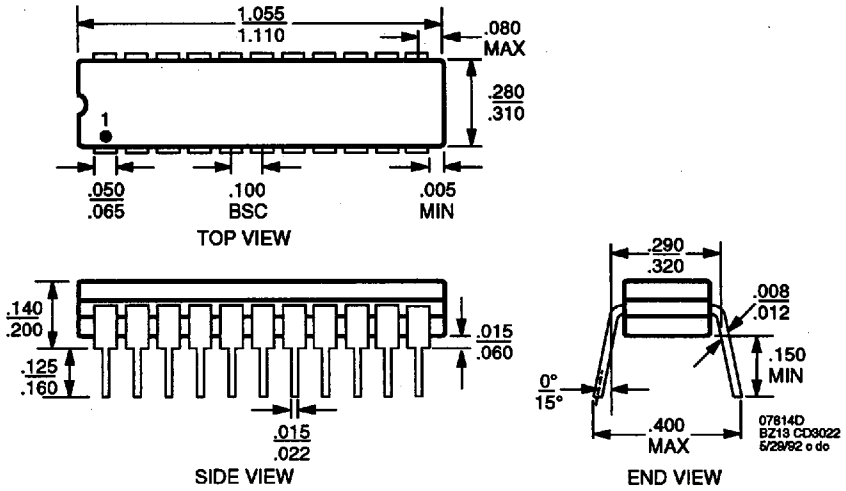
PHYSICAL DIMENSIONS

Preliminary; package in development. BSC is an ANSI standard for Basic Space Centering. Dimensions are measured in inches or millimeters.

T-90-20

CD022



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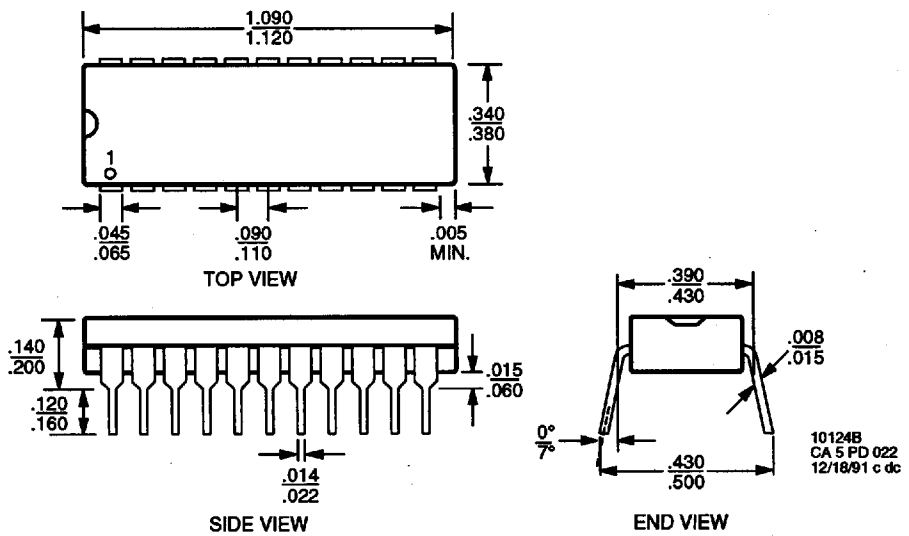

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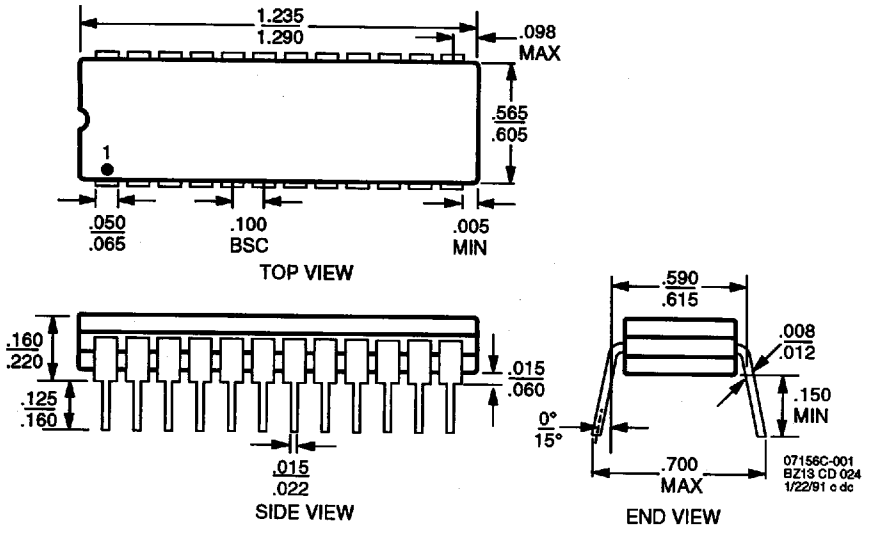

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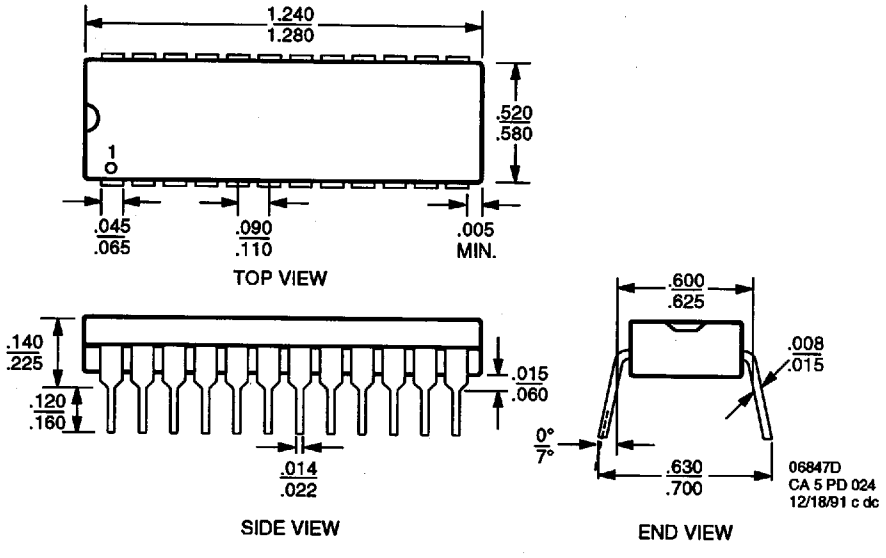

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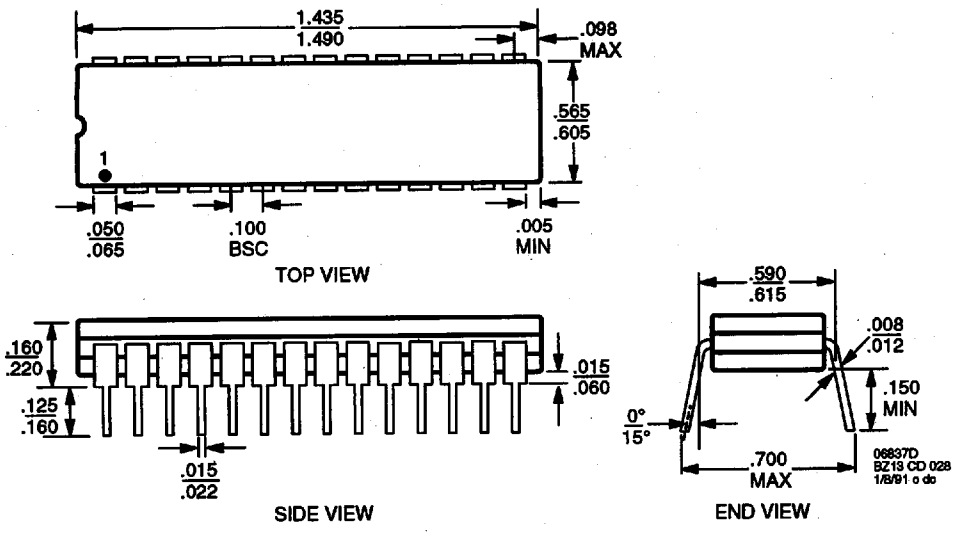

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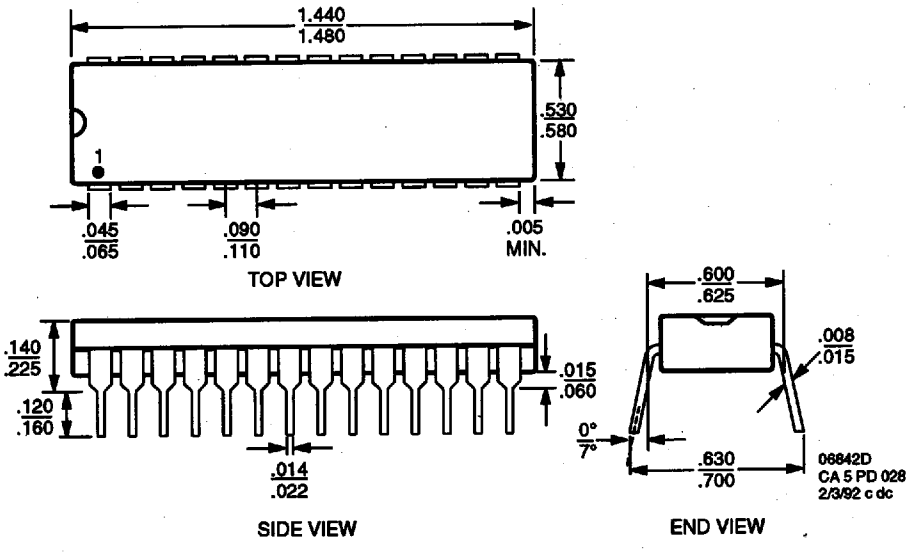

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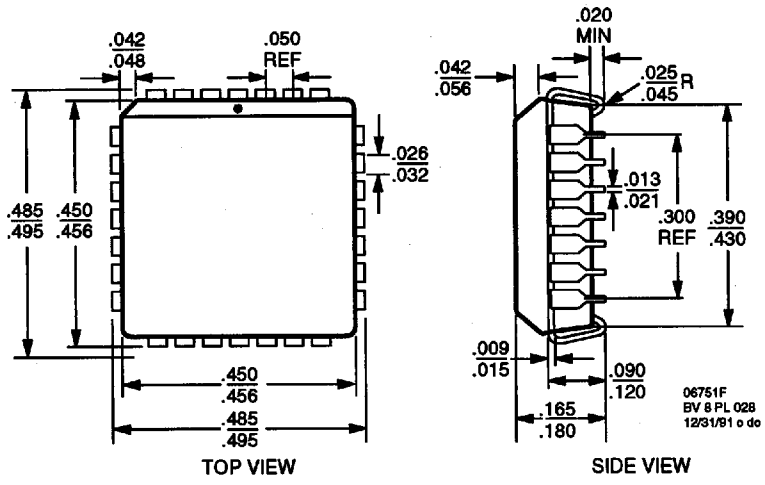

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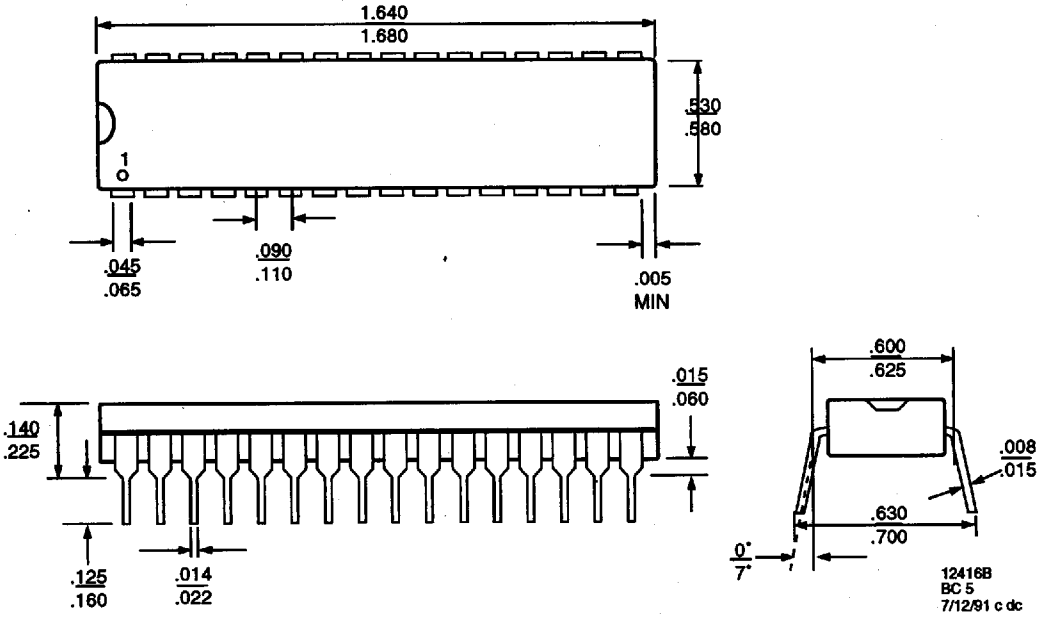

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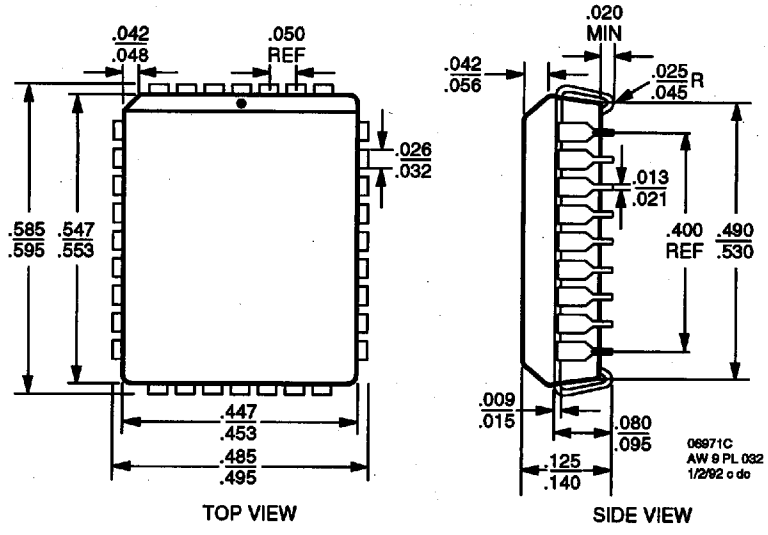
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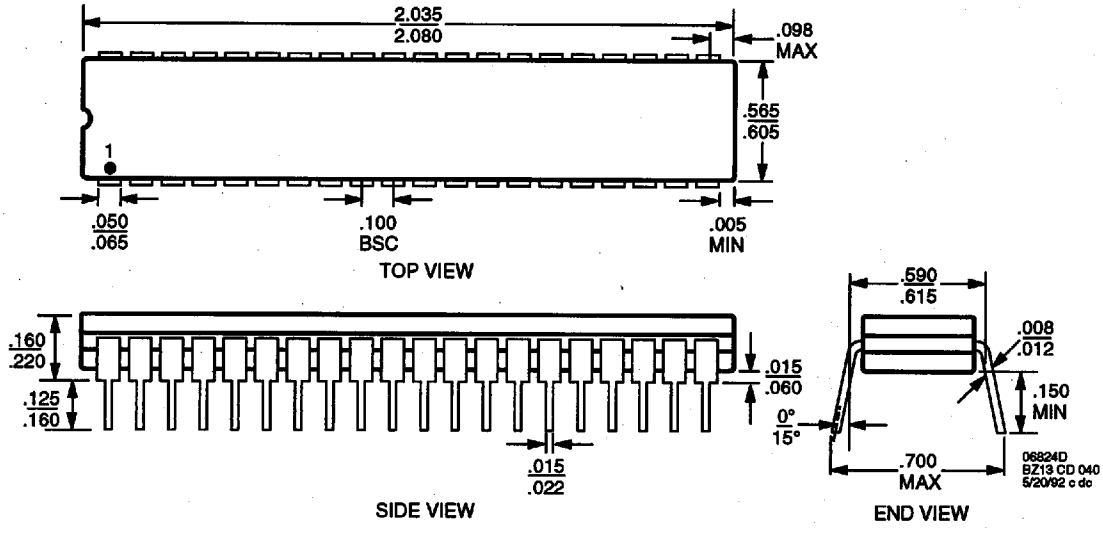
CD040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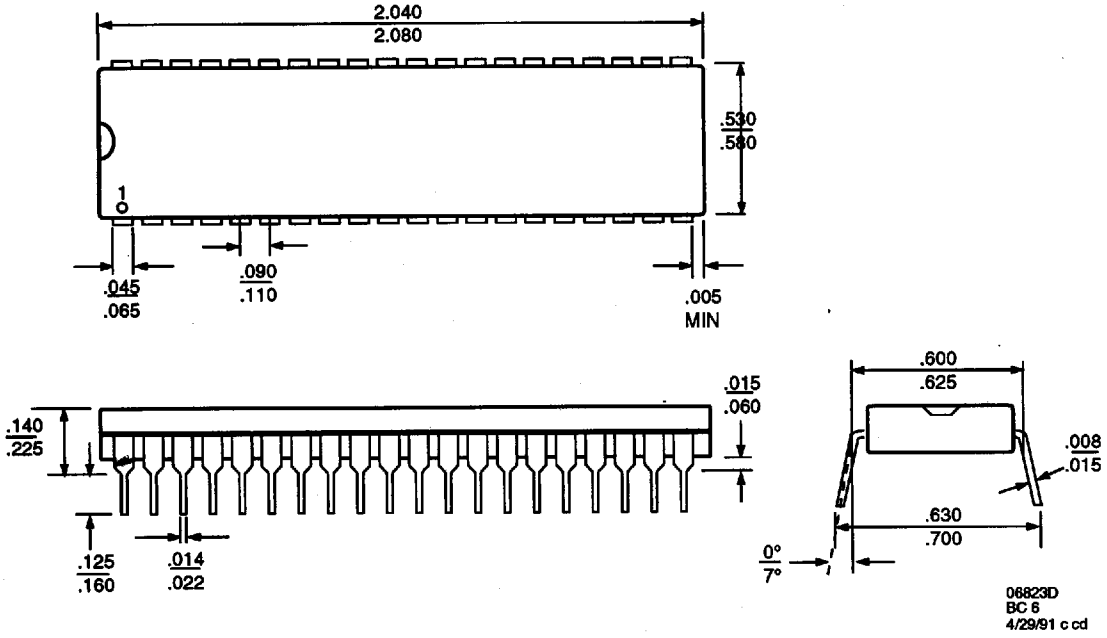
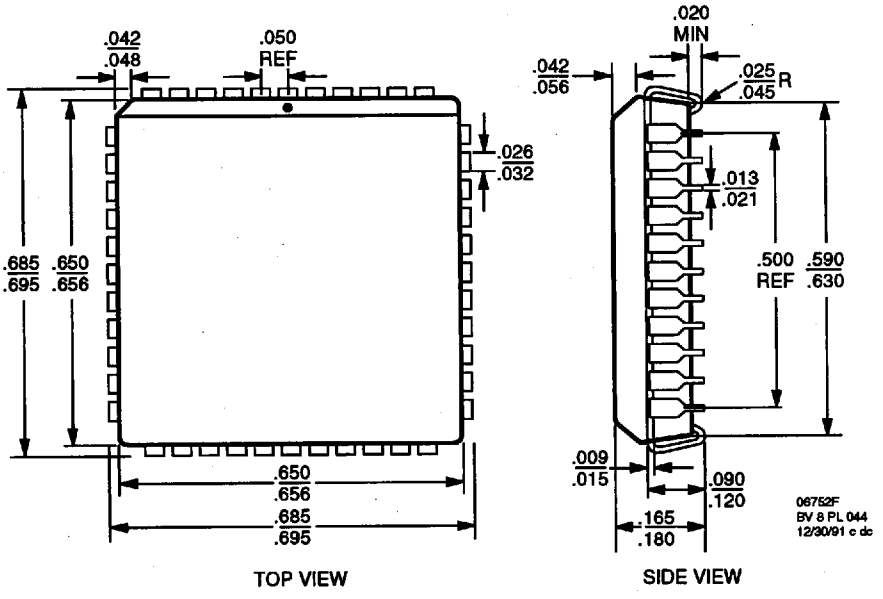


PL044



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