PRELIMINARY

AMD

# Am79C730

## Integrated Multiport Repeater for 100 Mbps (IMR100™)

## DISTINCTIVE CHARACTERISTICS

- **Fully integrated four-port 100BASE-TX repeater device compatible with IEEE 802.3u specifications**
- **Four 100BASE-TX ports with on-chip clock recovery and MLT-3 functionality**
- **Flexible configuration options to support 100BASE-TX and 100BASE-FX operation**
- **LED support for multiple per port and global attributes**
- **Asynchronous expansion port for interconnecting multiple IMR100 devices**
- **Enables the design of systems that meet IEEE Class II timing requirements**
- **Adjustable port delays to ensure compliance with IEEE 802.3u timing requirements (Section 27.3.1.4.4)**
- **Baseline wander correction included with integrated MLT-3 functionality**
- **User-enabled Far End Fault Indication (FEFI) to indicate an asymmetric link failure**
- **100-pin PQFP CMOS device with a single 5-V supply**

## GENERAL DESCRIPTION

The Am79C730 Integrated Multiport Repeater 100 (IMR100) device is an optimized system-level solution for unmanaged 100BASE-TX and 100BASE-FX hubs. The IMR100 device is a four-port, single-chip repeater that includes four 100BASE-TX ports which incorporate the entire physical layer, including the clock recovery and MLT-3 (Multi Level Threshold - 3 level) functional blocks. As a fully integrated CMOS solution, the IMR100 device substantially reduces power consumption and component cost when compared to discrete solutions.

In addition to enabling 100BASE-TX hubs, the IMR100 device is user-configurable to support 100BASE-FX operation on a single repeater port or on all four device ports. These 100BASE-FX options are selected via hardware and allow external fiber optic drivers to be connected directly to the IMR100 repeater ports.

To further reduce the total cost per repeater port, the expansion port allows multiple IMR100 devices to be interconnected to form a high port count repeater. A properly designed hub with multiple IMR100 devices connected together using the expansion port is capable of meeting IEEE Class II timing requirements for a single repeater.

When configuring the repeater device for a stackable design, the IMR100 device allows external expansion port delays to be considered. This enables system designers to meet the requirement that Start of Packet (SOP) delay be greater than or equal to End of Jam (EOJ) delay.

The IMR100 device provides per-port LED status indications for link, partition, and carrier sense. Rate-based LED support is included for percentage global activity and percentage global collision frequency.



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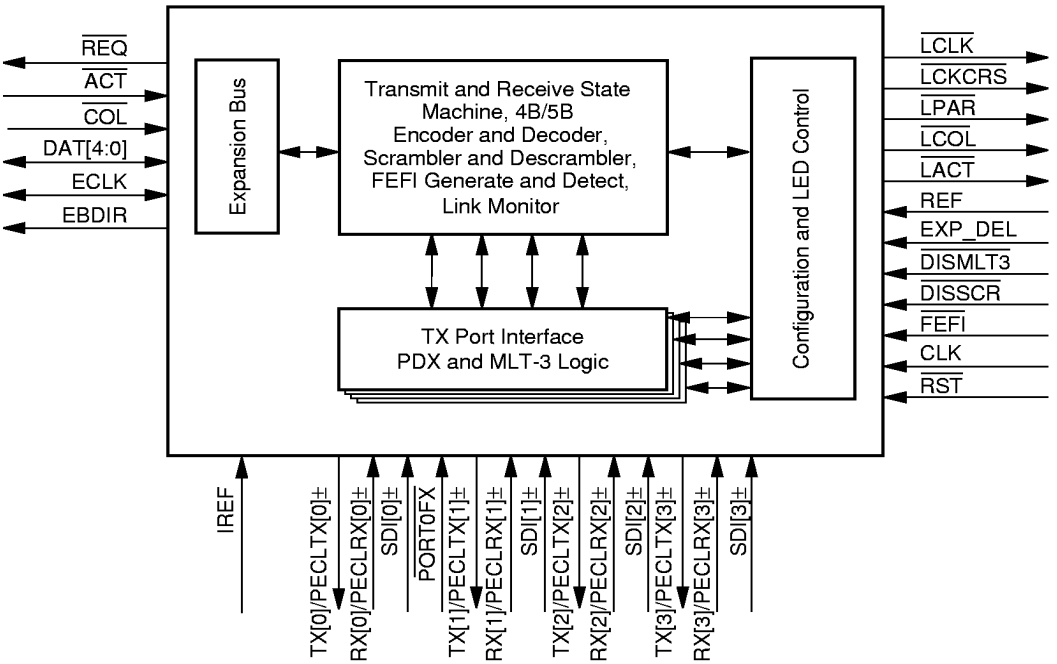
## BLOCK DIAGRAM

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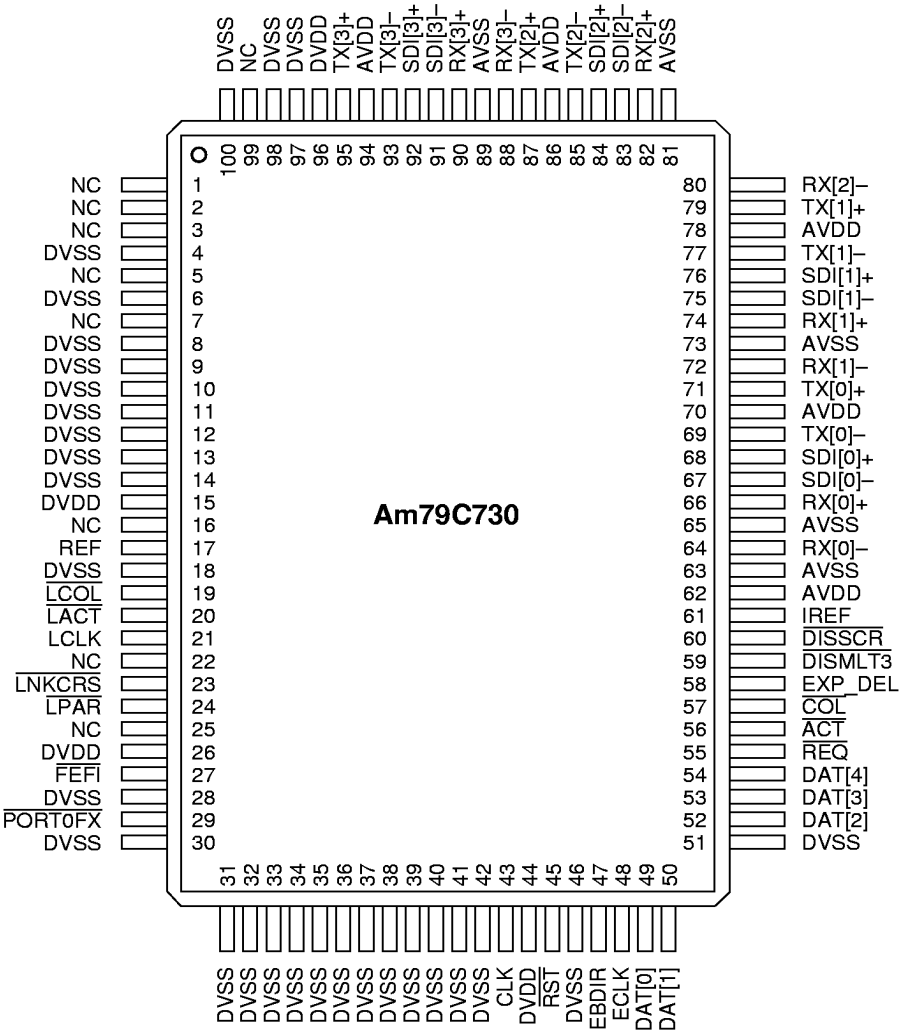
## RELATED PRODUCTS

| Part No. | Description |
|---|---|
| Am7992B | Serial Interface Adapter (SIA) |
| Am7996 | IEEE 802.3/Ethernet/Cheapernet Transceiver |
| Am79C90 | CMOS Local Area Network Controller for Ethernet (C-LANCE) |
| Am79C98 | Twisted Pair Ethernet Transceiver (TPEX) |
| Am79C100 | Twisted Pair Ethernet Transceiver Plus (TPEX+) |
| Am79C870 | Quad Fast Ethernet Transceiver (QFEX™) for 100BASE-X |
| Am79C871 | Quad Fast Ethernet Transceiver for 100BASE-X Repeater (QFEXr™) |
| Am79C981 | Integrated Multiport Repeater Plus (IMR+™) |
| Am79C982 | basic Integrated Multiport Repeater (bIMR™) |
| Am79C983 | Integrated Multiport Repeater 2 (IMR2™) |
| Am79C984A | enhanced Integrated Multiport Repeater (eIMR™) |
| Am79C985 | enhanced Integrated Multiport Repeater Plus (eIMR+™) |
| Am79C987 | Hardware Implemented Management Information Base (HIMIB™) |
| Am79C988 | Quad Integrated Ethernet Transceiver (QuIET™) |
| Am79C989 | Quad Ethernet Switching Transceiver (QuEST™) |
| Am79C940 | Media Access Controller for Ethernet (MACE™) |
| Am79C961 | PCnet™-ISA+ Single-Chip Ethernet Controller for ISA (with Microsoft® Plug n' Play® Support) |
| Am79C961A | PCnet™-ISA II Full Duplex Single-Chip Ethernet Controller for ISA |
| Am79C965 | PCnet™-32 Single-Chip 32-Bit Ethernet Controller |
| Am79C970A | PCnet™-PCI II Full Duplex Single-Chip Ethernet Controller (for PCI bus) |
| Am79C971 | PCnet™-*FAST* Single-Chip Full-Duplex 10/100 Mbps Ethernet Controller for PCI Local Bus |
| Am79C974 | PCnet™-SCSI Combination Ethernet and SCSI Controller for PCI Systems |

## CONNECTION DIAGRAM

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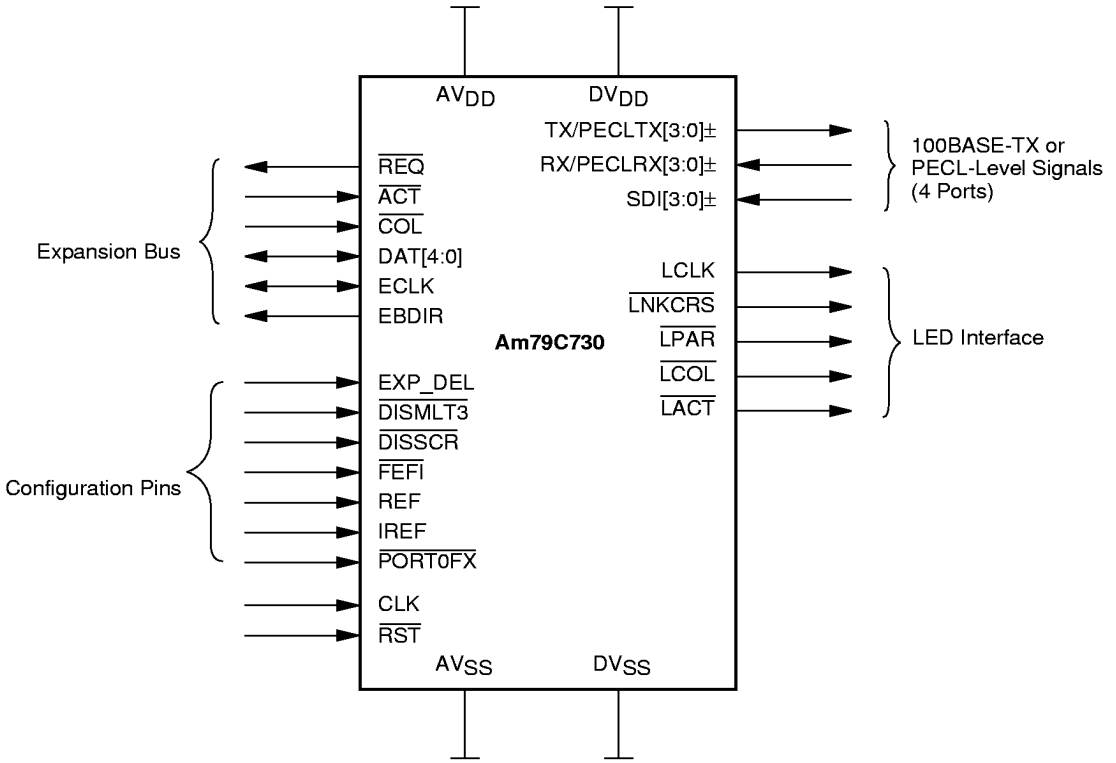
***Notes:***

1. *All TX and RX pins shown in this diagram are also PECLTX and PECLRX pins, respectively.*
2. *NC pins must be left floating. Do not tie to $V_{CC}$ or ground.*

## LOGIC SYMBOL

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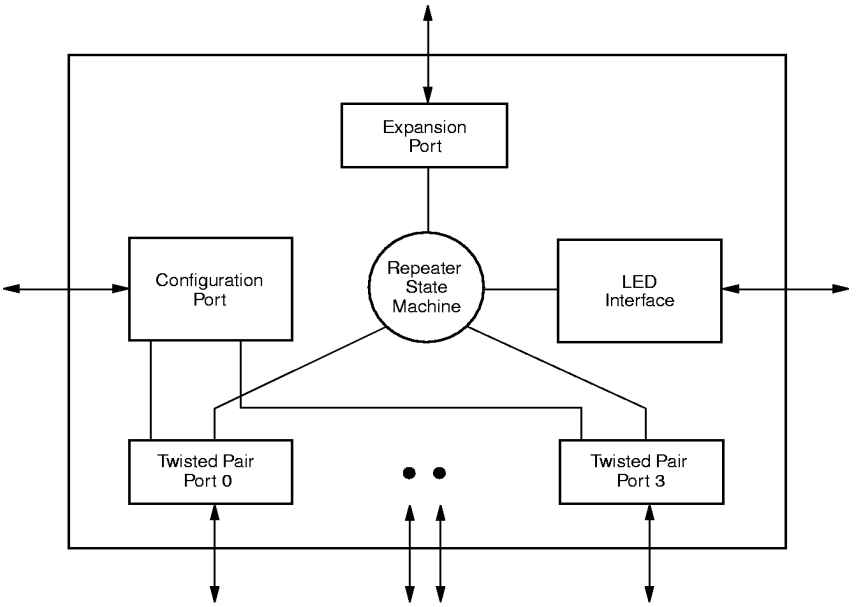
## LOGIC DIAGRAM

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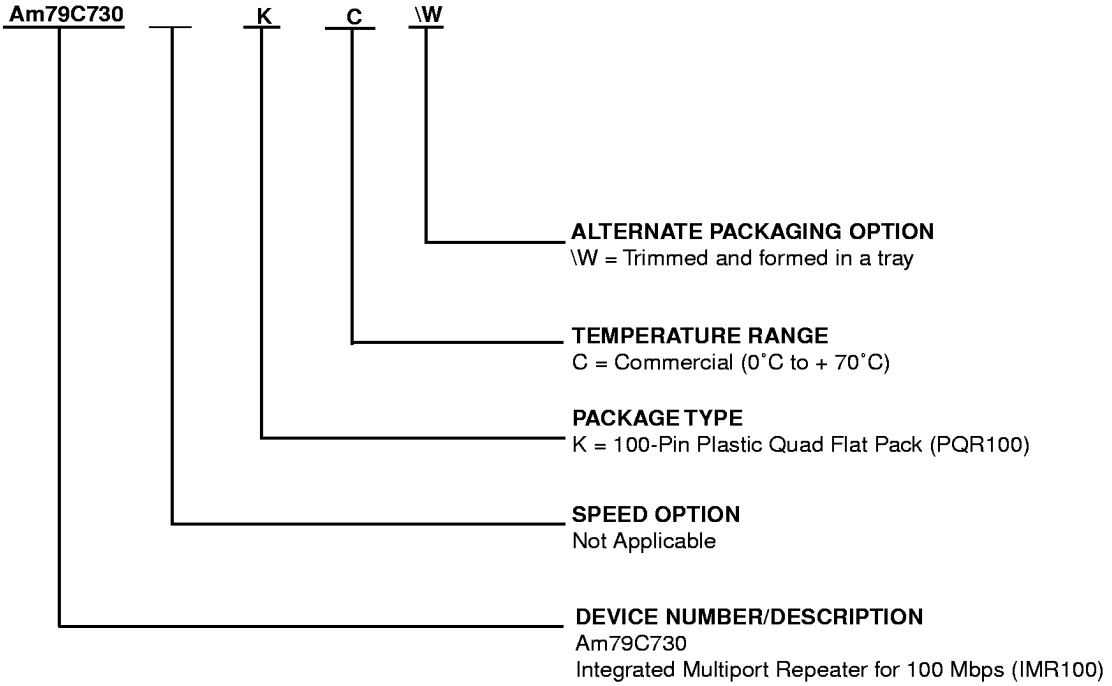
## ORDERING INFORMATION

### Standard Products

AMD standard products are available in several packages and operating ranges. The order number (Valid Combination) is formed by a combination of the elements below.




| Valid Combinations | |
|---|---|
| Am79C730 | KC\W |

**Valid Combinations**

Valid Combinations list configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations and to check on newly released combinations.

## TABLE OF CONTENTS

## PIN DESIGNATIONS

### Listed by Pin Number

| Pin No. | Pin Name | Pin No. | Pin Name | Pin No. | Pin Name | Pin No. | Pin Name |
|---|---|---|---|---|---|---|---|
| 1 | NC | 26 | $DV_{DD}$ | 51 | DVSS | 76 | SDI[1]+ |
| 2 | NC | 27 | $\overline{FEFI}$ | 52 | DAT[2] | 77 | TX/ PECLTX[1]- |
| 3 | NC | 28 | $DV_{SS}$ | 53 | DAT[3] | 78 | $AV_{DD}$ |
| 4 | $DV_{SS}$ | 29 | $\overline{PORT0FX}$ | 54 | DAT[4] | 79 | TX/ PECLTX[1]+ |
| 5 | NC | 30 | $DV_{SS}$ | 55 | $\overline{REQ}$ | 80 | RX/ PECLRX[2]- |
| 6 | $DV_{SS}$ | 31 | $DV_{SS}$ | 56 | $\overline{ACT}$ | 81 | $AV_{SS}$ |
| 7 | NC | 32 | $DV_{SS}$ | 57 | $\overline{COL}$ | 82 | RX/ PECLRX[2]+ |
| 8 | $DV_{SS}$ | 33 | $DV_{SS}$ | 58 | EXP_DEL | 83 | SDI[2]- |
| 9 | $DV_{SS}$ | 34 | $DV_{SS}$ | 59 | $\overline{DISMLT3}$ | 84 | SDI[2]+ |
| 10 | $DV_{SS}$ | 35 | $DV_{SS}$ | 60 | $\overline{DISSCR}$ | 85 | TX/ PECLTX[2]- |
| 11 | $DV_{SS}$ | 36 | $DV_{SS}$ | 61 | IREF | 86 | $AV_{DD}$ |
| 12 | $DV_{SS}$ | 37 | $DV_{SS}$ | 62 | $AV_{DD}$ | 87 | TX/ PECLTX[2]+ |
| 13 | $DV_{SS}$ | 38 | $DV_{SS}$ | 63 | $AV_{SS}$ | 88 | RX/ PECLRX[3]- |
| 14 | $DV_{SS}$ | 39 | $DV_{SS}$ | 64 | RX/ PECLRX[0]- | 89 | $AV_{SS}$ |
| 15 | $DV_{DD}$ | 40 | $DV_{SS}$ | 65 | $AV_{SS}$ | 90 | RX/ PECLRX[3]+ |
| 16 | NC | 41 | $DV_{SS}$ | 66 | RX/ PECLRX[0]+ | 91 | SDI[3]- |
| 17 | REF | 42 | $DV_{SS}$ | 67 | SDI[0]- | 92 | SDI[3]+ |
| 18 | $DV_{SS}$ | 43 | CLK | 68 | SDI[0]+ | 93 | TX/ PECLTX[3]- |
| 19 | $\overline{LCOL}$ | 44 | $DV_{DD}$ | 69 | TX/ PECLTX[0]- | 94 | $AV_{DD}$ |
| 20 | $\overline{LACT}$ | 45 | $\overline{RST}$ | 70 | $AV_{DD}$ | 95 | TX/ PECLTX[3]+ |
| 21 | LCLK | 46 | $DV_{SS}$ | 71 | TX/ PECLTX[0]+ | 96 | $DV_{DD}$ |
| 22 | NC | 47 | EBDIR | 72 | RX/ PECLRX[1]- | 97 | $DV_{SS}$ |
| 23 | $\overline{LNKCRS}$ | 48 | ECLK | 73 | $AV_{SS}$ | 98 | $DV_{SS}$ |
| 24 | $\overline{LPAR}$ | 49 | DAT[0] | 74 | RX/ PECLRX[1]+ | 99 | NC |
| 25 | NC | 50 | DAT[1] | 75 | SDI[1]- | 100 | $DV_{SS}$ |

***Note:*** *NC pins must be left floating. Do not tie to $V_{CC}$ or ground.*

## PIN DESCRIPTIONS

### 100BASE-TX/FX Ports

**TX[3:0]/PECLTX[3:0]±**
**Transmit Data**
**Differential Output**

These pins are differential drivers that transmit either MLT-3 or PECL-level signals. When configured for MLT-3 operation, the differential outputs are compliant with IEEE 802.3 Section 25 and connect directly with external isolation transformers and common-mode chokes. When set for PECL operation, the outputs are intended to be fed directly to fiber transmitters.

The transmit mode is selected by biasing SDI± and properly setting the $\overline{\text{DISMLT3}}$, $\overline{\text{DISSCR}}$, and $\overline{\text{PORT0FX}}$ pins. When $\overline{\text{DISMLT3}}$, $\overline{\text{DISSCR}}$, and $\overline{\text{PORT0FX}}$ are tied HIGH, all four device ports transmit MLT-3 signals suitable for 100BASE-TX operation. For fiber optic media, PECL-level NRZI signals are output by all four ports when $\overline{\text{DISMLT3}}$ and $\overline{\text{DISSCR}}$ are tied LOW.

$\overline{\text{PORT0FX}}$ is used to selectively configure port 0 for 100BASE-FX operation. When $\overline{\text{DISSCR}}$ and $\overline{\text{DISMLT3}}$ are tied HIGH and $\overline{\text{PORT0FX}}$ is tied LOW, the output from port 0 can be tied to a fiber transmitter. At the same time, ports 1-3 will transmit MLT-3 signals for 100BASE-TX operation.

**RX[3:0]/PECLRX[3:0]±**
**Receive Data**
**Differential Input**

These pins are differential inputs that receive either MLT-3 or PECL-level signals. When configured for MLT-3 operation, the differential inputs connect directly with external isolation transformers and common-mode chokes. When set for PECL operation, the inputs connect directly with fiber receivers.

The receive mode is selected by biasing SDI± and properly setting the $\overline{\text{DISMLT3}}$, $\overline{\text{DISSCR}}$, and $\overline{\text{PORT0FX}}$ pins. When $\overline{\text{DISMLT3}}$, $\overline{\text{DISSCR}}$, and $\overline{\text{PORT0FX}}$ are tied HIGH, all four ports receive MLT-3 signals suitable for 100BASE-TX operation. For fiber optic media, all four ports receive PECL-level NRZI data signals when $\overline{\text{DISMLT3}}$ and $\overline{\text{DISSCR}}$ are tied LOW.

$\overline{\text{PORT0FX}}$ is used to selectively configure port 0 for 100BASE-FX operation. When $\overline{\text{DISSCR}}$ and $\overline{\text{DISMLT3}}$ are tied HIGH and $\overline{\text{PORT0FX}}$ is tied LOW, port 0 input can be tied to a fiber transmitter. At the same time, ports 1-3 will receive MLT-3 signals for 100BASE-TX operation.

**SDI[3:0]±**
**Signal Detect**
**PECL Input**

The SDI differential pair input is driven by a fiber transceiver module to indicate whether the received optical signal is above the required threshold. There is one SDI pair per port.

When a port is configured for MLT-3 operation, SDI+ and SDI- must be tied to $AV_{SS}$. No pull-down resistor is required.

**Table 1. SDI[3:0]± Settings for Transceiver Operation**

| SDI[x]+ | SDI[x]- | Port Mode |
|---|---|---|
| $AV_{SS}$ | $AV_{SS}$ | MLT-3 Mode |
| $AV_{SS}$ | PECL Bias | Invalid Setting |
| PECL Bias | $AV_{SS}$ | Invalid Setting |
| PECL Bias | PECL Bias | PECL Mode |

### Expansion Port

**DAT[4:0]**
**Expansion Port Data**
**Input/Output/High Impedance**

DAT[4:0] carries 4B/5B encoded data and status information. The IMR100 device drives DAT[4:0] when both $\overline{\text{REQ}}$ and $\overline{\text{ACT}}$ pins are asserted. DAT[4:0] is an input when only $\overline{\text{ACT}}$ is asserted. If $\overline{\text{REQ}}$ and $\overline{\text{ACT}}$ are not asserted or $\overline{\text{COL}}$ is asserted, DAT[4:0] is in a high impedance state.

Table 2 defines DAT[4:0] content. DAT[4:0] must always be terminated to $V_{CC}$ with a 1-kΩ resistor.

**Table 2. Expansion Port Data Bus**

| DAT[4:0] | Data |
|---|---|
| 11111 | Idle |
| 00000 | Jam |
| 00100 | Symbol Error |
| 00010 | Bit Rate Error |
| 00001 | False Carrier |
| 4B/5B Code for 0 to F | Data 0 - F Hex |
| 4B/5B Code for JK | JK Header |

**ECLK**
**Expansion Port Clock**
**Input/Output**

Data transitions on DAT[4:0] are synchronized to this clock. ECLK is a 25-MHz output clock when DAT[4:0] is transmitting and a 25-MHz clock input when DAT[4:0] is receiving. ECLK must always be terminated to ground with a 1-kΩ resistor.

**$\overline{REQ}$**
**Request**
**Output, Active LOW**

$\overline{REQ}$ is driven LOW when the IMR100 device senses activity. An IMR100 device is defined as ACTIVE when it has one or more ports receiving data or experiencing collisions, or when it is still transmitting data from the internal FIFO. The assertion of this signal signifies that the IMR100 device requires the DAT[4:0] lines to transfer data, collision status information, or error status information to other IMR100 devices.

**$\overline{ACT}$**
**Activity**
**Input, Active LOW**

$\overline{ACT}$ is an input signal driven by an external arbiter. Assertion of $\overline{ACT}$ indicates that at least one IMR100 device is trying to control the Expansion Port ($\overline{REQ}$ is asserted).

***Note: If the expansion port is not used, $\overline{ACT}$ must be connected directly to $\overline{REQ}$.***

**$\overline{COL}$**
**Collision**
**Input, Active LOW**

$\overline{COL}$ is an input signal driven by an external arbiter. Assertion of $\overline{COL}$ indicates that more than one device has $\overline{REQ}$ true. When COL is asserted, DAT[4:0] enters a high impedance state and a JAM pattern is transmitted on the TX ports.

**EBDIR**
**External Buffer Direction Control**
**Output**

EBDIR is used to control the direction of external buffers on the Expansion Port. EBDIR is driven LOW when the device is driving DAT[4:0]. This is useful when the expansion port is routed off the board such as in stackable systems. When not driving the expansion port, the IMR100 expansion port drives EBDIR HIGH.

## LED Interface

**$\overline{LNKCRS}$**
**Port Link/Carrier Sense Status**
**Output**

$\overline{LNKCRS}$ outputs a serial bit stream indicating link status and carrier sense status for each port. $\overline{LNKCRS}$ is clocked by LCLK.

**$\overline{LPAR}$**
**Port Partition Status**
**Output**

$\overline{LPAR}$ outputs a serial bit stream indicating the partition status for each device port. Included in the bit stream is a designated bit that is set to "1" when an ALERT condition is detected. An ALERT condition is indicated when at least one of two conditions has occurred: (1) a device port has been partitioned during the previous 250-ms sampling period, or (2) network utilization was measured at 80 percent or greater during each of the previous four 250-ms sampling periods.

$\overline{LPAR}$ is clocked by LCLK.

**$\overline{LACT}$**
**Global Carrier Activity**
**Output**

$\overline{LACT}$ outputs an 8-bit serial stream indicating the amount of collision domain traffic. The number of consecutive LOW bits indicates the amount of activity. Activity is represented as a percentage of the total possible activity during the 250-ms sampling period. Refer to the *LED Support* section.

**$\overline{LCOL}$**
**Global Collision**
**Output**

$\overline{LCOL}$ outputs an 8-bit serial stream indicating the frequency of collisions experienced in the collision domain. The number of consecutive LOW bits indicates the percentage of total possible collisions that were experienced during the previous 250-ms sampling period. Refer to the *LED Support* section.

**LCLK**
**LED Clock**
**Output**

LCLK is the timing reference for the LED serial bit stream signals. It is a 12.5-MHz clock that operates in continuous bursts of 8 cycles. Each burst is separated by 250 ms.

## Miscellaneous Signals

**$\overline{RST}$**
**Reset**
**Input, Active LOW**

Assertion of $\overline{RST}$ clears the internal logic and resets all of the internal state machines. $\overline{RST}$ must be held LOW for at least 250 ms.

**CLK**
**Clock**
**Input**

CLK is the master clock signal for the IMR100 and must be a 25-MHz square wave.

**$\overline{DISSCR}$**
**Disable Scrambler**
**Input, Active LOW**

When $\overline{DISSCR}$ is LOW, the scrambling and descrambling circuits are disabled on all four ports. $\overline{DISSCR}$ is sampled at the rising edge of $\overline{RST}$.

**$\overline{\text{DISMLT3}}$**
**Disable MLT-3**
**Input, Active LOW**

When $\overline{\text{DISMLT3}}$ is LOW, the MLT-3 circuitry is disabled on all four ports and the TX drivers drive NRZI data signals. $\overline{\text{DISMLT3}}$ is sampled at the rising edge of $\overline{\text{RST}}$.

**$\overline{\text{FEFI}}$**
**Far End Fault Indication Enable**
**Input, Active LOW**

$\overline{\text{FEFI}}$ enables the far end fault capabilities of the IMR100 device. When asserted, any port detecting a signal loss will generate an error signal on the media as defined in IEEE 802.3u Section 24.3.2.1. $\overline{\text{FEFI}}$ is sampled at the rising edge of $\overline{\text{RST}}$.

**EXP_DEL**
**Expansion Port Delay**
**Input**

EXP_DEL sets the internal delay of the IMR100 device to compensate for the delay of the external circuitry on the expansion port. EXP_DEL should be tied LOW when the total expansion port delay is less than one clock cycle (40 ns). EXP_DEL should be tied HIGH when the total expansion port delay is greater than one clock cycle, but less than two clock cycles (80 ns). The total expansion port delay should be calculated as the sum of buffer, arbitration, and propagation delays. EXP_DEL is sampled at the rising edge of $\overline{\text{RST}}$.

Adjustment of internal delays is necessary to ensure compliance with IEEE 802.3u timing requirements (Section 27.3.1.4.4).

**IREF**
**Current Reference**
**Input**

IREF establishes the current reference for the IMR100 device. It must be tied to $V_{DD}$ via a 13-kΩ resistor with a 1 percent tolerance.

**$\overline{\text{PORT0FX}}$**
**Port 0 Select**
**Input, Active LOW**

$\overline{\text{PORT0FX}}$ is used to configure port 0 for fiber operation. When $\overline{\text{PORT0FX}}$ is pulled LOW, port 0 transmits and receives PECL-level signals, disables scrambling/descrambling, and enables the SDI± differential signal detect inputs. Thus, port 0 is placed in fiber mode regardless of the state of the $\overline{\text{DISSCR}}$ and $\overline{\text{DISMLT3}}$ pins. $\overline{\text{PORT0FX}}$ is sampled at the rising edge of $\overline{\text{RST}}$.

**REF**
**Voltage Reference**
**Input**

REF establishes the voltage reference for the IMR100 device. It must be tied to $V_{DD}$ via a 1k-Ω resistor with 5 percent tolerance.

## Power Supply

**$DV_{DD}$**
**Digital Power Pin**

These pins supply +5 V power for digital portions of the IMR100 circuitry.

**$DV_{SS}$**
**Digital Ground Pin**

These pins provide the ground reference for the digital portions of the IMR100 circuitry.

**$AV_{DD}$**
**Analog Power Pin**
These pins supply +5 V power for analog portions of the IMR100 circuitry.

**$AV_{SS}$**
**Analog Ground Pin**

These pins provide the ground reference for the analog portions of the IMR100 circuitry.

# FUNCTIONAL DESCRIPTION

## Overview

The Am79C730 IMR100 device is a single-chip, four port repeater that is ideally suited for unmanaged 100BASE-TX hubs. All four ports include the entire physical layer for 100BASE-TX, including MLT-3 functionality. In addition, user-configurable modes are provided which enable the IMR100 device to connect with external fiber transceivers to support 100BASE-FX applications.

When configured for 100BASE-TX operation, the IMR100 repeater is compatible with IEEE 802.3u Sections 24 and 25. The IMR100 device can be configured for 100BASE-FX operation on either one port or across all four repeater ports. For fiber applications, the selected IMR100 ports will transmit and receive PECL-level NRZI data signals.

An asynchronous expansion port is provided that allows multiple IMR100 devices to be connected together to form larger repeater systems. Properly designed systems using the IMR100 expansion port will meet IEEE Class II timing requirements. Comprehensive LED support is provided for multiple per port and global attributes.

## Basic Repeater Functionality

The IMR100 device implements the basic repeater functions as defined in Section 27 of IEEE 802.3, *Repeater for 100 Mbps Baseband Networks*.

### Repeater Function

If a single network port of a repeater system senses the start of a valid packet on its receive lines, the IMR100 device will retransmit the received data to all other enabled network ports (except when contention exists among any of the ports or when the receive port is partitioned). The repeated data will also be presented on DAT[4:0] of the expansion port to facilitate designs utilizing multiple IMR100 devices.

### Signal Regeneration

When retransmitting a packet, the IMR100 device ensures that the outgoing packet complies with the IEEE 802.3 specification in terms of preamble structure and timing characteristics for 100BASE-TX operation. The IMR100 repeater removes any receive jitter from incoming packets.

### Data Frame Forwarding

Packets received by any port connected to the repeater state machine are forwarded to all the ports.

### Partition Functional Requirements

The IMR100 device prevents the carrier activity of a faulty segment from propagating through the network. It accomplishes this by counting the number of consecutive collisions experienced on each port. This collision count is incremented on each transmission that suffers a collision and is reset upon successful transmission. If this collision count exceeds the value CCLIMIT (=63), the port will be partitioned.

When a partition condition is detected, the port in question will:

1. Stop receiving incoming packets.
2. Continue to send repeated packets.
3. Continue to monitor port activity.

The IMR100 device will reset the partition function when one of the following occurs:

1. Power-up or reset.
2. Detection of valid port activity that exceeds 450 to 560 bit times.
3. Exit from Link Fail.

### Receive Jabber Functional Requirements

The IMR100 device can detect illegally long data streams and prevent disruption of the network. If the data stream is longer than 45,000 to 75,000 bit times, the IMR100 will shut off the port receiving jabber.

Port functionality will be restored when one of the following occurs:

1. Power up or reset
2. Carrier is no longer detected

### Link Monitoring

The Link Monitor of the IMR100 device is responsible for determining whether the receive channel is providing reliable data. This takes advantage of the continuous signal detection of the Physical Medium Dependent (MLT-3) sublayer. The link is deemed reliable when the quality and level of the receive signal has been continuously satisfactory for a minimum of 330 μsec and maximum of 1000 μs.

The implementation of link monitoring in the IMR100 is compliant with IEEE 802.3 Clause 24.

### Carrier Integrity Monitor

The IMR100 device implements the Carrier Integrity Monitor (CIM) function for all ports. When a false carrier is detected, the repeater forces a JAM signal to all other ports. If the false carrier event reaches the 450 to 500 bit time boundary, the port is isolated (disabled). In addition, the port is isolated when two consecutive false carrier events are detected.

The affected port is re-enabled when at least one of the following conditions occur:

1. The port is idle for more than 33,333 bit times ±25%.
2. The port has a valid carrier that exceeds 450 to 500 bit times.

## Detailed Functions

### Port Interfaces

IMR100 repeater ports can support either 100BASE-TX or 100BASE-FX operation. Port operation is selected by properly configuring $\overline{\text{DISSCR}}$, $\overline{\text{DISMLT3}}$, $\overline{\text{PORT0FX}}$, and SDI± pins. The IMR100 can be hardware-configured to support the following options:

1. All four ports transmit and receive MLT-3 signals for 100BASE-TX compatibility.
2. All four ports transmit and receive PECL-level signals with stream cipher scrambling/descrambling disabled for connection to fiber transceivers.
3. Port 0 transmits and receives PECL-level signals for fiber operation, and ports 1-3 transmit and receive MLT-3 signals for 100BASE-TX operation. This option is useful when 100BASE-TX operation is desired on the majority ports, but a single fiber uplink is required.

Configuration requirements are described in detail below.

### Port Configuration

IMR100 repeater ports can support either 100BASE-TX or 100BASE-FX operation. 100BASE-TX operation requires that the IMR100 device transmit and receive MLT-3 signals with stream cipher scrambling/descrambling enabled. 100BASE-FX operation, however, requires the disabling of both the MLT-3 signaling and the scrambling/descrambling functionality.

MLT-3 signaling and scrambling/descrambling can be disabled via hardware by asserting $\overline{\text{DISMLT3}}$ and $\overline{\text{DISSCR}}$, respectively. When each pin is tied low, both MLT-3 and scrambling/descrambling are disabled on all four ports. In this configuration, each port transmits and receives PECL-level NRZI data, which is a requirement to connect with fiber transceivers.

Some applications will require 100BASE-TX operation on three IMR100 ports and 100BASE-FX operation on a single port. An example of this is a single fiber port on a TX hub. This configuration mode is supported by the $\overline{\text{PORT0FX}}$ pin. When $\overline{\text{PORT0FX}}$ is asserted, MLT-3 signaling and scrambling/descrambling functions are disabled on Port 0 regardless of the settings of $\overline{\text{DISSCR}}$ and $\overline{\text{DISMLT3}}$. An external fiber transceiver can then be attached to the PECL-level NRZI data signal of Port 0 to support 100BASE-FX operation. (Refer to the *Connection to Fiber Transceivers* section for proper biasing of the SDI± pins.) Assertion of $\overline{\text{PORT0FX}}$ does not disable MLT-3 signaling or scrambling/descrambling for ports 1-3. These three ports can be used for 100BASE-TX operation.

A summary of the proper pin settings for each mode of operation is shown in Table 3.

**Table 3. Port Configuration**

| Operation | $\overline{\text{DISSCR}}$ | $\overline{\text{DISMLT3}}$ | $\overline{\text{PORT0FX}}$ |
|---|---|---|---|
| All ports 100BASE-TX | HIGH | HIGH | HIGH |
| 100BASE-FX on port 0 and 100BASE-TX on ports 1-3 | HIGH | HIGH | LOW |
| All ports 100BASE-FX | LOW | LOW | X |
| Invalid Configuration | HIGH | LOW | X |
| Invalid Configuration | LOW | HIGH | X |

***Note:*** *Any port that is configured for MLT-3 signaling must have the SDI+ and SDI- pins pulled directly to analog ground.*

### MLT-3 Operation

When properly configured for MLT-3 operation, IMR100 driver outputs are compliant with IEEE 802.3 Section 25 specifications.

MLT-3 is a tri-level signaling scheme with all transitions between 0 V and +1 V or 0 V and -1 V. A transition in the MLT-3 signal during a clock cycle represents a data value of "1". A lack of transition in the MLT-3 signal represents a data value of "0". The stream cipher scrambling portion of the 100BASE-TX physical layer standard (integrated into the IMR100 device) ensures an adequate number of transitions in the data stream. An example of MLT-3 signaling is shown in Figure 1.

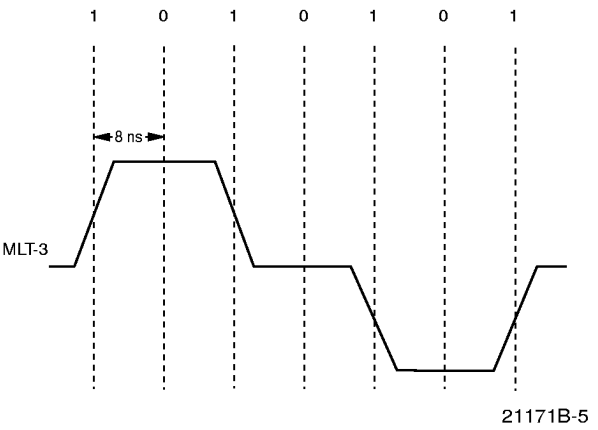



**Figure 1. MLT-3 Waveform**

The benefit of MLT-3 is that it reduces the fundamental frequency of the transmitted data which improves electromagnetic compliance (EMC) performance. MLT-3 reduces the 125 Mbps data rate of 100BASE-TX to a maximum line frequency of 31.25 MHz. A reduction in line frequency allows 100BASE-TX products to more easily pass regulatory EMC limits, such as FCC and CISPR. MLT-3 signal requirements are described in detail in ANSI X.3.263:1995 TP-PMD Revision 2.1 (1994).

Refer to the *Connection to Twisted Pair Media* section for the necessary terminations for MLT-3 operation using the IMR100 device.

The MLT-3 circuitry of the IMR100 includes protection against baseline wander, which is a DC bias effect generated by certain data patterns. The IMR100 receiver can tolerate a DC bias shift up to the full peak value of the signal without experiencing data loss.

### PECL Operation

When the IMR100 drivers are configured for PECL operation, the IMR100 ports can be connected directly to fiber transceivers to support 100BASE-FX operation. (See *Connection to Fiber Transceivers* section). In PECL mode, device ports transmit and receive non-return to zero inverted (NRZI) data at $AV_{DD}$ -1.475 V (logic LOW) and $AV_{DD}$ -0.88 V (logic HIGH) at a data rate of 100 MBaud.

### Expansion Port

The expansion port can be used to connect multiple IMR100 devices together to increase the number of ports in a single repeater system. Multiple IMR100 devices can be used in single-board applications, or in stackable or chassis-based systems. The expansion port signaling includes a 5-bit data bus (DAT[4:0]) and the following control signals: ECLK, $\overline{REQ}$, $\overline{ACT}$, and $\overline{COL}$. In addition to carrying 4B/5B encoded data, DAT[4:0] indicates various error and status conditions as shown in Table 4.

DAT[4:0] is transmitted synchronously to ECLK. All other expansion port signals operate asynchronously to ECLK. Timing diagrams illustrating the operation of the IMR100 expansion port signals are included in the *Switching Waveforms* section.

The IMR100 device requires external arbitration when using the expansion port. The arbiter allows only one IMR100 device to control the expansion port. If more than one device attempts to take control, the arbiter terminates all access and signals a collision condition.

**Table 4. DAT[4:0]**

| DAT[4:0] | Data |
|---|---|
| 11111 | Idle |
| 00000 | JAM |
| 00100 | Symbol Error |
| 00010 | Bit Rate Error |
| 00001 | False Carrier |
| 4B/5B Code for 0 to F | Data 0 - F Hex |
| 4B/5B Code for JK | JK Header |

$\overline{REQ}$ is an output that is asserted when an IMR100 device is receiving incoming data and wishes to control the expansion port. $\overline{ACT}$ is an input that is driven by an external arbiter. The arbiter should assert $\overline{ACT}$ when at least one IMR100 device in the system is requesting control of the expansion port ($\overline{REQ}$ is LOW). If multiple IMR100 devices are asserting $\overline{REQ}$, the arbiter should assert $\overline{COL}$ to indicate that a collision condition exists.

When an active IMR100 device ($\overline{REQ}$ asserted) receives a LOW $\overline{ACT}$ signal and a HIGH $\overline{COL}$ signal from the arbiter it drives the expansion port. When an active IMR100 device receives a LOW $\overline{COL}$ signal it indicates a JAM condition on DAT[4:0].

To aid in the design of stackable systems, the expansion port provides a direction control signal for external buffers. EBDIR is a TTL output and is driven LOW when DAT[4:0] is driving the bus. When not driving the expansion port, the IMR100 expansion port drives EBDIR HIGH. (See Figure 2).

The expansion port is always monitored by the IMR100 device. If the IMR100 expansion port is not utilized, the following connections must be made:

1. $\overline{ACT}$ must be directly connected to $\overline{REQ}$.
2. DAT[4:0] should be tied to $DV_{DD}$ via 1-kΩ resistors. $\overline{COL}$ must be tied directly to $DV_{DD}$.
3. ECLK should be tied LOW via a 1-kΩ resistor.

In a typical single-board application, six IMR100 devices can be connected together without the use of external buffers. (See Figure 3). The total number of IMR100 devices that can be used in a more complex architecture will depend on the drive capability, system timing limitations, and system design.

The total delay on the expansion port must be calculated in order to properly set the EXP_DEL pin. Proper setting of the EXP_DEL pin will ensure that an IMR100-based system complies with IEEE timing requirements. Refer to the *Internal Delay Adjustments* section.

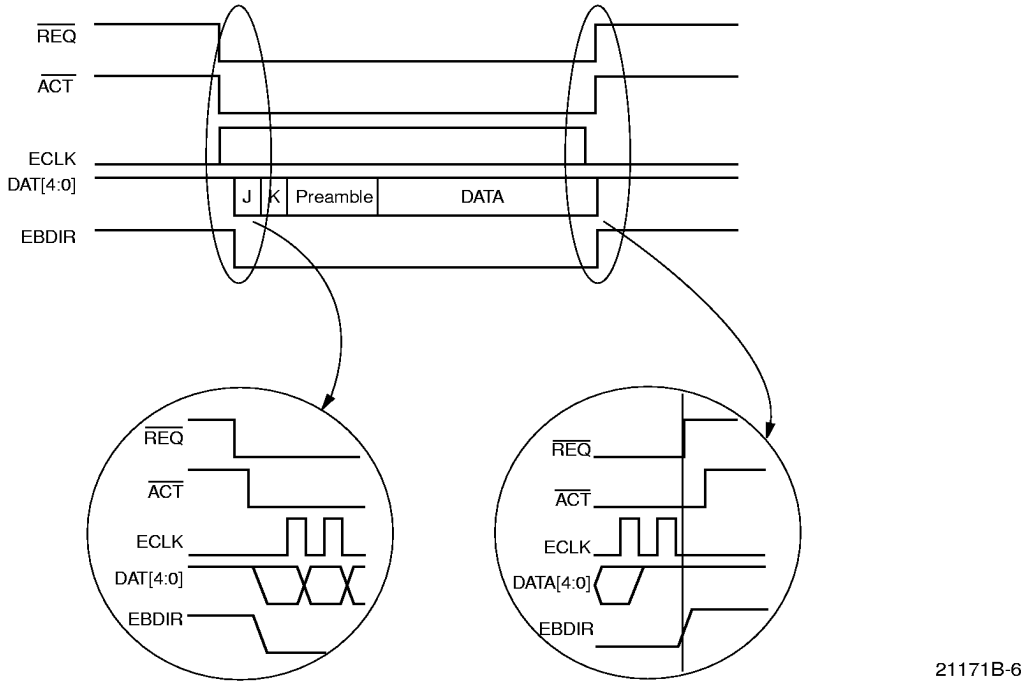



**Figure 2. Expansion Port Signals with the Edges of EBDIR Highlighted**

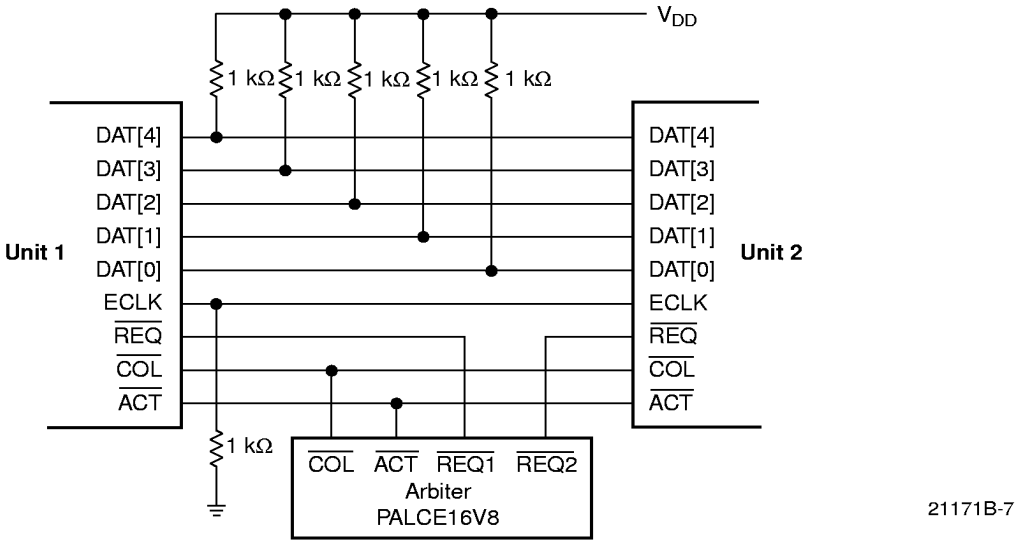



**Figure 3. Expansion Port Connection**

### Internal Delay Adjustments

IEEE 802.3u Section 27.3.1.4.4 specifies timing requirements that 100Mbps hubs must meet in order to claim compliance.

The EXP_DEL pin must be properly configured for an IMR100-based hub to meet the SOP ≥ EOJ timing requirement. Proper configuration is based on the expansion port delay and is shown in Table 5.

**Table 5. Recommended EXP_DEL Configuration**

| Total Expansion Port Delay | Pin Setting |
|---|---|
| Less than 40 nsec | LOW |
| Greater than 40 nsec but less than 80 nsec | HIGH |

Total expansion port delay consists of arbitration, buffer, and propagation delays. To meet Class II timing requirements, IMR100-based systems must have a total expansion port delay of less than or equal to 40 ns. Class I systems can be designed with expansion port delays of 40 to 80 ns. The IMR100 device is not designed to support expansion port delays greater than 80 ns.

### Reset Operation

The RESET pin must be held low for a minimum of 1.2 mS. During reset all inputs are ignored, all active high outputs are LOW, and all active low outputs are HIGH. Additionally, the device is configured on the rising edge of RESET as follows:

— MLT-3 enable/disable

— Scrambler and descrambler enable/disable

— Far End Fault Indication enable/disable

— Port 0 (fiber or MLT-3) enable/disable

### Far End Fault Generation and Detection

Far End Fault Indication (FEFI) can be set with the IMR100 device by setting $\overline{\text{FEFI}}$ at the rising edge of $\overline{\text{RST}}$. When $\overline{\text{FEFI}}$ is asserted, any port that senses a receive error (loss of signal or below threshold signal level) will transmit a far end fault indication as defined in IEEE 802.3u Section 24.3.2.1. This FEFI signal will indicate to the far end transceiver that a media fault condition exists. Any IMR100 port that receives a FEFI signal will enter a link fail state and start transmitting idles.

The Far End Fault Indiction signal is made up of three or more repeating cycles. Each cycle is composed of 84 consecutive ones followed by a single zero.

## LED Support

### Overview

The IMR100 device provides per port LED indications for link status, receive activity (carrier sense), and partition status. Global (collision domain) indications are given for network utilization and collision frequency. Network utilization and collision frequency are rate-based indications and can be used to drive bar graph displays. In addition, the IMR100 includes an Alert LED indication that is enabled during high network utilization or the partitioning of a local port.

The IMR100 LED control circuitry monitors activity and drives the LED outputs based on approximately 250 ms sampling period. For each 250 ms sampling period, the IMR100 device outputs four 8-bit serial streams ($\overline{\text{LPAR}}$, $\overline{\text{LNKCRS}}$, $\overline{\text{LCOL}}$, and $\overline{\text{LACT}}$) clocked by LCLK. LCLK is a 12.5 MHz clock that operates in bursts of 8 cycles. Data is output in bursts approximately every 250 ms and can be latched with external shift registers to drive status displays. The clock is automatically stopped until the beginning of the next 8-bit burst as shown in Figure 4.

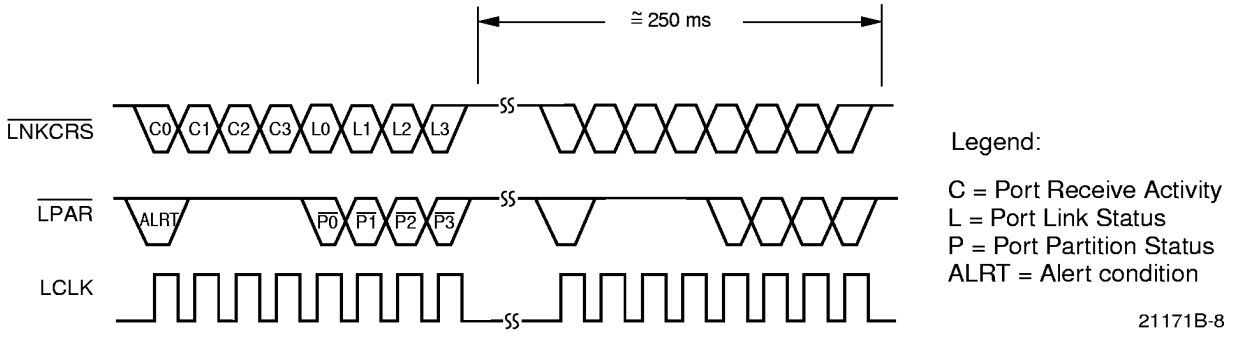



**Figure 4. LED Status Driver Waveform**

### Per Port LED Attributes

$\overline{\text{LNKCRS}}$ and $\overline{\text{LPAR}}$ output pins are used to indicate per port LED status information. Designated bits in the 8-bit serial stream output on the $\overline{\text{LPAR}}$ pin indicate the partition status of a particular port during the previous 250 ms sampling period (example: P0 indicates the partition status of port 0). If a particular port has been partitioned, the corresponding bit will be set to "1," turning the LED off.

The 8-bit serial stream output on $\overline{\text{LNKCRS}}$ indicates both link status and receive activity (carrier sense) for all four ports. Each bit indicates either link status or receive activity for a designated port. If a bit has been set to "1" by the IMR100 device, the corresponding port has a valid link signal or receive activity has been detected on that port.

The IMR100 LED outputs can be connected directly to a shift register as shown in Figure 5. The state of the shift register is frozen after the last bit in the burst, with the shift register indicating the state of the previous sampling period.

### Alert LED Status Indication

An alert condition is indicated by the first bit in the $\overline{\text{LPAR}}$ serial bit stream. This alert bit can be used to warn of anomalous network behavior. The ALRT bit is set to "1" if at least one of the following two conditions occur:

1. Any local port was partitioned during the last 250 ms sampling period
2. Network utilization was 80 percent or greater during each of the previous four 250 ms sampling periods.

### Global LED Attributes

Pins $\overline{\text{LACT}}$ and $\overline{\text{LCOL}}$ can be used to drive rate-based displays indicating receive activity and collision activity, respectively. Each output consists of an 8-bit value that can be fed to a shift register to drive a rate-based display, such as a bar graph. The 8-bit bursts are based on 250 ms sampling periods. LCLK is automatically stopped between 8-bit bursts.

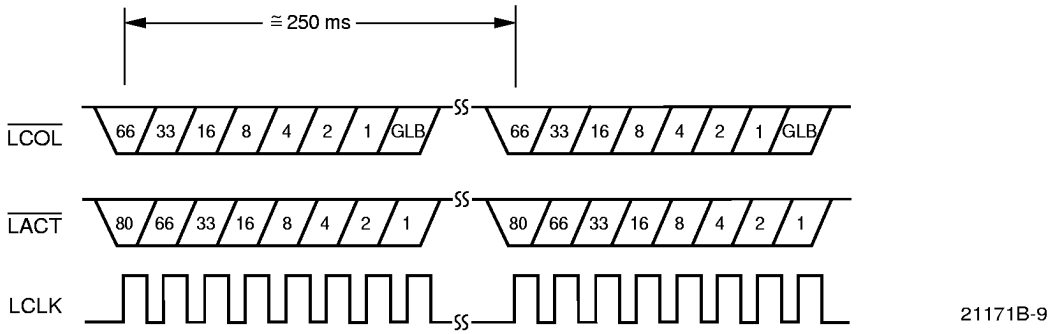



**Figure 5. Bar Graph LED Driver Waveform**

The output on $\overline{\text{LACT}}$ indicates the amount of receive activity during the previous 250 ms sampling period. Similarly, the output on $\overline{\text{LCOL}}$ indicates the amount of collisions during the previous 250 ms sampling period. The correlation between the 8-bit value and the amount of receive activity or collisions is shown in Table 6.

The output on $\overline{\text{LACT}}$ and $\overline{\text{LCOL}}$ can be connected directly to an external shift register as shown in Figure 12.

Bit 7 of LCOL is the global collision bit, GLB. It indicates whether or not a collision occurred during the last 250-ms sampling period. It can be implemented through an external register gate if collision rate status is not needed.

**Table 6. Collision Rate and Activity**

| % of Maximum Occurrence of Collision | % of Maximum Activity | Number of LEDs Lit |
|---|---|---|
| 1 | 1 | 1 |
| 2 | 2 | 2 |
| 4 | 4 | 3 |
| 8 | 8 | 4 |
| 16 | 16 | 5 |
| 33 | 33 | 6 |
| 66 | 66 | 7 |
| | 80 | 8 |

## SYSTEM LEVEL CONSIDERATIONS

### IEEE Timing Requirements

End of JAM is referred to as EOJ. Section 27 uses these parameters to define a repeater as either Class I or Class II. A Class I repeater has delays such that a single repeater can be placed between any two DTEs. A Class II repeater allows two repeaters to be placed between any two DTEs. The official definition is given in Table 7.

**Table 7. Repeater Classes Relating to TX and FX**

| Class I Repeater | Class II Repeater With All Ports TX |
|---|---|
| SOP + SOJ ≤ 140 BT | SOP ≤ 46 BT, SOJ ≤ 46BT |
| SOP ≥ EOJ | SOP ≥ EOJ |

***Notes:***

1. *Start of Packet is referred to as SOP. Start of JAM is referred to SOJ.*
2. *BT = Bit Time.*

The goal of the IMR100 is to enable the IMR100-system to meet Class II requirements. A properly designed system with multiple IMR100 devices (connected together by the expansion port) will meet Class II requirements, if the delay of the expansion port's arbitration circuitry is less than 40 ns. If the delay of the arbitration circuitry is between 40 ns and 80 ns, the system can meet Class I requirements. The IMR100 device is not designed to work with arbitration circuitry with delay greater than 80 ns.

### Board Layout Recommendations

The Am79C730 device has digital and analog power pins. It is recommended that the designer use separate digital and analog power planes. The planes should meet at a point near the power source on the board.

Although separate power planes present the optimum solution, it is possible to design a working system with a single power plane and a single ground plane. A separate ground plane must be placed under the RJ45 connectors (Figure 6) to prevent cross talk problems.

When separate planes are used the following recommendations are made:

- The digital and analog planes should be connected at the power source as shown in Figure 6.
- Digital signals should only be run over the digital plane and analog signals over the analog plane. If it is necessary to run a signal over both the analog and digital plane, the power planes should be bridged as shown in Figure 7.
- The void (area between the digital plane and the analog plane) should be under pin 59 (some overlap to pins 60 and 58) and pin 97 (some overlap to pins 96 and 100). Care should be taken to ensure that pin 96 is not over the analog plane.
- Since there is no internal connection between the analog power lines and the digital power lines, a bridge should be provided between the planes near the IMR100 device. A ferrite bead is recommended.

In all cases, the following recommendations are made:

- Do not run signal traces through areas not covered by power planes.
- Keep clock lines as short as possible. To ensure this, lay out the clock signal traces before laying out any other signal traces.
- In stackable systems, the cable for the Expansion Port should include sufficient ground lines, which should be interlaced with signal lines.

Figure 8 shows the recommended decoupling capacitor placement. They should be surface-mount 0.01-µF capacitors. The capacitors must be placed as close as possible to the pins.

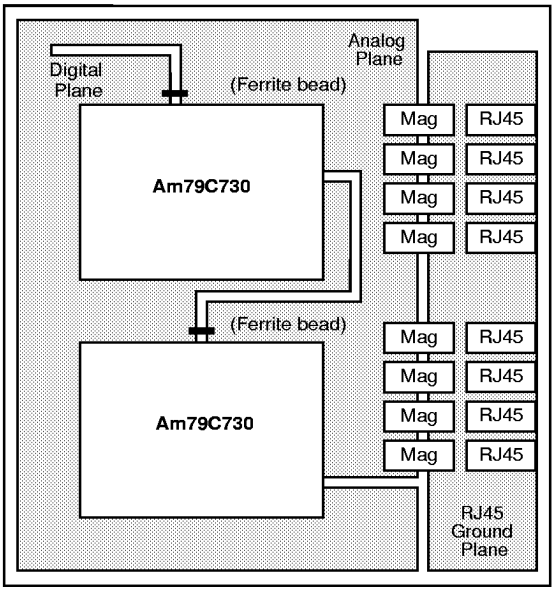



**Figure 6. Layout Recommendation for the IMR100**

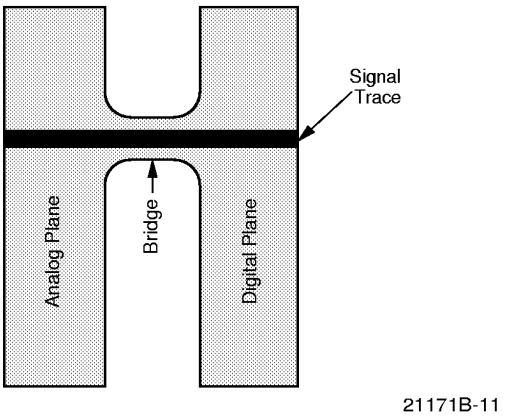



**Figure 7. Bridge between Analog and Digital**

## Connection to Twisted Pair Media

The pin locations on the IMR100 are optimized for straight across wiring to the RJ45 connectors. That is, it is not necessary to cross the traces on different layers of the board. Halo, Pulse, and Valor provide isolation transformers with the optimized configuration. Figure 9 illustrates the recommended wiring of the TX ports. Proper termination consists of a 100-Ω resistor and a 1:1 isolation transformer with common-mode chokes. External filters are not required.

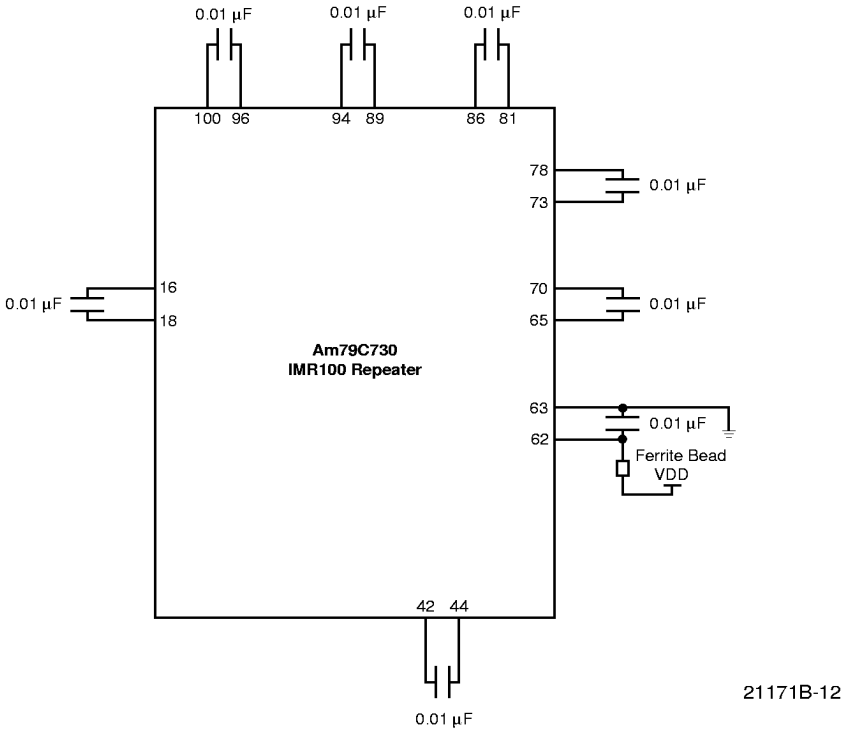



**Figure 8. Recommended Decoupling for the IMR100**

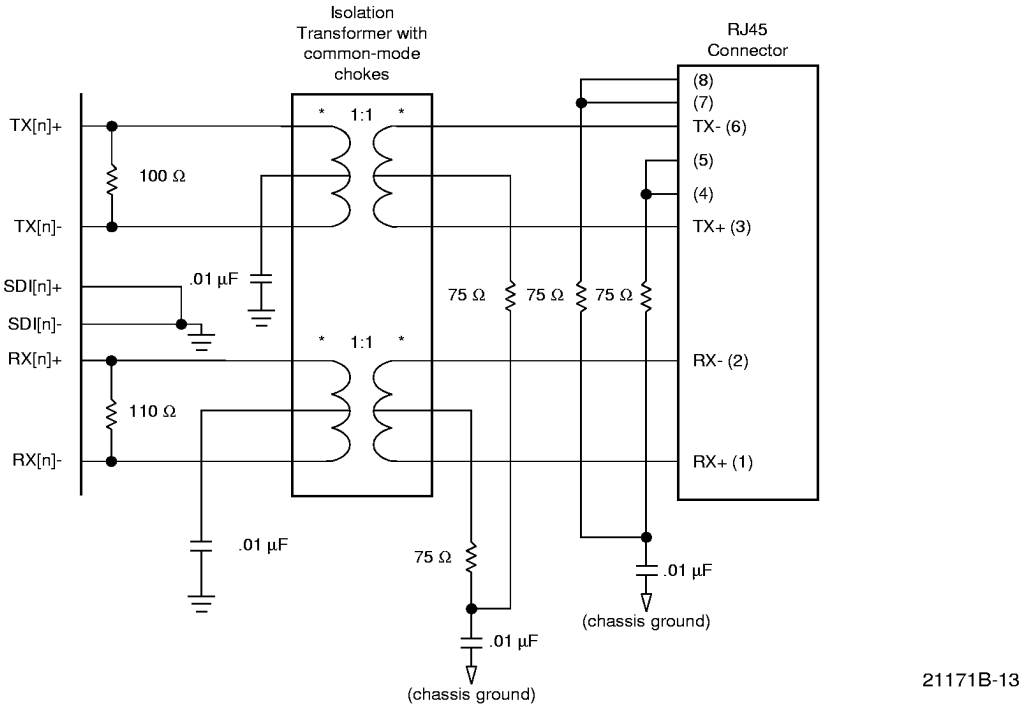



**Figure 9. TX Port Wiring Diagram**

## Connection to Fiber Transceivers

The IMR100 device is designed to interoperate with standard fiber optic data links (ODLs) to support 100BASE-FX repeater applications. When used in such an application, the IMR100 device's transmit and receive pairs must be configured properly.

When configuring the device for FX operation on all four ports, follow these setting options:

1. The transmit and receive pins need to be set for PECL mode. This is done by properly biasing those signal pins at 3 V with the resistor network shown in Figure 10.
2. The $\overline{\text{DISMLT3}}$ pin must be tied LOW to enable the reception and transmission of PECL type signals.
3. The $\overline{\text{DISSCR}}$ pin must be tied LOW to disable the scrambler/descrambler function.

***Note:*** *All 3 configuration conditions must be met for proper IMR100 fiber operation on all four ports.*

When configuring the device for FX operation on Port 0 *only*, follow these setting options:

1. Port 0 transmit and receive pins need to be set for PECL mode. This is done by properly biasing those signal pins at 3 V with the resistor network shown in Figure 10.
2. The $\overline{\text{PORT0FX}}$ pin must be tied LOW to enable PECL operation on Port 0. (When $\overline{\text{PORT0FX}}$ is pulled LOW, Port 0 transmits and receives PECL-level signals, disables scrambling/descrambling, and enables the SDI± differential signal detect inputs. Thus, Port 0 is placed in fiber mode regardless of the state of the $\overline{\text{DISSCR}}$ and $\overline{\text{DISMLT3}}$ pins.)

***Note:*** *Both configuration conditions must be met for proper IMR100 fiber operation on Port 0 only.*

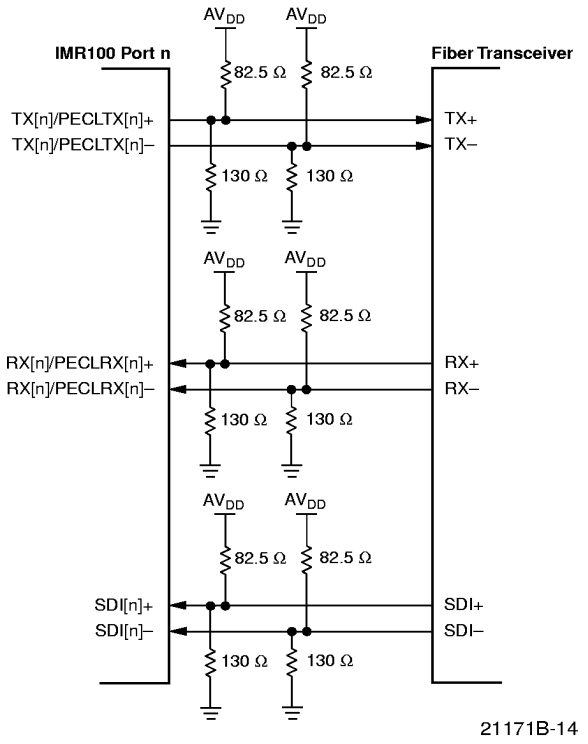



**Figure 10. FX Connection**

## Expansion Port Arbitration

The external arbiter can be a simple PAL device, such as a PALCE16V8. It is programmed so that when at least one $\overline{REQ}$ is true, $\overline{ACT}$ is true and when more than one $\overline{REQ}$ is true, $\overline{COL}$ is true. The recommended equations for $\overline{ACT}$ and $\overline{COL}$ are

$\overline{ACT}$ = ($\overline{REQ}$[0] *$\overline{REQ}$[1]..... * $\overline{REQ}$[n])

$\overline{COL}$ = ($\overline{REQ}$[0] + ($\overline{REQ}$[1] * $\overline{REQ}$[2] ..... *$\overline{REQ}$[n])) *

($\overline{REQ}$[1] + ($\overline{REQ}$[2] * $\overline{REQ}$[3] ..... *$\overline{REQ}$[n])) *

.....

.....

($\overline{REQ}$[n-1] +$\overline{REQ}$[n])

Where

Overbar = negation

* = AND

+ = OR

$\overline{REQ}$[x] = $\overline{REQ}$ from an IMR100 device.

***Note:*** *These equations are not optimized.*

## LED Implementation Examples

Although information on Link status and Partition status is contained in two different 8-bit serial streams, a single shift register can be used to drive LEDs that will display status indications for both attributes. Configuration examples are illustrated in Figures 11, 12, and 13.

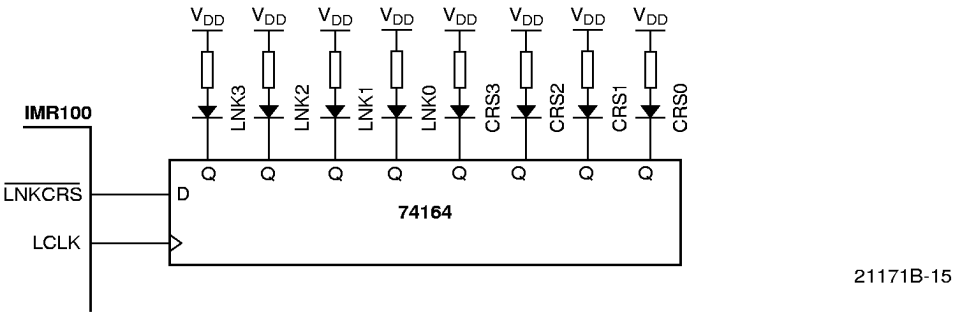
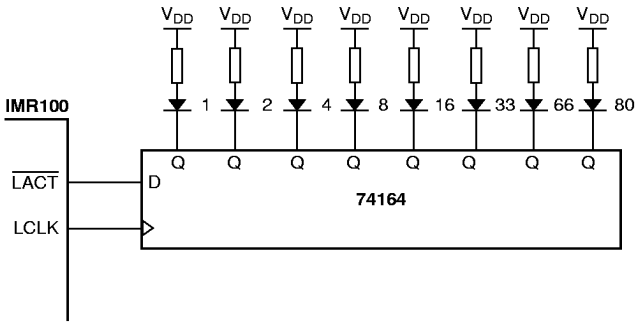
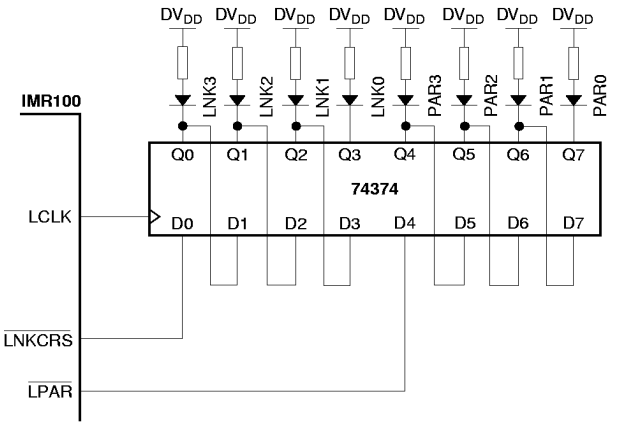



**Figure 11. Example: LED Connections Illustrating $\overline{LNKCRS}$**




21171B-16

**Figure 12. Example: LED Circuit for Activity**




21171B-17

**Figure 13. Example: LED Connection with Link and Partition**

## ABSOLUTE MAXIMUM RATINGS

Storage Temperature:. . . . . -65°C to +150°C

Ambient Temperature Under Bias: . . . . 0°C to +70°C

Supply Voltage to
$AV_{SS}$ or $DV_{SS}$ ($AV_{DD}$, $DV_{DD}$): . . . . . -0.3 V to +6.0 V

DC Voltage applied to
any Pin Referenced to $V_{SS}$: . . . . -0.5 V to $V_{CC}$ + 0.5 V

*Stresses above those listed under Absolute Maximum Ratings may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to absolute maximum ratings for extended periods may affect device reliability.*

## OPERATING RANGES

Temperature (TA): . . . . . .0°C to +70°C

Supply Voltages ($AV_{DD,}$ $DV_{DD}$): . . +4.75 V to +5.25 V

*Operating ranges define those limits between which functionality of the device is guaranteed.*

## DC CHARACTERISTICS

### Digital I/O

| Symbol | Parameter Description | Test Conditions | Min | Max | Unit |
|---|---|---|---|---|---|
| $V_{IL}$ | Input Low Voltage | $DV_{SS}$ = 0.0V | -0.5 | 0.8 | V |
| $V_{IH}$ | Input High Voltage | $DV_{SS}$ = 0.0V | 2.0 | $V_{DD}$ + 0.5 | V |
| $V_{OL}$ | Output Low Voltage | $I_{OL}$ = 4 mA | - | 0.4 | V |
| $V_{OH}$ | Output High Voltage | $I_{OH}$ = -0.4 mA | 2.4 | - | V |
| $I_{OZ}$ | Output Leakage Current (Note 1) | 0.4 V < $V_{OUT}$ < $DV_{DD}$ | -10 | 10 | µA |
| $I_{IL}$ | Input Leakage Current | $DV_{SS}$ < $V_{IN}$ < $DV_{DD}$ | | 10 | µA |

### Analog I/O – MLT-3 Mode

| Symbol | Parameter Description | Test Conditions | Min | Max | Unit |
|---|---|---|---|---|---|
| $V_{TXD}$ | Differential Output Peak Voltage (Note 2) | VDD = Maximum | 950 | 1050 | mV |
| $V_{SDA}$ | Input Differential Assert Threshold (See Figure 16) | VDD = Maximum | | 950 | mV |
| $V_{SDD}$ | Input Differential De-assert Threshold (See Figure 16) | VDD = Maximum | 200 | | mV |
| $I_{IX}$ | Input Leakage Current | 0V < VIN < VDD | -10 | 10 | µA |

***Notes:***

1. *$I_{OZ}$ applies to all three-state output pins and bidirectional pins.*
2. *$V_{TXD}$ is measured with a 100-Ω termination and a standard Ethernet transformer with a UTP-test load (100Ω) across the secondary winding.*

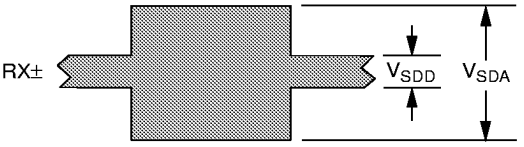



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**Figure 16. Receiver Differential Input**

## Analog I/O – PECL Mode

| Symbol | Parameter Description | Test Conditions | Min | Max | Unit |
|---|---|---|---|---|---|
| $V_{OHP}$ | Output HIGH Voltage | $V_{DD}$ = Maximum PECL Test Load | $V_{DD}$-1.075 | $V_{DD}$-0.830 | V |
| $V_{OLP}$ | Output LOW Voltage | $V_{DD}$ = Maximum PECL Test Load | $V_{DD}$-1.860 | $V_{DD}$-1.570 | V |
| $V_{SDD}$ | Input Voltage Differential | $V_{DD}$ = Maximum | 0.35 | 1.1 | V |
| $V_{CM}$ | Input Common Mode Voltage | $V_{DD}$ = Maximum | $V_{DD}$-2.0 | $V_{DD}$-0.55 | V |
| $I_{LX}$ | Input Leakage Current | 0V < VIN < VDD | -10 | 10 | µA |

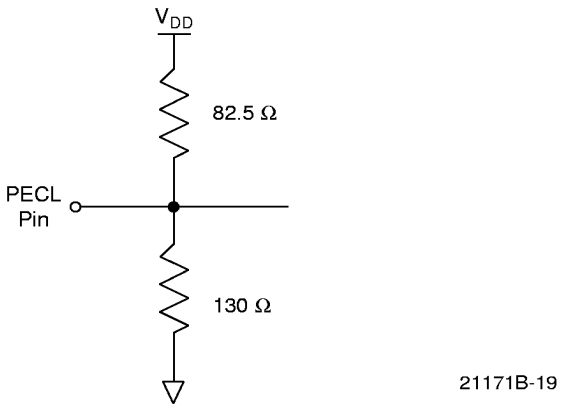
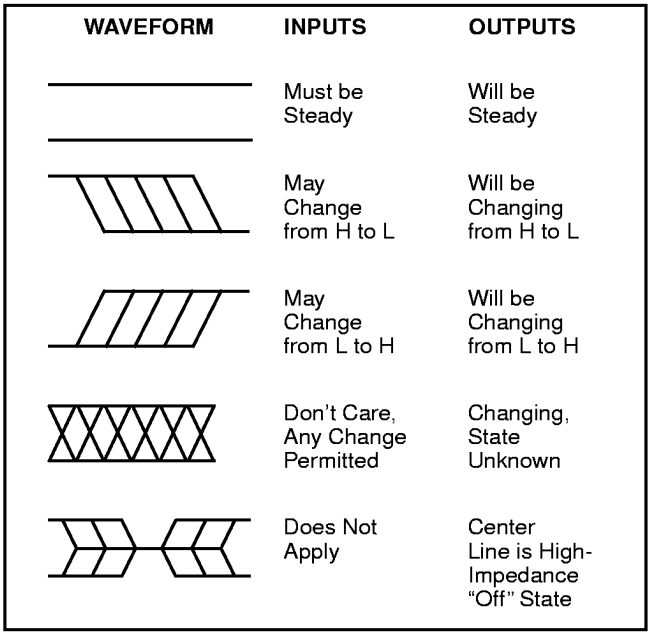



**Figure 17. PECL Test Load**

## Power Supply Current

| Symbol | Parameter Description | Test Conditions | Min | Max | Unit |
|---|---|---|---|---|---|
| $I_{DD}$ | Power Supply Current | $V_{DD}$ = Maximum MLT-3 Mode | – | TBD | mA |
| | | $V_{DD}$ = Maximum PECL Mode | – | TBD | mA |

## KEY TO SWITCHING WAVEFORMS



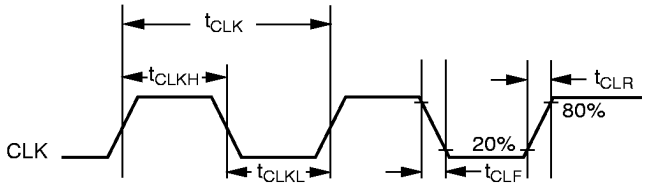

KS000010-PAL

## SWITCHING CHARACTERISTICS AND WAVEFORMS

### Clock Timing

| Symbol | Parameter Description | Min | Max | Unit |
|---|---|---|---|---|
| $t_{CLK}$ | CLK Period | 39.996 | 40.004 | ns |
| $t_{CLKH}$ | CLK High Pulse Width | 18 | 22 | ns |
| $t_{CLKL}$ | CLK Low Pulse Width | 18 | 22 | ns |
| $t_{CLR}$ | Clock Rise Time (Note 1) | | 5 | ns |
| $t_{CLF}$ | Clock Fall Time (Note 1) | | 5 | ns |

***Note:***
*1. Parameter not tested.*




21171B-20

**Figure 18. Clock Timing**

## Expansion Port Timing

| Symbol | Parameter Description | Min | Max | Unit |
|---|---|---|---|---|
| $t_{DEV}$ | DAT[4:0] Valid Before the Rising Edge of ECLK | 17.5 | – | ns |
| $t_{EDV}$ | DAT[4:0] Valid After the Rising Edge of ECLK | 12.5 | – | ns |
| $t_{DES}$ | DAT[4:0] Setup Time to the Rising Edge of ECLK | 10 | – | ns |
| $t_{EDH}$ | DAT[4:0] Hold Time From the Rising Edge of ECLK | 5 | – | ns |
| $t_{ERT}$ | ECLK Rise Time When DAT[4:0] is transmitting (Note 1) | – | 6 | ns |
| $t_{EFT}$ | ECLK Fall Time When DAT[4:0] is transmitting (Note 1) | – | 6 | ns |
| $t_{ERR}$ | ECLK Rise Time When DAT[4:0] is Receiving (Note 1) | – | 6 | ns |
| $t_{EFR}$ | ECLK Fall Time When DAT[4:0] is Receiving (Note 1) | – | 6 | ns |

***Note:***
*1. Parameter not tested.*

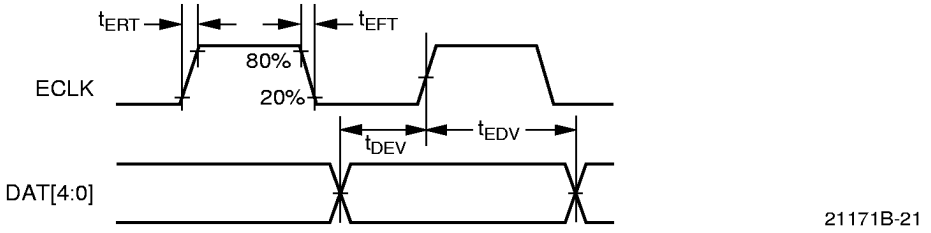



**Figure 19. Expansion Port Source Timing**

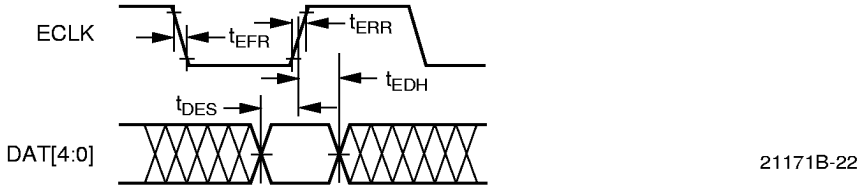



**Figure 20. Expansion Port Receive Timing**

## Device Configuration Interface Timing

| Symbol | Parameter Description | Min | Max | Unit |
|---|---|---|---|---|
| $t_{RST}$ | $\overline{RST}$ pulse width low | 1.2 | – | ms |
| $t_{MRS}$ | Input setup time to the rising edge of $\overline{RST}$ for $\overline{DISSCR}$, $\overline{DISMLT3}$, $\overline{PORT0FX}$, EXP_DEL, and $\overline{FEFI}$ | 80 | – | ns |
| $t_{RMH}$ | Input hold time from the rising edge of $\overline{RST}$ for $\overline{DISSCR}$, $\overline{DISMLT3}$, $\overline{PORT0FX}$, EXP_DEL, and $\overline{FEFI}$ | 0 | – | ns |

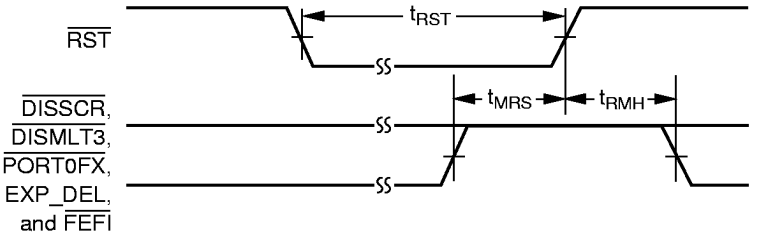



**Figure 21. Configuration Timing**

## LED Timing

| Symbol | Parameter Description | Min | Max | Unit |
|---|---|---|---|---|
| $t_{LCP}$ | LCLK Period | 79 | 81 | ns |
| $t_{LCH}$ | LCLK HIGH | 35 | 45 | ns |
| $t_{LCL}$ | LCLK LOW | 35 | 45 | ns |
| $t_{LDCV}$ | Data Valid Before the Rising Edge of LCLK | 25 | – | ns |
| tLCDV | Data Valid After the Rising Edge of LCLK | 25 | – | ns |

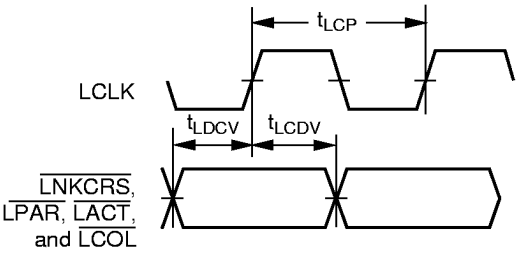



**Figure 22. LED Control Signal**

## MLT-3 Timing

| Symbol | Parameter Description | Min | Max | Unit |
|---|---|---|---|---|
| $t_{TXR}$ | Rise Time of TXD Output Signal (Note 1) | 3.0 | 5.0 | ns |
| $t_{TXF}$ | Fall Time of TXD Output Signal (Note 1) | 3.0 | 5.0 | ns |
| $t_{TXRFS}$ | Rise and Fall Time Symmetry of TXD Output Signal (Note 1) | — | 0.5 | ns |
| $t_{DCDJ}$ | Duty Cycle Distortion Jitter (Note 2) | — | ±2.5 | ns |
| $t_{TXJ}$ | Transmit Jitter | — | 1.4 | ns |

***Notes:***

1. *Parameter not tested.*
2. *Measured using data pattern 10101010.*

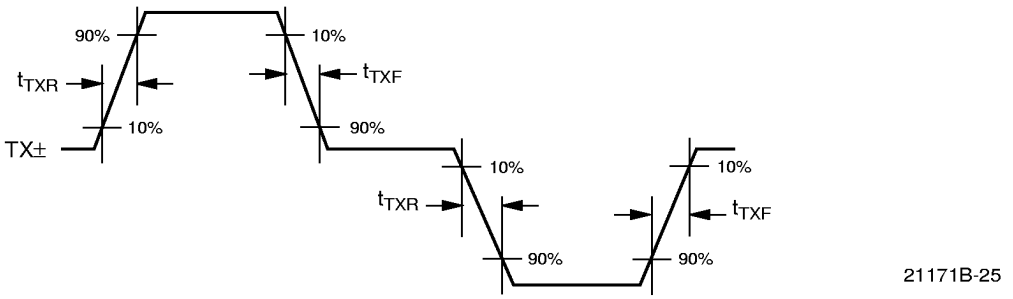



**Figure 23. TX± Rise and Fall Times**

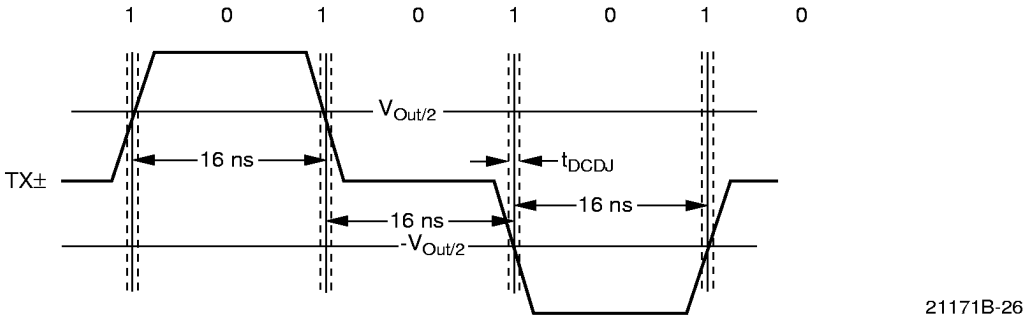



**Figure 24. TX± Duty Cycle and Jitter**

## PECL Timing

| Symbol | Parameter Description | Min | Max | Unit |
|---|---|---|---|---|
| $t_{PRT}$ | Rise Time of PECLTX± (Note 1) | – | 0.3 | ns |
| $t_{PFT}$ | Fall Time of PECLTX± (Note 1) | – | 0.3 | ns |
| $t_{PRFST}$ | Rise and Fall Time Symmetry of PECLTX± (Note 1) | -200 | 200 | ps |
| $t_{SDISU}$ | SDI± Setup Time to Clock | 7 | – | ns |
| $t_{SDIH}$ | SDI± Hold Time From Clock | 5 | – | ns |
| $t_{PRR}$ | Rise Time of PECLRX± | – | 2 | ns |
| $t_{PFR}$ | Fall Time of PECLRX± | – | 2 | ns |

***Note:***
*1. Parameter not tested.*

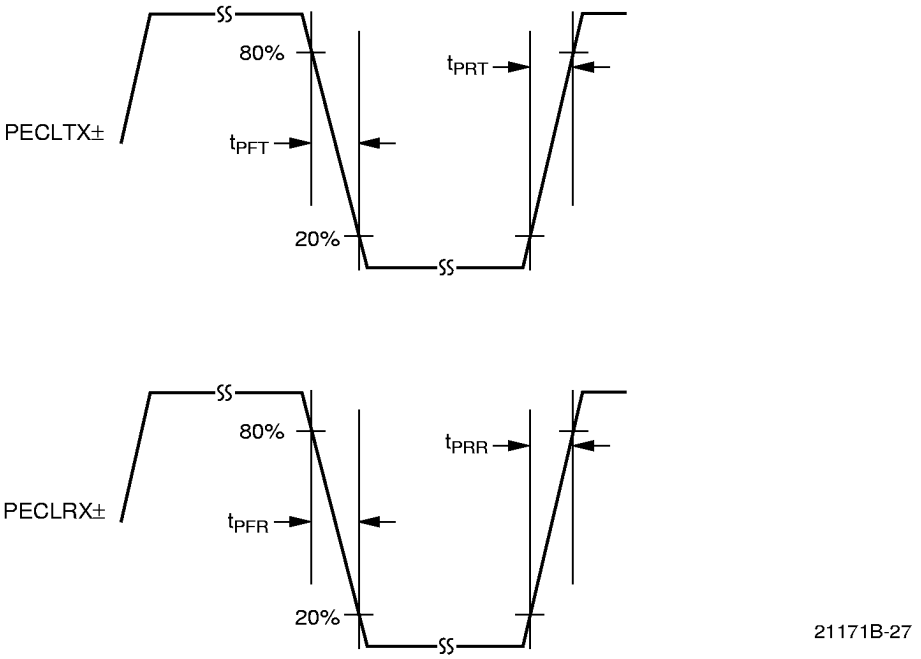



**Figure 25. PECL Rise and Fall Times**

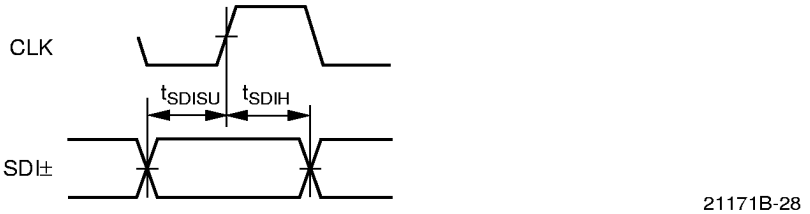



**Figure 26. SDI± Input Parameters**

## System Timing Information

The following section gives timing information useful for assessing the system's operation as a Class I repeater or a Class II repeater.

***Note:*** *$\overline{REQ}$, $\overline{ACT}$, and $\overline{COL}$ are not synchronized to ECLK; therefore, no phase relationship is implied. Also, no phase relationship is implied between ECLK and RXD or ECLK and TXD.*

### Start of Packet Timing

| Symbol | Parameter Description | Min | Max | Unit |
|---|---|---|---|---|
| $t_{SOPJR}$ | First J Bit received by a TX Port to leading edge of $\overline{REQ}$ | 90 | 142 | ns |
| $t_{SOPRA}$ | Allowed Delay of $\overline{ACT}$ after $\overline{REQ}$ (Note 1) | – | ΔE | ns |
| $t_{SOPRD}$ | $\overline{REQ}$ TRUE to DAT Valid and EBDIR LOW (Note 1) | 20 + ΔE | 30 + ΔE | ns |
| $t_{SOPRE}$ | $\overline{REQ}$ TRUE to First Falling Edge of ECLK (Notes 1, 2, and 3) | 60 + ΔE | 70 + ΔE | ns |
| $t_{SOPETX}$ | First Falling Edge of ECLK to First J Bit Transmitted by a TX Port (Notes 1, 2, and 3) | 160 | 200 | ns |

***Notes:***

1. *ΔE refers to the anticipated arbiter delay in bit times. ΔE can have one of two values: 40 or 80. The value of ΔE is based on the setting of the EXP_DEL pin. If EXP_DEL is LOW, ΔE is equal to 40. If EXP_DEL is HIGH, ΔE is equal to 80.*
2. *ECLK becomes active in the LOW state. Because ECLK should be tied LOW via an external resistor, this will not be seen o monitoring equipment.*
3. *DAT[4:0] is latched on the rising edge of ECLK. However, it is shifted into the synchronizer on the falling edge of ECLK. Thus, delays should be measured from the falling edge of ECLK.*

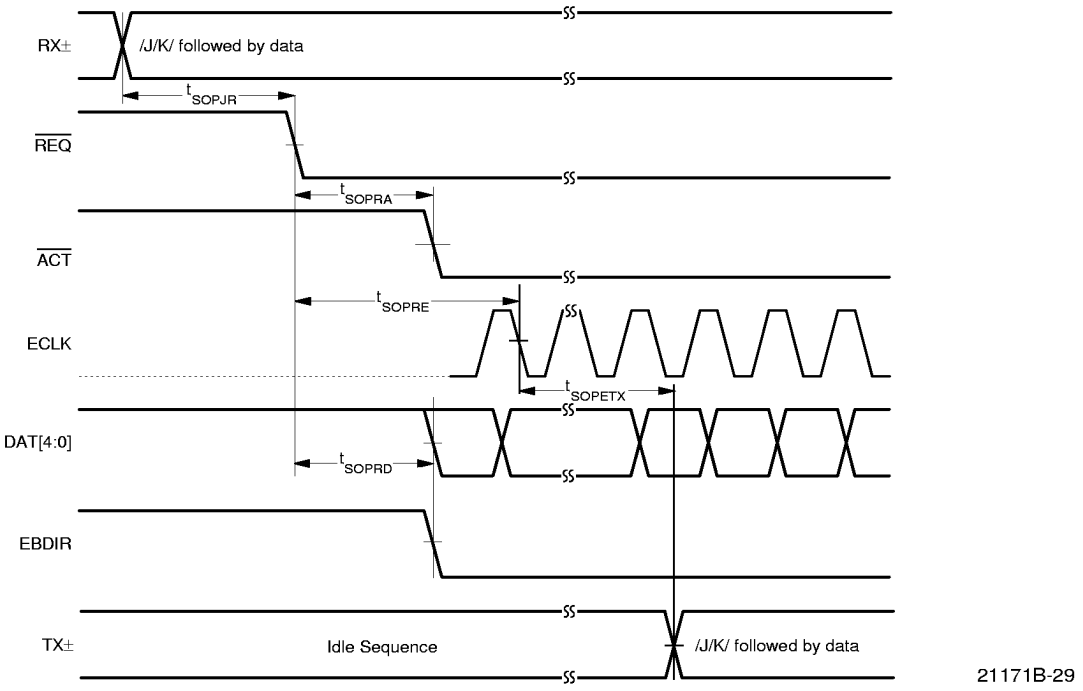



**Figure 27. Start of Packet**

## System Timing Information (Continued)

### Collision Timing - Single Chip Collisions (Note 1)

| Symbol | Parameter Description | Min | Max | Unit |
|---|---|---|---|---|
| $t_{SOJRD}$ | $\overline{REQ}$ Valid to JAM Signal on DAT[4:0] (Notes 2 & 3) | ΔE | 60 + ΔE | ns |
| $t_{SOJRE}$ | $\overline{REQ}$ Valid to First Falling Edge of ECLK | 20 + ΔE | 100 + ΔE | ns |
| $t_{SOJETX}$ | First Falling Edge of ECLK to JAM on all TX ports | 80 | 160 | ns |
| $t_{SOJJD}$ | First Bit of J on RX to JAM on DAT[4:0] (Note 4) | 90 | 170 | ns |
| $t_{SOJE}$ | First Bit of J on RX to First Falling Edge of ECLK after JAM on DAT[4:0] (Note 4) | 130 | 210 | ns |
| $t_{EOJOPL}$ | Only 1 Port Receiving to the First Bit of T Transmitting on that Port (One Port Left) | 290 | 402 | ns |
| $t_{EOJTR}$ | First Bit of T to $\overline{REQ}$ HIGH | 170 | 262 | ns |
| $t_{EOJTD}$ | First Bit of T to Idle on DAT[4:0] | 130 | 222 | ns |
| $t_{EOJTE}$ | First Bit of T on RX to First Falling Edge of ECLK after Idle on DAT[4:0] | 170 | 262 | ns |
| $t_{EOJET}$ | Falling Edge of ECLK after Idle on DAT[4:0] to First Bit of T on all TX Ports | 120 | 160 | ns |

***Notes:***

1. *Collision Timing when the active ports are on the same IMR100 device.*
2. *ΔE refers to the anticipated arbiter delay in bit times. ΔE can have one of two values: 40 or 80. The value of ΔE is based on the setting of the EXP_DEL pin. If EXP_DEL is LOW, ΔE is equal to 40. If EXP_DEL is HIGH, ΔE is equal to 80.*
3. *Collision results from multiple ports on the same IMR100 device simultaneously receiving the first bit of J.*
4. *Collision results from one or more ports on the same IMR100 device becoming active after another port on that IMR100 device has already been active.*

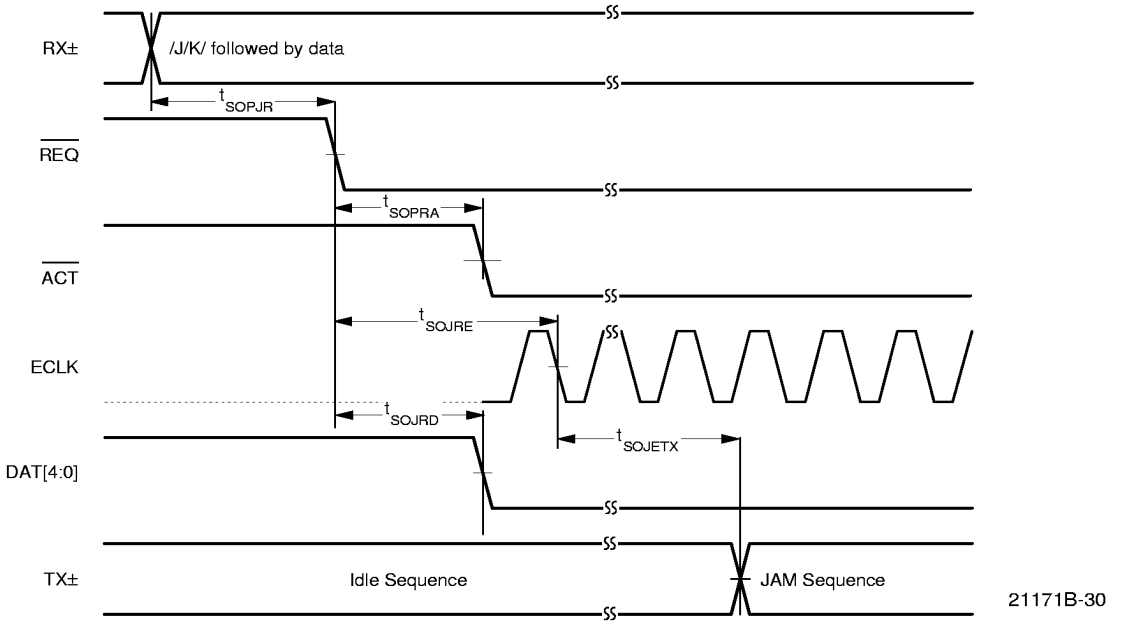



**Figure 28. Single Device Start of Jam - Both Ports Start Simultaneously**

## System Timing Information (Continued)

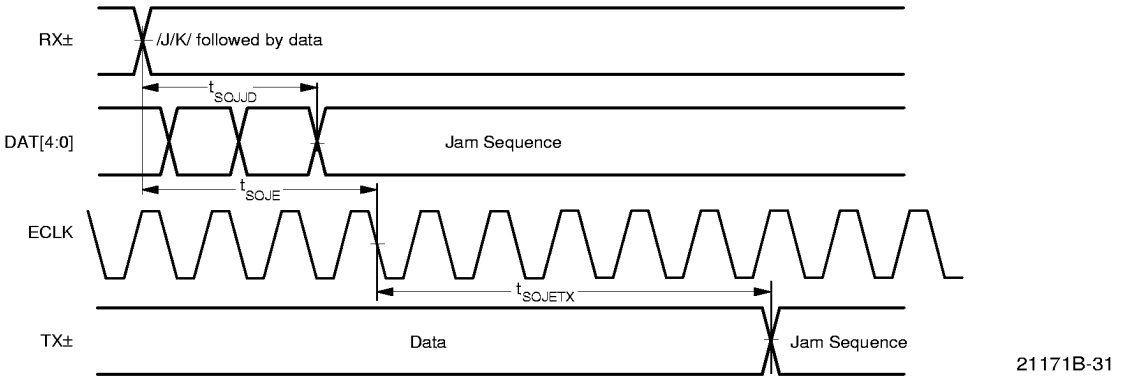



**Figure 29. Single Device Start of JAM - One Port Starts after Arbitration**

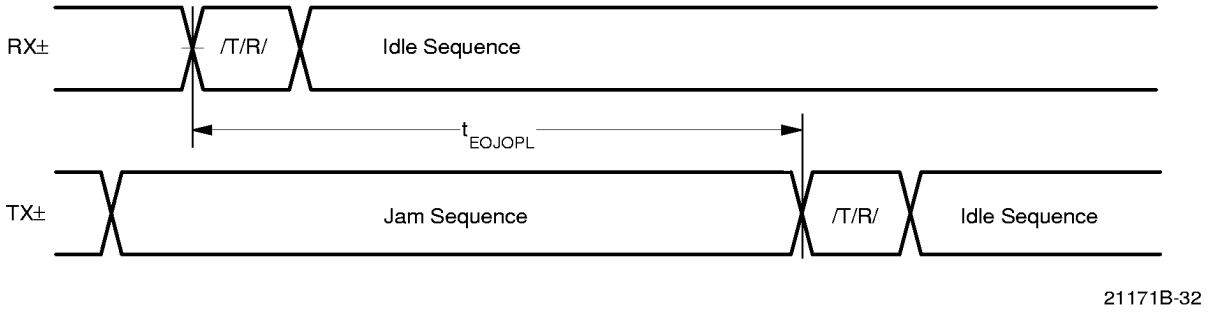



**Figure 30. Single Device - One Port Left**

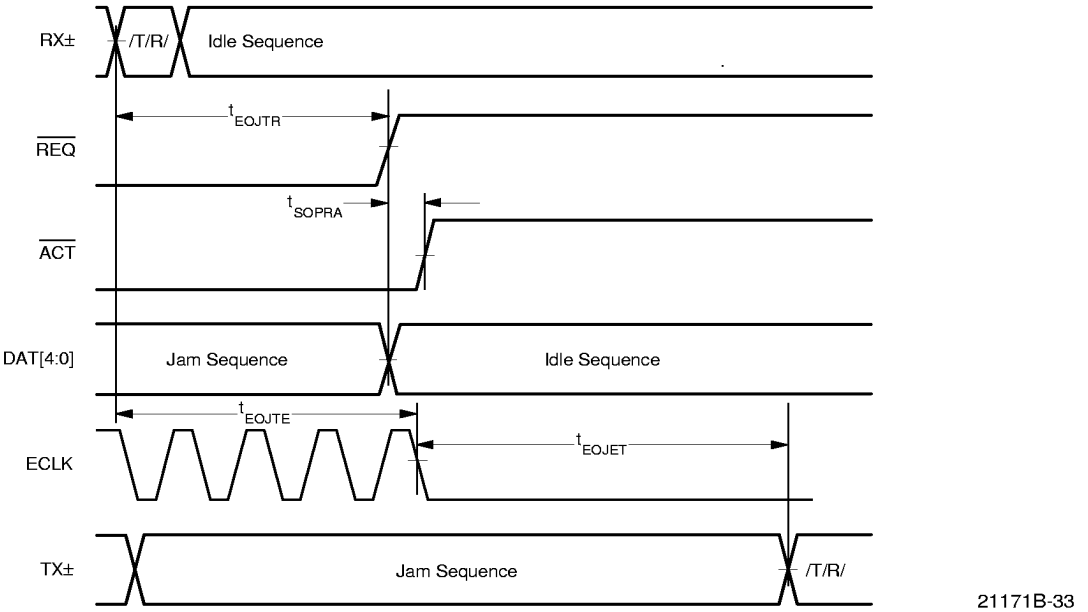



**Figure 31. Single Device - End of Jam**

## System Timing Information (Continued)

### Collision Timing - Multiple Chip Collisions (Note 1)

| Symbol | Parameter Description | Min | Max | Unit |
|---|---|---|---|---|
| $t_{SOJRC}$ | Required Assertion of $\overline{COL}$ After $\overline{REQ}$ Asserted | – | ΔE | ns |
| $t_{SOJCJ}$ | $\overline{COL}$ to JAM Transmitted on all Ports | 140 | 180 | ns |
| $t_{SOJCD}$ | $\overline{COL}$ Asserted to DAT[4:0], ECLK, and EBDIR Asserted | – | 20 | ns |
| $t_{EOJTR}$ | First T on RX to $\overline{REQ}$ Deasserted | 130 | 182 | ns |
| $t_{EOJRC}$ | Required Deassertion of $\overline{COL}$ after $\overline{REQ}$ Deasserts | – | ΔE | ns |
| $t_{EOJCTX}$ | $\overline{COL}$ Deasserted to First Bit of T Transmitted on all Ports | 140 | 180 | ns |

***Note:***

*1. Collision results from signals received on different IMR100 devices that are connected together via the Expansion Port.*

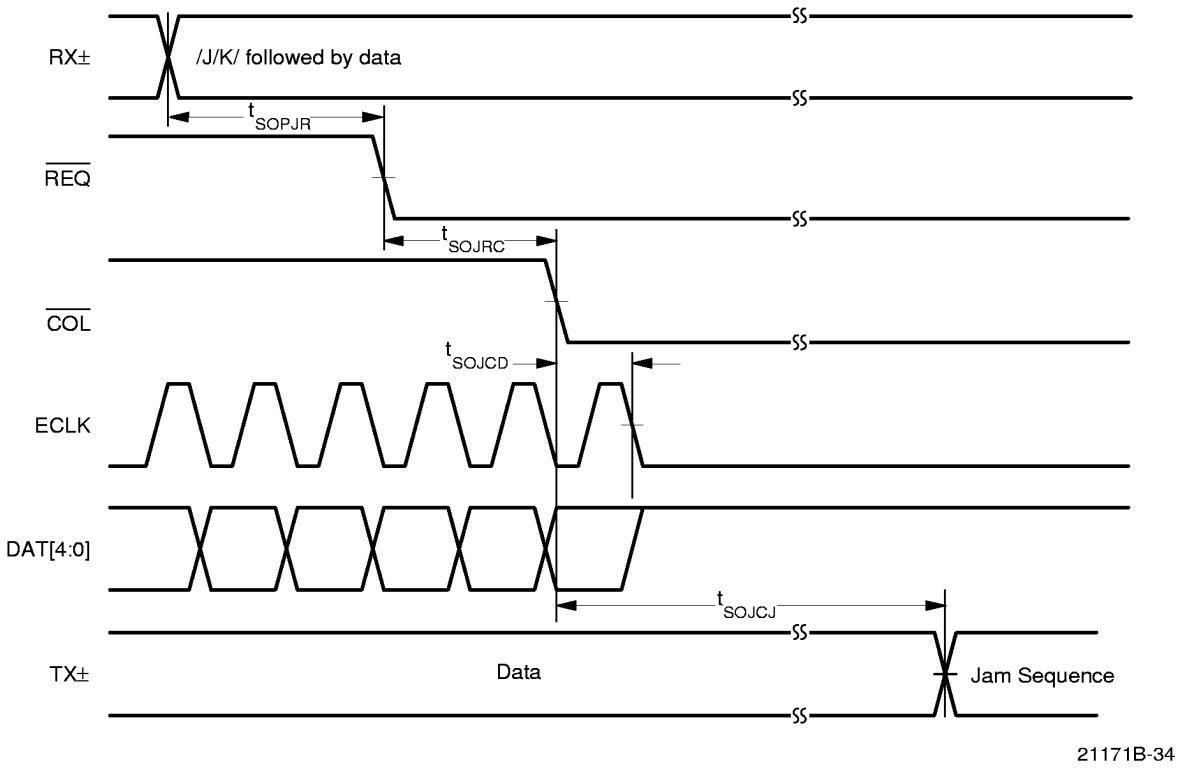



**Figure 32. Start of JAM - Multiple Devices**

## System Timing Information (Concluded)

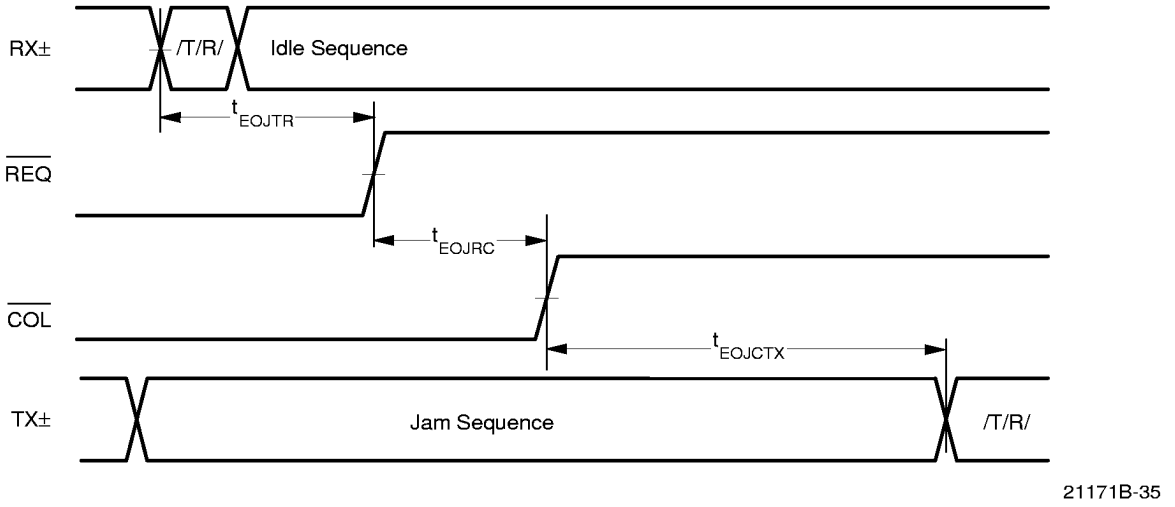
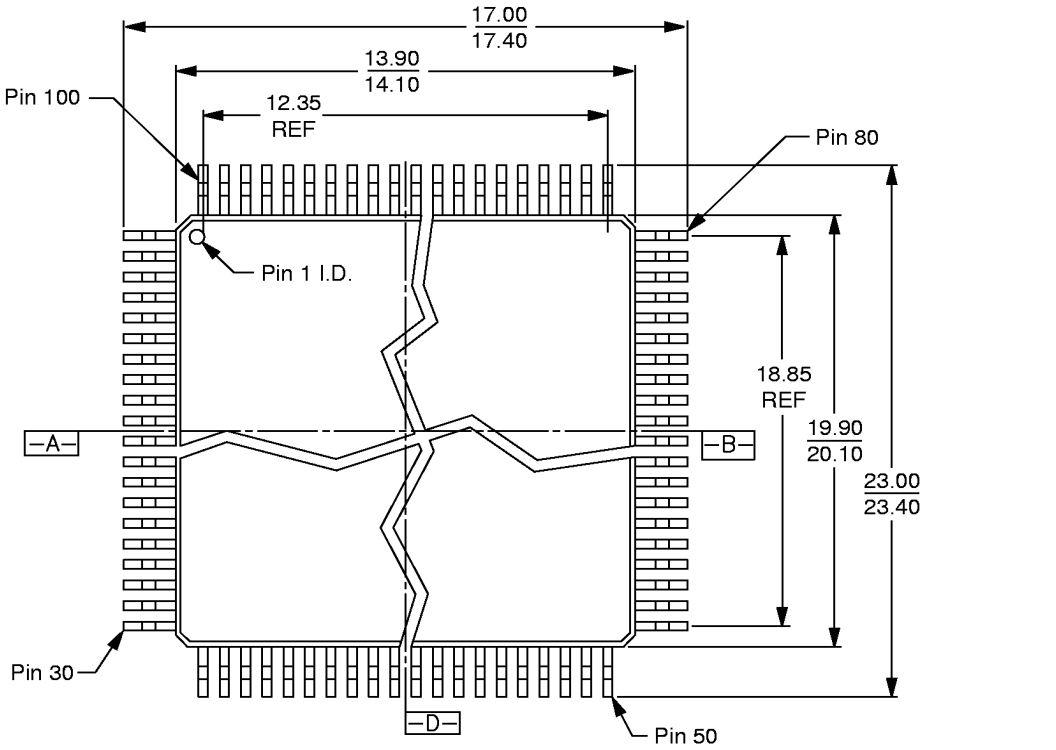


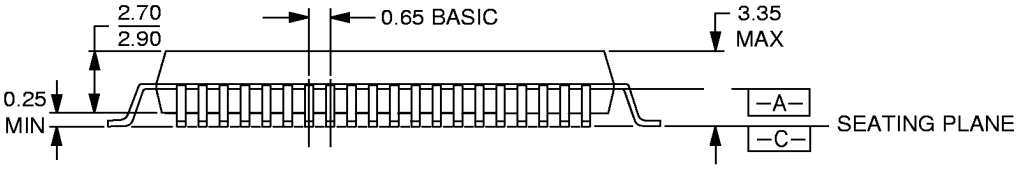

**Figure 33. End of Jam - Multiple Devices**

## PHYSICAL DIMENSIONS

## PQR100

**Plastic Quad Flat Pack (measured in millimeters)**

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DP92
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