PRELIMINARY

Am79C980

Integrated Multiport Repeater (IMR)

Advanced Micro Devices

DISTINCTIVE CHARACTERISTICS

- CMOS device features high integration and low power with a single +5 V supply
- Repeater functions conform to IEEE 802.3 Repeater Unit specifications
- Eight integral 10BASE-T transceivers utilize the required pre-distortion transmission technique
- Attachment Unit Interface (AUI) port allows connectivity with 10BASE5 (Ethernet) and 10BASE2 (Cheapernet) networks, as well as Fiber Optic Inter-repeater Link (FOIRL) segments
- On board PLL, Manchester encoder/decoder, and FIFO
- Expandable to increase number of repeater ports
- All ports can be separately isolated (partitioned) in response to excessive collision conditions or fault conditions
- Network management and optional features are accessible through a dedicated serial management port
- Twisted Pair Link Test capability conforming to the 10BASE-T standard. The receive Link Test Function can be optionally disabled through the management port to facilitate interoperability with devices that do not implement the Link Test Function
- Programmable option of Automatic Polarity Detection and Correction permits automatic recovery due to wiring errors
- Full amplitude and timing regeneration for re-transmitted waveforms
- Preamble loss effects eliminated by deep FIFO

GENERAL DESCRIPTION

The Integrated Multiport Repeater (IMR) is a VLSI circuit that provides a system level solution to designing a compliant 802.3 repeater incorporating 10BASE-T transceivers. The device integrates the Repeater functions specified by section 9 of the IEEE 802.3 standard and Twisted Pair Transceiver functions conforming to the 10BASE-T standard. The Am79C980 provides eight integral Twisted Pair Medium Attachment Units (MAUs) and an Attachment Unit Interface (AUI) port in an 84-pin Plastic Leaded Chip Carrier (PLCC).

A network based on the 10BASE-T standard uses unshielded twisted pair cables, therefore providing an economical solution to networking by allowing the use of existing telephone wiring.

The total number of ports per repeater unit can be increased by connecting multiple IMR devices through their expansion ports, hence minimizing the total cost per repeater port. Furthermore, a general purpose Attachment Unit Interface (AUI) provides connection capability to 10BASE-5 (Ethernet) and 10BASE-2 (Cheapernet) networks, as well as Fiber Optic Inter-repeater Link (FOIRL) segments. Network management and test functions are provided through TTL compatible I/O pins.

The device is fabricated in CMOS technology and requires a single +5 V supply.

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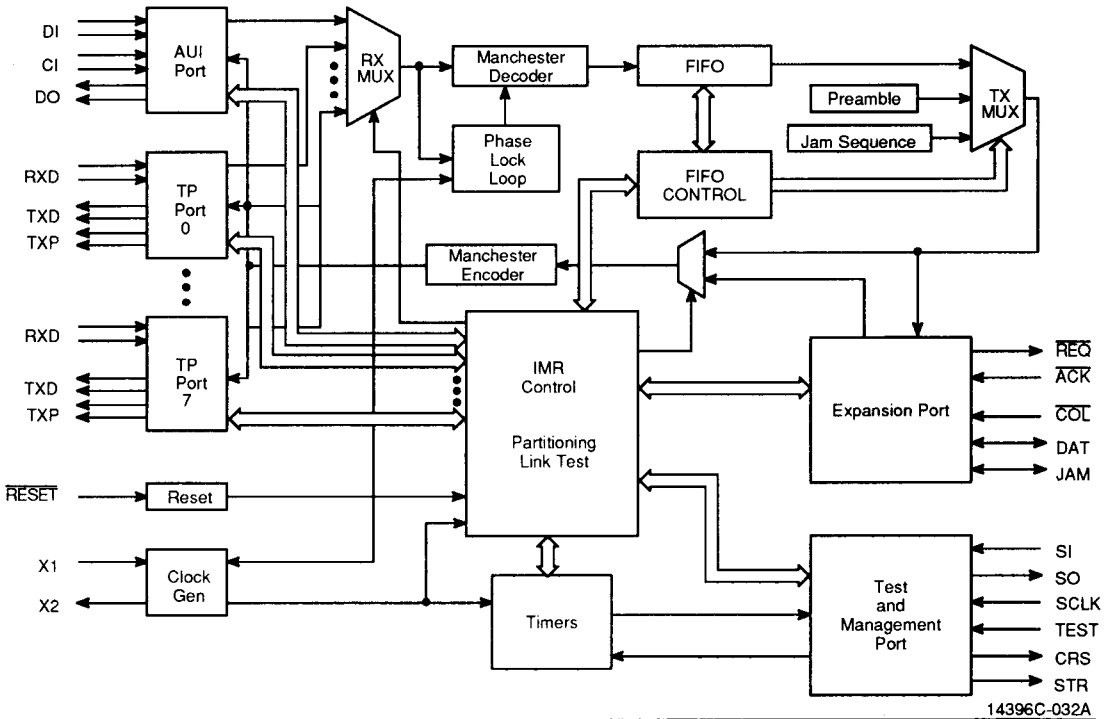
BLOCK DIAGRAM

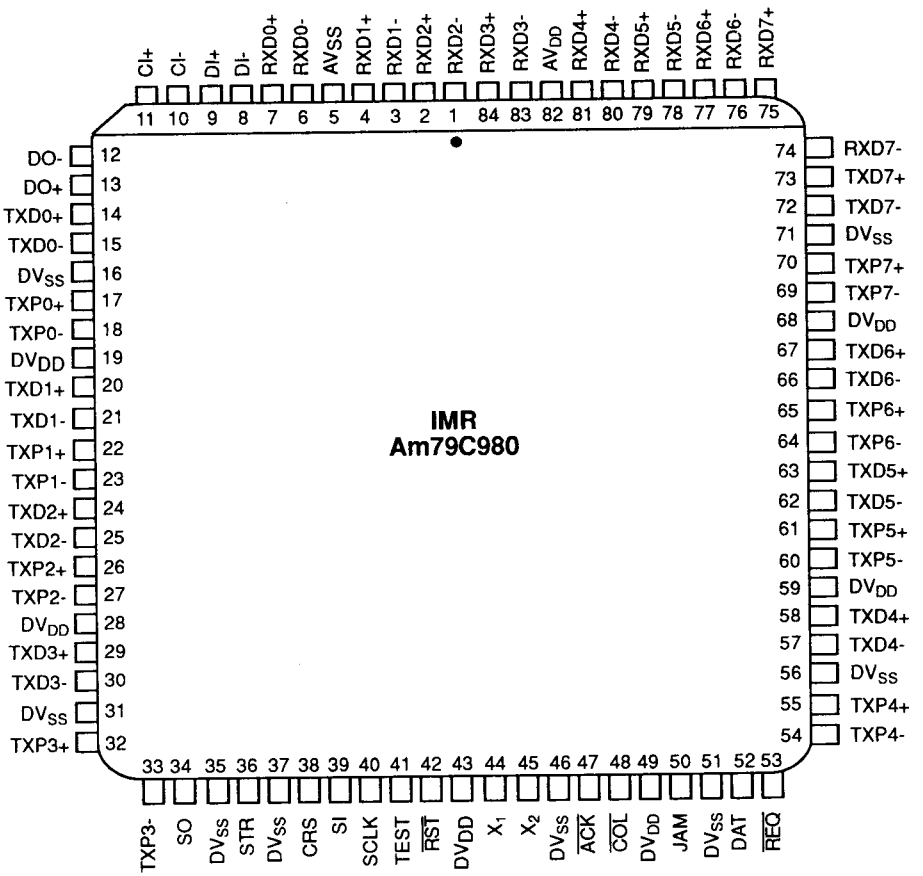


RELATED AMD PRODUCTS

Part No.	Description
Am79C900	32-Bit Integrated Local Area Communications Controller (ILACC)
Am7990	Local Area Network Controller for Ethernet (LANCE)
Am7992B	Serial Interface Adapter (SIA)
Am79C98	Twisted Pair Ethernet Transceiver (TPEX)
Am7996	IEEE 802.3/Ethernet/Cheapernet Transceiver
Am7997	IEEE 802.3 Compliant Tap Transceiver

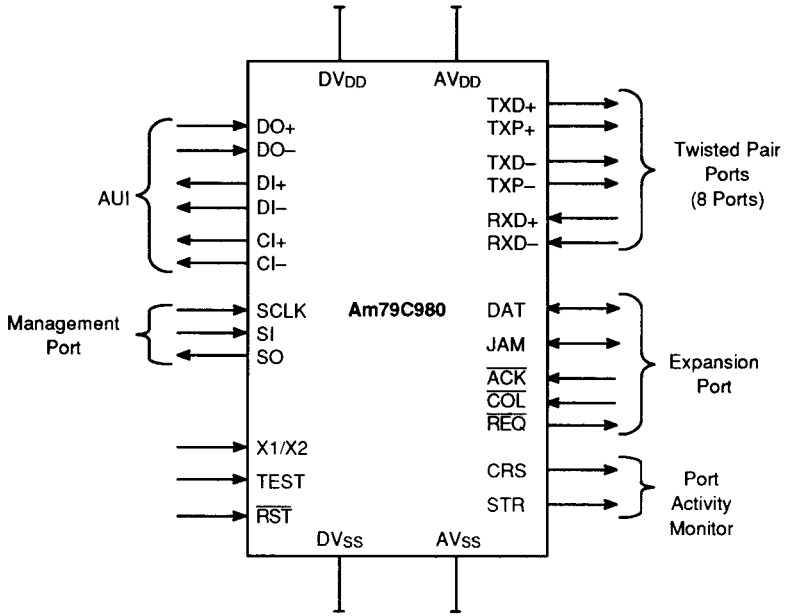
CONNECTION DIAGRAM

PLCC



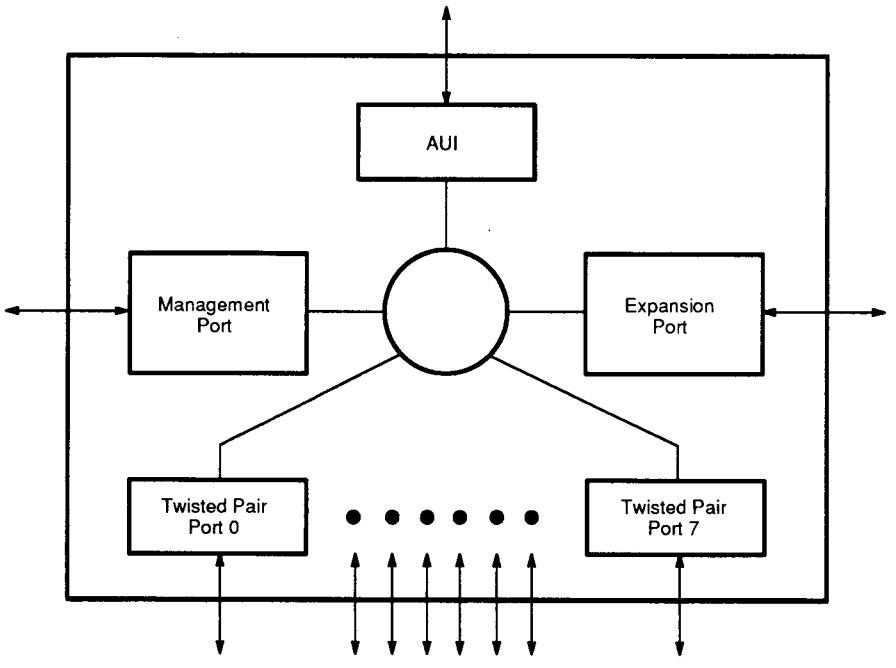
14396C-001B

LOGIC SYMBOL



14396C-035A

LOGIC DIAGRAM

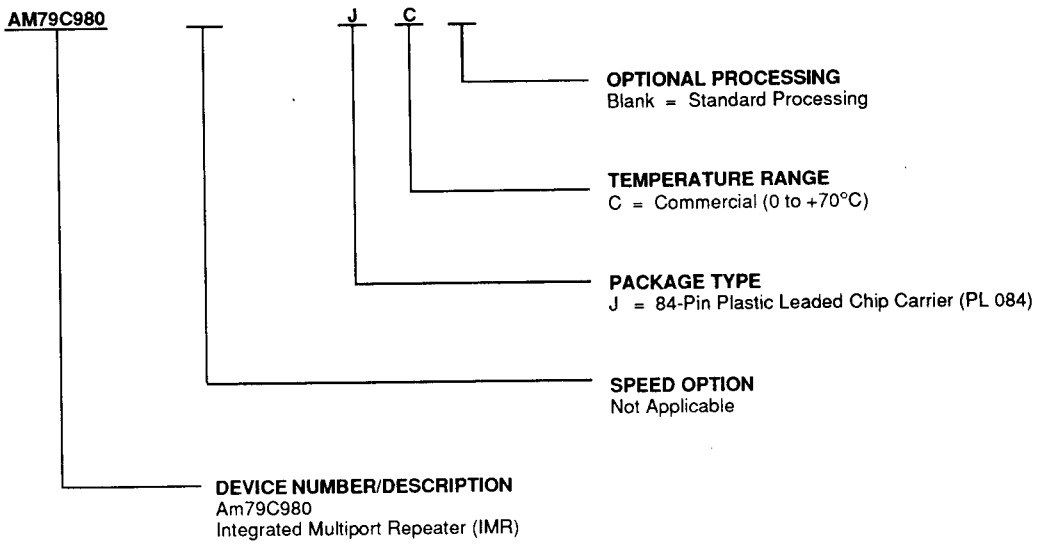


14396-002A

ORDERING INFORMATION

Standard Products

AMD standard products are available in several packages and operating ranges. The order number (Valid Combination) is formed by a combination of:



Valid Combinations	
AM79C980	JC

Valid Combinations

Valid Combinations list configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations or to check on newly released combinations, and to obtain additional data on AMD's standard military grade products.

PIN DESCRIPTION

$\overline{ACK}$

Acknowledge

Input, Active LOW

When this input is asserted, it signals to the requesting IMR that it may control the DAT and JAM pins. If the IMR is not requesting control of the DAT line ($\overline{REQ}$ pin HIGH), then the assertion of the $\overline{ACK}$ signal indicates the presence of valid collision status on the JAM or valid data on the DAT line.

AV_{DD}

Analog Power

Power Pin

These pins supply the +5 V to the RXD+/- receivers, the DI+/- and CI+/- receivers, the DO+/- drivers, the internal PLL, and the internal voltage reference of the IMR. These power pins should be decoupled with a 47 µF capacitor and kept separate from other power and ground planes.

AV_{SS}

Analog Ground

Ground Pin

These pins are the 0 V reference for AV_{DD}.

$\overline{COL}$

Expansion Collision

Input, Active LOW

When this input is asserted by an external arbiter, it signifies that more than one IMR is active and that each IMR should generate Collision Jam Sequence independently.

CI+, CI-

Control In

Input

AUI port differential receiver.

CRS

Carrier Sense

Output

The states of the internal carrier sense signals for the AUI port and the eight twisted pair ports is serially output on this pin continuously. The output serial bit stream is synchronized to the X_1 clock.

DAT

Data

Input/Output

When there is a single IMR active (in a multiple IMR design), the IMR with both $\overline{REQ}$ and $\overline{ACK}$ pins asserted drives the DAT line with NRZ data. The pin is an input when only the $\overline{ACK}$ signal is asserted, and is in a high impedance state if neither $\overline{REQ}$ or $\overline{ACK}$ is asserted.

DI+, DI-

Data In

Input

AUI port differential receiver.

DO+, DO-

Data Out

Output

AUI port differential driver.

DV_{DD}

Digital Power

Power Pin

These pins supply the +5 V to the logic portions of the IMR and the TXP+/-, TXD+/-, and DO+/- line drivers.

DV_{SS}

Digital Ground

Ground Pin

These pins are the 0 V reference for DV_{DD}.

DV_{DD} Pin #	DV_{SS} Pin #	Function
19	16	TP ports 0 & 1 drivers
28	31	TP ports 2 & 3 drivers
43, 49	35, 37, 46, 51	Core logic and expansion and control pins
59	56	TP ports 4 & 5 drivers
68	71	TP ports 6 & 7 drivers

JAM

Jam

Input/Output

This pin is an output on the single active IMR ($\overline{REQ}$ and $\overline{ACK}$ both asserted). The active IMR drives the JAM pin HIGH to indicate that it is in a Collision state. The pin is an input when only the $\overline{ACK}$ signal is asserted, and is in a high impedance state if neither $\overline{REQ}$ or $\overline{ACK}$ is asserted.

$\overline{REQ}$

Request

Output, Active LOW

This pin is driven LOW when the IMR is active. An active IMR is defined as an IMR which has one or more ports receiving or colliding or is in the state where it is still transmitting data from the internal FIFO. The assertion of this signal signifies that the IMR is requesting the use of the DAT and JAM lines for the transfer of repeated data or collision status to other IMRs.

$\overline{RST}$

Reset

Input, Active LOW

Driving this pin LOW resets the internal logic of the IMR. Reset should be synchronized to X_1 clock if either expansion or port activity monitor is used.

$RXD+_{0-7}$, $RXD-_{0-7}$

Receive Data

Input

10BASE-T port differential receive inputs (8 ports).

SCLK

Serial Clock

Input

Serial data (input or output) is clocked (in or out) on the rising edge of the signal on this pin.

SI

Serial In

Input

Test/Management serial input port. Management commands are clocked in on this pin synchronous to the SCLK input.

SO

Serial Out

Output

Test/Management serial output port. Management results are clocked out on this pin synchronous to the SCLK input.

STR

Store

Output

This pin goes HIGH for two X_1 clock cycle times after the nine carrier sense bits are output on the CRS pin. Note that the carrier sense signals arriving from each port are latched internally, so that an active transition is remembered between samples. The accuracy of the carrier sense signals produced in this manner is 10 bit times (one microsecond).

TEST

Test Pin

Input, Active HIGH

This pin should be tied LOW for normal operation. If this pin is driven HIGH, then the IMR can be programmed for Loopback Test Mode.

$TXD+_{0-7}$, $TXD-_{0-7}$

Transmit Data

Output

10BASE-T port differential drivers (8 ports).

$TXP+_{0-7}$, $TXP-_{0-7}$

Transmit Pre-distort

Output

10BASE-T transmit waveform pre-distortion control differential outputs (8 ports).

X_1

Crystal 1

Crystal Connection

The internal clock generator uses a 20 MHz crystal attached to pins X_1 and X_2. Alternatively, an external 20 MHz CMOS clock signal can be used to drive this pin.

X_2

Crystal 2

Crystal Connection

The internal clock generator uses a 20 MHz crystal attached to pins X_1 and X_2. If an external clock source is used, this pin should be left unconnected.

FUNCTIONAL DESCRIPTION

The Am79C980 Integrated Multiport Repeater is a single chip implementation of an IEEE 802.3/Ethernet repeater or hub. In addition to the eight integral 10BASE-T ports plus one AUI port comprising the basic repeater, the IMR also provides the hooks necessary for complex network management and evaluation. The IMR is also expandable, enabling the implementation of repeaters based on several IMRs.

The IMR complies with the full set of repeater basic functions as defined in section 9 of ISO 8802.3 (ANSI/IEEE 802.3c). These functions are summarized below.

Repeater Function

If any single network port senses the start of a valid packet on its receive lines, then the IMR will re-transmit the received data to all other enabled network ports. The repeated data will also be presented on the DAT line to facilitate multiple-IMR repeater applications.

Signal Regeneration

When re-transmitting a packet, the IMR ensures that the outgoing packet complies to the 802.3 specification in terms of preamble structure, voltage amplitude, and timing characteristics. Specifically, data packets repeated by the IMR will contain a minimum of 56 preamble bits before the Start of Frame Delimiter. In addition, the voltage amplitude of the repeated packet waveform will be restored to levels specified in the 802.3 spec. Finally, signal symmetry is restored to data packets repeated by the IMR, removing jitter and distortion caused by the network cabling.

Jabber Lockup Protection

The IMR implements a built-in jabber protection scheme to ensure that the network is not disabled due to transmission of excessively long data packets. This protection scheme will automatically interrupt the transmitter circuits of the IMR for 96 bit times if the IMR has been transmitting continuously for more than 65,536 bit times.

Collision Handling

The IMR will detect and respond to collision conditions as specified in 802.3. A multiple-IMR repeater implementation also conforms to the 802.3 spec due to the inter-IMR status communication provided by the expansion port of the IMR. Specifically, a repeater based on one or more IMRs will handle the transmit collision and one-port-left collision conditions correctly as specified in section 9 of the 802.3 spec.

Fragment Extension

If the total packet length received by the IMR is less than 96 bits, including preamble, the IMR will extend the repeated packet length to 96 bits by appending a Jam sequence to the original runt packet.

Auto Partitioning/Reconnection

Any of the integral TP ports and AUI port can be partitioned under excessive duration or frequency of collision conditions. Once partitioned, the IMR will continue to transmit data packets to a partitioned port, but will not respond (as a repeater) to activity on the partitioned port's receiver. The IMR will monitor the port and reconnect it once certain criteria indicating port 'wellness' are met. The criteria for reconnection are specified by the 802.3 standard. In addition to the standard reconnection algorithm, the IMR implements an alternative reconnection algorithm which provides a more robust partitioning function for the TP ports and/or the AUI port. Each TP port and the AUI port are partitioned and/or reconnected separately and independently of other network ports.

Either one of the following conditions occuring on any enabled IMR network port will cause the IMR to partition that port:

a. A collision condition exists continuously for a time between 1024 and 2048 bit times (AUI port – SQE signal active; TP port – simultaneous transmit and receive)

b. A collision condition occurs during each of 32 consecutive attempts to transmit to that port.

Once a network port is partitioned, the IMR will reconnect that port if the following is met:

a. (Standard reconnection algorithm) A data packet longer than 488 bit times (nominal) is transmitted or received by the partitioned port without a collision

b. (Alternate reconnection algorithm) A data packet longer than 488 bit times (nominal) is transmitted by the partitioned port without a collision

The reconnection algorithm option (standard or alternate) is a global function for the TP ports, i.e. all TP ports use the same reconnection algorithm. The AUI reconnection algorithm option is programmed independently of the TP port reconnection option.

Link Test

The integral TP ports implement the Link Test function as specified in the 802.3 10BASE-T standard. The IMR will transmit Link Test pulses to any TP port after that port's transmitter has been inactive for more than 16 milliseconds (nominal). Conversely, if a TP port does not receive any data packets or Link Test pulses for more than 50 to 150 milliseconds and the Link Test function is enabled for that port then that port will enter link fail state. A port in link fail state will be disabled by the IMR (repeater transmit and receive functions disabled) until it receives either four consecutive Link Test pulses or a data packet. The Link Test receive function itself can be disabled via the IMR management port on a port-by-port basis to allow the IMR to interoperate with pre-10BASE-T twisted pair networks that do not implement the Link Test function. This interoperability is possible because the IMR will not allow the TP port to enter link fail state, even if no Link Test pulses or data packets are being received. Note however that the IMR will always transmit Link Test pulses to all TP ports regardless of whether or not the port is enabled, partitioned, in link fail state, or has its Link Test receive function disabled.

Polarity Reversal

The TP ports have the optional (programmable) ability to invert (correct) the polarity of the received data if the TP port senses that the received data packet waveform polarity is reversed due to a wiring error. This receive circuitry polarity correction allows subsequent packets to be repeated with correct polarity. This function is executed once following reset or link fail, and has a programmable enable/disable option on a port-by-port basis. This function is disabled upon reset and can be enabled via the IMR Management Port.

Reset

The IMR enters reset state when the $\overline{\text{RESET}}$ pin is driven LOW. The RESET pin should be held LOW for a minimum of 150 µs (3000 X1 clock cycles). This allows the IMR to reset the internal logic and permits the internal PLL to stabilize. During reset, the output signals are placed in their inactive states. That is, all analog signals are placed in their idle states, all bidirectional signals are not driven, active LOW signals are driven HIGH, and all active HIGH signals are driven LOW.

In a multiple IMR repeater the $\overline{\text{RESET}}$ signal should be applied simultaneously to all IMRs and should be synchronized to the external X_1 CLOCK. Reset synchronization is also required when accessing PAM (Port Activity Monitor).

SI should be held HIGH for at least 500 ns following the rising edge of $\overline{\text{RST}}$.

The following table summarizes the state of the IMR following reset.

Table 1. IMR after Reset

Function	State after Reset
Active LOW outputs	HIGH
Active HIGH outputs	LOW
SO Output	HIGH
Bidirectional Pins	HI-IMPEDANCE
Transmitters (TP and AUI)	IDLE
Receivers (TP and AUI)	ENABLED
AUI Partitioning/Reconnection Algorithm	STANDARD ALGORITHM
TP Port Partitioning/Reconnection Algorithm	STANDARD ALGORITHM
Link Test Function for TP Ports	ENABLED, TP PORTS IN LINK FAIL
Automatic Receiver Polarity Reversal Function	DISABLED

Expansion Port

The IMR Expansion Port is comprised of five pins; two are bi-directional signals (DAT and JAM), two are input signals ($\overline{\text{ACK}}$ and $\overline{\text{COL}}$), and one is an output signal ($\overline{\text{REQ}}$). These signals are used when a multiple-IMR repeater application is employed. In this configuration, all IMRs must be clocked synchronously with a common clock connected to the X1 inputs of all IMRs.

The IMR expansion scheme allows the use of multiple IMRs in a single board repeater or a modular multiport repeater with a backplane architecture. As many as three IMRs can be connected together without using external bus transceivers. The DAT pin is a bidirectional I/O pin which can be used with external bus transceivers to transfer data between the IMRs in a multiple-IMR design. The data sent over the DAT line is in NRZ format

and is synchronized to the common clock. The JAM pin is another bidirectional I/O pin that is used by the active IMR to communicate its internal status to the remaining (inactive) IMRs. When JAM is asserted HIGH, it indicates that the active IMR has detected a collision condition and is generating Jam Sequence. During this time when JAM is asserted HIGH, the DAT line is used to indicate whether the active IMR is detecting collision on one port only or on more than one port. When DAT is driven HIGH by the IMR (while JAM is asserted by the IMR), then the active IMR is detecting a collision condition on one port only. This 'one-port-left' signaling is necessary for a multiple-IMR repeater to function correctly as a single multiport repeater unit. The IMR also signals the 'one port left' collision condition in the event of a runt packet or collision fragment; this signal will continue for one expansion port bus cycle (100 nanoseconds) before deasserting $\overline{REQ}$.

The arbitration for access to the bussed bi-directional signals (DAT and JAM) is provided by one output ($\overline{REQ}$) and two inputs ($\overline{ACK}$ and $\overline{COL}$). The IMR asserts the $\overline{REQ}$ pin to indicate that it is active and wishes to drive the DAT and JAM pins. An external arbiter senses the $\overline{REQ}$ lines from all the IMRs and asserts the $\overline{ACK}$ line when one and only one IMR is asserting its $\overline{REQ}$ line. If more than one IMR is asserting its $\overline{REQ}$ line, the arbiter must assert the $\overline{COL}$ signal, indicating that more than one IMR is active. More than one active IMR at a time constitutes a collision condition, and all IMRs are notified of this occurence via the $\overline{COL}$ line of the Expansion Port.

Note that a transition from multiple IMRs arbitrating for the DAT and JAM pins (with $\overline{COL}$ asserted, $\overline{ACK}$ deasserted) to a condition when only one IMR is arbitrating for the DAT and JAM pins (with $\overline{ACK}$ asserted, $\overline{COL}$ deasserted) involves one expansion port bus cycle (100 nanoseconds). During this transitional bus cycle, $\overline{COL}$ is deasserted, $\overline{ACK}$ is asserted, and the DAT and JAM pins are not driven. However, each IMR will remain in the collision state (transmitting jam sequence) during this transitional bus cycle. In subsequent expansion port bus cycles ($\overline{REQ}$ and $\overline{ACK}$ still asserted), the IMRs will return to the 'master and slaves' condition where only one IMR is active (with collision) and is driving the DAT and JAM pins. An understanding of this sequence is crucial if non-IMR devices (such as an Ethernet controller) are connected to the expansion bus. Specifically, the last device to back off of the expansion bus after a multi-IMR collision must assert the JAM line until it too drops its request for the expansion bus.

External Arbiter

A simple arbitration scheme is required when multiple IMRs are connected together to increase the total number of repeater ports. The arbiter should have one input ($\overline{REQ1}$...$\overline{REQn}$) for each of the n IMRs to be used, and two global outputs ($\overline{COL}$ and $\overline{ACK}$). This function is easily implemented in a PAL® device, with the following logic equations:

$$\overline{ACK} = \overline{REQ1} \cdot \overline{REQ2} \cdot \overline{REQ3} \cdot \ldots \overline{REQn} + \overline{REQ1} \cdot REQ2 \cdot \overline{REQ3} \cdot \ldots \overline{REQn}$$

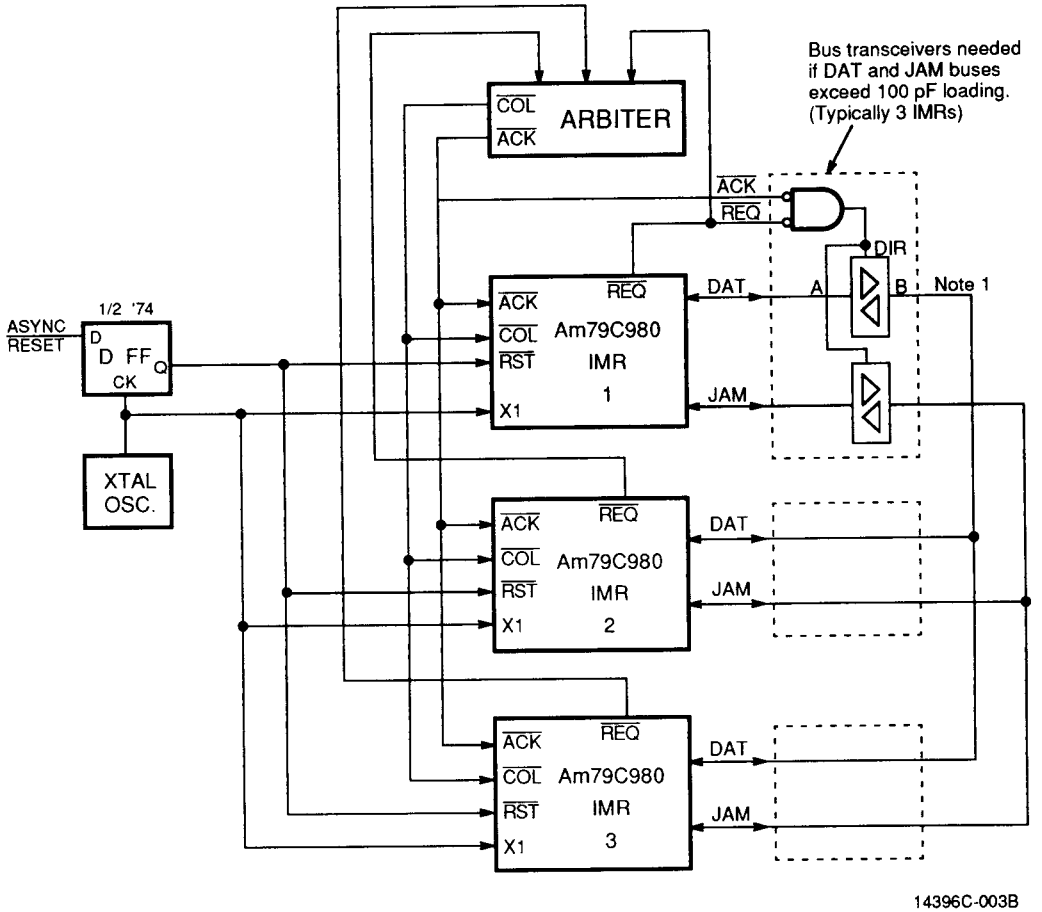
$$\vdots$$

$$+ \overline{REQ1} \cdot \overline{REQ2} \cdot \overline{REQ3} \cdot \ldots REQn$$

$$\overline{COL} = \overline{ACK} \cdot (REQ1 + REQ2 + REQ3 + \ldots REQn)$$

Above equations are in positive logic, i.e., a variable is true when asserted.

A single PALCE16V8 will perform the arbitration function for a repeater based on eight IMRs.



Note 1:

Direction	DIR
B → A	LOW
A → B	HIGH

Figure 1. Multiple IMRs

Modular Repeater Design

The expansion port of the IMR also allows for modular expansion. By sharing the arbitration duties between a backplane bus architecture and several separate repeater modules one can build an expandable repeater based on modular 'plug-in' cards. Each repeater module performs the local arbitration function for the IMRs on that module, and provides signals to the backplane for use by a global arbiter.

Figure 2 shows an expandable repeater based on 3 modules that each use 3 IMRs. In this design, each module provides 24 10BASE-T ports and requires a single PALCE16V8-15 to perform the local arbitration function. The backplane portion of the modular repeater consists only of the global arbiter, also a single PALCE16V8-15.

Local Arbiter Logic Equations (for n IMRs per module):

$$Rm = REQ1 * \overline{REQ2} * \overline{REQ3} * \ldots \overline{REQn}$$
$$+ \overline{REQ1} * REQ2 * \overline{REQ3} * \ldots \overline{REQn}$$
$$+ \overline{REQ1} * \overline{REQ2} * REQ3 * \ldots \overline{REQn}$$
$$\vdots$$
$$+ \overline{REQ1} * \overline{REQ2} * \overline{REQ3} * \ldots REQn$$

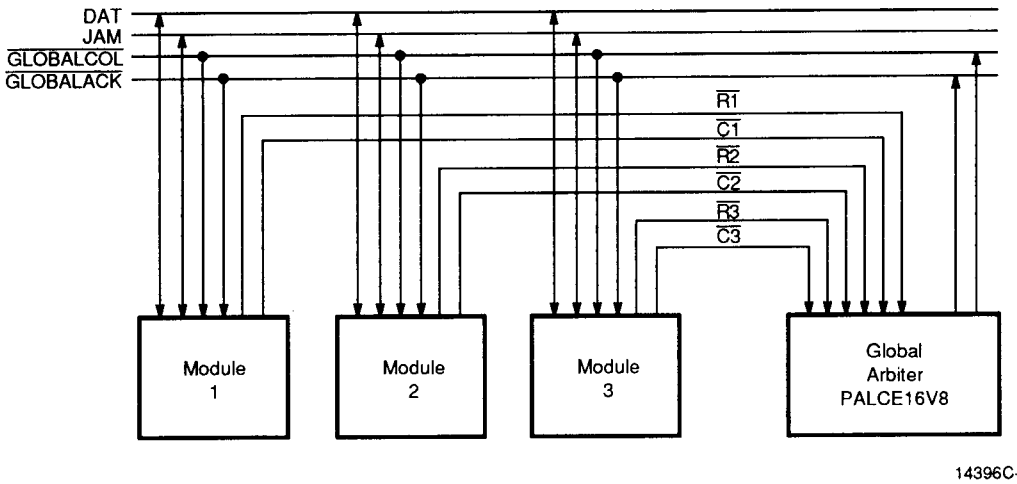
$$Cm = \overline{Rm} * (REQ1 + REQ2 + REQ3 + \ldots REQn)$$
$$DIR = Rm * GLOBALACK$$

The DIR signal is HIGH when the module drives the DAT and JAM backplane bus signals. A single PALCE16V8 can support up to 8 IMRs per module.

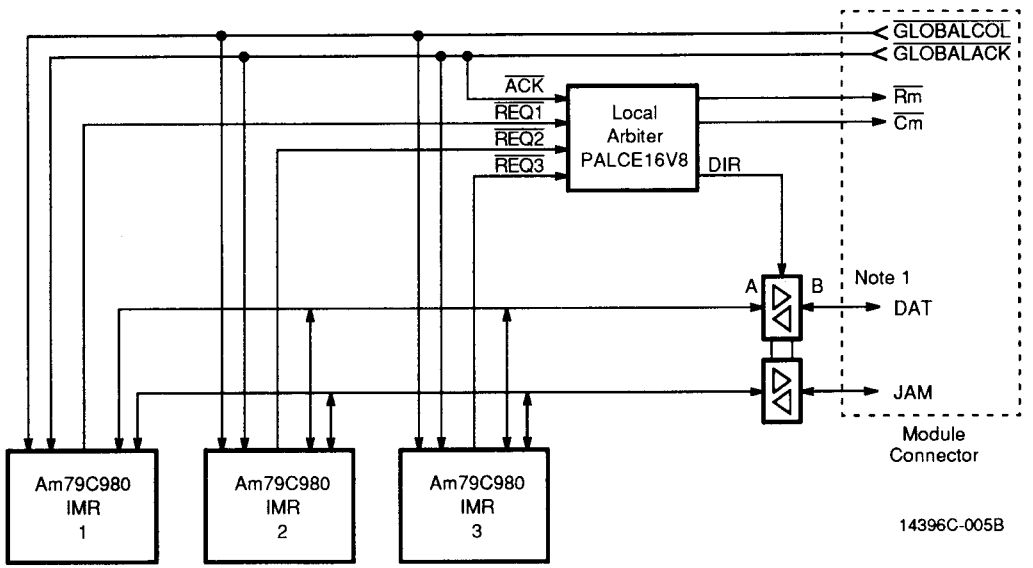
Global Arbiter Logic Equations (for m modules):

$$GLOBALACK$$
$$= \overline{C1} * \overline{C2} * \overline{C3} * \ldots \overline{Cm} * R1 * \overline{R2} * \overline{R3} * \ldots \overline{Rm}$$
$$+ \overline{C1} * \overline{C2} * \overline{C3} * \ldots \overline{Cm} * \overline{R1} * R2 * \overline{R3} * \ldots \overline{Rm}$$
$$+ \overline{C1} * \overline{C2} * \overline{C3} * \ldots \overline{Cm} * \overline{R1} * \overline{R2} * R3 * \ldots \overline{Rm}$$
$$\vdots$$
$$+ \overline{C1} * \overline{C2} * \overline{C3} * \ldots \overline{Cm} * \overline{R1} * \overline{R2} * \overline{R3} * \ldots Rm$$
$$GLOBALCOL = \overline{GLOBALACK} * (R1 + R2 + \ldots Rm)$$
$$+ (C1 + C2 + C3 + \ldots Cm)$$

A single PALCE22V10 can perform the global arbitration for up to 8 modules.



Modular Repeater



Repeater Module with 3 IMRs

Note 1:

Direction	DIR
B → A	LOW
A → B	HIGH

Figure 2. Expandable Modular Repeater

In-Band Hub Management

Because all repeated data in the IMR or multi-IMR design is available on the expansion port, all network traffic can be monitored by an external Media Access Controller (MAC) device such as the Am7990 or Am79C900. A repeater with such a controller is capable of providing extensive Hub Management functions, as well as being addressable as a network node. The MAC device can gather statistics and data concerning the state of the hub and the network, and the network addressability allows a remote Management Station to monitor this statistical data and to request actions to be performed by the repeater (i.e. port enable/disable).

Figure 3 shows how to interface a repeater based on two IMRs to an Ethernet controller such as the Am79C900 ILACC or the Am7990 LANCE.

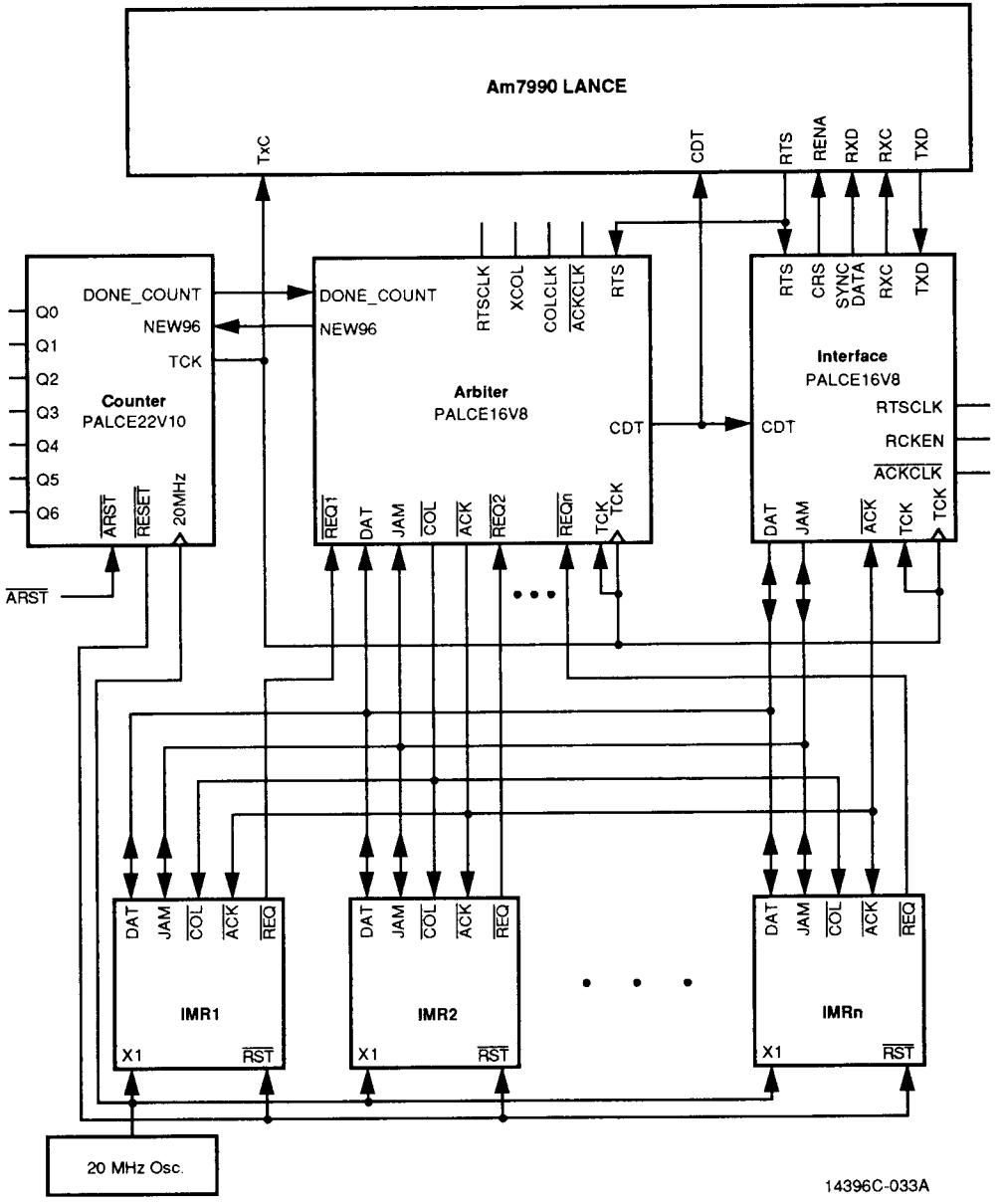


Figure 2. Expandable Modular Repeater

ARBITER LOGIC EQUATIONS

ACK = $\overline{REQ1} * \overline{REQ2} * ... \overline{REQn} * \overline{RTS}$ + $\overline{REQ1} * REQ2 * ... \overline{REQn} * \overline{RTS}$ + • + $\overline{REQ1} * \overline{REQ2} * ... REQn * \overline{RTS}$ + $\overline{REQ1} * \overline{REQ2} * ... \overline{REQn} * RTS$ + $\overline{REQ1} * \overline{REQ2} * ... \overline{REQn} * RTSCLK * ACKCLK * \overline{CDT}$	ACK is asserted when one and only one expansion bus request is active Term to extend ACK when MAC device finishes sourcing data onto expansion bus
ACKCLK := ACK	Clock delayed ACK signal (ACK*ACKCLK defines first clock period with valid DAT and JAM)
COL = $\overline{ACK} * (REQ1 + REQ2 + . . REQn + RTS)$	COL is asserted when more than one expansion bus request is active
COLCLK := COL	Clock delayed COL signal
CDT := COL + ACK * ACKCLK * JAM + COLCLK * ACK + $\overline{DONE\_COUNT} * CDT$	CDT causes the MAC device to back off/stay off the expansion bus Arbiter detects collision Single IMR collision Holds CDT active during 'dead' clock cycle Maintains CDT (suppresses new MAC requests) until 96 bit timeout
XCOL := ACK * ACKCLK * JAM * $\overline{DAT}$ + COL + COLCLK * ACK	Present transmit collision state Ongoing single IMR transmit collision Ongoing multiple IMR transmit collision Ongoing multiple IMR transmit collision ('dead' clock cycle)
RTSCLK := RTS	Clock delayed RTS signal (RTS*RTSCLK defines first recognized RTS from MAC)
NEW96 := ACK * $\overline{ACKCLK}$ * $\overline{CDT}$ + ACK * $\overline{ACKCLK}$ * JAM * $\overline{DAT}$ * $\overline{XCOL}$ + COL * $\overline{XCOL}$	Triggers or re–triggers counter (96 bit times) New repeater data (start of repeated packet, ACK∠ with no existing collision) (Trigger only) New transmit collision (Single IMR) New transmit collision (Multi-IMR)

INTERFACE LOGIC EQUATIONS

DAT.TRST = ACK * ACKCLK * RTSCLK	Enabled if MAC request gets arbiter ACK (delayed)
DAT = SYNCDATA * $\overline{CLK}$ + DAT * CLK + DAT * SYNCDATA + CDT	Synchronized and latched MAC data (if enabled) guarantees hold time for slave IMRs Overriding HIGH if collision exists (if enabled)
JAM.TRST = ACK * ACKCLK * RTSCLK	Enabled if MAC request gets arbiter ACK (delayed)
JAM = CDT	HIGH if collision exists
ACKCLK := ACK	Clock delayed ACK signal (ACK*ACKCLK defines first clock period with valid DAT and JAM)
CRS = ACK * ACKCLK * $\overline{JAM}$ * $\overline{CDT}$ + RCKEN	Single active IMR or MAC sourcing data Term to extend CRS at end of MAC receive
SYNCDATA := $\overline{RTS}$ * DAT * ACK * ACKCLK + TXD * RTS	Synchronized receive data for the MAC Synchronized TxD data for MAC transmit
RXC = RCKEN * $\overline{CLK}$	Inverted clock for synchronized data for MAC receive
RCKEN := ACK * ACKCLK * $\overline{RTS}$ * $\overline{RTSCLK}$ * $\overline{JAM}$ + ACK * RTS * $\overline{CDT}$	RCLK enabled if non–MAC data transfer (MAC is slave device) RCLK enabled on transmit to allow data loopback to MAC
RTSCLK := RTS	Clock delayed RTS signal (RTS*RTSCLK defines first recognized RTS from MAC)

COUNTER LOGIC EQUATIONS

Upon RESET, the counter is initialized to the terminal value of 60H (96), and remains there until triggered. If (re)triggered by NEW96, the counter is reset to 00H. The counter will count at 10 MHz until it reaches the terminal value, and will stop there until triggered.TCK and $\overline{RESET}$ are also generated here.

TCK := $\overline{TCK} * \overline{RESET} * \overline{ARST}$ — Generates TCK for MAC use

RESET := ARST — Synchronizes the async reset signal

Q0 := $\overline{Q0} * \overline{TCK} * \overline{DONE\_COUNT} * \overline{RESET} * \overline{NEW96}$ — Toggle if still counting LOW at reset, LOW when triggered by NEW96

+ Q0 * (TCK + DONE_COUNT) * $\overline{RESET} * \overline{NEW96}$ — Stop at terminal value

Q1 := $\overline{Q1} * Q0 * \overline{TCK} * \overline{DONE\_COUNT} * \overline{RESET} * \overline{NEW96}$ — LOW at reset, LOW when (re)triggered by NEW96

+ Q1 * ($\overline{Q0}$ + TCK + DONE_COUNT) * $\overline{RESET} * \overline{NEW96}$

Q2 := $\overline{Q2} * Q1 * Q0 * \overline{TCK} * \overline{DONE\_COUNT} * \overline{RESET} * \overline{NEW96}$ — LOW at reset, LOW when (re)triggered by NEW96

+ Q2 * ($\overline{Q1}$ + $\overline{Q0}$ + TCK + DONE_COUNT) * $\overline{RESET} * \overline{NEW96}$

Q3 := $\overline{Q3} * Q2 * Q1 * Q0 * \overline{TCK} * \overline{DONE\_COUNT} * \overline{RESET} * \overline{NEW96}$ — LOW at reset, LOW when (re)triggered by NEW96

+ Q3 * ($\overline{Q2}$ + $\overline{Q1}$ + $\overline{Q0}$ + TCK + DONE_COUNT) * $\overline{RESET} * \overline{NEW96}$

Q4 := $\overline{Q4} * Q3 * Q2 * Q1 * Q0 * \overline{TCK} * \overline{DONE\_COUNT} * \overline{RESET} * \overline{NEW96}$ — LOW at reset, LOW when (re)triggered by NEW96

+ Q4 * ($\overline{Q3}$ + $\overline{Q2}$ + $\overline{Q1}$ + $\overline{Q0}$ + TCK + DONE_COUNT) * $\overline{RESET} * \overline{NEW96}$

Q5 := $\overline{Q5} * Q4 * Q3 * Q2 * Q1 * Q0 * \overline{TCK} * \overline{DONE\_COUNT} * \overline{NEW96}$ — Toggle if all lower bits HIGH and still counting LOW if (re)triggered by NEW96

+ Q5 * ($\overline{Q4}$ + $\overline{Q3}$ + $\overline{Q2}$ + $\overline{Q1}$ + $\overline{Q0}$ + TCK + DONE_COUNT) * $\overline{NEW96}$ — Stay if any lower bit is LOW or if done counting "

+ RESET — HIGH at reset

Q6 := $\overline{Q6} * Q5 * Q4 * Q3 * Q2 * Q1 * Q0 * \overline{TCK} * \overline{DONE\_COUNT} * \overline{NEW96}$ — LOW when (re)triggered by NEW96

+ Q6 * ($\overline{Q5}$ + $\overline{Q4}$ + $\overline{Q3}$ + $\overline{Q2}$ + $\overline{Q1}$ + $\overline{Q0}$ + TCK + DONE_COUNT) * $\overline{NEW96}$ "

+ RESET — HIGH at reset

DONE_COUNT = Q6 * Q5 * $\overline{Q4} * \overline{Q3} * \overline{Q2} * \overline{Q1} * \overline{Q0}$ — Terminal count (96)

Management Port

The IMR management functions are enabled when the TEST pin is tied LOW. The management commands are byte oriented data and are input serially on the SI pin. Any responses generated during execution of a management command are output serially in a byte-oriented format by the IMR on the SO pin. Both the input and output data streams are clocked with the rising edge of the SCLK pin. The serial command data stream and any associated results data stream are structured in a manner to be compatible with the RS232 serial data format, i.e. one Start Bit followed by eight Data Bits.

The externally generated clock at the SCLK pin can be either a free running clock synchronized to the input bit patterns or a series of individual transitions meeting the setup and hold times with respect to the input bit pattern. If the latter method is used, it is to be noted that 20 SCLK clock transitions are required for proper execution of management commands that produce SO data, and that 14 SCLK clock transitions are needed to execute management commands that do not produce SO data.

Management Commands

The following section details the operation of each management command available in the IMR. In all cases, the individual bits in each command byte are shown with the MSB on the left and the LSB on the right. Data bytes are received and transmitted LSB first and MSB last. See Table 2 for a summary of the management commands.

AUI Port Disable

SI data: 0 0 1 0 1 1 1 1
SO data: None

The AUI port will be disabled upon receiving this command. Subsequently, the IMR will ignore all inputs (Carrier Sense and SQE) appearing at the AUI port and will not transmit any data or Jam Sequence on the AUI port. Issuing this command will also cause the AUI port to have its internal partitioning state machine forced to its idle state.

AUI Port Enable

SI data: 0 0 1 1 1 1 1 1
SO data: None

This command enables a previously disabled AUI port. Note that a partitioned AUI port may be reconnected by first disabling (AUI Port Disable Command) and then re-enabling the port with this command.

TP Port Disable

SI data: 0 0 1 0 0 b b b
(b b b is TP port #)
SO data: None

The TP port designated in the command byte will be disabled upon receiving this command. Subsequently, the IMR will ignore all inputs appearing at the disabled port's receive pins and will not transmit any data or Jam Sequence on that port's transmit pins. Issuing this command will also cause a TP port to enter the Link Fail state and to have its partitioning state machine returned to its idle state.

TP Port Enable

SI data: 0 0 1 1 0 b b b
(b b b is TP port #)
SO data: None

This command enables a previously disabled TP port. Note that to force a TP port into the Link Fail state and/or to reconnect a partitioned TP port, the port can first be disabled (TP Port Disable Command) and then re-enabled with this command.

AUI Port Partitioning Status

SI data: 1 0 0 0 1 1 1 1
SO data: P 0 0 0 0 0 0 0

P = 0 – Partitioned
P = 1 – Connected

The Partitioning Status of the AUI port is accessed by this command. If a port is disabled, reading its partitioning status will indicate that it is connected.

TP Port Partitioning Status

SI data: 1 0 0 0 0 0 0 0
SO data: P_7 P_6 P_5 P_4 P_3 P_2 P_1 P_0

$P_n = 0$ TP port n partitioned
$P_n = 1$ TP port n connected

The Partitioning Status of all eight TP ports are accessed by this command. If a port is disabled, reading its partitioning status will indicate that it is connected.

Alternate Reconnection Algorithm (AUI Port)

SI data: 0 0 0 1 1 1 1 1
SO data: None

The AUI port Partitioning/Reconnection scheme can be programmed for the alternate (transmit only) reconnection algorithm by invoking this command. To return the

AUI back to the standard (transmit or receive) reconnection algorithm , it is necessary to reset the IMR.

Alternate Reconnection Algorithm (TP Ports)

SI data: 0 0 0 1 0 0 0 0
SO data: None

The TP ports Partitioning/Reconnection scheme can be programmed for the alternate (transmit only) reconnection algorithm by invoking this command. All TP ports are affected as a group by this command. To return the TP ports back to the standard (transmit or receive) reconnection algorithm, it is necessary to reset the IMR.

Link Test Status of TP Ports

SI data: 1 1 0 1 0 0 0 0
SO data: L_7 L_6 L_5 L_4 L_3 L_2 L_1 L_0

$L_n = 0$ TP Port n in Link Test Fail
$L_n = 1$ TP Port n in Link Test Pass

The Link Test Statuses of all eight TP ports are accessed by this command. If a twisted pair port is disabled, reading its Link Test Status indicates it being in Link Test Pass state. Upon reenabling, the port will be forced into Link Fail.

Disable Link Test Function

SI data: 0 1 0 0 0 b b b
(b b b is TP port #)
SO data: None

This command disables the Link Test function at the TP port designated in the command byte, i.e. the TP port will no longer be disconnected due to Link Test Fail. A TP port which has its Link Test function disabled will continue to transmit Link Test Pulses. If a twisted pair port has Link Test disabled, then reading the Link Test Status indicates it being in Link Test Pass.

Enable Link Test Function

SI data: 0 1 0 1 0 b b b
(b b b is TP port #)
SO data: None

This command re-enables the Link Test Function in the TP port designated in the command byte. This command executes only if the designated TP port has had the Link Test Function disabled by the Disable Link Test Function command. Otherwise, the command is ignored.

Polarity Status of TP Ports

SI data: 1 1 1 0 0 0 0 0
SO data: P_7 P_6 P_5 P_4 P_3 P_2 P_1 P_0

$P_n = 0$ TP Port n polarity correct
$P_n = 1$ TP Port n polarity reversed

The statuses of all eight TP port polarities are accessed with this command. The IMR has the ability to detect and correct reversed polarity on the TP ports' RXD+/- pins. If the polarity is detected as reversed for a TP port, then the IMR will set the appropriate bit in this command's results byte only if the Polarity Reversal Function is enabled for that port.

Enable Automatic Receiver Polarity Reversal

SI data: 0 1 1 1 0 b b b
(b b b is TP port #)
SO data: None

This command enables the Automatic Receiver Polarity Reversal Function for the TP port designated in the command byte. If enabled in a TP port, the IMR will automatically invert the polarity of that TP port's receiver circuitry if the TP port is detected as having reversed polarity (due to a wiring error). After reversing the receiver polarity , the TP port could then receive subsequent (reverse polarity) packets correctly.

Disable Automatic Receiver Polarity Reversal

SI data: 0 1 1 0 0 b b b
(b b b is TP port #)
SO data: None

This command disables the Automatic Receiver Polarity Reversal Function for the TP port designated in the command byte. If this function is disabled on a TP port with reverse polarity (due to a wiring error), then the TP port will fail Link Test due to the reversed polarity of the Link Pulses. If the Link Test Function is also disabled on the TP port, then the received reverse polarity packets would be repeated to all other network ports in the IMR as inverted data.

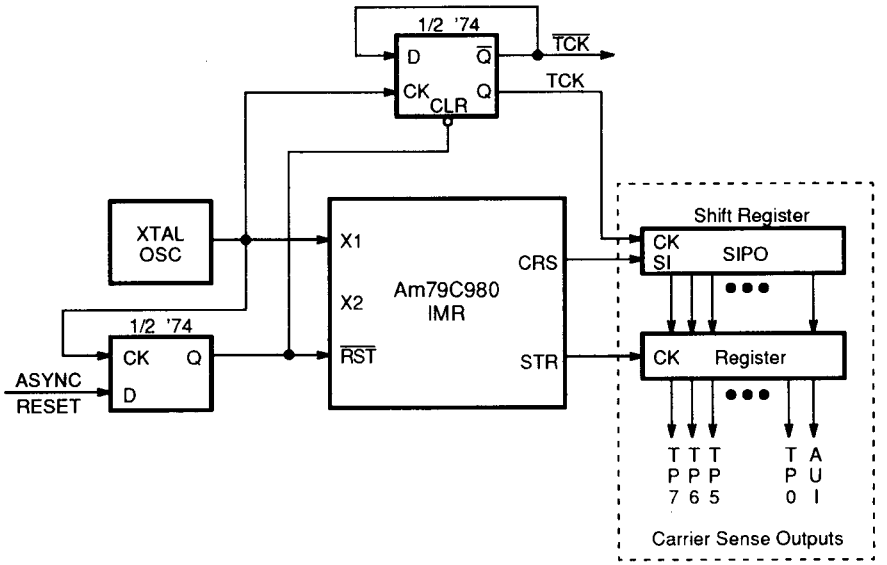
Table 2. Management Port Command Summary

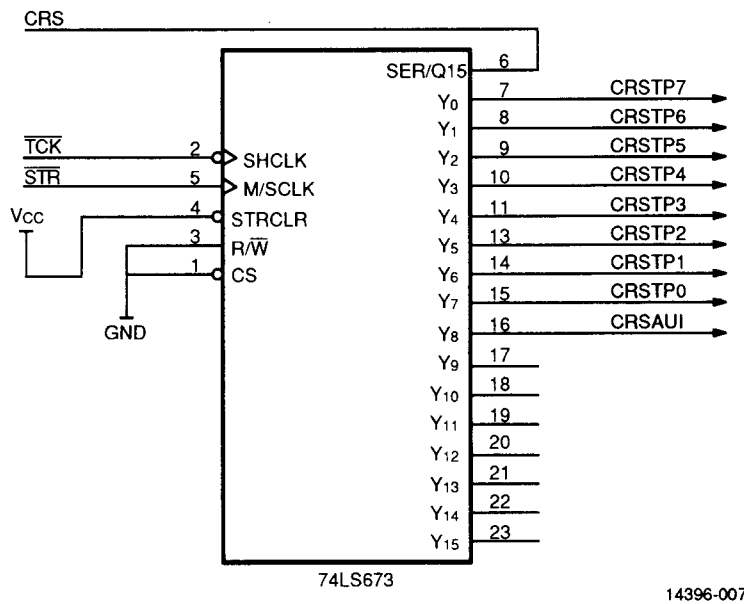
Command	SI data	SO data
AUI Port Disable	00101111	–
AUI Port Enable	00111111	–
TP Port Disable	00100bbb	–
TP Port Enable	00110bbb	–
AUI Port Partitioning Status	10001111	P0000000
TP Port Partitioning Status	10000000	$P_7 - P_0$
Alternate Reconnection Algorithm (AUI)	00011111	–
Alternate Reconnection Algorithm (TP)	00010000	–
Link Test Status of TP Ports	11010000	$L_7 - L_0$
Disable Link Test Function	01000bbb	–
Enable Link Test Function	01010bbb	–
Polarity Status of TP Ports	11100000	$P_7 - P_0$
Enable Automatic Receiver Polarity Reversal	01110bbb	–
Disable Automatic Receiver Polarity Reversal	01100bbb	–

Port Activity Monitor

Two pins, CRS and STR, are used to serially output the state of the internal Carrier Sense signals from the AUI and the eight TP ports. This function together with external hardware and/or software can be used to monitor repeater receive and/or collision activity.

The diagram below shows typical external hardware employed to convert the serial bit stream into parallel form. The accuracy of the CRS signals is 10 Bit Times (BT) (1 microsecond). Specifically, a transition to active state by any of the internal carrier sense bits that lasts for less than 10BT is latched internally and is used to set the appropriate bit during the next sample period.





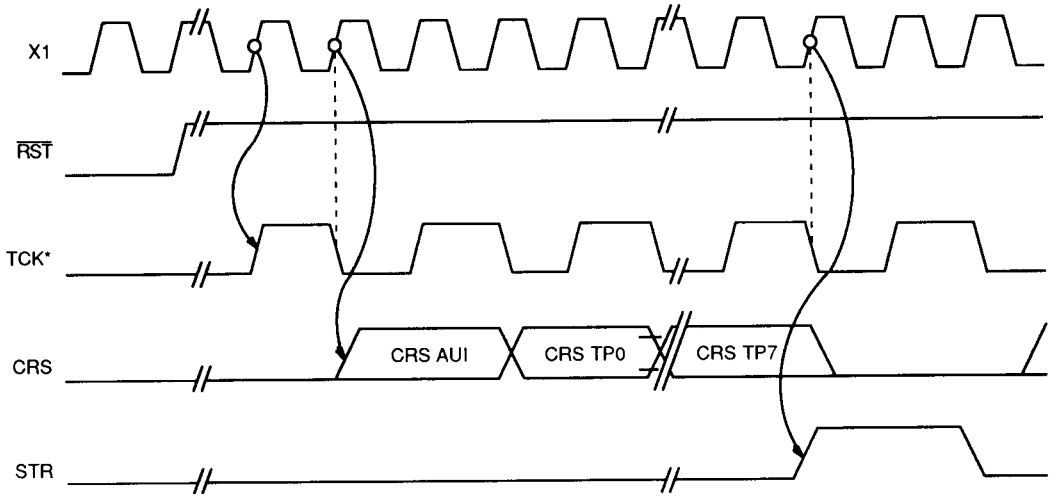
Single IC Implementation of the SIPO and Output Register.

Figure 4a. Port Activity Monitor Implementation

Loopback Test Mode

The IMR can be programmed to enter Loopback Mode on all network ports. This is accomplished by first driving the TEST pin HIGH, then clocking (using the SCLK pin) a minimum of three 0s into the SI pin. This causes the IMR to loop all received data on each port back to each port's corresponding transmit outputs. Specifically, the AUI DI input is passed unaltered to the AUI DO output, and each RXD input on the twisted pair ports is passed (unaltered) to the respective TXD and TXP outputs. Only receive data that passes the required amplitude squelch criteria is looped back to the transmit outputs. Note that the data is looped back unaltered, meaning that no signal retiming or regeneration takes place. Therefore, any signal distortion present on the receive data paths will be retransmitted.

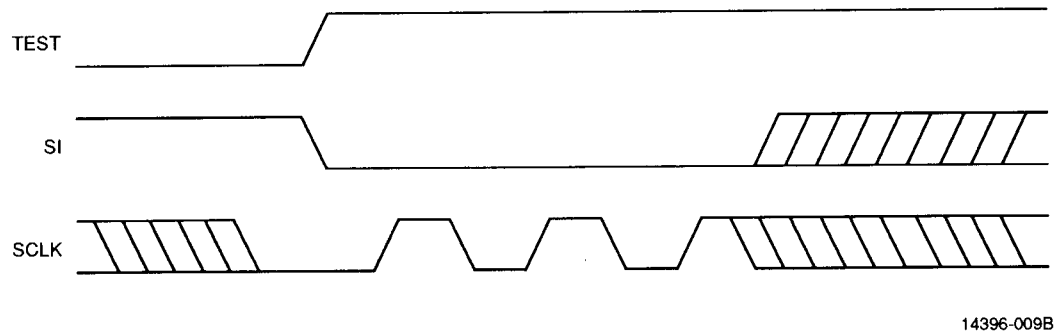
The IMR will return to normal operation when the TEST pin is again driven LOW.



*Externally generated signal illustrates internal IMR clock phase relationship.

14396C-008B

Figure 4b. Port Activity Monitor Implementation (Continued)



14396-009B

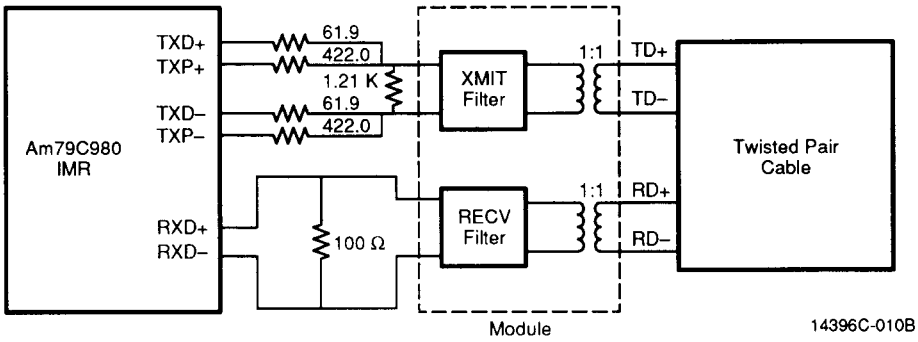
Figure 5. Programming the IMR for Loopback Mode

IMR External Components

Fig. 6 shows a typical twisted pair port external components schematic. The resistors used should have a 1% tolerance to ensure interoperability with 10BASE-T compliant networks. The filters and pulse transformers are necessary devices that have a major influence on the performance and compliance of the 10BASE-T ports of the repeater. Specifically, the transmitted waveforms are heavily influenced by the filter characteristics and the twisted pair receivers employ several criteria to continuously monitor the incoming signal's amplitude and timing characteristics to determine when and if to assert

the internal carrier sense. For these reasons, it is crucial that the values and tolerances of the external components be as specified. Several manufacturers produce a module that combines the functions of the transmit and receive filters and the pulse transformers into one package.

The AUI port, if used in a repeater design, should comply with IEEE 802.3. This is accomplished through the use of standard AUI pulse transformers and drop cable termination networks.



The Filter/Transformer Module shown is available from the following manufacturers:

Belfuse	TDK
Pulse Engineering	PCA
Valor Electronics	Nano Pulse

Figure 6a. Typical TP Port External Components

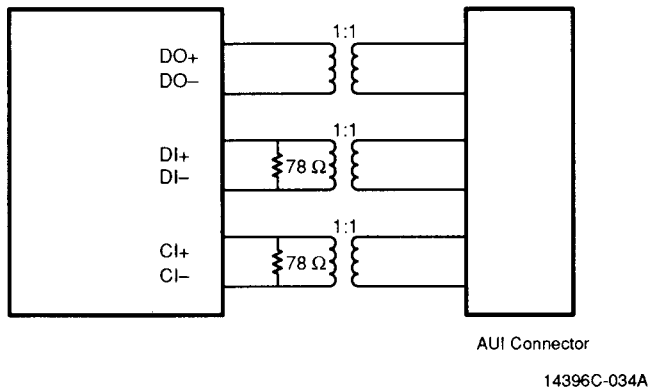
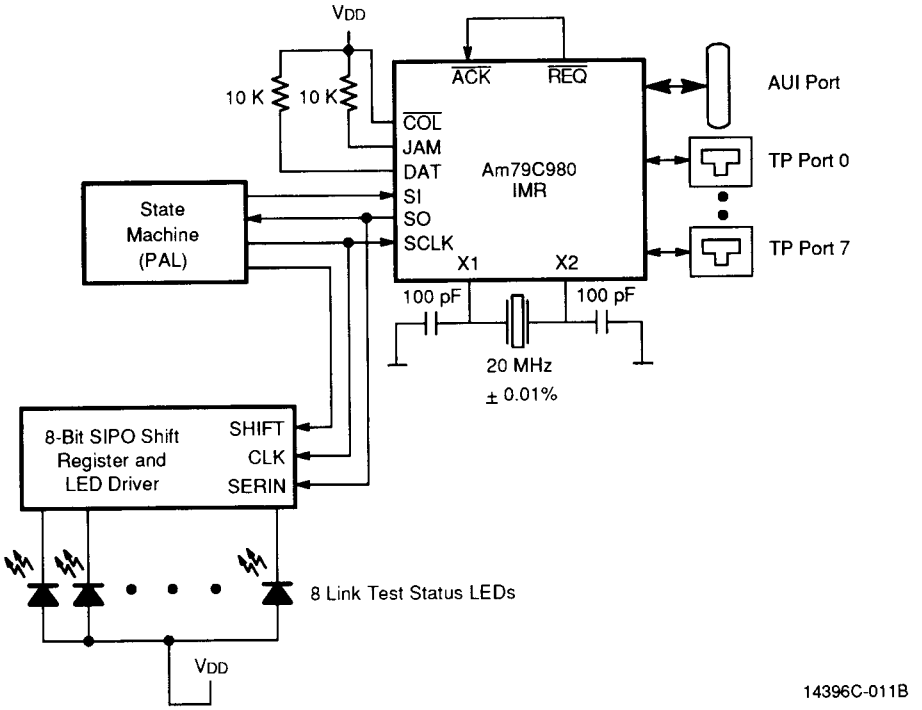


Figure 6b. Typical AUI Port Components

APPLICATIONS



Note: Unused receiver pairs (DI +/–, CI +/–, RXD_n +/–) should be shorted together.

Figure 7. Low Cost 10BASE-T Repeater

APPLICATIONS (Continued)

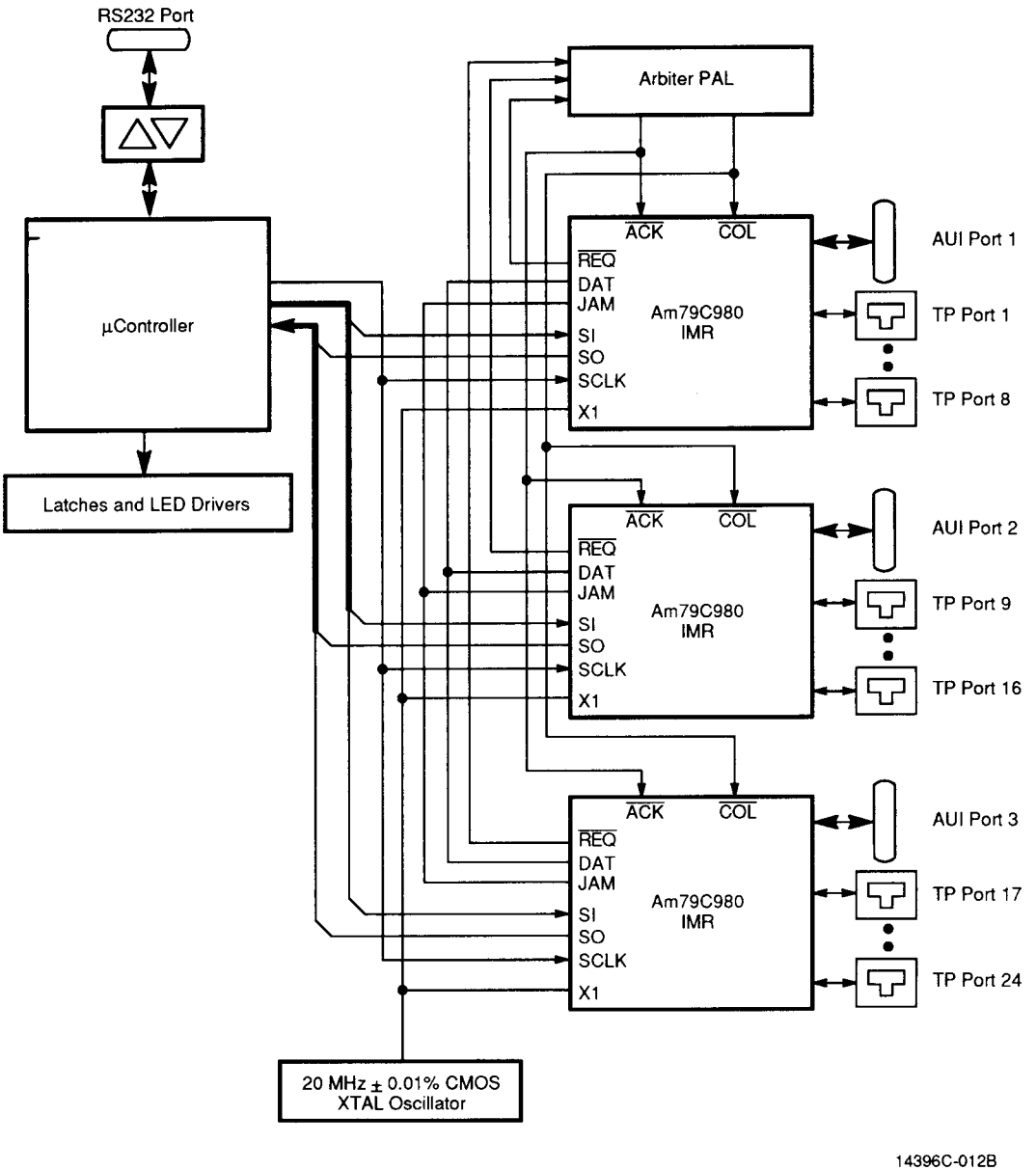


Figure 8. Intelligent Multi-IMR Based Repeater

ABSOLUTE MAXIMUM RATINGS

Storage Temperature	−65°C to +150°C
Ambient Temperature Under Bias	0 to 70°C
Supply Voltage referenced to AVSS or DVSS (AVDD, DVDD)	−0.3 to +6 V

Stresses above those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to absolute maximum ratings for extended periods may affect device reliability.

OPERATING RANGES

Commercial (C) Devices

Temperature (T_A)	0 to +70°C
Supply Voltage (AV_{DD}, DV_{DD})	5 V to ±5%

Operating ranges define those limits between which the functionality of the device is guaranteed.

DC CHARACTERISTICS over operating ranges unless otherwise specified

Parameter Symbol	Parameter Description	Test Conditions	Min.	Max.	Unit
Digital I/O					
V_{IL}	Input LOW Voltage	DV_{SS} = 0.0 V	−0.5	0.8	V
V_{IH}	Input HIGH Voltage		2.0	DV_{DD}+0.5	V
V_{OL}	Output LOW Voltage	I_{OL} = 4.0 mA	–	0.4	V
V_{OH}	Output HIGH Voltage	I_{OH} = −0.4 mA	2.4	–	V
I_{IL}	Input Leakage Current (also DAT and JAM as inputs)	DV_{SS}<V_{IN}<DV_{DD}	–	10	µA
V_{ILX}	X_1 Crystal Input LOW Voltage	DV_{SS} = 0.0 V	−0.5	1.0	V
V_{IHX}	X_1 Crystal Input HIGH Voltage	DV_{SS} = 0.0 V	3.8	DV_{DD}+0.5	V
I_{ILX}	Crystal Input LOW Current	V_{IN} = DV_{SS}	–	10	µA
I_{IHX}	Crystal Input HIGH Current	V_{IN} = DV_{DD}	–	10	µA
AUI Port					
I_{IAXD}	Input Current at DI+/- and CI+/- pairs	AV_{SS} < V_{IN} < AV_{DD}	−500	+500	µA
V_{AICM}	DI+,DI-,CI+,CI- Open Circuit Input Common Mode Voltage (bias)	I_{IN} = 0A, AV_{SS} = 0 V	AV_{DD} − 3.0	AV_{DD}−1.0	V
V_{AIDV}	Differential Mode Input Voltage Range (DI, CI)	AV_{DD} = 5.0 V	−2.5	+2.5	V
V_{ASQ}	DI, CI Squelch Threshold		−275	−160	mV
V_{ATH}	DI Switching Threshold	(Note 1)	−35	+35	mV
V_{AOD}	Differential Output Voltage |(DO+) − (DO-)|	R_L = 78 Ω	620	1100	mV
V_{ADDI}	DO Differential Output Voltage Imbalance	R_L = 78 Ω	−25	+25	mV
V_{AOD}OFF	DO Differential Idle Output Voltage	R_L = 78 Ω	−40	+40	mV
I_{AOD}OFF	DO Differential Idle Output Current	R_L = 78 Ω (Note 1)	−1	+1	mA
V_{AOCM}	DO+/- Common Mode Output Voltage	R_L = 78 Ω	2.5	AV_{DD}	V

DC CHARACTERISTICS (Continued)

Parameter Symbol	Parameter Description	Test Conditions	Min.	Max.	Unit
Twisted Pair Ports					
I_{IRXD}	Input current at RXD+/-	$AV_{SS}<V_{IN}<AV_{DD}$	–500	+500	µA
R_{RXD}	RXD differential input resistance	(Note 1)	10	–	KΩ
V_{TIVB}	RXD+,RXD- open circuit input voltage (bias)	I_{IN} = 0 mA	AV_{DD}–3.0	AV_{DD}–1.5	V
V_{TID}	Differential Mode input voltage range (RXD)	AV_{DD} = 5.0 V	–3.1	+3.1	V
V_{TSQ+}	RXD positive squelch threshold (peak)	Sinusoid 5 MHz <f< 10 MHz	300	520	mV
V_{TSQ-}	RXD negative squelch threshold (peak)	Sinusoid 5 MHz <f< 10 MHz	–520	–300	mV
V_{THS+}	RXD post-squelch positive threshold (peak)	Sinusoid 5 MHz <f< 10 MHz	150	293	mV
V_{THS-}	RXD post-squelch negative threshold (peak)	Sinusoid 5 MHz <f< 10 MHz	–293	–150	mV
V_{RXDTH}	RXD switching threshold	(Note 1)	–60	+60	mV
V_{TXH}	TXD+/- and TXP+/- output HIGH voltage	DV_{SS} = 0 V (Note 2)	DV_{DD}–0.6	DV_{DD}	V
V_{TXL}	TXD+/- and TXP+/- output LOW voltage	DV_{DD} = 5 V (Note 2)	DV_{SS}	DV_{SS}+0.6	V
V_{TXI}	TXD+/- and TXP+/- differential output voltage imbalance		–40	+40	mV
V_{TXOFF}	TXD+/- and TXP+/- differential idle output voltage	DV_{DD} = 5 V	–	40	mV
R_{TXD}	TXD+/- differential driver output impedance	(Note 1)	–	40	Ω
R_{TXP}	TXP+/- differential driver output impedance	(Note 1)	–	80	Ω
Power Supply Current					
I_{DD}	Power supply current (idle)	fx_1 = 20 MHz	–	180	mA
	Power supply current (transmitting – no TP load)	fx_1 = 20 MHz	–	300	mA
	Power supply current (transmitting – with TP load)	fx_1 = 20 MHz	–	Note 8	mA

SWITCHING CHARACTERISTICS over operating ranges unless otherwise specified

Parameter Symbol	Parameter Description	Test Conditions	Min.	Max.	Unit
Clock and Reset					
t_{X1}	X1 Clock Period		49.995	50.005	ns
t_{X1H}	X1 Clock HIGH		20	30	ns
t_{X1L}	X1 Clock LOW		20	30	ns
t_{X1R}	X1 Clock Rise Time		–	10	ns
t_{X1F}	X1 Clock Fall Time		–	10	ns
t_{RST}	Reset pulse width ($\overline{RST}$ pin LOW)		150	–	µs
t_{RSTSET}	$\overline{RST}$ HIGH setup time with respect to X1 Clock		20	–	ns
t_{RSTHLD}	$\overline{RST}$ LOW hold time with respect to X1 Clock		0	–	ns
Management Port					
t_{SCLK}	SCLK Clock Period		100	–	ns
t_{SCLKH}	SCLK Clock HIGH		30	–	ns
t_{SCLKL}	SCLK Clock LOW		30	–	ns
t_{SCLKR}	SCLK Clock Rise Time		–	10	ns
t_{SCLKF}	SCLK Clock Fall Time		–	10	ns
t_{SISET}	SI input setup time with respect to SCLK rising edge		10	–	ns
t_{SIHLD}	SI input hold time with respect to SCLK rising edge		10	–	ns
t_{SODLY}	SO output delay with respect to SCLK rising edge	C_L = 100 pF	–	40	ns
t_{X1HCRS}	X1 rising edge to CRS valid	C_L = 100 pF	–	40	ns
t_{X1HSTH}	X1 rising edge to STR HIGH	C_L = 100 pF	–	40	ns
t_{X1HSTL}	X1 rising edge to STR LOW	C_L = 100 pF	–	40	ns
$t_{TESTSET}$	TEST input setup time with respect to SCLK rising edge		10	–	ns
$t_{TESTHLD}$	TEST input hold time with respect to SCLK rising edge		10	–	ns
Expansion Port					
t_{X1HRL}	X1 rising edge to $\overline{REQ}$ driven LOW	C_L = 100 pF	14	40	ns
t_{X1HRH}	X1 rising edge to $\overline{REQ}$ driven HIGH	C_L = 100 pF	14	40	ns
t_{X1HDR}	X1 rising edge to DAT/JAM driven	C_L = 100 pF	14	40	ns
t_{X1HDZ}	X1 rising edge to DAT/JAM not driven	C_L = 100 pF	14	40	ns
t_{DJSET}	DAT/JAM setup time		10	–	ns
t_{DJHOLD}	DAT/JAM hold time		14	–	ns
t_{CASET}	$\overline{COL}$/$\overline{ACK}$ setup time		5	–	ns
t_{CAHOLD}	$\overline{COL}$/$\overline{ACK}$ hold time		14	–	ns

SWITCHING CHARACTERISTICS (Continued)

Parameter Symbol	Parameter Description	Test Conditions	Min.	Max.	Unit
AUI Port					
t_{DOTD}	X1 rising edge to DO toggle		–	30	ns
t_{DOTR}	DO+,DO- rise time (10% to 90%)		2.5	5.0	ns
t_{DOTF}	DO+,DO- fall time (90% to 10%)		2.5	5.0	ns
t_{DORM}	DO+,DO- rise and fall time mismatch		–	1.0	ns
t_{DOETD}	DO+/- End of Transmission		275	375	ns
t_{PWODI}	DI pulse width accept/reject threshold	$\|V_{IN}\| > \|V_{ASQ}\|$ Note 3	15	45	ns
t_{PWKDI}	DI pulse width maintain/turn-off threshold	$\|V_{IN}\| > \|V_{ASQ}\|$ Note 4	136	200	ns
t_{PWOCI}	CI pulse width accept/reject threshold	$\|V_{IN}\| > \|V_{ASQ}\|$ Note 5	10	26	ns
t_{PWKCI}	CI pulse width maintain/turn-off threshold	$\|V_{IN}\| > \|V_{ASQ}\|$ Note 6	90	160	ns
Twisted Pair Ports					
t_{TXTD}	X1 rising edge to TXD+,TXP+ TXD-,TXP- transition delay		–	45	ns
t_{TR}	TXD+,TXD-,TXP+,TXP- rise time		–	20	ns
t_{TF}	TXD+,TXD-,TXP+,TXP- fall time		–	20	ns
t_{TM}	TXD+,TXD-,TXP+,TXP- rise and fall time mismatch		–	6	ns
t_{TETD}	Transmit End of Transmission		275	375	ns
t_{PWKRD}	RXD pulse width maintain/turn-off threshold	$\|V_{IN}\| > \|V_{THS}\|$ Note 7	136	200	ns
t_{PERLP}	Idle signal period		8	24	ms
t_{PWLP}	Idle Link Test pulse width (TXD+)		75	120	ns
t_{PWPLP}	Idle Link Test pulse width (TXP+,TXP-)		40	60	ns

Notes:

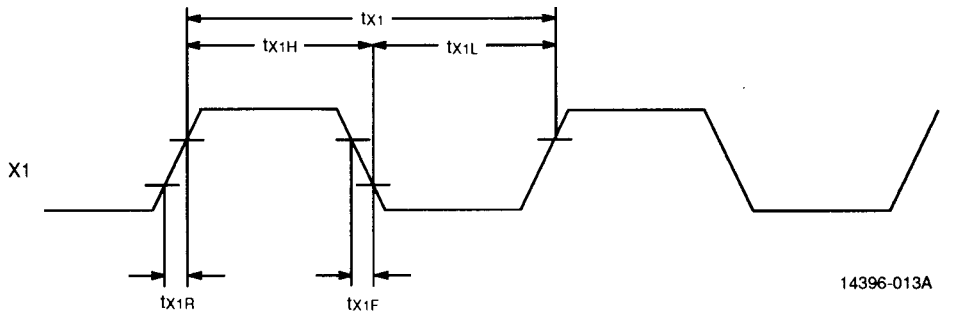
1. Parameter not tested.
2. Uses switching test load.
3. DI pulses narrower than t_{PWODI} (min) will be rejected; pulses wider than t_{PWODI} (max) will turn internal DI carrier sense on.
4. DI pulses narrower than t_{PWKDI} (min) will maintain internal DI carrier sense on; pulses wider than t_{PWKDI} (max) will turn internal DI carrier sense off.
5. CI pulses narrower than t_{PWOCI} (min) will be rejected; pulses wider than t_{PWOCI} (max) will turn internal CI carrier sense on.
6. CI pulses narrower than t_{PWKCI} (min) will maintain internal CI carrier sense on; pulses wider than t_{PWKCI} (max) will turn internal CI carrier sense off.
7. RXD pulses narrower than t_{PWKRD} (min) will maintain internal RXD carrier sense on; pulse wider than t_{PWKRD} (max) will turn internal RXD carrier sense off.
8. For the typical twisted pair load as shown in Figure 6, using a 100 Ω cable, an additional 28 mA (max) of I_{DD} current is required for each twisted pair port used. Less than 18% of the power associated with this additional current is dissipated by the IMR; the remainder is dissipated externally in the twisted pair load and cable.

KEY TO SWITCHING WAVEFORMS

WAVEFORM	INPUTS	OUTPUTS
	Must Be Steady	Will Be Steady
	May Change from H to L	Will Be Changing from H to L
	May Change from L to H	Will Be Changing from L to H
	Don't Care Any Change Permitted	Changing State Unknown
	Does Not Apply	Center Line is High Impedance "Off" State

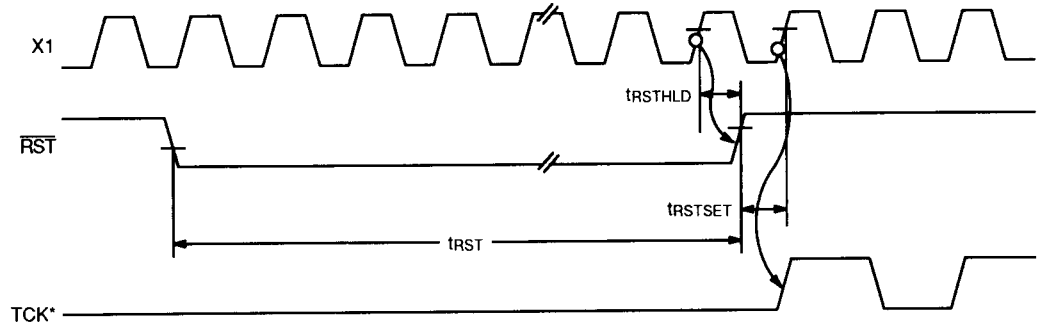
KS000010

SWITCHING WAVEFORMS



Clock Timing

SWITCHING WAVEFORMS (Continued)



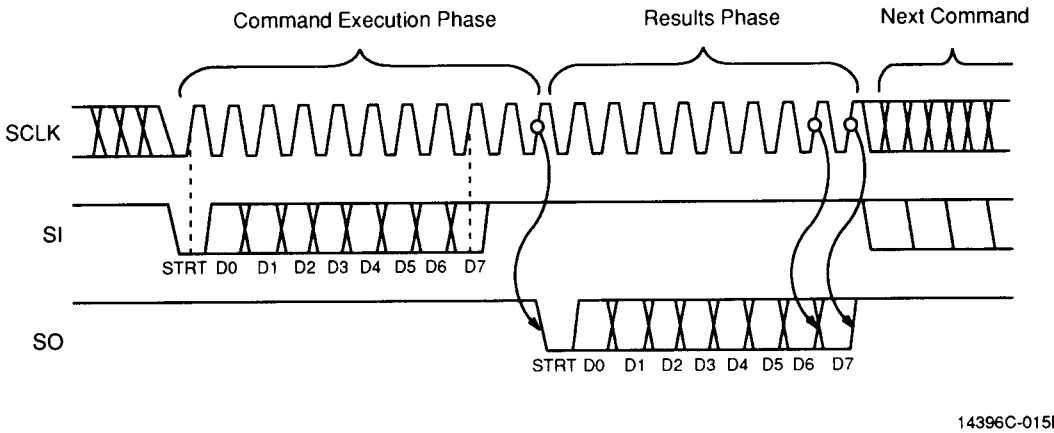
Note:

14396C-014B

tRSTSET refers to synchronous Reset Timing.

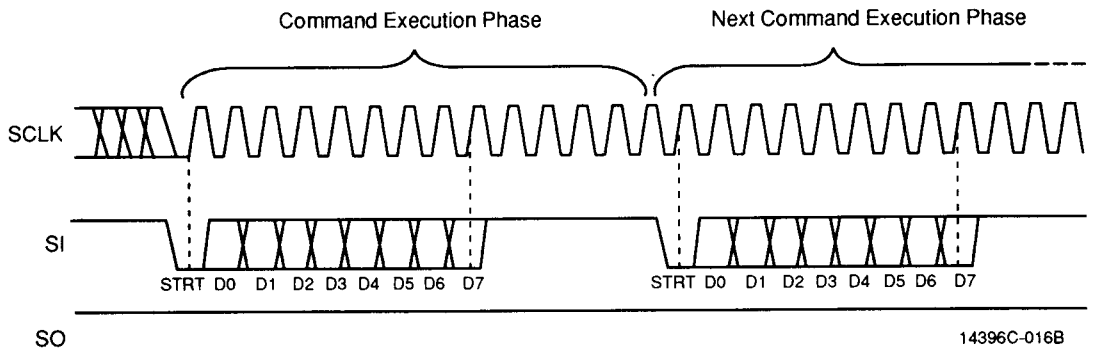
*Externally generated (Figure 4) signal illustrates internal IMR clock phase relationships.

Reset Timing



14396C-015B

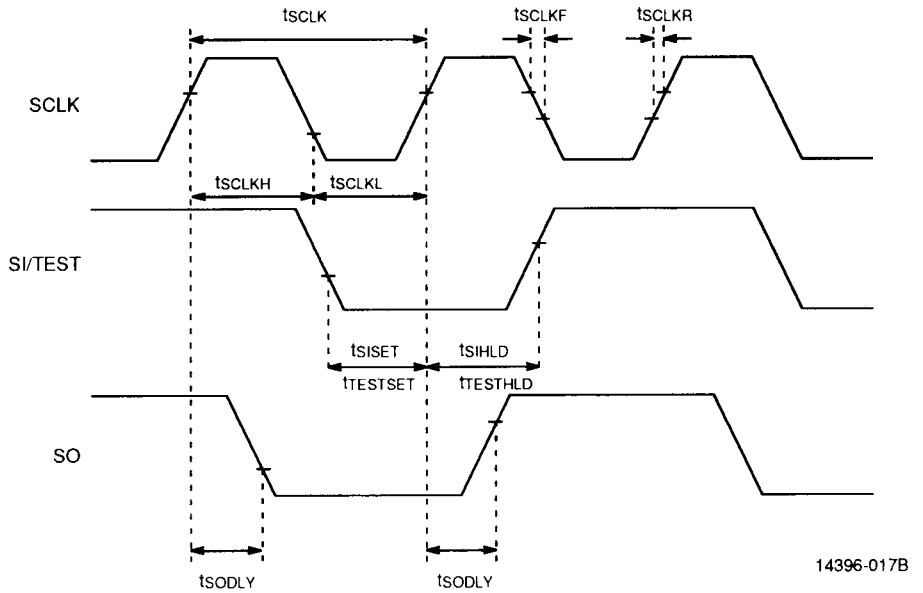
Management Command with Results Data



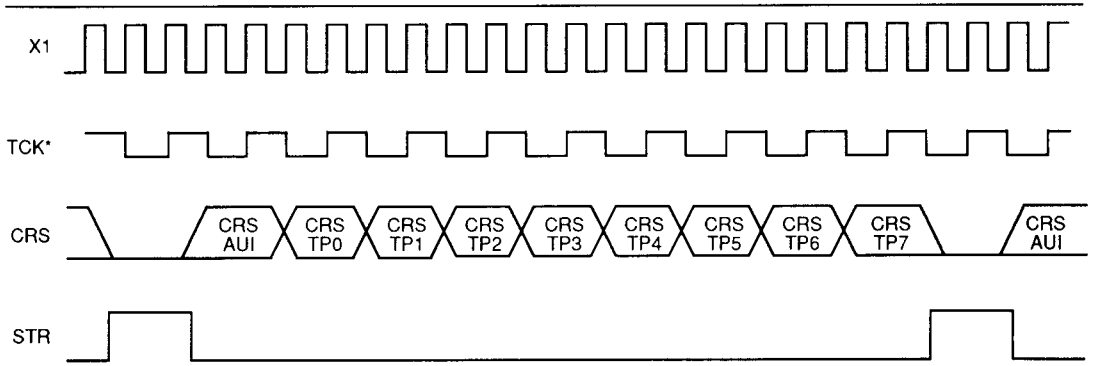
14396C-016B

No-results Management Command Timing

SWITCHING WAVEFORMS (Continued)



Management Port Clock Timing

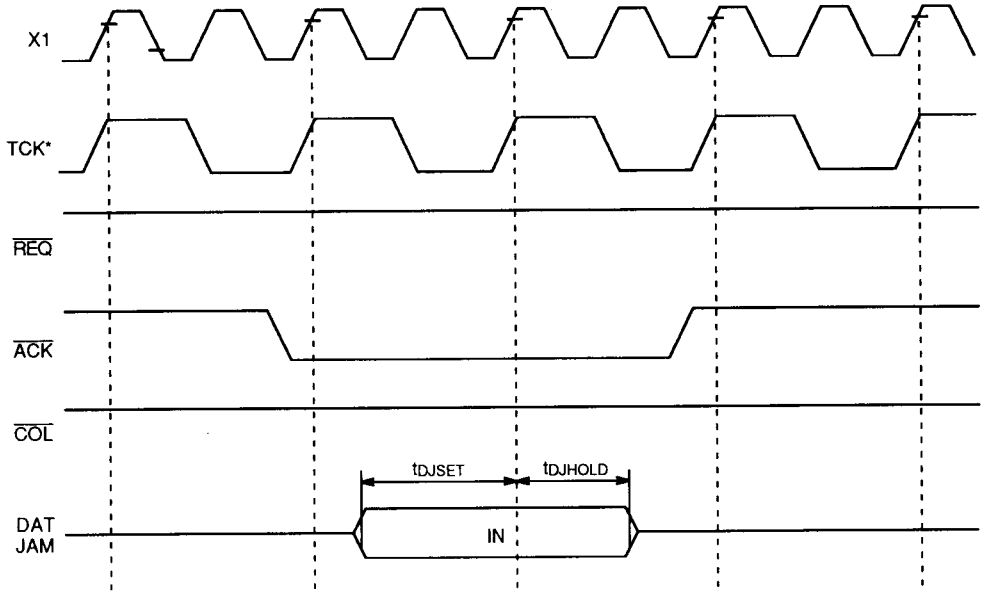


*Externally generated (Figure 4) signal illustrates internal IMR clock phase relationships.

14396C-018B

Carrier Sense Timing

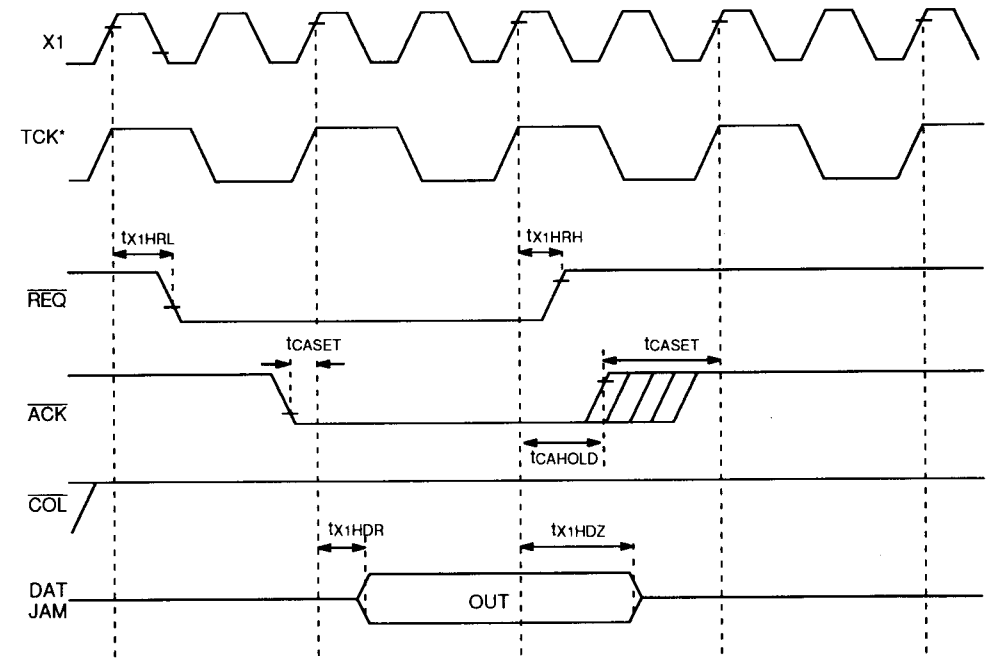
SWITCHING WAVEFORMS (Continued)



*Externally generated (Figure 4) signal illustrates internal IMR clock phase relationships.

14396C-019B

Expansion Port Input Timing

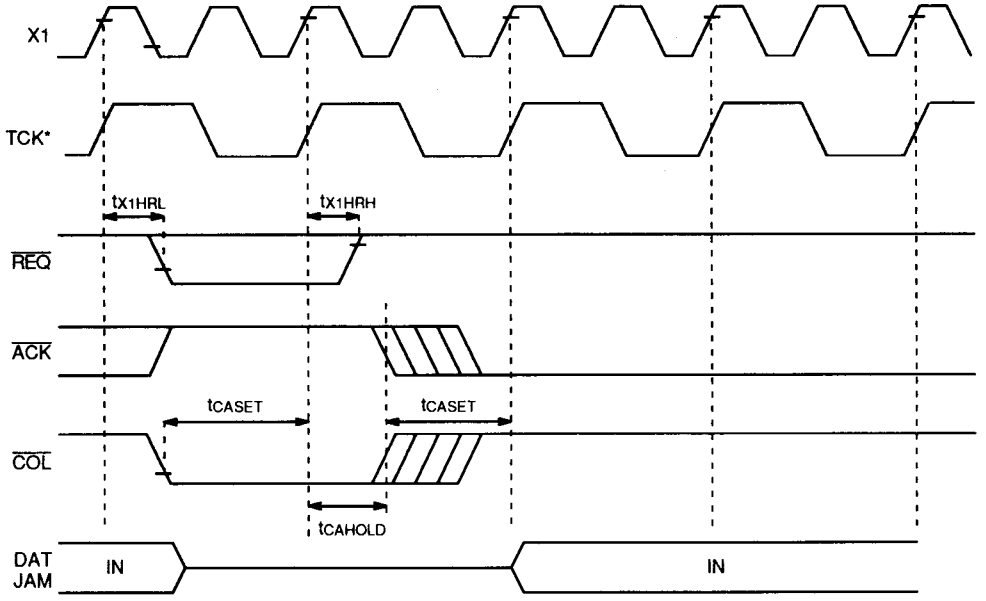


*Externally generated (Figure 4) signal illustrates internal IMR clock phase relationships.

14396C-020B

Expansion Port Output Timing

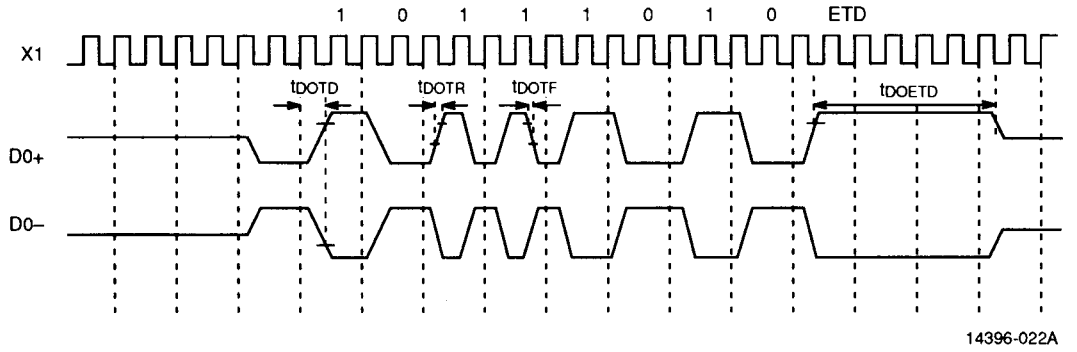
SWITCHING WAVEFORMS (Continued)



14396C-021B

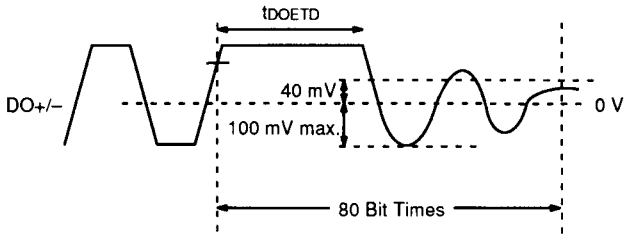
*Externally generated (Figure 4) signal illustrates internal IMR clock phase relationships.

Expansion Port Collision Timing



14396-022A

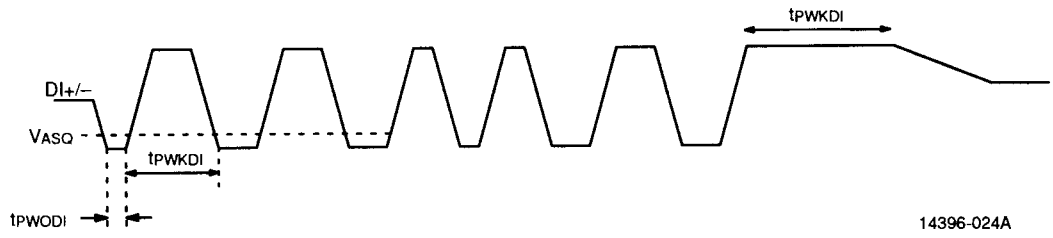
AUI DO Timing Diagram



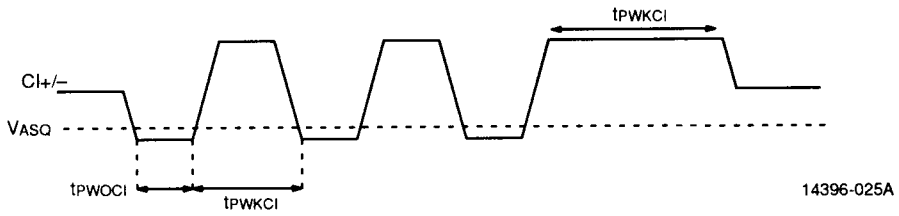
14396-023A

AUI Port DO ETD Waveform

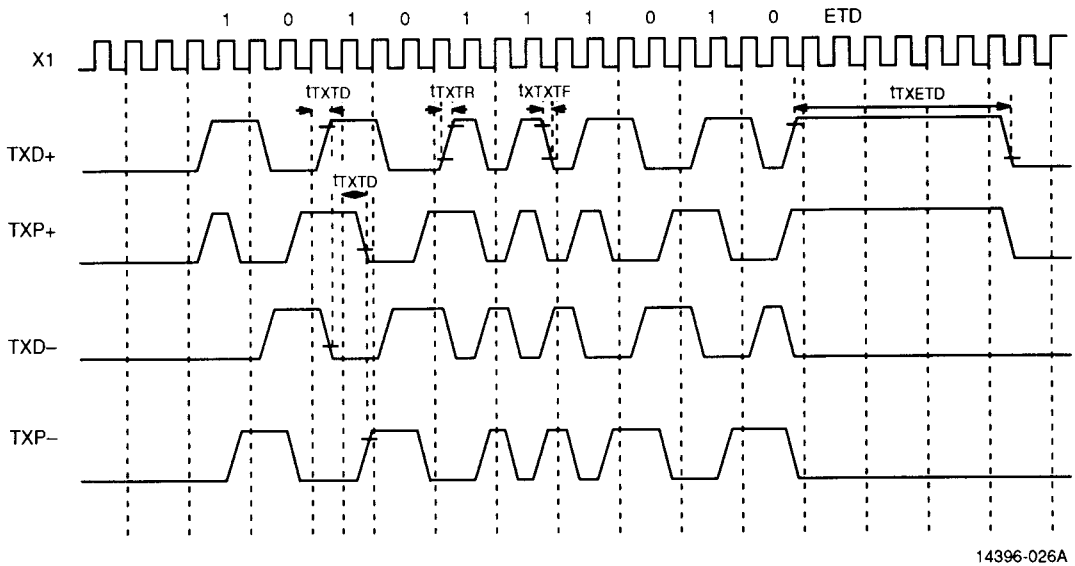
SWITCHING WAVEFORMS (Continued)



AUI Receive Timing Diagram

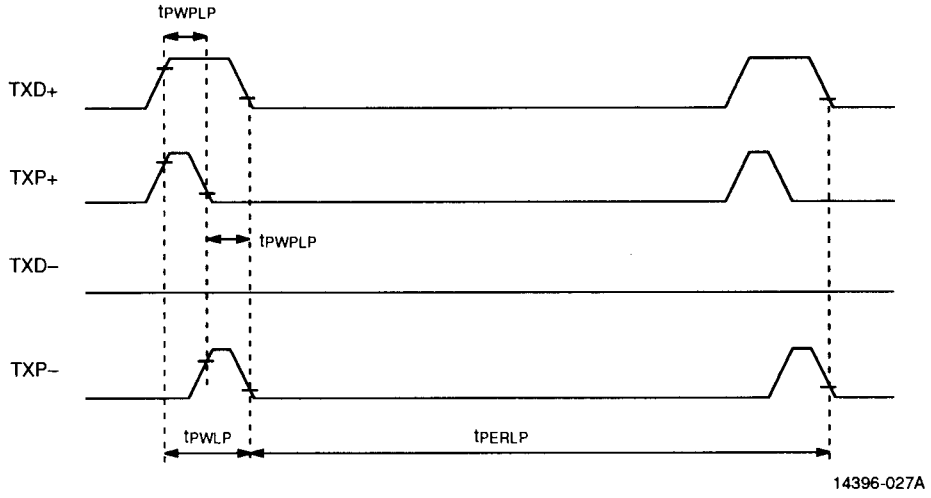


AUI Collision Timing Diagram

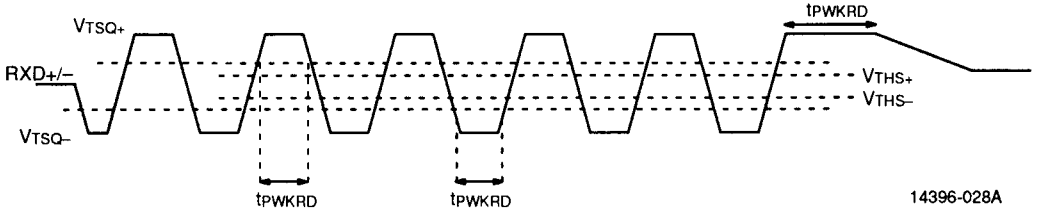


TP Ports Output Timing Diagram

SWITCHING WAVEFORMS (Continued)

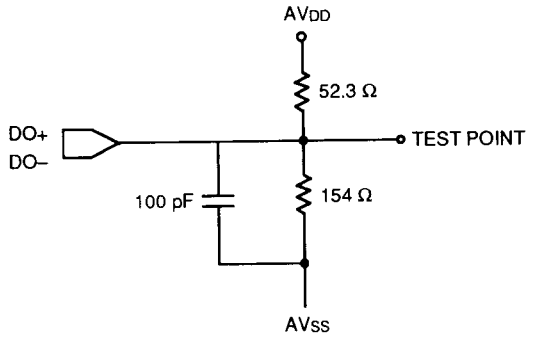


TP Idle Link Test Pulse

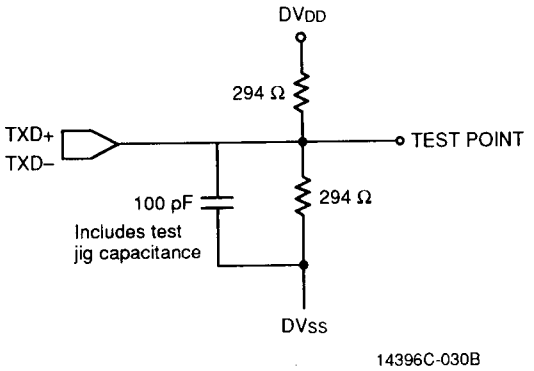


TP Receive Timing Diagram

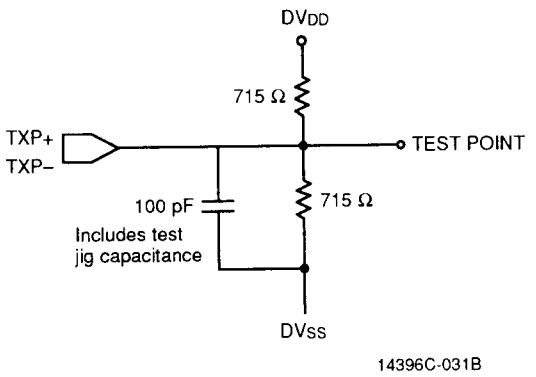
SWITCHING TEST CIRCUITS



AUI DO Switching Test Circuit



TXD Switching Test Circuit



TXP Outputs Test Circuit

APPENDIX

Glossary

Active Status

In a non-collision state, an IMR is considered active if it is receiving data on any one of its network ports, or is in the process of broadcasting (repeating) FIFO data from a recently completed data reception. In a collision state (the IMR is generating Jam Sequence), an IMR is considered active if any one or more network ports is receiving data. The IMR asserts the $\overline{REQ}$ line to indicate that it is active.

Collision

In a carrier sense multiple access/collision detect (CSMA/CD) network such as Ethernet, only one node can successfully transfer data at any one time. When two or more separate nodes (DTEs or repeaters) are simultaneously transmitting data onto the network, a Collision state exists. In a repeater using one or more IMRs, a Collision state exists when more than one network port is receiving data at any instant, or when any one or more network ports receives data while the IMR is transmitting (repeating) data, or when the CI+/- pins become active (nominal 10 MHz signal) on the AUI port.

Jam Sequence

A signal consisting of alternating 1s and 0s that is generated by the IMR when a Collision state is detected. This signal is transmitted by the IMR to indicate to the network that one or more network ports in the repeater is involved in a collision.

Network Port

Any of the eight 10BASE-T ports or the AUI port present in the IMR (i.e. not the Expansion Port or the Management Port).

Partitioning

A network port on a repeater has been partitioned if the repeater has internally 'disconnected' it from the repeater due to localized faults that would otherwise bring the entire network down. These faults are generally cable shorts and opens that tend to cause excessive collisions at the network ports. The partitioned network port will be internally re-connected if the network port starts behaving correctly again, usually when successful 'collisionless' transmissions and/or receptions resume.

Receive Collision

A network port is in a Receive Collision state when it detects collision and is not one of the colliding network 'nodes'. This applies mainly to a non-transmitting AUI port because a remote collision is clearly identified by the presence of a nominal 10 MHz signal on the CI+/- pins. However, any repeater port would be considered to be in a receive collision state if the repeater unit is receiving data from that port as the 'one-port-left' in the collision sequence.

Transmit Collision

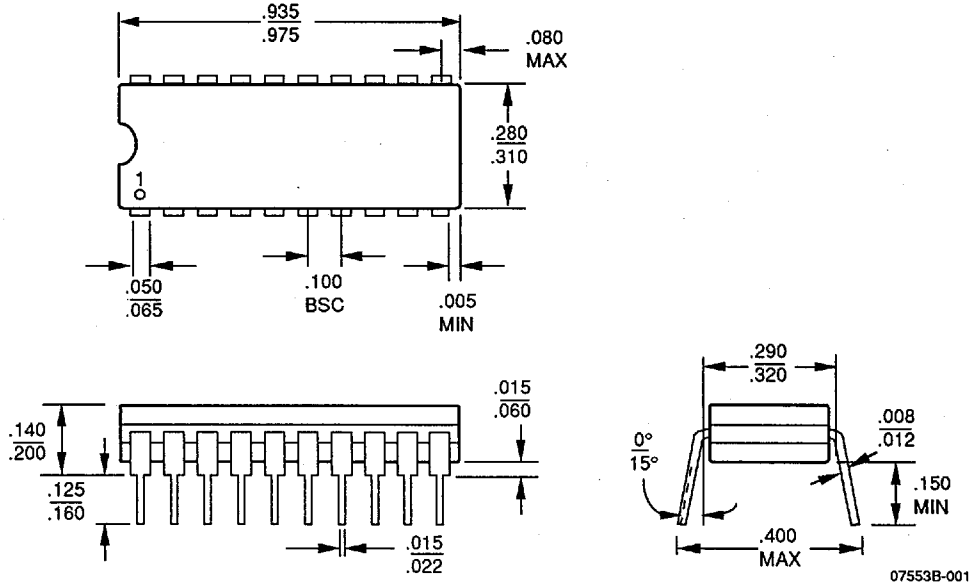
A network port is in a Transmit Collision state when collision occurs while that port is transmitting. On the AUI port, Transmit Collision is indicated by the presence of a nominal 10 MHz signal on the CI+/- pins while the AUI port is transmitting on the DO+/- pins. On a 10BASE-T port, Transmit Collision occurs when incoming data appears on the RXD+/- pins while the 10BASE-T port is transmitting on the TXD+/- and TXP+/- pins.

SECTION 5

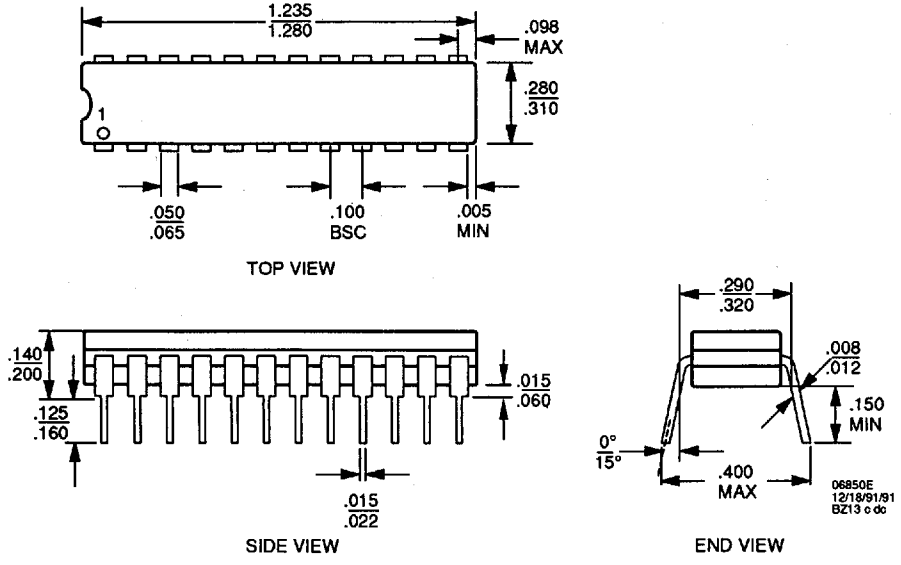
T-90-20

Physical Dimensions

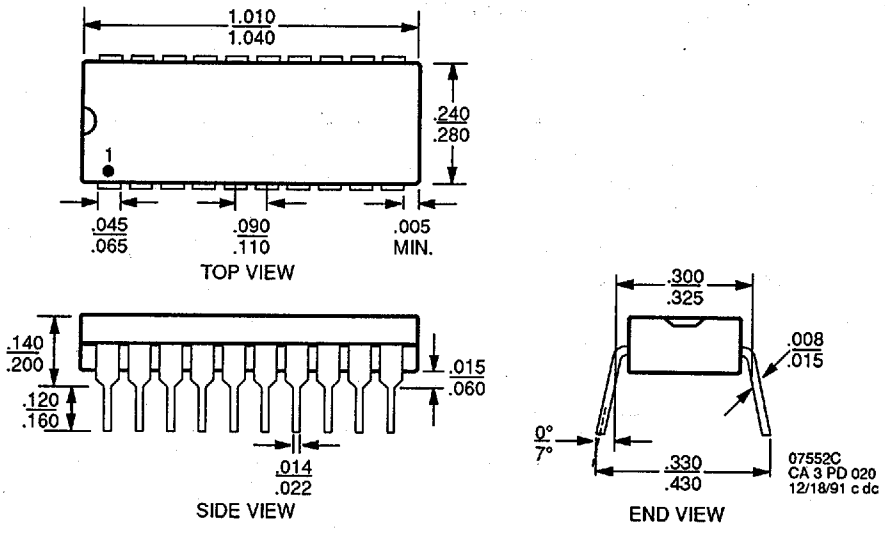
CD 020
20-Pin Ceramic DIP



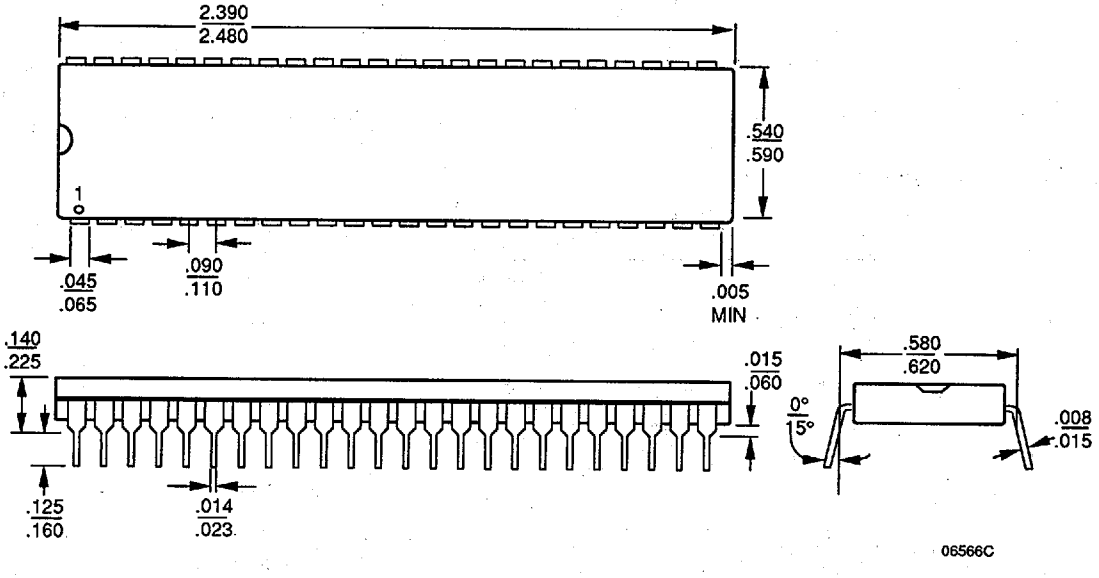
CD3024
24-Pin (Slim) Ceramic DIP



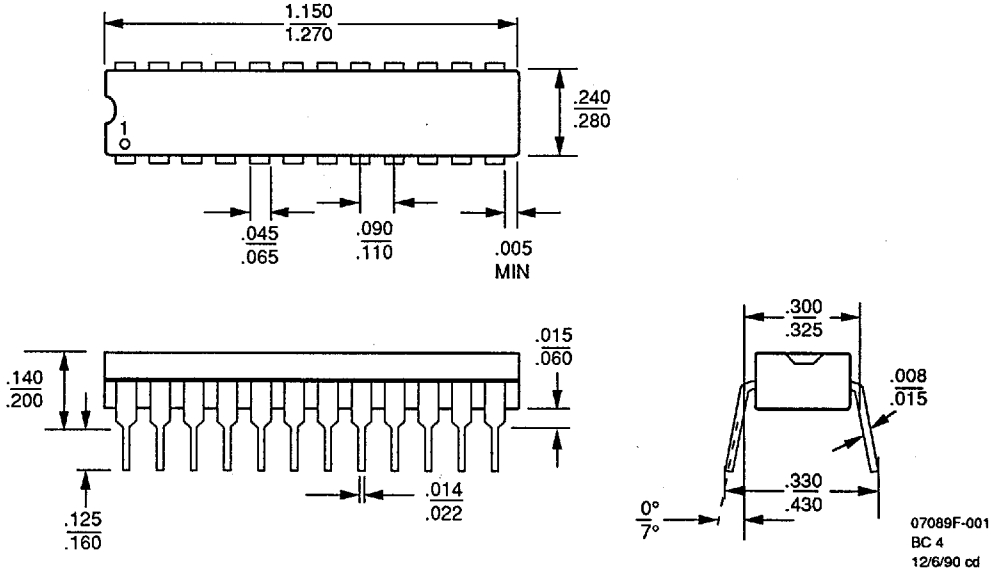
PD 020
20-Pin Plastic DIP



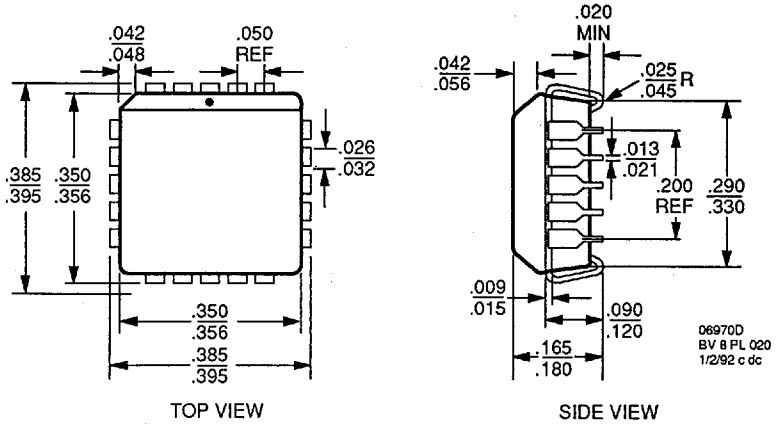
PD 048
48-Pin Plastic DIP



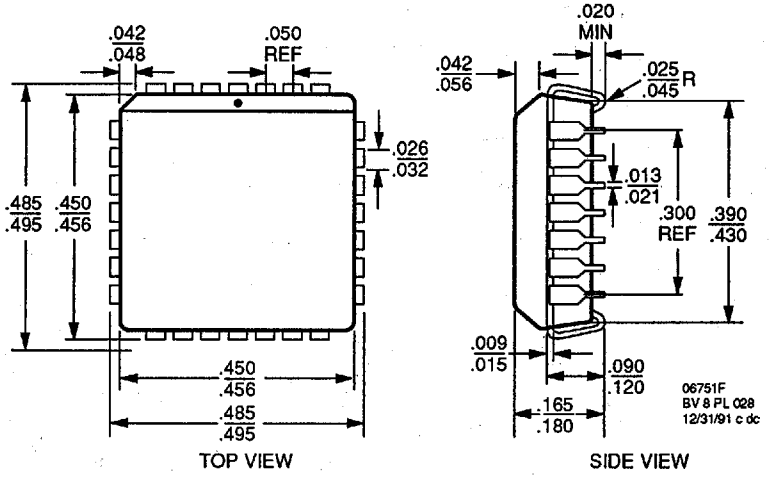
PD3024
24-Pin (Slim) Plastic DIP



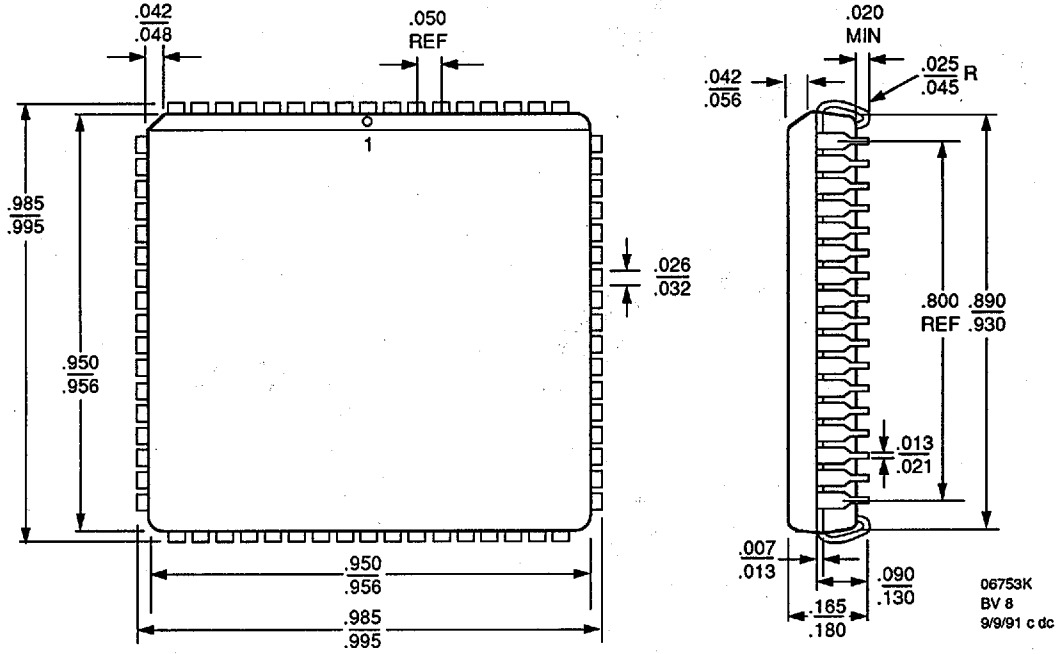
PL 020
20-Pin Plastic Leaded Chip Carrier



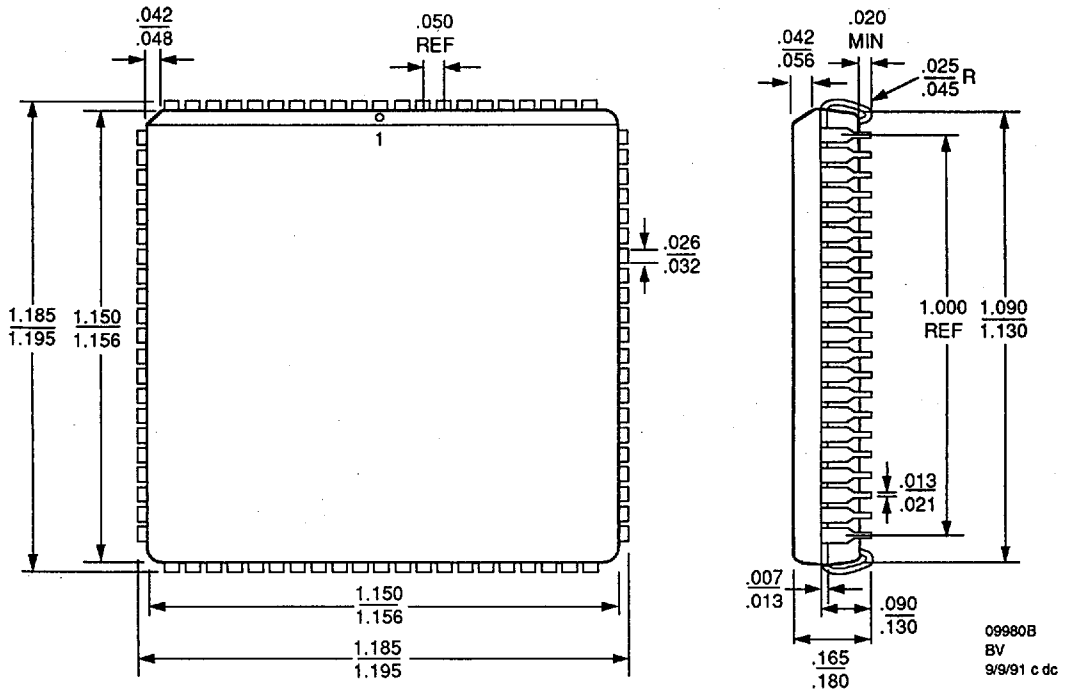
PL 028
28-Pin Plastic Leaded Chip Carrier



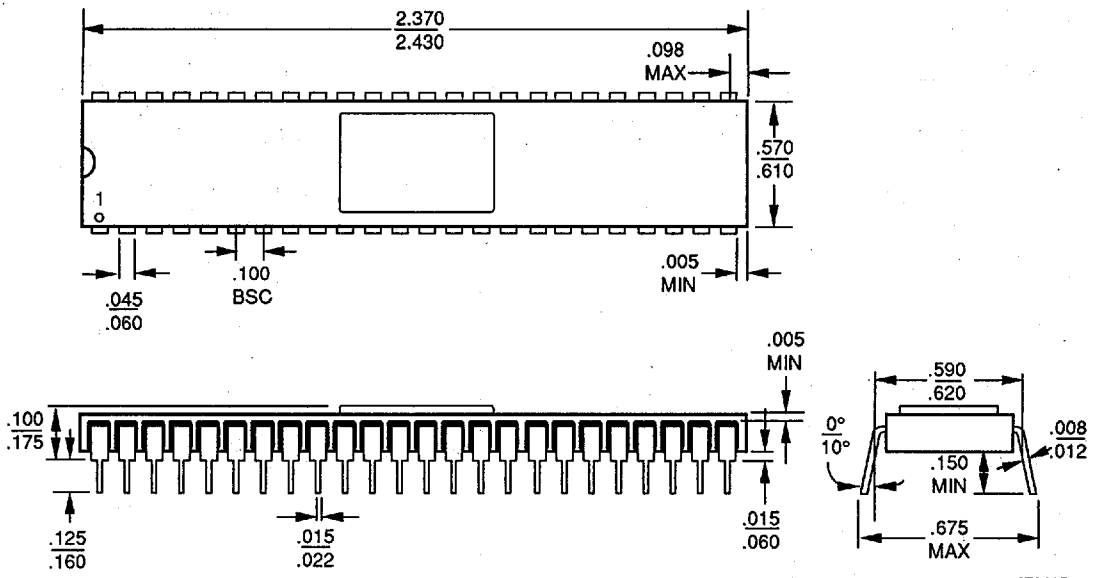
PL 068
68-Pin Plastic Leaded Chip Carrier



PL 084
84-Pin Plastic Leaded Chip Carrier



SD 048
48-Pin Sidebrazed Ceramic DIP



07644C
AW 25
8/14/91 c dc