# Quad ISLAC™

## *Quad Intelligent Subscriber Line Audio-processing Circuit (Quad ISLAC™)*
## Am79Q2241/2242/2243 Device

## APPLICATIONS

- **Voice over IP/DSL — Integrated Access Devices (IAD), Smart Residential Gateways (SRG), Home Gateway/ Router**
- **Cable Telephony — NIU, Set-Top Box, Home Side Box, Cable Modem, Cable PC**
- **Fiber — Fiber in the Loop (FITL), Fiber to the Home (FTTH)**
- **Wireless Local Loop, Intelligent PBX**
- **DLC-MUX**
- **CO**

## FEATURES

- **High performance digital signal processor provides programmable control of all major linecard functions**
  - — A-law/μ-law and linear codec
    - — Transmit and receive gain
    - — Two-wire AC impedance
    - — Transhybrid balance
    - — Equalization
  - — DC loop feeding
    - — Smooth or abrupt polarity reversal
  - — Loop supervision
    - — Off-hook debounce circuit
    - — Ground-key and ring-trip filters
  - — Ringing generation and control
  - — Adaptive hybrid balance
  - — Line and circuit testing
  - — Tone generation
  - — Metering generation at 12 kHz and 16 kHz
    - — Envelope shaping and level control
- **Selectable PCM/MPI or GCI digital interfaces**
  - — Supports most available master clock frequencies from 512 kHz to 8.192 MHz
- **General purpose I/O pins**
- **+3.3 V DC operation**
- **Exceeds LSSGR and ITU requirements**
- **Supports external ringing with on-chip ring-trip circuit**
  - — Automatic or manual ring-trip modes

## ORDERING INFORMATION

| Device | Package |
|---|---|
| Am79Q2241 VC | 64-pin TQFP |
| Am79Q2242 JC | 68-pin PLCC |
| Am79Q2243 VC | 80-pin TQFP |

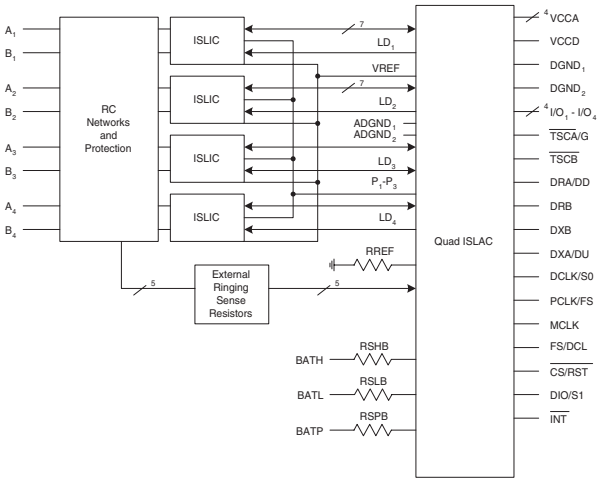
## DESCRIPTION

The Quad ISLAC™ device, in combination with an ISLIC™ device, implements a four channel universal telephone line interface. This enables the design of a single, low cost, high performance, fully software programmable line interface for multiple country applications. All AC, DC, and signaling parameters are fully programmable via microprocessor or GCI interfaces. Additionally, the Quad ISLAC device has integrated self-test and line-test capabilities to resolve faults to the line or line circuit. The integrated test capability is crucial for remote applications where dedicated test hardware is not cost effective.

## RELATED LITERATURE

- **080274 Am79D2251 Dual ISLAC Data Sheet**
- **080248 Am79231 ISLIC Data Sheet**
- **080693 Am79240 ISLIC Data Sheet**
- **080249 Am79241 ISLIC Data Sheet**
- **080253 Am79251 ISLIC Data Sheet**
- **080344 Am79R2xx/Am79Q224x Technical Reference**
- **080345 Am79R240/Am79D2251 Technical Reference**

## BLOCK DIAGRAM




Publication# **080250** Rev: **G**
Version:1.0 Date: **Dec 20, 2001**

## TABLE OF CONTENTS

## PRODUCT DESCRIPTION

The Intelligent Access™ voice chipsets integrate all functions of the subscriber line for four subscriber lines. One or more of two chip types are used to implement the linecard; an ISLIC device and a Quad ISLAC device. These provide the following basic functions:

1. The ISLIC device: A high voltage, bipolar IC that drives the subscriber line, maintains longitudinal balance and senses line conditions.
2. The Quad ISLAC device: A low voltage CMOS IC that provides conversion and DSP functions for all 4 channels.

Complete schematics of linecards using the Intelligent Access voice chipsets for internal and external ringing are shown in “Application Circuits” on page 26.

The ISLIC device uses reliable, bipolar technology to provide the power necessary to drive a wide variety of subscriber lines. It can be programmed by the ISLAC device to operate in eight different modes that control power consumption and signaling modes. This enables it to have full control over the subscriber loop. The ISLIC device is designed to be used exclusively with the ISLAC device as part of a multiple-line chipset. The ISLIC device requires only +5 V power and the battery supplies for its operation.

The ISLIC device implements a linear loop-current feeding method with the enhancement of intelligent thermal management in a controlled manner. This limits the amount of power dissipated on the ISLIC chip by dissipating excess power in external resistors.

Each ISLAC device contains high-performance codec circuits that provide A/D and D/A conversion for voice (codec), DC-feed and supervision signals for four subscriber channels. The ISLAC device contains a DSP core that handles signaling, DC-feed, supervision and line diagnostics for all four channels.

The DSP core selectively interfaces with three types of backplanes:

- Standard PCM/MPI
- Standard GCI
- Modified GCI with a single analog line per GCI channel

The Intelligent Access voice chipset provides a complete software configurable solution to the BORSCHT functions as well as complete programmable control over subscriber line DC-feed characteristics, such as current limit and feed resistance. In addition, these chipsets provide system level solutions for the loop supervisory functions and metering. In total, they provide a programmable solution that can satisfy worldwide linecard requirements by software configuration.

Software programmed filter coefficients, DC-feed data and supervision data are easily calculated with the WinSLAC™ software. This PC software is provided free of charge. It allows the designer to enter a description of system requirements. WinSLAC then computes the necessary coefficients and plots the predicted system results.

The ISLIC interface unit inside the ISLAC device processes information regarding the line voltages, loop currents and battery voltage levels. These inputs allow the ISLAC device to place several key ISLIC performance parameters under software control.

The main functions that can be observed and/or controlled through the ISLAC backplane interface are:

- DC-feed characteristics
- Ground-key detection
- Off-hook detection
- Metering signal
- Longitudinal operating point
- Subscriber line voltage and currents
- Ring-trip detection
- Abrupt and smooth battery reversal
- Subscriber line matching
- Ringing generation
- Sophisticated line and circuit tests

To accomplish these functions, the ISLIC device collects the following information and feeds it, in analog form, to the ISLAC device:

- The metallic (IMT) and longitudinal (ILG) loop currents
- The AC (VTX) and DC (VSAB) loop voltages
- The outputs supplied by the ISLAC device to the ISLIC device are then:
- A voltage (VHLi) that provides control for the following high-level ISLIC device outputs:
- DC loop current
- Internal ringing signal
- 12 or 16 kHz metering signal

- A low-level voltage proportional to the voice signal (VOUTi)
- A voltage that controls longitudinal offset for test purposes (VLBi)

The ISLAC device performs the codec and filter functions associated with the four-wire section of the subscriber line circuitry in a digital switch. These functions involve converting an analog voice signal into digital PCM samples and converting digital PCM samples back into an analog signal. During conversion, digital filters are used to band-limit the voice signals.

The user-programmable filters set the receive and transmit gain, perform the transhybrid balancing function, permit adjustment of the two-wire termination impedance and provide frequency attenuation adjustment (equalization) of the receive and transmit paths. Adaptive transhybrid balancing is also included. All programmable digital filter coefficients can be calculated using WinSLAC software. The PCM codes can be either 16-bit linear two's-complement or 8-bit companded A-law or µ-law.

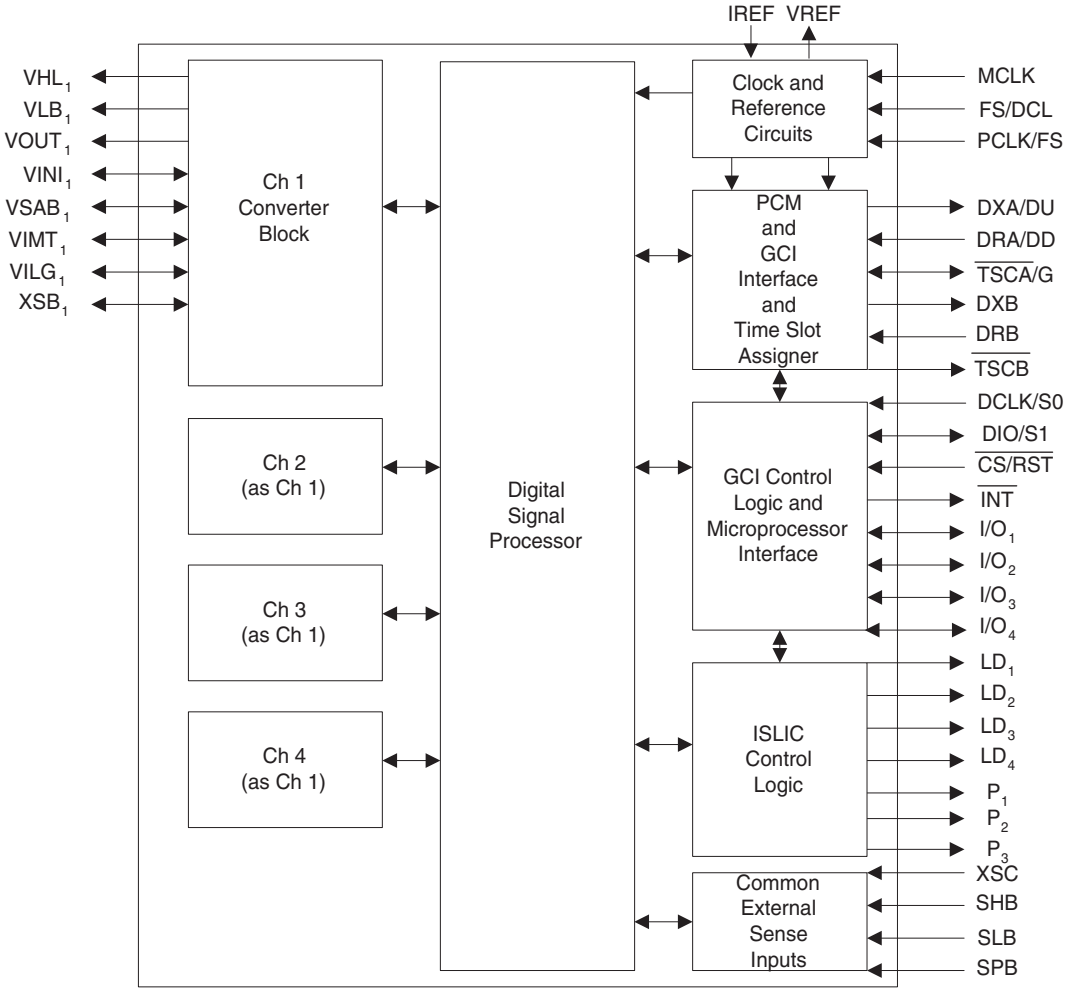
Besides the codec functions, the Intelligent Access voice chipset provides all the sensing, feedback, and clocking necessary to completely control ISLIC device functions with programmable parameters. System-level parameters under programmable control include active loop current limits, feed resistance, and feed mode voltages.

The ISLAC device supplies complete mode control to the ISLIC device using the control bus and (P1-P3) tri-level load signal (LDi).

The Intelligent Access voice chipset provides extensive loop supervision capability including off-hook, ring-trip and ground-key detection. Detection thresholds for these functions are programmable. A programmable debounce timer is available that eliminates false detection due to contact bounce.

For subscriber line diagnostics, AC and DC line conditions can be monitored using built in test tools. Measured parameters can be compared to programmed threshold levels to set a pass/fail bit. The user can choose to send the actual PCM measurement data directly to a higher level processor by way of the voice channel. Both longitudinal and metallic resistance and capacitance can be measured, which allows leakage resistance, line capacitance, and telephones to be identified.

## Quad ISLAC™ Device Internal Block Diagram



## Features of the Intelligent Access™ Chipset

- Performs all battery feed, ringing, signaling, hybrid and test (BORSCHT) functions
- Two chip solution supports high density, multi-channel architecture
- Single hardware design meets multiple country requirements through software programming of:
  - Ringing waveform and frequency
  - DC loop-feed characteristics and current-limit
  - Loop-supervision detection thresholds
    - Off-hook debounce circuit
    - Ground-key and ring-trip filters
  - Off-hook detect de-bounce interval
  - Two-wire AC impedance
  - Transhybrid balance
  - Transmit and receive gains
  - Equalization
  - Digital I/O pins
  - A-law/µ-law and linear selection
- Supports internal and external battery-backed ringing
  - Self-contained ringing generation and control
  - Supports external ringing generator and ring relay
  - Ring relay operation synchronized to zero crossings of ringing voltage and current
  - Integrated ring-trip filter and software enabled manual or automatic ring-trip mode
- Supports metering generation with envelope shaping
- Smooth or abrupt polarity reversal
- Adaptive transhybrid balance
  - Continuous or adapt and freeze
- Supports both loop-start and ground-start signaling
- Exceeds LSSGR and CCITT central office requirements
- Selectable PCM or GCI interface
  - Supports most available master clock frequencies from 512 kHz to 8.192 MHz
- On-hook transmission
- Power/service denial mode
- Line-feed characteristics independent of battery voltage
- Only 5 V, 3.3 V and battery supplies needed
- Low idle-power per line
- Linear power-feed with intelligent power-management feature
- Compatible with inexpensive protection networks; Accommodates low-tolerance fuse resistors while maintaining longitudinal balance
- Monitors two-wire interface voltages and currents for subscriber line diagnostics
- Built-in voice-path test modes
- Power-cross, fault, and foreign voltage detection
- Integrated line-test features
  - Leakage
  - Line and ringer capacitance
  - Loop resistance
- Integrated self-test features
  - Echo gain, distortion, and noise
- Small physical size
- Up to three relay drivers per ISLIC™ device
  - Configurable as test load switches

## CONNECTION DIAGRAMS

**Figure 1. 68-Pin PLCC Connection Diagram**

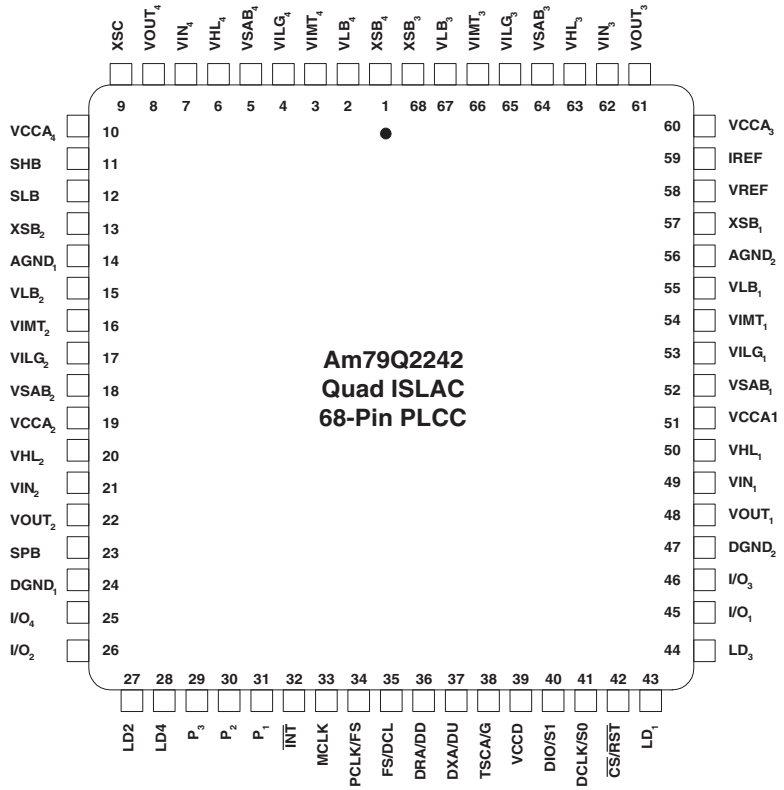



**Figure 2. 64-Pin TQFP Connection Diagram**

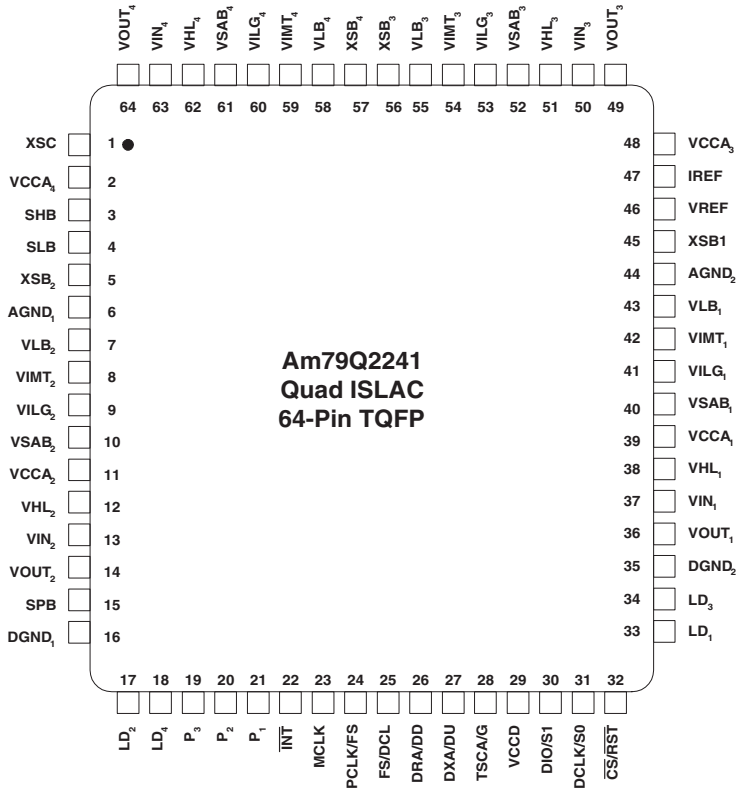
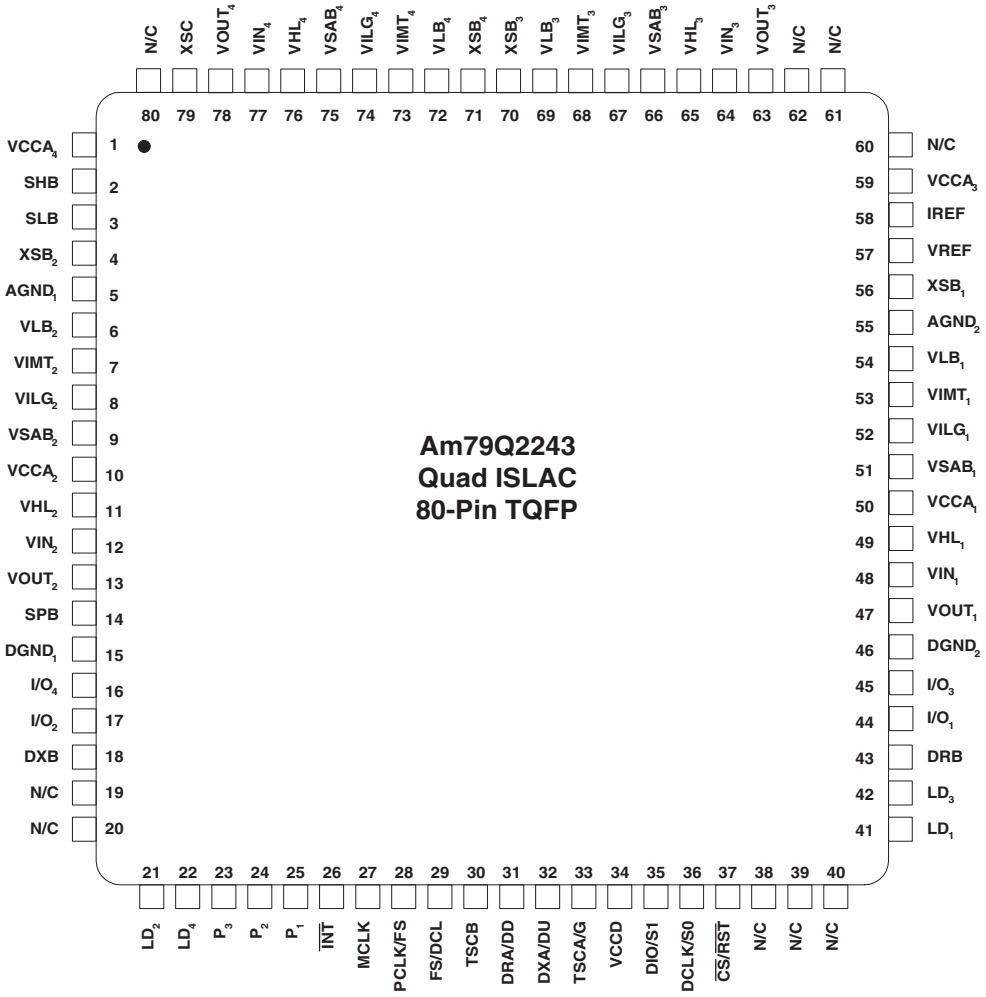


**Figure 3. 80-Pin TQFP Connection Diagram**



## PIN DESCRIPTIONS

| Pin | Pin Name | I/O | Description |
|---|---|---|---|
| $AGND_1$, $AGND_2$ | Analog Ground | | Analog circuitry ground returns |
| DCLK/S0 | Data Clock/GCI Address Strap 0 | I | Provides data control for MPI interface control. For GCI operation, this pin is device address bit 0.5 V tolerant. |
| $DGND_1$, $DGND_2$ | Digital Ground | | Digital ground returns |
| DIO/S1 | Data I/O/GCI Address Strap 1 | I/O | For PCM backplane operation, control data is serially written into and read out of the ISLAC device via the DIO pin with the MSB first. The data clock (DCLK) determines the data rate. DIO is high impedance except when data is being transmitted from the ISLAC device under control of $\overline{CS}$/$\overline{RST}$. For GCI operation, this pin is device address bit 1. 5 V tolerant. |
| DRA/DD, DRB | RX Path A Backplane Data/ GCI data Downstream, Receive Path B backplane data | I | For the PCM highway, the receive PCM data is input serially through the DRA or DRB ports. The data input is received every 125 µs and is shifted in, MSB first, in 8-bit PCM or 16-bit linear bursts at the PCLK rate. The receive port can receive information for direct control of the ISLIC device. This mode is selected in Device Configuration Register 2 (RTSEN=1, RTSMD=1). When selected, this data is received in an independently programmable timeslot from the PCM data. For the GCI mode, downstream receive and control data is accepted on this pin. The DRB pin is available only on the 80-pin TQFP package. 5 V tolerant. |
| DXA/DU, DXB | TX Path A Backplane Data/ GCI Data Upstream, TX Path B Backplane Data | O | For the PCM highway, the transmit PCM data is transmitted serially through the DXA or DXB ports. The transmission data output is available every 125 µs and is shifted out, MSB first, in 8-bit PCM or 16-bit linear bursts at the PCLK rate. DXA and DXB are high impedance between bursts and while the device is in the inactive mode. Can also select a mode (RTSEN= 1, RTSMD=1 or 0 in Device Configuration Register 2) that transmits the Signaling Register MSB contents first, in an independently programmable timeslot from the PCM data. This data is transmitted in all modes except disconnect. For the GCI mode, upstream transmit and signaling data is transferred on this pin. The DXB pin is available only on the 80-pin TQFP package. 5 V tolerant. |
| FS/DCL | Frame sync/GCI Downstream Clock | I | For PCM operation, pin is Frame Sync. PCM operation is selected by the presence of an 8 kHz Frame Sync signal on this pin in conjunction with the PCLK on the PCLK/FS pin (see below). This 8 kHz pulse identifies the beginning of a frame. The ISLAC device references individual timeslots with respect to this input, which must be synchronized to PCLK. GCI operation is selected by the presence of the downstream clock DCL, on this pin in conjunction with the presence of a FS on the PCLK/FS pin. In GCI mode, the data rate is 2 MHz and DCL must be either 2 or 4 MHz. 5 V tolerant. |
| INT | Interrupt | O | For PCM operation, when a subscriber line requires service, this pin goes to a logic 0 to interrupt a higher level processor. Several registers work together to control operation of the interrupt: Signaling and Global Interrupt Registers with their associated Mask Registers, and the Interrupt Register. See the description at channel configuration register 6 (Mask) for operation. Logic drive is selectable between open drain and TTL-compatible outputs. |
| $I/O_1$–$I/O_4$ | Control Ports | I/O | General purpose, TTL-compatible, logic input/output connection for each of 4 channels. These control lines are TTL-compatible and each can be programmed as an input or output in the Global I/O Direction Register. When programmed as outputs, they can control an external logic device. When programmed as inputs, they can monitor external, TTL-compatible logic circuits. Data for these pins can be written or read individually (from the channel specific I/O Register) or as a group (from the Global I/O Data Register). Not available on the 64-pin package. |
| IREF | Current Reference | I | External resistor (RREF) connected between this pin and analog ground generates an accurate, on-chip reference current for the A/D's and D/A's on the ISLAC chip. |
| $LD_1$–$LD_4$ | Register Load | O | The LD pins output 3-level voltages. When $LD_n$ is a logic 0 (< 0.4 V), the destination of the code on $P_1$–$P_3$ is the relay control latches in the ISLIC control register. When $LD_n$ is a logic 1 (>$V_{CC}$–0.4 V), the destination of $P_1$–$P_3$ is the mode control latches. $LD_n$ is driven to VREF when the contents of the ISLIC control register must not change. |

| Pin | Pin Name | I/O | Description |
|---|---|---|---|
| MCLK | Master Clock | I | For PCM backplane operation, the DSP master clock connects here. A signal is required only for PCM backplane operation when PCLK is not used as the master clock. MCLK can be a wide variety of frequencies. Upon initialization the MCLK input is disabled, and relevant circuitry is driven by a connection to PCLK. 5 V tolerant. |
| PCLK/FS | PCM Clock/ Frame Sync | I | For PCM operation, this is PCM Clock. PCM operation is selected by the presence of a PCLK signal on this pin in conjunction with the FS on the FS/DCL pin (see below). For PCM backplane operation, connect a data clock, which determines the rate at which PCM data is serially shifted into or out of the PCM ports. PCLK can be any multiple of the FS frequency. The minimum clock frequency for linear/ companded data plus signaling data is 256 kHz. For GCI operation, this pin is Frame Sync. The FS signal is an 8 kHz pulse that identifies the beginning of a frame. The ISLAC device references individual timeslots with respect to this input, which must be synchronized to DCL. 5 V tolerant. |
| $P_1$–$P_3$ | ISLIC Control | O | Control the operating modes of the four ISLIC devices connected to the Quad ISLAC device. |
| $\overline{CS}/\overline{RST}$ | Chip Select/ Reset | I | For PCM backplane operation, a logic low on this pin for 16 or more DCLK cycles resets the sequential logic in the ISLAC device into a known mode. A logic low placed on this pin for less than 15 DCLK cycles is a chip select and enables serial data transmission into or out of the DIO port. For GCI operation, a logic low on this pin for 1 ms or longer resets the sequential logic into a known mode. See Table 2-4 in the Technical Reference for details. 5 V tolerant. |
| SHB, SLB, SPB | Battery Sense | I | Resistors that sense the high, low and positive battery voltages connect here. If only one negative battery is used, connect both resistors at the supply. If the positive battery is not used, leave the pin unconnected. These pins are current inputs whose voltage is held at VREF. |
| $\overline{TSCA}$/G | Timeslot Control A/GCI Mode | O (PCM) I (GCI) | For PCM backplane operation, $\overline{TSCA}$ or $\overline{TSCB}$ is active low when PCM data is output on the DXA or DXB pins. The outputs are open-drain and are normally inactive (high impedance). Pull-up loads should be connected to VCCD. $\overline{TSCB}$ is only available on the 80 pin TQFP package. When GCI mode is selected, one of two GCI modes may be selected by connecting $\overline{TSCA}$/G to DGND or VCCD. |
| $\overline{TSCB}$ | Time Slot Control B | O | |
| $VSAB_1$–$VSAB_4$ | Loop voltage sense | I | Connect to the VSAB pins of four ISLIC devices. |
| $VCCA_1$–$VCCA_4$ | Power Supply | | +3.3 VDC supplies to the analog sections in each of the four channels. |
| VCCD | Power Supply | | +3.3 VDC supply to all digital sections. |
| VREF | Analog Reference | O | This pin provides a 1.4 V, single-ended reference to the four ISLIC devices to which the ISLAC device is connected. |
| $VHL_1$–$VHL_4$ | High Level D/A | O | High-level loop control voltages on these pins are used to control DC-feed, internal ringing, metering and polarity reversal for each ISLIC device. |
| $VIN_1$–$VIN_4$ | TX Analog | I | Analog transmit signals (VTX) from each ISLIC device connect to these pins. The ISLAC device converts these signals to digital words and processes them. After processing, they are multiplexed into serial time slots and sent out of the DXA/DU pin. |
| $VLB_1$–$VLB_4$ | Longitudinal Reference | O | Normally connected to VCCA internally. They supply longitudinal reference voltages to the ISLIC devices during certain test procedures. These outputs are connected internally to VCCA during ISLIC Active, Standby, Ringing, and Disconnect modes. During test modes, it can be connected to the receive D/A. |

| Pin Options | Package Type | | |
|---|---|---|---|
| | 80 pin | 68 pin | 64 pin |
| DRB | √ | x | x |
| DXB | √ | x | x |
| TSCB | √ | x | x |
| $I/O_1$–$I/O_4$ | √ | √ | x |

# ELECTRICAL CHARACTERISTICS

## Absolute Maximum Ratings

Stresses greater than those listed under Absolute Maximum Ratings can cause permanent device failure. Functionality at or above these limits is not implied. Exposure to absolute maximum ratings for extended periods can affect device reliability

| | |
|---|---|
| Storage Temperature | –60º C ≤ $T_A$ ≤ +125º C |
| Ambient Temperature, under Bias | –40º C ≤ $T_A$ ≤ +85º C |
| Ambient relative humidity (non condensing) | 5 to 100% |
| $V_{CCA}$ with respect to DGND | –0.4 to + 3.6 V |
| $V_{CCD}$ with respect to DGND | –0.4 to + 3.6 V |
| $V_{IN}$ with respect to DGND | –0.4 to VCCA + 0.4 V |
| 5 V tolerant pins | –0.4 to Vcc + 2.25 or 5.25 V, whichever is less |
| AGND | DGND ± 0.4 V |
| Latch up immunity (any pin) | ±100 mA |
| Any other pin with respect to DGND | –0.4 V to $V_{CC}$ |

## Operating Ranges

Operating ranges define those limits between which device functionality is guaranteed. Functionality of the device from 0 to 70º C is guaranteed by production testing. Performance from –40 to 85ºC is guaranteed by characterization and periodic sampling of production units.

### Environmental Ranges

| | |
|---|---|
| Ambient Temperature | –40 to +85º C |
| Ambient Relative Humidity | 15 to 85% |

### Electrical Ranges

| | |
|---|---|
| Analog Supply $V_{CCA}$ | +3.3 V ± 5% |
| Digital Supply $V_{CCD}$ | +3.3 V ± 5% |
| DGND | 0 V |
| AGND | DGND ±50 mV |

# SPECIFICATIONS

The performance targets defined in this section are for the entire linecard comprised of both chips in the Intelligent Access voice chipsets unless otherwise noted. Specifications for the individual chips in the set will be published separately (see note 1). $T_A$ = 0 to 70º C unless otherwise noted.

## Intelligent Access Voice Chipsets System Target Specifications

| Item | Condition | Min | Typ | Max | Unit | Note |
|---|---|---|---|---|---|---|
| Peak Ringing Voltage | Active Ringing mode, RLOAD =1500 Ω, VBH = 80 V | | 70 | | V | |
| Output Impedance during internal ringing | Active Ringing mode, Quad ISLAC generating internal ringing | | 200 | | Ω | |
| Sinusoidal Ringing THD | Active Ringing mode, RLOAD =1500Ω, VBH = 80V, ISLAC generating internal sinusoidal ringing | | 2 | | % | |
| PSRR (VBH, VBL) | Loop open, in anti-sat | | | | dB | 1, 2 |
| | f = 50 Hz | 2 | | | | |
| | f = 200 to 3400 Hz | 12 | | | | |

***Note:***

1. *Not tested or partially-tested in production.*
2. *These numbers are only valid when an ISLIC device operates with an ISLAC device, because the ISLAC generates the anti-sat feed characteristic. When the Intelligent Access voice chipsets operate in the normal feed region, the performance is dominated by the ISLIC device. See appropriate ISLIC data sheet for specific PSRR.*

## DC Specifications

| No. | Item | Condition | Min | Typ | Max | Unit | Note |
|---|---|---|---|---|---|---|---|
| 1 | Input Low Voltage, $I/O_1$–$I/O_4$ | | –0.05 | | 1.36 V | V | |
| | All other digital inputs | | –0.50 | | 0.80 V | | |
| 2 | Input High Voltage, $I/O_1$–$I/O_4$ | | 2.36 | | Vcc+0.4 | | |
| | All other digital inputs | | 2.0 | | 5.25 | | |
| 4 | Input Leakage Current, $I/O_1$–$I/O_4$ | 0 to $V_{CC}$ | –10 | | +10 | µA | |
| | All other digital inputs | 0 to 5.25 V | –120 | | +180 | | |
| 5 | Input hysteresis (PCLK/FS, FS/DCL, MCLK, DIO, DRA, DRB) | | .15 | .225 | .3 | V | 2 |
| | I/O1–I/O4 | | .16 | .25 | .34 | | |
| 6 | Ternary output voltages, $LD_1$–$LD_4$ | | | | | | |
| | High voltage | Iout = 1 mA | VCC–.4 | | — | | |
| | Low voltage | Iout = 2 mA | — | | 0.4 | | |
| | Medium voltage | ±10 µA | | VREF | | | |
| 7 | Output Low Voltage (DXA/DU, DIO, $I/O_1$–$I/O_4$, $\overline{INT}$, $\overline{TSCA}$, $\overline{TSCB}$, DXB, $P_1$-$P_3$) | Iol = 1 mA | | | 0.4 | V | |
| 8 | Output Low Voltage ($I/O_1$ –$I/O_4$, $\overline{INT}$, $\overline{TSCA}$, $\overline{TSCB}$) | Iol = 10 mA | | | 1.0 | | |
| 9 | Output High Voltage (All digital outputs except $\overline{INT}$ in open drain mode and $\overline{TSCA}$, $\overline{TSCB}$) | Ioh = 400 µA | VCC–0.4 | | | | |
| 10 | Input Leakage Current ($VIN_1$–$VIN_4$, $VSAB_1$–$VSAB_4$, $VILG_1$–$VILG_4$, $VIMT_1$–$VIMT_4$) | | –1 | 0.2 | 1 | µA | |
| 12 | Input voltage ($VIN_1$–$VIN_4$) | | | | | V | |
| | µ-law | 3.205 dBm0 | VREF | | VREF | | |
| | A-law | 3.14 dBm0 to insertion loss in ADC | –1.02 | | +1.02 | | |
| 13 | Input Voltage ($VSAB_1$–$VSAB_4$ or $VIMT_1$–$VIMT_4$ or $VILG_1$–$VILG_4$) | \|Vov–VREF\| where Vov is input overload voltage | 0.99 | 1.02 | 1.05 | | |
| 14 | Offset voltage allowed on $VIN_1$–$VIN_4$ | | –50 | | +50 | mV | 4 |
| 15 | $VOUT_1$–$VOUT_4$ offset Voltage | DISN off | –40 | | +40 | | |
| | | DISN on | –80 | | +80 | | |
| 16 | VHL output offset voltage | | | TBD | | | |
| 17 | Output voltage, VREF | Load current = 0 to 10 mA | | 1.4 | | V | |
| | | Source or Sink | | | | | |
| 18 | Capacitance load on VREF or $VOUT_1$–$VOUT_4$ | | | | 200 | pF | 2 |
| 19 | Output drive current, $VOUT_1$–$VOUT_4$ or $VLB_1$–$VLB_4$ | Source or Sink | –1 | | +1 | mA | 2 |
| 20 | Output Leakage Current $VOUT_1$–$VOUT_4$ or $VLB_1$–$VLB_4$ | | 500 | 200 | 500 | nA | |

| No. | Item | Condition | Min | Typ | Max | Unit | Note |
|---|---|---|---|---|---|---|---|
| 21 | Maximum output voltage on VOUT | \|VOUT–VREF\| with peak digital input | 0.99 | 1.02 | 1.05 | V | 8 |
| 22 | $VLB_1$–$VLB_4$ operating voltage | Source current < 250µA or | VREF | | VREF | | |
| | | Sink current < 25 µA. | –1.02 | | +1.02 | | |
| 23 | Maximum output voltage on VHL (KRFB) | \|VHL–VREF\| with peak digital input | 0.97 | 1.00 | 1.03 | | 8 |
| 24 | Gain from VSAB to VHL | VFD = 1 | 4.9 | 5 | 5.1 | V/V | |
| 25 | Gain from VSAB to VHL | VFD = 0 | –.0255 | –.025 | –.0245 | V/V | |
| 26 | % error of VLB voltage (For VLB equation, see *Am79R2xx/ Am79Q224x Technical Reference*) | | –5 | | +5 | % | |
| 27 | Capacitance load on $VLB_1$–$VLB_4$ | | | | 120 | pF | 2 |
| 28 | Capacitance load on $XSB_1$–$XSB_4$, XSC | | | | 400 | | 2 |
| 29 | Quad ISLAC Power Dissipation | One channel active (ISLIC state register set to active); three channels inactive (ISLIC state register set to standby) | | 183 | 235 | mW | |
| | | All channels active (ISLIC state register set to active) | | 264 | 340 | | |
| | | All channels inactive (ISLIC state register set to standby) | | 143 | 188 | | |

## Transmission and Signaling Specifications

### Table 1. 0 dBm0 Voltage Definitions with Unity Gain in X, R, GX, GR, AX, and AR

| Signal at Digital Interface | Transmit | Receive | Unit |
|---|---|---|---|
| A-law digital mW or equivalent (0 dBm0) | 0.5026 | 0.5026 | Vrms |
| µ-law digital mW or equivalent (0 dBm0) | 0.4987 | 0.4987 | |
| ±5,800 peak linear coded sine wave | 0.5026 | 0.5025 | |

| No. | Item | Condition | Min | Typ | Max | Unit | Note |
|---|---|---|---|---|---|---|---|
| 1 | Insertion Loss A-D | Input: 1014Hz, –10dBm0 AR = AX = GR = GX = 0 dB, DISN, R, X, B and Z disabled | –0.25 | 0 | +0.25 | dB | 3, 8 |
| | D-A | | | | | | |
| | A-D + D-A | Temperature = 70°C | –0.15 | 0 | +0.15 | | |
| | A-D – D-A | Variation over temperature | –0.1 | 0 | +0.1 | | |
| 2 | Level set error (Error between setting and actual value) | A-D AX + GX D-A AR + GR | –0.1 | | 0.1 | | |
| 3 | DR to DX gain in full digital loopback mode | DR Input: 1014 Hz, –10 dBm0 AR=AX=GR=GX=0 dB, DISN, R, X, B and Z filters default | –0.3 | | +0.3 | | |
| 4 | Idle Channel Noise, Psophometric Weighted (A-law) | A-D (PCM output) | | | –69 | dBm0p | 5 |
| | | D-A ($V_{OUT}$) | | | –78 | | |
| 5 | Idle Channel Noise, C Message weighted (µ-law) | A-D (PCM output) | | | +19 | dBrnC0 | |
| | | D-A ($V_{OUT}$ | | | +12 | | |
| 6 | Coder Offset decision value, Xn | A-D, Input signal = 0 V | –7 | | +7 | Bits | 2 |

| No. | Item | Condition | Min | Typ | Max | Unit | Note |
|---|---|---|---|---|---|---|---|
| 7 | PSRR (VCC) A-D | Input: 4.8 to 7.8 kHz, 200 mV p-p | 37 | | | dB | 1 |
| | Image frequency D-A | Measure 8000 Hz-Input frequency | | | | | |
| 8 | DISN gain accuracy | Gdisn = –0.9375 to 0.9375<br>Vin = 0 dBm0 | –0.25 | | +0.25 | dB | |
| 9 | End-to-end group delay | 1014Hz; –10dBm0<br>B = Z = 0; X = R = 1 | | | 525 | µS | 2, 6, 7 |
| 10 | Crosstalk TX to RX | 0 dBm0 300 Hz to 3400 Hz | | | –75 | dBm0 | 2 |
| | same channel RX to TX | 0 dBm0 300 Hz to 3400 Hz | | | | | |
| 11 | Crosstalk TX or RX to TX | 0 dBm0 1014 Hz | | | –76 | dBm0 | 2 |
| | Crosstalk TX or RX to RX | 0 dBm0 1014 Hz | | | –78 | | |

1. *Not tested or partially tested in production. This parameter is guaranteed by characterization or correlation to other tests.*
2. *Guaranteed by design.*
3. *Overall 1.014 kHz insertion loss error of the Intelligent Access voice chipset is guaranteed to be 0.34 dB*
4. *These voltages are referred to VREF.*
5. *When relative levels (dBm0) are used, the specification holds for any setting of (AX + GX) gain from 0 to 12 dB or (AR + GR) from 0 to –12 dB.*
6. *Group delay spec valid only when Channels 1–4 occupy consecutive slots in the frame. Programming channels in non-consecutive timeslots can add up to 1 frame delay in the Group delay measurements.*
7. *The Group delay specification is defined as the sum of the minimum values of the group delays for transmit and the receive paths when the B, X, R, and Z filters are disabled with null coefficients. See Figure 8 for Group Delay Distortion.*
8. *Requires that the calibration command (7Ch) must be performed to achieve this performance.*

## Transmit and Receive Paths

In this section, the transmit path is defined as the analog input to the ISLAC device ($VIN_n$) to the PCM voice output of the ISLAC A-law/µ-law speech compressor. The receive path is defined as the PCM voice input to the ISLAC speech expander to the analog output of the ISLAC device ($VOUT_n$). All limits defined in this section are tested with B = 0, Z = 0 and X = R = GR = 1.

When AR is enabled, a nominal gain of –6.02 dB is added to the analog section of the receive path.

When AX is enabled, a nominal gain of +6.02 dB is added to the analog section of the transmit path.

When relative levels (dBm0) are used in any of the following transmission characteristics, the specification holds for any setting of (AX + GX) gain from 0 to 12 dB or (AR + GR) from 0 to –12 dB.

These transmission characteristics are valid for 0 to 70$^{o}$ C.

## Attenuation Distortion

The attenuation of the signal in either path is nominally independent of the frequency. The deviations from nominal attenuation will stay within the limits shown in Figure 4 and Figure 5. The reference frequency is 1014 Hz and the signal level is –10 dBm0. The minimum transmit attenuation at 60 Hz is 24 dB.

**Figure 4. Transmit Path Attenuation vs. Frequency**

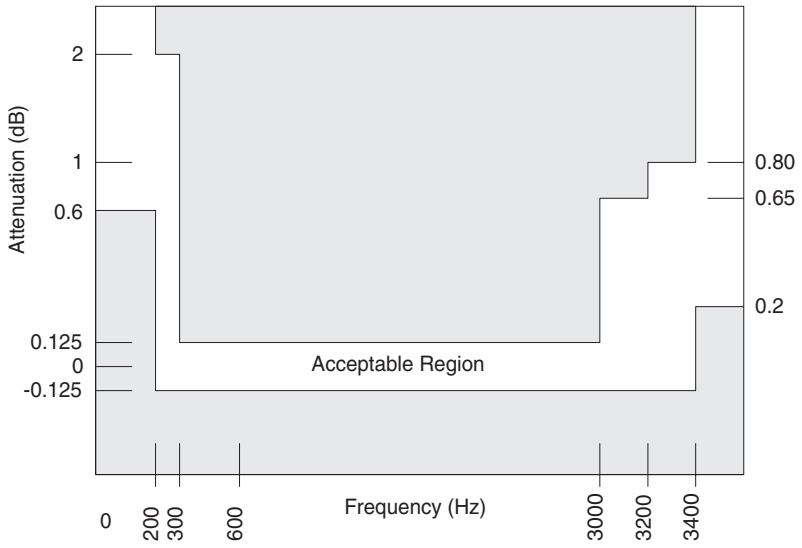
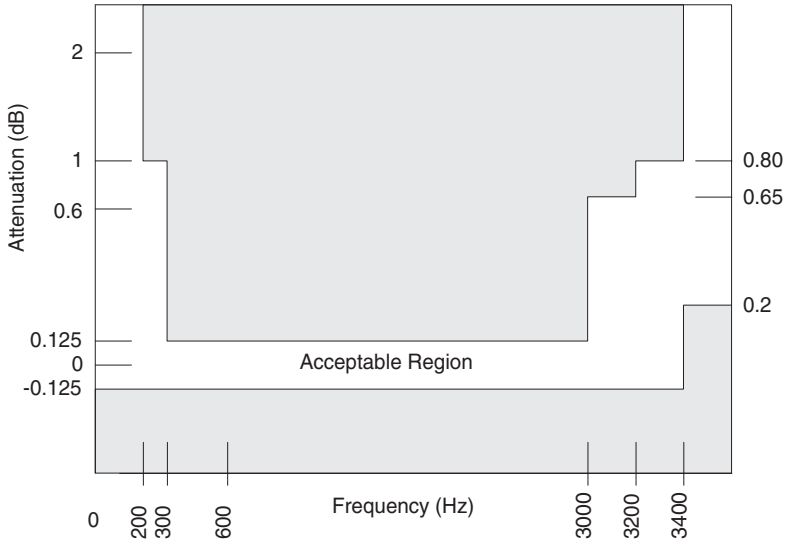


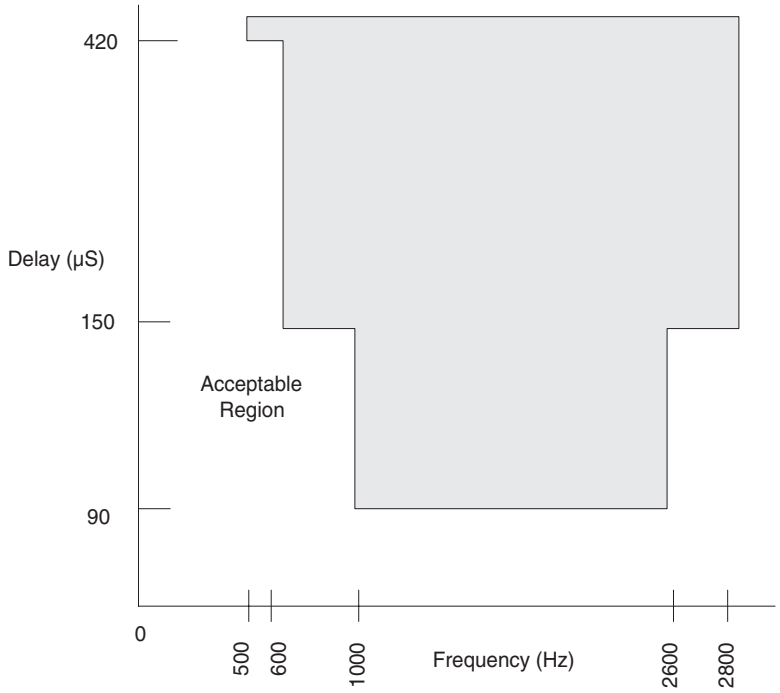

**Figure 5. Receive Path Attenuation vs. Frequency**



## Group Delay Distortion

For either transmission path, the group delay distortion is within the limits shown in Figure 6. The minimum value of the group delay is taken as the reference. The signal level is –10 dBm0.

**Figure 6. Group Delay Distortion**




## Single Frequency Distortion

The output signal level, at any single frequency in the range of 300 to 3400 Hz, other than that due to an applied 0 dBm0 sine wave signal with frequency f in the same frequency range, is less than –46 dBm0. With f swept between 0 to 300 Hz and 3.4 to 12 kHz, any generated output signals other than f are less than –28 dBm0. This specification is valid for either transmission path.

## Intermodulation Distortion

TBD

## Gain Linearity

The gain deviation relative to the gain at –10 dBm0 is within the limits shown in Figure 7 (A-law) and Figure 8 (μ-law) for either transmission path when the input is a sine wave signal of 1014 Hz.

**Figure 7. A-law Gain Linearity with Tone Input (Both Paths)**

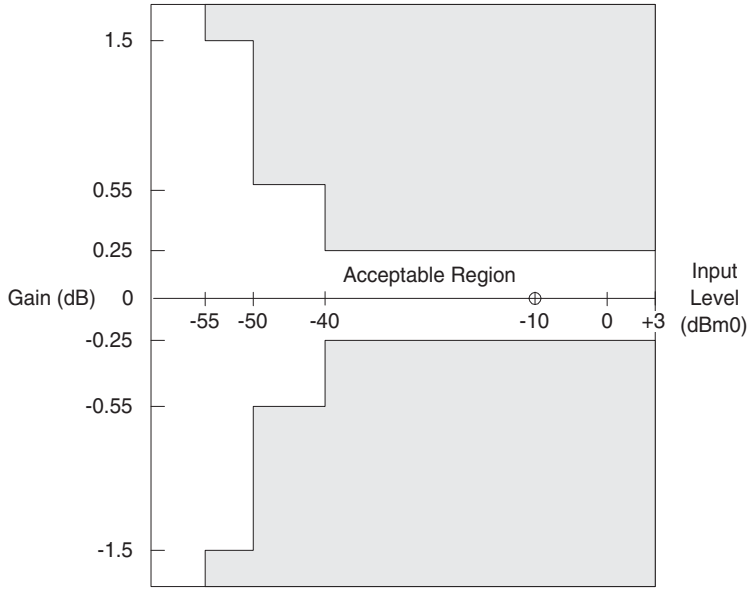
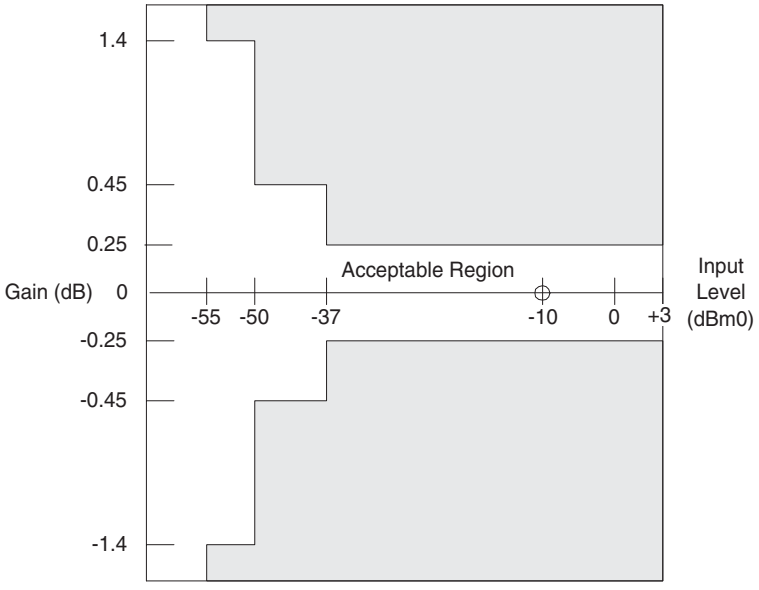


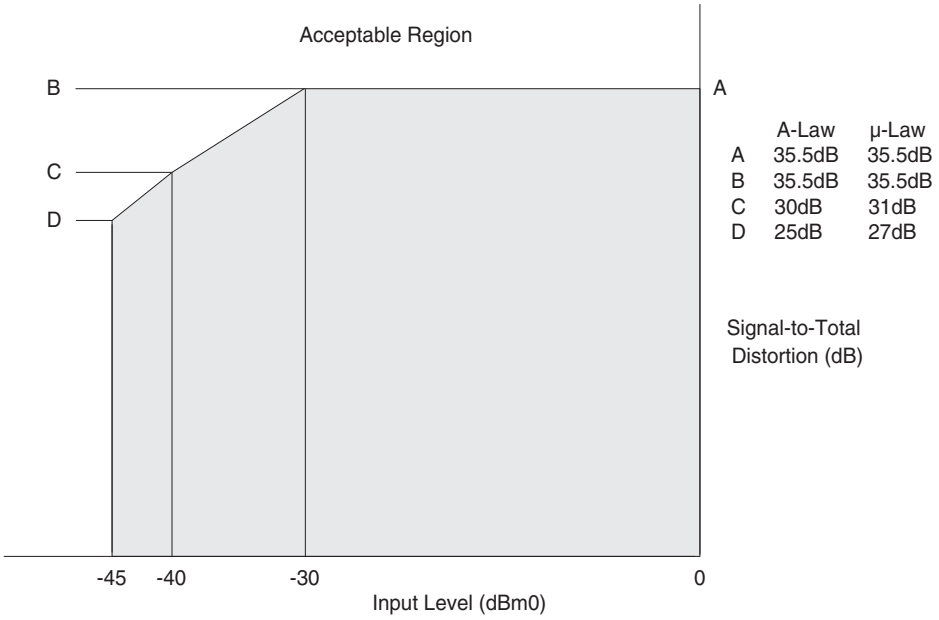

**Figure 8. μ-law Gain Linearity with Tone Input (Both Paths)**



## Total Distortion Including Quantizing Distortion

The signal to total distortion ratio will exceed the limits shown in Figure 9 for either path when the input signal is a sine wave signal of frequency 1014 Hz.

**Figure 9. Total Distortion with Tone Input, Both Paths**

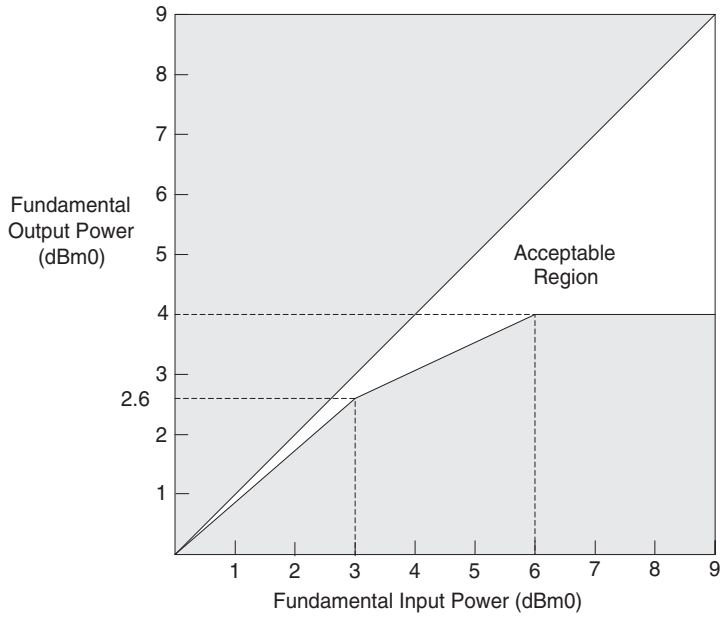



## Overload Compression

Figure 10 shows the acceptable region of operation for input signal levels above the reference input power (0 dBm0). The conditions for this figure are:

(1) 1 dB < GX ≤ +12 dB; (2) –12 dB ≤ GR < –1 dB; (3) Digital voice output connected to digital voice input; and (4) measurement analog to analog.

**Figure 10. A/A Overload Compression**



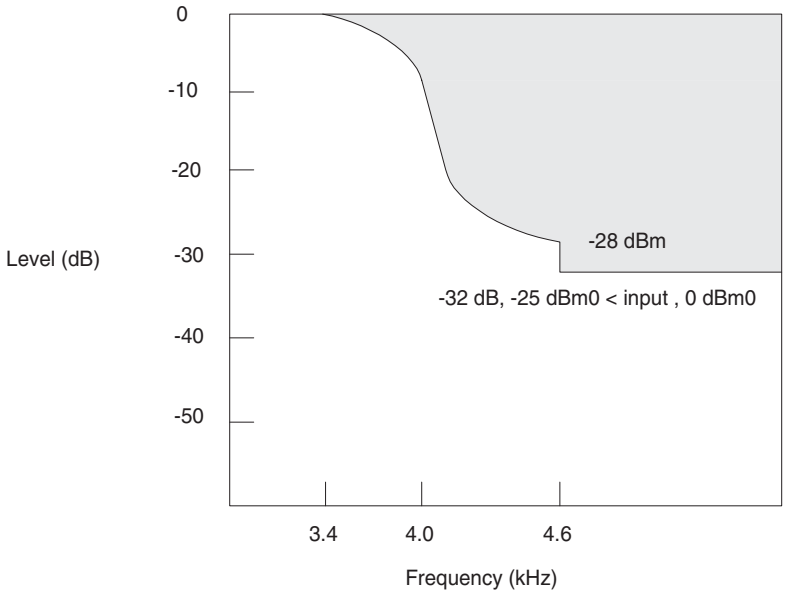
## Discrimination Against Out-of-Band Input Signals

When an out-of-band sine wave signal with frequency and level A is applied to the analog input, there may be frequency components below 4 kHz at the digital output which are caused by the out-of-band signal. These components are at least the specified dB level below the level of a signal at the same output originating from a 1014 Hz sine wave signal with a level of A dBm0 also applied to the analog input. The minimum specifications are shown in the following table

**Table 2. Minimum Specifications for Out-of-Band Input Signals**

| Frequency of Out-of-Band Signal | Amplitude of Out-of-Band Signal | Level below A |
|---|---|---|
| 16.6 Hz < f < 45 Hz | –25 dBm0 < A ≤ 0 dBm0 | 18 dB |
| 45 Hz < f < 65 Hz | –25 dBm0 < A ≤ 0 dBm0 | 25 dB |
| 65 Hz < f < 100 Hz | –25 dBm0 < A ≤ 0 dBm0 | 10 dB |
| 3400 Hz < f < 4600 Hz | –25 dBm0 < A ≤ 0 dBm0 | see Figure 11 |
| 4600 Hz < f < 100 kHz | –25 dBm0 < A ≤ 0 dBm0 | 32 dB |

**Figure 11. Discrimination Against Out-of-Band Signals**




***Note:***

*The attenuation of the waveform below amplitude A between 3400 Hz and 4600 Hz is given by the formula:*

$$\text{Attenuation (db)} = 14 - 14\sin\frac{\pi(4000 - f)}{1200}$$

## Spurious Out-of-Band Signals at the Analog Output

With PCM code words representing a sine wave signal in the range of 300 Hz to 3400 Hz at a level of 0 dBm0 applied to the digital input, the level of the spurious out-of-band signals at the analog output is less than the limits shown below.

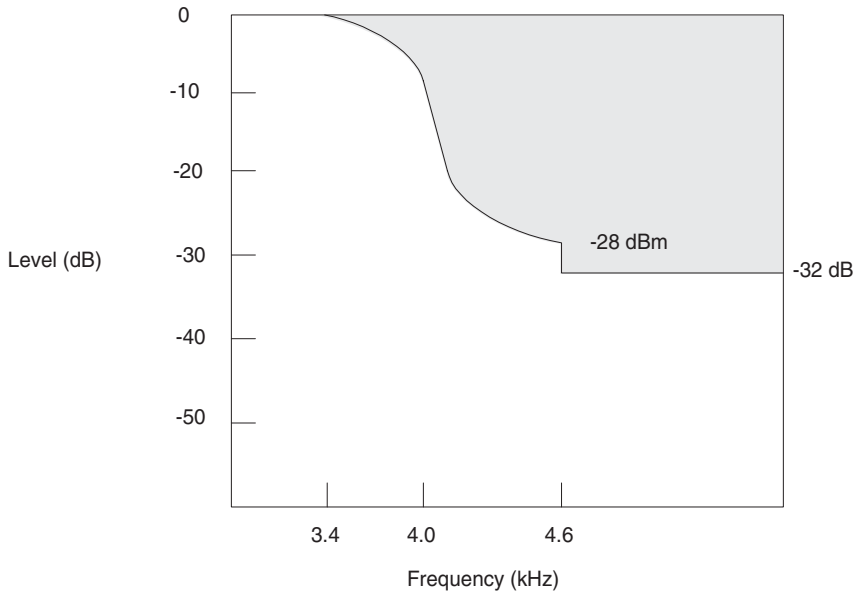
**Table 3. Limits for Spurious Out-of-Band Signals**

| Frequency | Level |
|---|---|
| 4.6 kHz to 40 kHz | –32 dBm0 |
| 40 kHz to 240 kHz | –46 dBm0 |
| 240 kHz to 1 MHz | –36 dBm0 |

With code words representing any sine wave signal in the range 3.4 kHz to 4.0 kHz at a level of 0 dBm0 applied to the digital input, the level of the signals at the analog output are below the limits in Figure 12. The amplitude of the spurious out-of-band signals between 3400 Hz and 4600 Hz is given by the formula:

$$A = -14 - 14\sin\frac{\pi(f - 4000)}{1200}\text{dBm0}$$

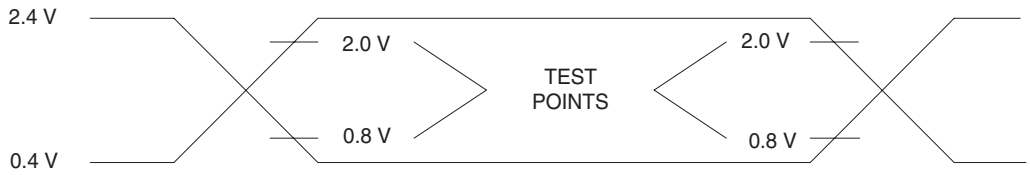
**Figure 12. Spurious Out-of-Band Signals**




## SWITCHING CHARACTERISTICS

### PCM Switching Characteristics

**Figure 13. PCM Switching Characteristics**




VCC = 3.3 V ±5%, AGND = DGND = 0 V.

### Microprocessor Interface

Min and max values are valid for all digital outputs with a 100 pF load, except DIO,DXA, $\overline{INT}$, TSCA, TSCB and DXB which are valid with 150 pF loads.

| No. | Symbol | Parameter | Min | Typ | Max | Unit | Note |
|---|---|---|---|---|---|---|---|
| 1 | $t_{DCY}$ | Data clock period | 122 | | | ns | |
| 2 | $t_{DCH}$ | Data clock HIGH pulse width | 48 | | | | 1 |
| 3 | $t_{DCL}$ | Data clock LOW pulse width | 48 | | | | 1 |
| 4 | $t_{DCR}$ | Rise time of clock | | | 15 | | |
| 5 | $t_{DCF}$ | Fall time of clock | | | 15 | | |
| 6 | $t_{ICSS}$ | Chip select setup time, Input mode | 30 | | $t_{DCY}$–10 | | |
| 7 | $t_{ICSH}$ | Chip select hold time, Input mode | 0 | | $t_{DCH}$–20 | | |
| 8 | $t_{ICSL}$ | Chip select pulse width, Input mode | | $7.5t_{DCY}$ | | | 7 |
| 9 | $t_{ICSO}$ | Chip select off time, Input mode | | | | | 1,6 |
| 10 | $t_{IDS}$ | Input data setup time | 25 | | | | 5 |
| 11 | $t_{IDH}$ | Input data hold time | 30 | | | | |
| 13 | $t_{OCSS}$ | Chip select setup time, Output mode | 30 | | $t_{DCY}$–10 | ns | |
| 14 | $t_{OCSH}$ | Chip select hold time, Output mode | | | $t_{DCH}$–20 | | |
| 15 | $t_{OCSL}$ | Chip select pulse width, Output mode | | $8t_{DCY}$ | | | |
| 16 | $t_{OCSO}$ | Chip select off time, output Mode | 2000 | | | | 1,6 |
| 17 | $t_{ODD}$ | Output data turn on delay | | | 50 | | |
| 18 | $t_{ODH}$ | Output data hold time | 3 | | | | |
| 19 | $t_{ODOF}$ | Output data turn off delay | | | 50 | | |
| 20 | $t_{ODC}$ | Output data valid | 0 | | 50 | | |

### PCM Interface

| No. | Symbol | Parameter | Min. | Typ | Max | Unit | Note |
|---|---|---|---|---|---|---|---|
| 22 | $t_{PCY}$ | PCM clock period | 0.122 | | 7.8125 | µs | 2 |
| 23 | $t_{PCH}$ | PCM clock HIGH pulse width | 48 | | | ns | |
| 24 | $t_{PCL}$ | PCM clock LOW pulse width | 48 | | | | |
| 25 | $t_{PCF}$ | Fall time of clock | | | 15 | | |
| 26 | $t_{PCR}$ | Rise time of clock | | | 15 | | |
| 27 | $t_{FSS}$ | FS setup time | 30 | | $t_{PCY}$–30 | | |
| 28 | $t_{FSH}$ | FS hold time | 50 | | | | |
| 29 | $t_{TSD}$ | Delay to $\overline{TSCX}$ valid | 5 | | 80 | | 3 |
| 30 | $t_{TSO}$ | Delay to $\overline{TSCX}$ off | 5 | | | | 4 |
| 31 | $t_{DXD}$ | PCM data output delay | 5 | | 70 | | |
| 32 | $t_{DXH}$ | PCM data output hold time | 5 | | 70 | | |
| 33 | $t_{DXZ}$ | PCM data output delay to high-Z | 10 | | 70 | | 4 |
| 34 | $t_{DRS}$ | PCM data input setup time | 25 | | | | |
| 35 | $t_{DRH}$ | PCM data input hold time | 5 | | | | |
| 36 | $t_{FST}$ | PCM or frame sync jitter time | –97 | | 97 | | |

**Master Clock**:

For a 2.048 mHz ± 100 PPM, 4.096 mHz ± 100 PPM, or 8.192 ± 100 PPM operation:

| No. | Symbol | Parameter | Min | Typ | Max | Unit | No |
|---|---|---|---|---|---|---|---|
| 37 | $t_{MCY}$ | Period | 122 | | 7812 | ns | 2,8 |
| 38 | $t_{MCR}$ | Rise time of clock | | | 15 | | |
| 39 | $t_{MCF}$ | Fall time of clock | | | 15 | | |
| 40 | $t_{MCH}$ | MCLK HIGH pulse width | 48 | | | | |
| 41 | $t_{MCL}$ | MCLK LOW pulse width | 48 | | | | |

***Note:***

1. *DCLK may be stopped in the HIGH or LOW state indefinitely without loss of information. When $\overline{CS}$ makes a transition to the High state, the last byte received will be interpreted by the Microprocessor Interface logic.*
2. *The PCM clock (PCLK) frequency must be an integer multiple of the frame sync (FS) frequency and synchronous to the MCLK frequency. The actual PCLK rate is dependent on the number of channels allocated within a frame. A PCLK of 1.544 mHz can be used for standard US transmission systems. The minimum clock frequency is 128 kHz.*
3. *$\overline{TSCA}$ is delayed from FS by a typical value of* N • $t_{PCY}$, *where N is the value stored in the time/clock slot register.*
4. *$t_{TSO}$ is defined as the delay time the output driver turns off after the PCLK transaction. The actual delay time is dependent on the load circuitry. The maximum load capacitance on $\overline{TSCX}$ is 150 pF and the minimum pull-up resistance is 360 Ω.*
5. *The first data bit is enabled on the falling edge of $\overline{CS}$ or on the falling edge of DCLK, whichever occurs last.*
6. *If the MPI is being accessed while the MCLK (or PCLK if combined with MCLK) input is not active, a Chip Select Off time of 20 µs is required when accessing coefficient RAM.*
7. *If chip select is held low for 16 or more DCLK cycles, the part will reset.*
8. *MCLK's frequency can range from 128 kHz to 8.192 MHz and can be set with: Write/Read Device Configuration Register 1, and if necessary Write/Read Master Clock Correction Register.*

## PCM Switching Waveforms

**Figure 14. Master Clock Timing**

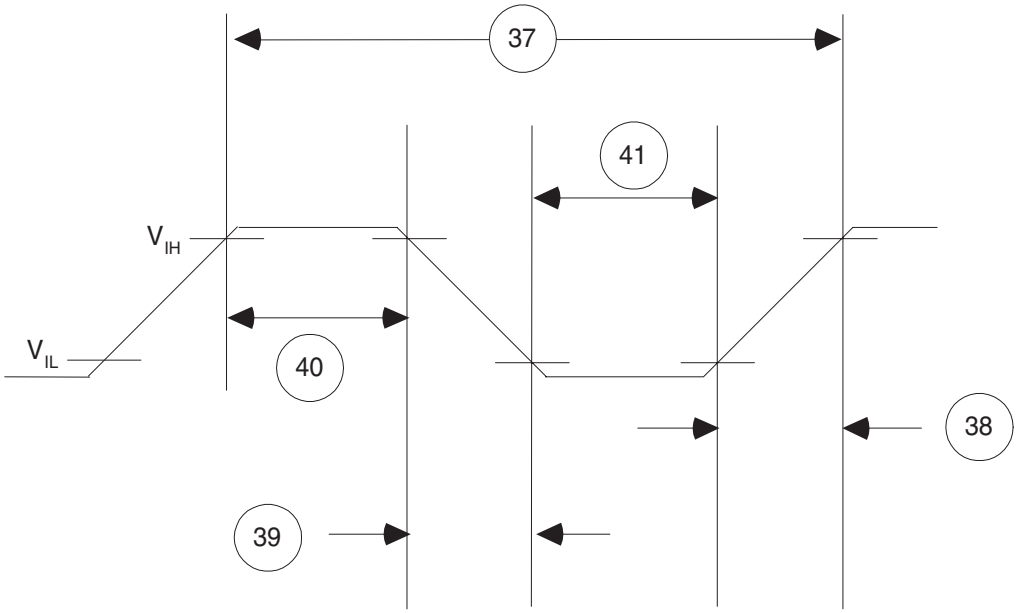



**Figure 15. Microprocessor Interface (Input Mode)**

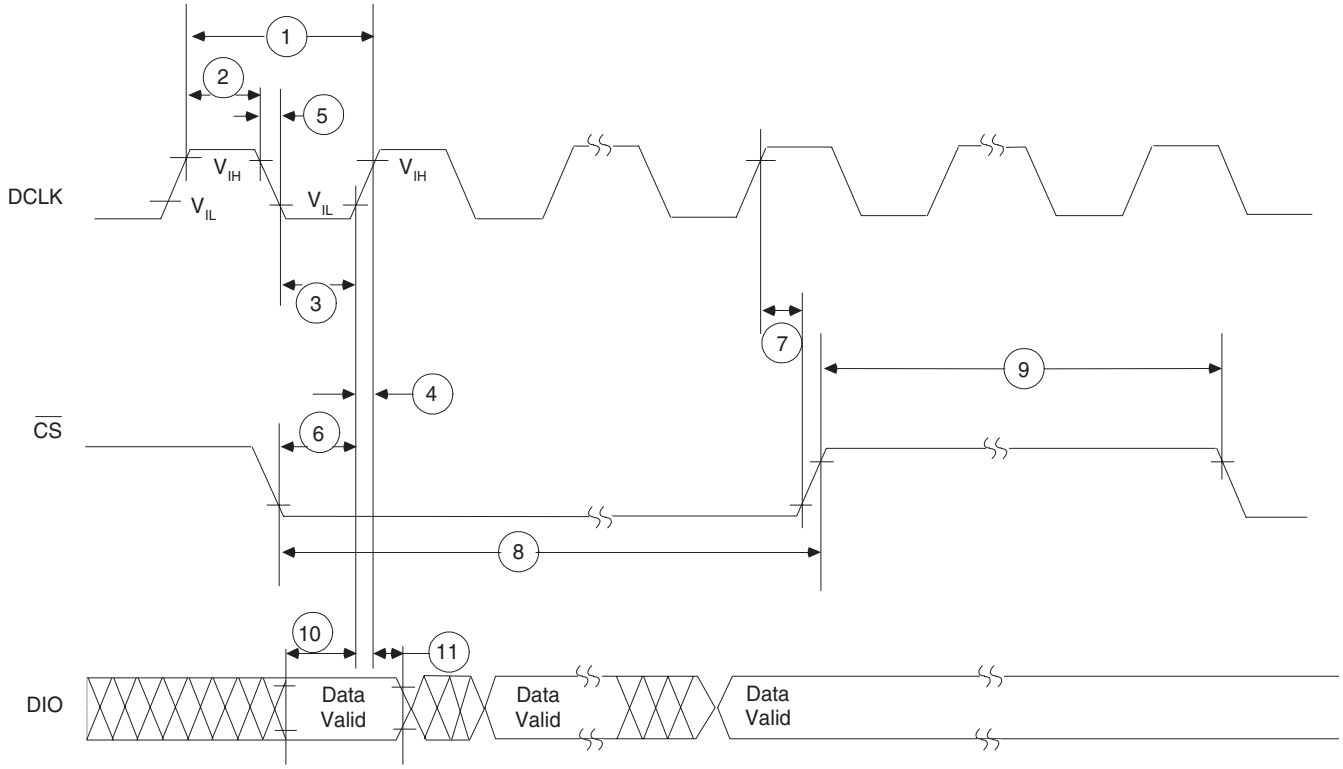


**Figure 16. Microprocessor Interface (Output Mode)**

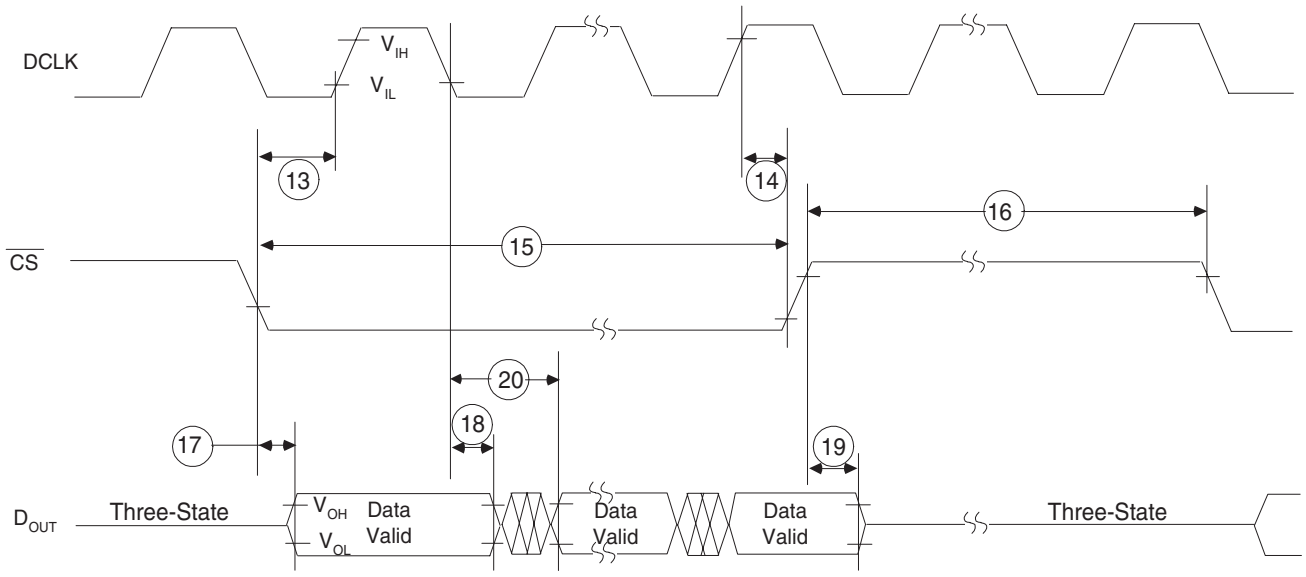



**Figure 17. PCM Highway Timing for XE = 0 (Transmit on Negative PCLK Edge)**

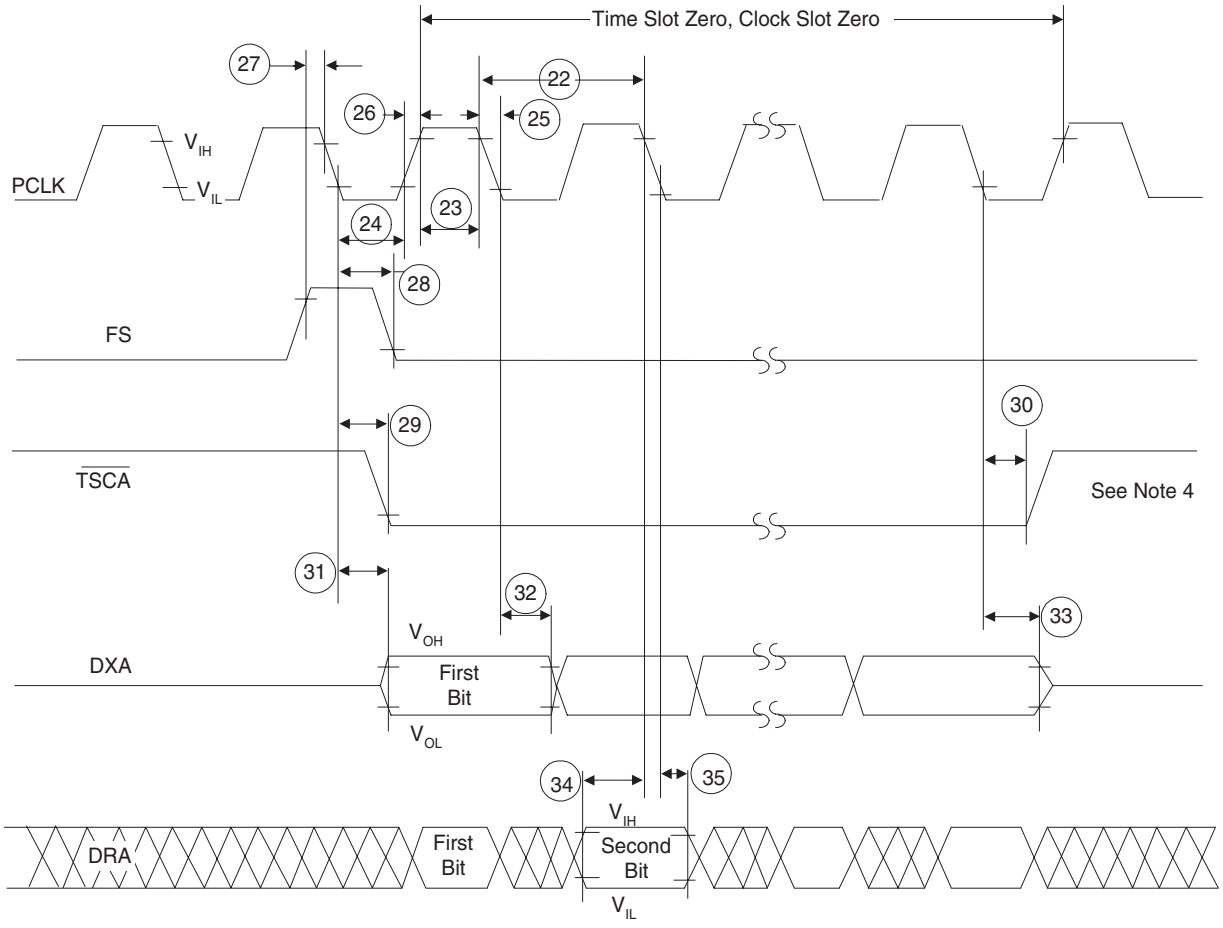
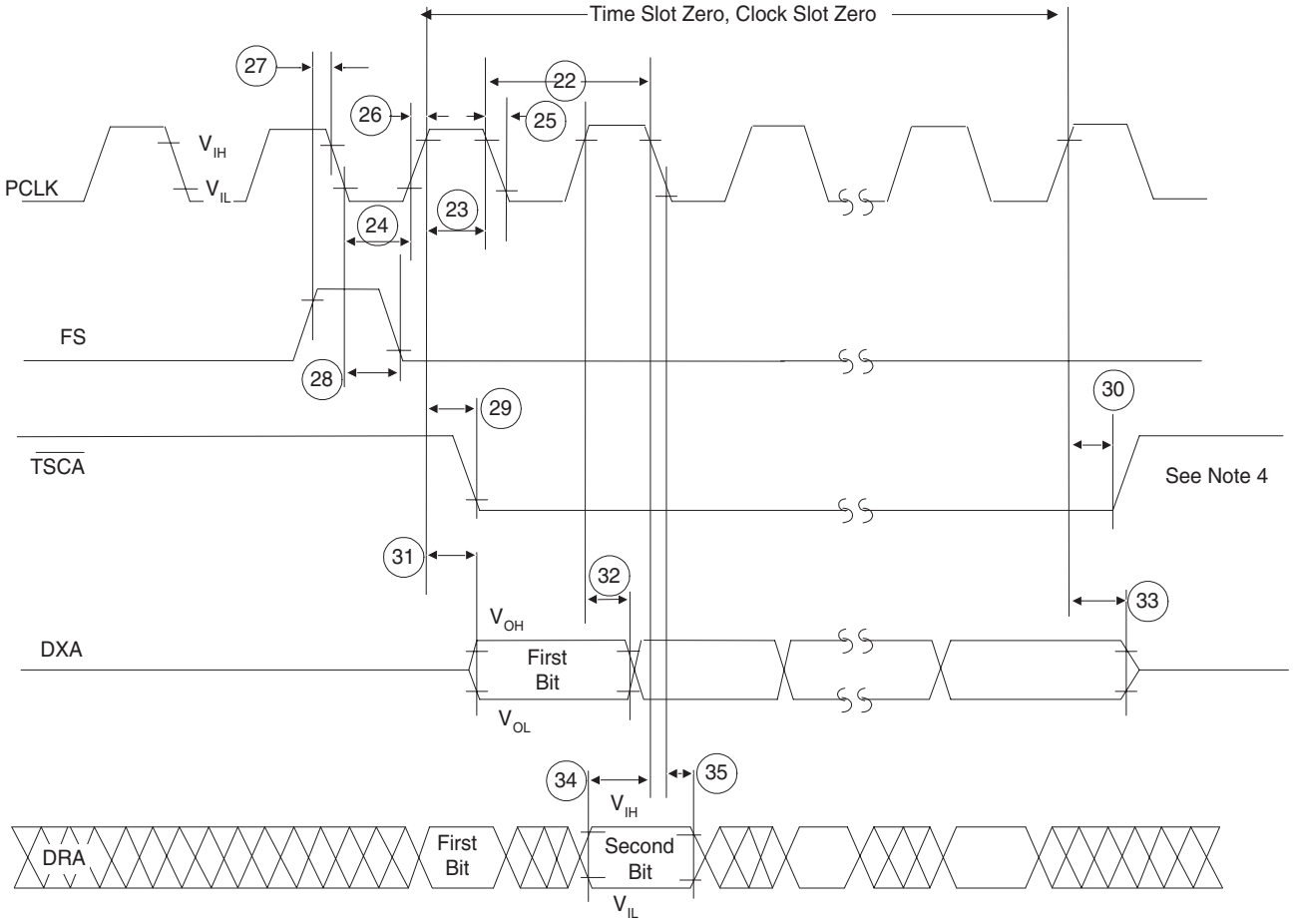


**Figure 18. PCM Highway Timing for XE = 1 (Transmit on Positive PCLK Edge)**



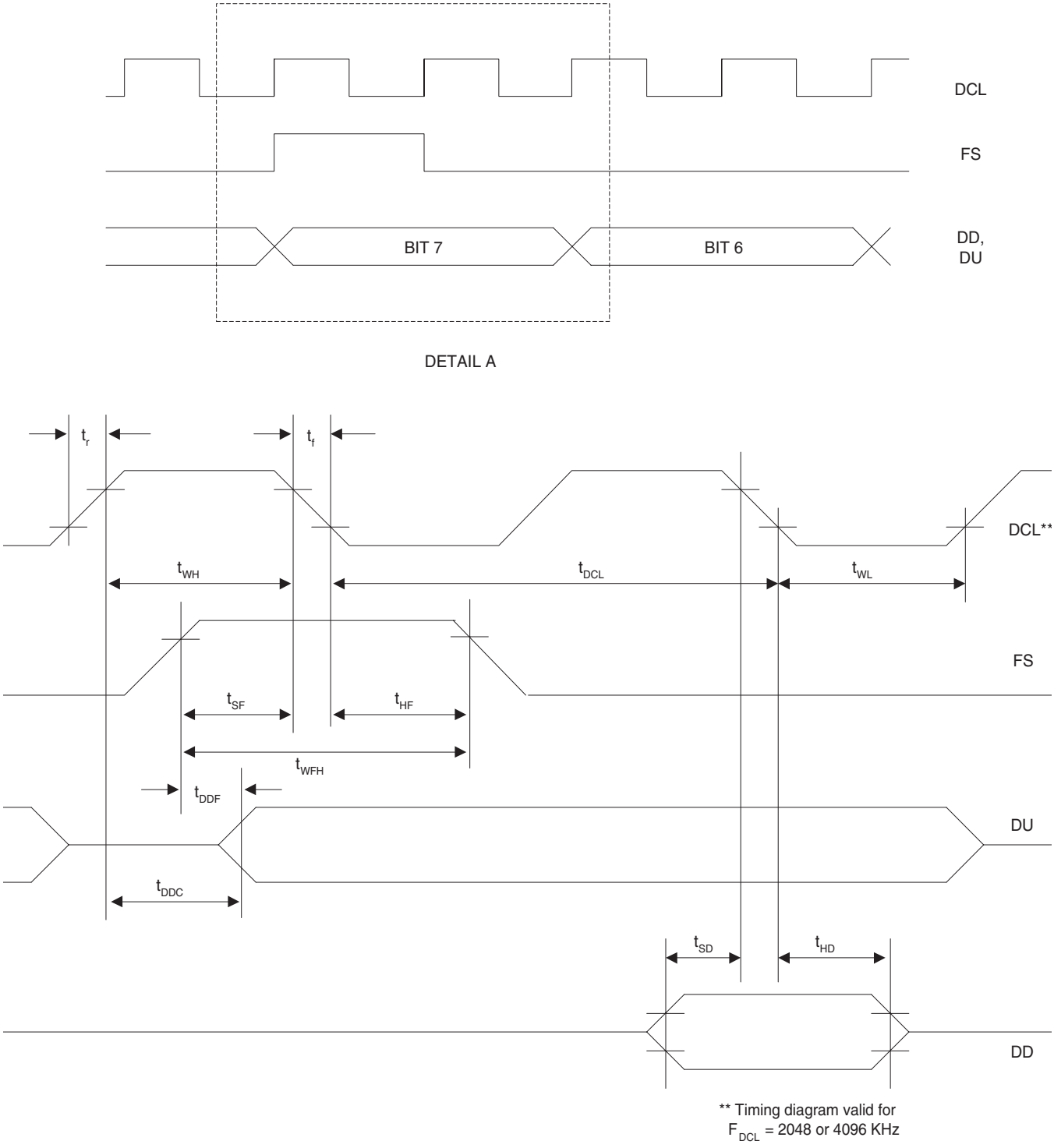

## GCI Timing Specifications

| Symbol | Signal | Parameter | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $t_R$, $t_F$ | DCL | Rise/fall time | | | 60 | ns |
| $t_{DCL}$ | DCL | Period, $F_{DCL}$ = 2048 kHz<br>$F_{DCL}$ = 4096 kHz | 478<br>239 | | 498<br>249 | |
| $t_{WH}$, $t_{WL}$ | DCL | Pulse width | 90 | | | |
| $t_R$, $t_F$ | FS | Rise/fall time | | | 60 | |
| $t_{SF}$ | FS | Setup time | 70 | | $t_{DCL}$–50 | |
| $t_{HF}$ | FS | Hold time | 50 | | | |
| $t_{WFH}$ | FS | High pulse width | 130 | | | |
| $t_{DDC}$ | DU | Delay from DCL edge | | | 100 | |
| $t_{DDF}$ | DU | Delay from FS edge | | | 150 | |
| $t_{SD}$ | DD | Data setup | twH+20 | | | |
| $t_{HD}$ | DD | Data hold | 50 | | | |
| $t_{RST}$ | RST | Reset pulse width | 1.1 | | | ms |

***Note:***

1. *The Data Clock (DCL) can be stopped in the high or low state without loss of information.*
2. *A temporary stoppage of DCL must not put the ISLAC into a state in which it does not respond to a software reset command.*
3. *All frequency-dependent specifications are guaranteed for clock frequencies within ±100 PPM from nominal.*

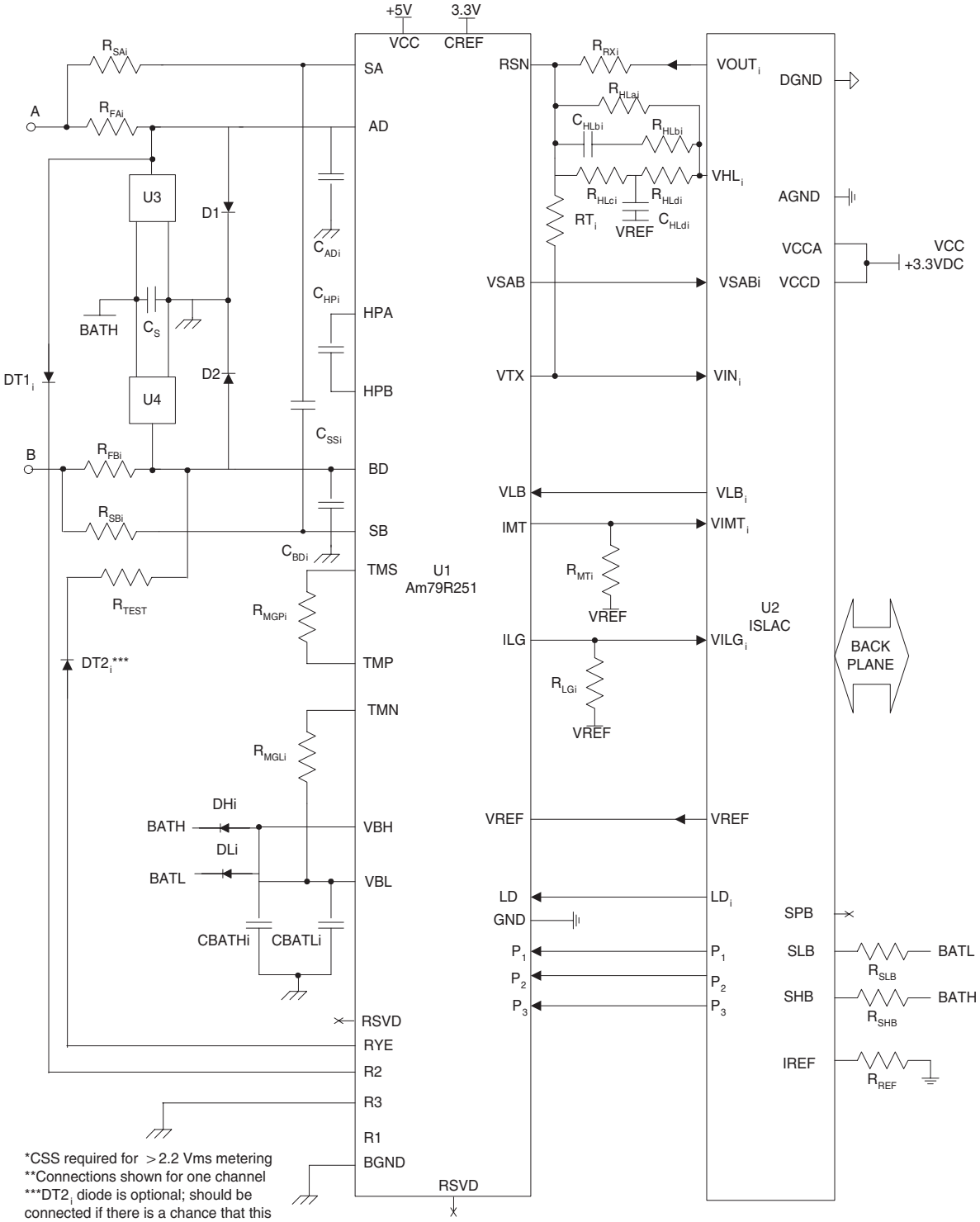
## GCI Waveforms




** Timing diagram valid for
$F_{DCL}$ = 2048 or 4096 KHz

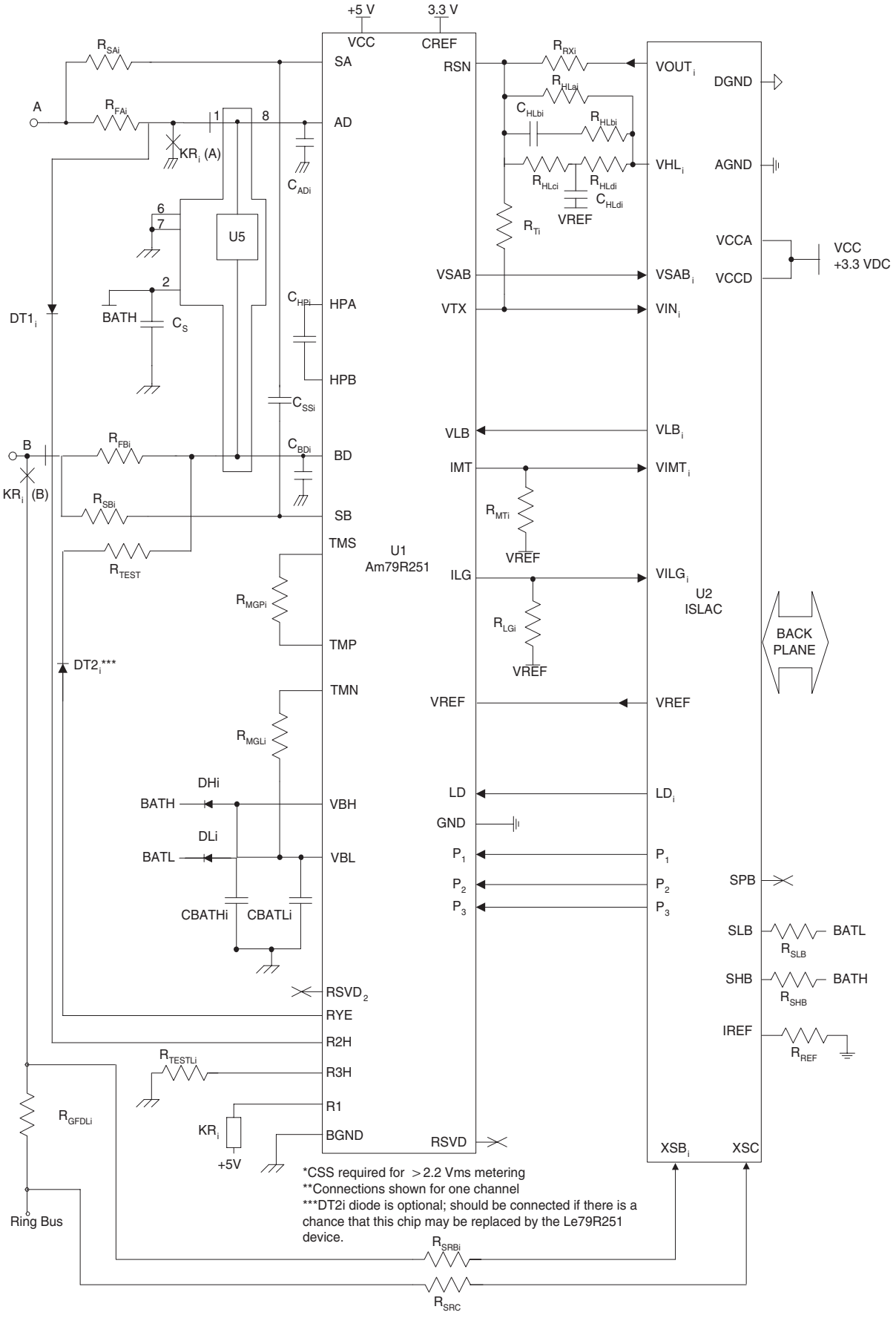
# APPLICATION CIRCUITS

## Internal Ringing Linecard Schematic




*CSS required for > 2.2 Vms metering
**Connections shown for one channel
***DT2$_i$ diode is optional; should be connected if there is a chance that this chip may be replaced by the Le79R251 device. Otherwise, it creates a short.

## External Ringing Linecard Schematic



## LINECARD PARTS LIST

The following list defines the parts and part values required to meet target specification limits for channel i of the linecard (i = 1, 2, 3, 4)..

| Item | Type | Value | Tol. | Rating | Comments |
|---|---|---|---|---|---|
| U1 | Am79R241 | | | | ISLIC device |
| U2 | Am79X22xx | | | | ISLAC device |
| U3, U4 | B1100CC | | | 100 V | TECCOR Battrax protector |
| U5 | TISP61089A | | | | Transient Voltage Suppressor, Power Innovations |
| D1, D2 | Diode | 1 A | | 100 V | |
| $DH_i$, $DL_i$, $DT1_i$, $DT2_i$[4] | Diode | 100 mA | | 100 V | 50 ns |
| $R_{FAi}$, $R_{FBi}$ | Resistor | 50 Ω | 2% | 2 W | Fusible PTC protection resistors |
| $R_{SAi}$, $R_{SBi}$ | Resistor | 200 kΩ | 2% | 1/4 W | Sense resistors |
| $R_{Ti}$ | Resistor | 80.6 kΩ | 1% | 1/10 W | |
| $R_{RXi}$ | Resistor | 100 kΩ | 1% | 1/10 W | |
| $R_{REF}$ | Resistor | 69.8 kΩ | 1% | 1/10 W | Current reference |
| $R_{MGLi}$, $R_{MGPi}$ | Resistor | 1 kΩ | 5% | 1 W | Thermal management resistors |
| $R_{SHB}$, $R_{SLB}$ | Resistor | 750 kΩ | 1% | 1/8 W | |
| $R_{HLai}$ | Resistor | 40.2 kΩ | 1% | 1/10 W | |
| $R_{HLbi}$ | Resistor | 4.32 kΩ | 1% | 1/10 W | |
| $R_{HLci}$ | Resistor | 2.87 kΩ | 1% | 1/10 W | |
| $R_{HLdi}$ | Resistor | 2.87 kΩ | 1% | 1/10 W | |
| $C_{HLbi}$ | Capacitor | 3.3 nF | 10 % | 10 V | Not Polarized |
| $C_{HLdi}$ | Capacitor | 0.82 mF | 10 % | 10 V | Ceramic |
| $R_{MTi}$ | Resistor | 3.01 kΩ | 1% | 1/8 W | |
| $R_{LGi}$ | Resistor | 6.04 kΩ | 1% | 1/8 W | |
| $R_{TEST}$ | Resistor | 2 kΩ | 1% | 1 W | Test board |
| $C_{ADi}$, $C_{BDi}$[1] | Capacitor | 22 nF | 10% | 100 V | Ceramic, not voltage sensitive |
| $C_{BATHi}$, $C_{BATLi}$ | Capacitor | 100 nF | 20% | 100 V | Ceramic |
| $C_{HPi}$ | Capacitor | 22 nF | 20% | 100 V | Ceramic |
| $C_{Si}$[1] | Capacitor | 100 nF | 20% | 100 V | Protector speed up capacitor |
| $C_{SSi}$[3] | Capacitor | 56 pF | 5% | 100 V | Ceramic |
| **Components for External Ringing** | | | | | |
| $R_{GFDi}$ | Resistor | 510 Ω | 2% | 2 W | 1.2 W typ |
| $R_{SRBi}$, $R_{SRc}$ | Resistor | 750 kΩ | 2% | 1/4 W | Matched to within 0.2% for initial tolerance and 0 to 70° C ambient temperature range.[2] 17 mW typ |
| $K_{Ri}$ | Relay | 5 V Coil | | | DPDT |

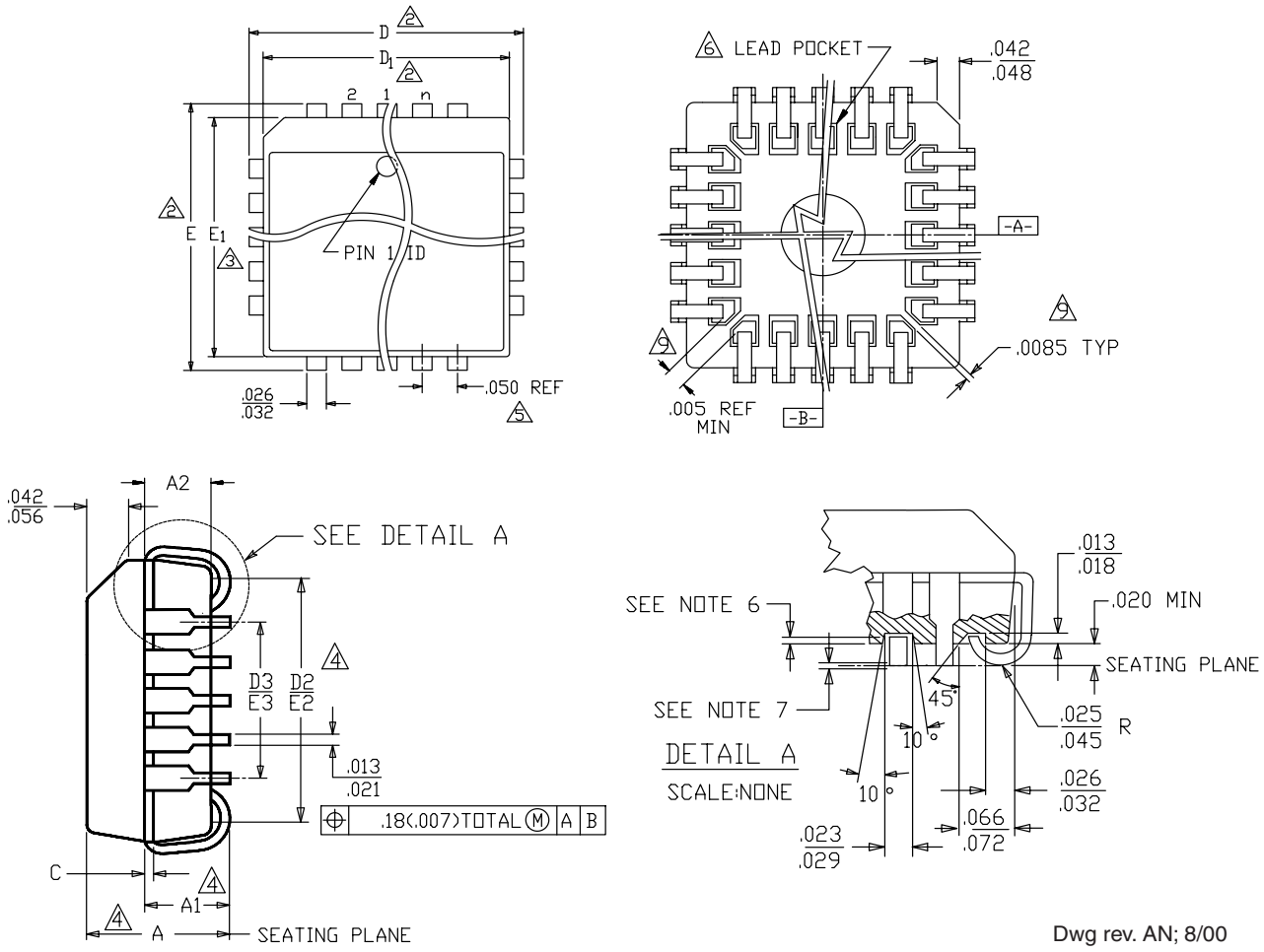
***Note:***

1. *Value can be adjusted to suit application.*
2. *Can be less stringent for relaxed ring-trip requirements.*
3. *Required for metering > 2.2 Vrms, otherwise must be omitted.*
4. *$DT2_i$ is optional - Should be put if there is a chance that this chip may be replaced by Am79R251.*

## PHYSICAL DIMENSIONS

### 68-Pin PLCC

PL 068




Dwg rev. AN; 8/00

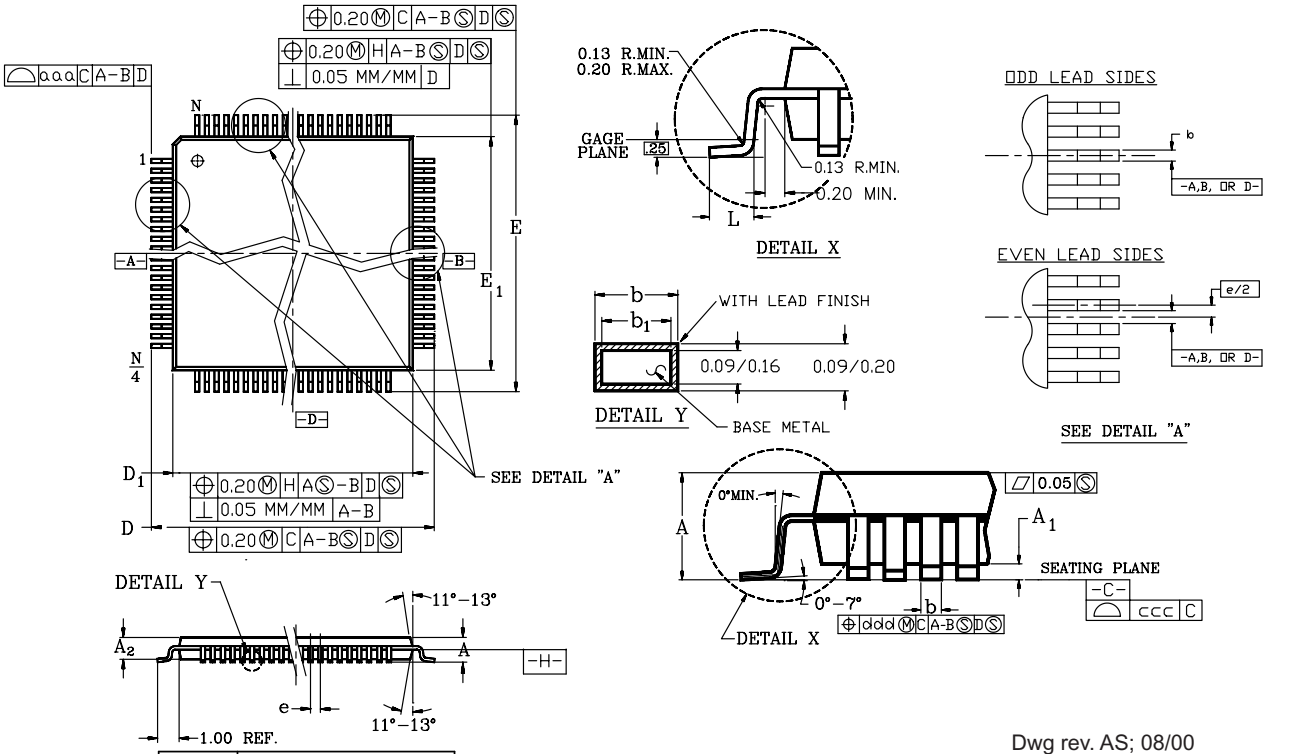
| PACKAGE | PL 068 | |
|---|---|---|
| JEDEC | MO-047(B)AE | |
| SYMBOL | MIN | MAX |
| A | .165 | .180 |
| A1 | .090 | .130 |
| A2 | .062 | .083 |
| D | .985 | .995 |
| D1 | .950 | .956 |
| D2 | .890 | .930 |
| D3 | .800 | REF |
| E | .985 | .995 |
| E1 | .950 | .956 |
| E2 | .890 | .930 |
| E3 | .800 | REF |
| C | .007 | .013 |

NOTES: (UNLESS OTHERWISE SPECIFIED)

1. ALL DIMENSIONS ARE IN INCHES.
2. DIMENSIONS "D" AND "E" ARE MEASURED FROM OUTERMOST POINT.
3. DIMENSIONS D1 AND E1 DO NOT INCLUDE CORNER MOLD FLASH. ALLOWABLE CORNER MOLD FLASH IS .010 INCH
4. DIMENSIONS "A", "A1", "D2" AND "E2" ARE MEASURED AT THE POINTS OF CONTACT TO BASE PLANE
5. LEAD SPACING AS MEASURED FROM CENTERLINE TO CENTERLINE SHALL BE WITHIN ±.005 INCH.
6. J-LEAD TIPS SHOULD BE LOCATED INSIDE THE "POCKET.
7. LEAD COPLANARITY SHALL BE WITHIN .004 INCH AS MEASURED FROM SEATING PLANE. COPLANARITY IS MEASURED PER AMD 06-500.
8. LEAD TWEEZE SHALL BE WITHIN .0045 INCH ON EACH SIDE AS MEASURED FROM A VERTICAL FLAT PLANE. TWEEZE IS MEASURED PER AMD 06-500.
9. LEAD POCKET MAY BE RECTANGULAR (AS SHOWN) OR OVAL. IF CORNER LEAD POCKETS ARE CONNECTED THEN 5 MILS MINIMUM CORNER LEAD SPACING IS REQUIRED.

## 64-Pin Thin Quad Flat Pack (TQFP)

PQT 064




Dwg rev. AS; 08/00

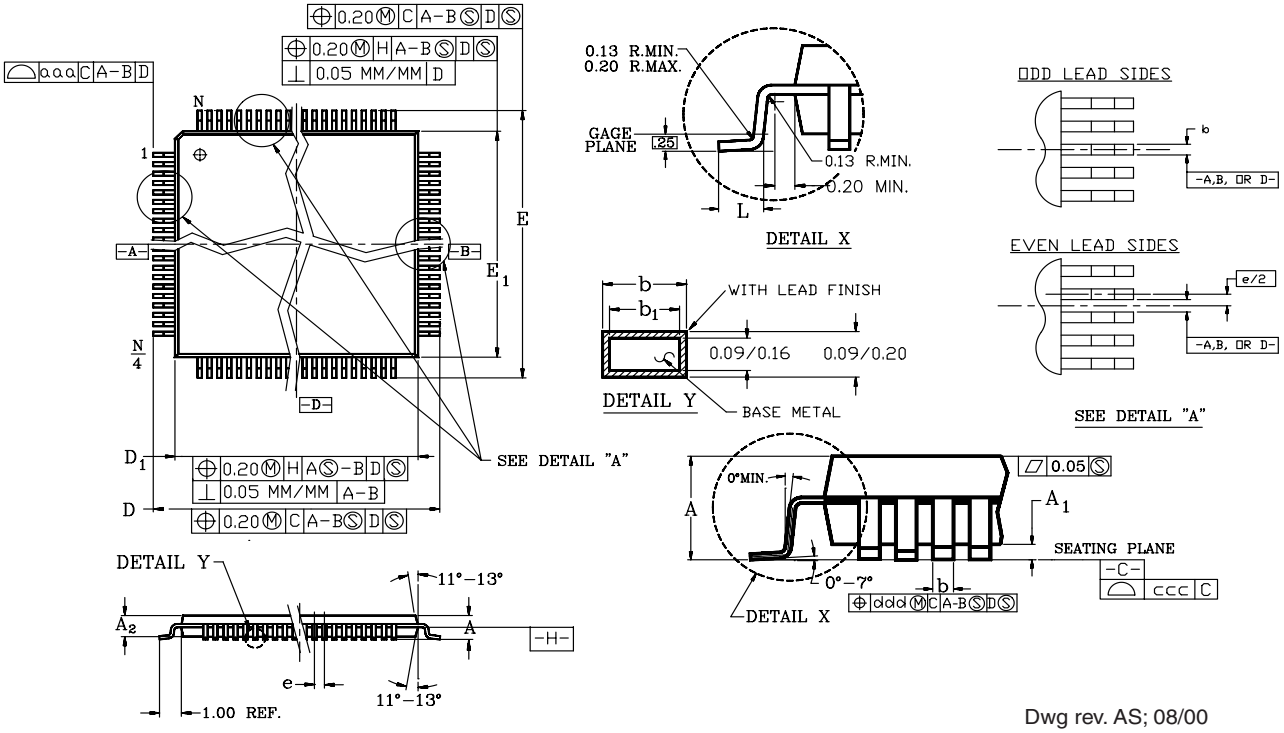
| PACKAGE | PQT 064 | | |
|---|---|---|---|
| JEDEC | MS-026 (C) ACD | | |
| SYMBOL | MIN | NOM | MAX |
| A | — | — | 1.20 |
| A1 | 0.05 | -- | 0.15 |
| A2 | 0.95 | 1.00 | 1.05 |
| D | 12.00 BSC | | |
| D1 | 10.00 BSC | | |
| E | 12.00 BSC | | |
| E1 | 10.00 BSC | | |
| L | 0.45 | 0.60 | 0.75 |
| N | 64 | | |
| e | 0.50 BSC. | | |
| b | 0.17 | 0.22 | 0.27 |
| b1 | 0.17 | 0.20 | 0.23 |
| TOLERANCES OF FORM AND POSITION | | | |
| ccc | 0.08 | | |
| ddd | 0.08 | | |
| aaa | 0.20 | | |

NOTES:

1. ALL DIMENSIONS AND TOLERANCES CONFORM TO ANSI Y14.5M-1982.
2. DATUM PLANE -H- IS LOCATED AT THE MOLD PARTING LINE AND IS COINCIDENT WITH THE BOTTOM OF THE LEAD WHERE THE LEAD EXITS THE PLASTIC BODY.
3. DIMENSIONS "D1" AND "E1" DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS 0.254mm PER SIDE. DIMENSIONS "D1" AND "E1" INCLUDE MOLD MISMATCH AND ARE DETERMINED AT DATUM PLANE -H-
4. DIMENSION "B" DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08mm TOTAL IN EXCESS OF THE b DIMENSION AT MAXIMUM MATERIAL CONDITION. DAMBAR CAN NOT BE LOCATED ON THE LOWER RADIUS OR THE FOOT.
5. CONTROLLING DIMENSIONS: MILLIMETER.
6. DIMENSIONS "D" AND "E" ARE MEASURED FROM BOTH INNERMOST AND OUTERMOST POINTS.
7. DEVIATION FROM LEAD-TIP TRUE POSITION SHALL BE WITHIN ±0.076 MM. FOR PITCH >0.5mm. AND WITHIN ±0.04 FOR PITCH ≤ 0.5 mm.
8. LEAD COPLANARITY SHALL BE WITHIN: (REFER TO 06-500)
   1- 0.10 mm FOR DEVICES WITH LEAD PITCH OF 0.65-0.80 mm.
   2- 0.076 mm FOR DEVICES WITH LEAD PITCH OF 0.50 mm.
   COPLANARITY IS MEASURED PER SPECIFICATION 06-500.
9. HALF SPAN (CENTER OF PACKAGE TO LEAD TIP) SHALL BE 15.30±.165{.602"±.0065"}
10. "N" IS THE TOTAL NUMBER OF TERMINALS.
11. THE TOP OF PACKAGE IS SMALLER THAN THE BOTTOM OF THE PACKAGE BY 0.15 MILLIMETERS.
12. THIS OUTLINE CONFORMS TO JEDEC PUBLICATION 95 REGISTRATION MS-026.
13. THE 160 LEAD IS A COMPLIANT DEPOPULATION OF THE 176 LEAD MS-026 VARIATION BGA.

## 80-Pin Thin Quad Flat Pack (TQFP)

PQT 080




Dwg rev. AS; 08/00

| PACKAGE | PQT 080 | | |
|---|---|---|---|
| JEDEC | MS-026 (C) ADD | | |
| SYMBOL | MIN | NOM | MAX |
| A | — | — | 1.20 |
| A1 | 0.05 | — | 0.15 |
| A2 | 0.95 | 1.00 | 1.05 |
| D | 14.00 BSC | | |
| D1 | 12.00 BSC | | |
| E | 14.00 BSC | | |
| E1 | 12.00 BSC | | |
| L | 0.45 | 0.60 | 0.75 |
| N | 80 | | |
| e | 0.50 BASIC | | |
| b | 0.17 | 0.22 | 0.27 |
| b1 | 0.16 | 0.20 | 0.23 |
| TOLERANCES OF FORM AND POSITION | | | |
| ccc | — | — | 0.08 |
| ddd | — | — | 0.08 |
| aaa | — | — | 0.20 |

NOTES:

1. ALL DIMENSIONS AND TOLERANCES CONFORM TO ANSI Y14.5M–1982.
2. DATUM PLANE -H- IS LOCATED AT THE MOLD PARTING LINE AND IS COINCIDENT WITH THE BOTTOM OF THE LEAD WHERE THE LEAD EXITS THE PLASTIC BODY.
3. DIMENSIONS "D1" AND "E1" DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS 0.254mm PER SIDE. DIMENSIONS "D1" AND "E1" INCLUDE MOLD MISMATCH AND ARE DETERMINED AT DATUM PLANE -H-
4. DIMENSION "B" DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08mm TOTAL IN EXCESS OF THE b DIMENSION AT MAXIMUM MATERIAL CONDITION. DAMBAR CAN NOT BE LOCATED ON THE LOWER RADIUS OR THE FOOT.
5. CONTROLLING DIMENSIONS: MILLIMETER.
6. DIMENSIONS "D" AND "E" ARE MEASURED FROM BOTH INNERMOST AND OUTERMOST POINTS.
7. DEVIATION FROM LEAD–TIP TRUE POSITION SHALL BE WITHIN ±0.076 MM. FOR PITCH >0.5mm. AND WITHIN ±0.04 FOR PITCH ≤ 0.5 mm.
8. LEAD COPLANARITY SHALL BE WITHIN: (REFER TO 06–500)
   1– 0.10 mm FOR DEVICES WITH LEAD PITCH OF 0.65–0.80 mm.
   2– 0.076 mm FOR DEVICES WITH LEAD PITCH OF 0.50 mm.
   COPLANARITY IS MEASURED PER SPECIFICATION 06–500.
9. HALF SPAN (CENTER OF PACKAGE TO LEAD TIP) SHALL BE 15.30±.165{.602"±.0065"}
10. "N" IS THE TOTAL NUMBER OF TERMINALS.
11. THE TOP OF PACKAGE IS SMALLER THAN THE BOTTOM OF THE PACKAGE BY 0.15 MILLIMETERS.
12. THIS OUTLINE CONFORMS TO JEDEC PUBLICATION 95 REGISTRATION MS–026.
13. THE 160 LEAD IS A COMPLIANT DEPOPULATION OF THE 176 LEAD MS–026 VARIATION BGA.

# REVISION SUMMARY

## Revision A to Revision B

- Revision A was a condensed version of the datasheet while Revision B contains the full version.

## Revision B to RevisionC

- Page 14, Linecard Parts List, Rows CHLbi and CHLdi: switched the numbers in the “Values” column.

## Revision C to Revision D

- Page 12, Figure 5, DT1i was added and the last note was modified.
- Page 14, Linecard Parts List, Item U3, U4 Type information was changed.

## Revision D to Revision E

- Updated document to new format.
- In Pin Descriptions Table, changed I/O status of $\overline{\text{TSCB}}$ to "O"
- In DC Specifications Table, the following changes were made:
  - changed information for "Quad ISLAC Power Dissipation".
  - Updated "Min", "Max", and "Typ" values for Input Leakage Current (VIN1-4, VSAB1-4, VILG1-4, VIMT1-4, VSAB1-4)
  - Updated "Min", "Max", and "Typ" values for Output Leakage Current (VOUT1-4 or VLB1-4)
- Made the following changes to the Transmission and Signaling Specifications table:
  - Reformatted table
  - For Insertion Loss, changed one of the "A-D + D-A" items to "A-D – D-A"
  - For PSRR, added "A-D" to item; added Min value of 37
  - For Image frequency, added "D-A" to item; added Min value of 37
  - For DISN gain accuracy, changed conditions to: Gdisn = –0.9375 to 0.9375; Vin = 0 dBm0
  - For Crosstalk TX or RX to TX; TX or RX to RX, added 0dBm0 to conditions
- Divided Transmit and Receive Path Attenuation vs. Frequency graphic into two separate graphics
- In the "Intermodulation Distortion" section, changed text to "TBD"
- Updated PCM Switching Characteristics graphic.
- In "Master Clock" section, added information for $t_{MCY}$; added Note 8
- Updated External Ringing Linecard schematic.
- Added a linecard parts list.
- Updated all "Physical Dimensions" graphics.

## Revision E to Revision F

- In Pin Descriptions Table, pins LD1-LD4, changed description for logic 0 to < 0.4 V; changed description for logic 1 to ($V_{CC}$ – 0.4 V)
- In DC Specifications Table, item 6, removed "Output current" row; inserted "Medium Voltage" row.
- Subscripted channel numbers throughout document.

## Revision F to G

- Corrected physical dimensions for 64-Pin TQFP.

**Trademarks**

Legerity, the Legerity logo and combinations thereof, and QISLAC™, ISLAC™, and ISLIC™ are trademarks of Legerity, Inc.
Other product names used in this publication are for identification purposes only and may be trademarks of their respective companies.


Mailing: P.O. Box 18200
Austin, TX 78760-8200
Shipping: 4509 Freidrich Lane
Austin, TX 78744-1812

Telephone: (512) 228-5400
Fax: (512) 228-5510
North America Toll Free: (800) 432-4009


# *Worldwide Sales Offices*

## *Americas*


**ATLANTA**
6465 East Johns Crossing, Suite 400
Duluth, GA USA 30097
MainLine: 770-814-4252
Fax: 770-814-4253

**AUSTIN**
4509 Freidrich Lane
Austin, TX USA 78744-1812
MainLine: 512-228-5400
Fax: 512-228-5510

**BOSTON**
6 New England Executive Park Suite 400
Burlington, MA USA 01803
MainLine: 781-229-7320
Fax: 781-272-3706

**CHICAGO**
8770 W. Bryn Mawr, Suite 1300
Chicago, IL USA 60631
MainLine: 773-867-8034
Fax: 773-867-2910

**DALLAS**
4965 Preston Park Blvd., Suite 280
Plano, TX USA 75093
MainLine: 972-985-5474
Fax: 972-985-5475

**HUNTSVILLE**
600 Boulevard South, Suite 104
Huntsville, AL USA 35802
MainLine: 256-705-3504
Fax: 256-705-3505

**IRVINE**
1114 Pacifica Court, Suite 250
Irvine, CA USA 92618
MainLine: 949-753-2712
Fax: 949-753-2713

**NEW JERSEY**
3000 Atrium Way, Suite 270
Mt. Laurel, NJ USA 08054
MainLine: 856-273-6912
Fax: 856-273-6914

**OTTAWA**
600 Terry Fox Drive
Ottawa, Ontario, Canada K26 4B6
MainLine: 613-599-2000
Fax: 613-599-2002

**RALEIGH**
2500 Regency Parkway, Suite 226
Cary, NC USA 27511
MainLine: 919-654-6843
Fax: 919-654-6781

**SAN JOSE**
1740 Technology Drive, Suite 290
San Jose, CA USA 95110
MainLine: 408-573-0650
Fax: 408-573-0402


## *Europe*


**BELGIUM**
Baron Ruzettelaan 27
8310 Brugge
Belgium
MainLine: 32-50-28-88-10
Fax: 32-50-27-06-44

**FRANCE**
7, Avenue G. Pompidou
Suite 402
92300 Levallois-Perret, France
MainLine: 33-1-47-48-2206
Fax: 33-1-47-48-2568

**GERMANY**
Freisinger Str. 1
85737 Ismaning, Germany
MainLine: 49-89-1893-99-0
Fax: 49-89-1893-99-44

**ITALY**
Via F. Rosselli 3/2
20019 Settimo Mse, Milano Italy
MainLine: 39-02-3355521
Fax: 39-02-33555232

**SWEDEN**
Frösundaviks Allé 15, 4tr
SE-16970 Solna
Sweden
MainLine: 46-8-509-045-45
Fax: 46-8-509-046-36

**UK**
Regus House, Windmill Hill Business Park
Whitehill Way
SN5 6QR Swindon
Wiltshire UK
MainLine: 44-(0)1793-441408
Fax: 44-(0)1793-441608


## *Asia*


**HONG KONG**
Units 2401-2, 24th Floor
Jubilee Centre, 18 Fenwick Street
Wanchai, Hong Kong
MainLine: 852-2864-8300
Fax: 852-2866-1323

**KOREA**
135-090 18th Fl., Kyoung Am Bldg
157-26, Samsung-dong, Kangnam-ku
Seoul, Korea
MainLine: 82-2-565-5951
Fax: 82-2-565-3788

**SHENZHEN**
Room 703, Block D1
Fu Yuan Garden
Futian Free Trade Zone
Shenzhen, PR China 518031
MainLine: 86-755-3567-008
Fax: 86-755-3567-191

**TOKYO**
Shinjuku NS Bldg. 5F
2-4-1 Nishi Shinjuku, Shinjuku-ku
Tokyo, Japan 163-0805
MainLine: 81-3-5339-2011
Fax: 81-3-5339-2012


*To download or order product literature, visit our website at **www.legerity.com**.*

*To order literature in North America, call: (800) 572-4859 or 512-349-3193 or email: americalit@legerity.com*

*To order literature in Europe or Asia, call: 44-0-1179-341607*
*or email: Europe — eurolit@legerity.com*
*Asia — asialit@legerity.com*