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1M x 32 SRAM MODULE

PUMA 84S32000 - 012/015/020

Issue 1.2 : January 1999

Description

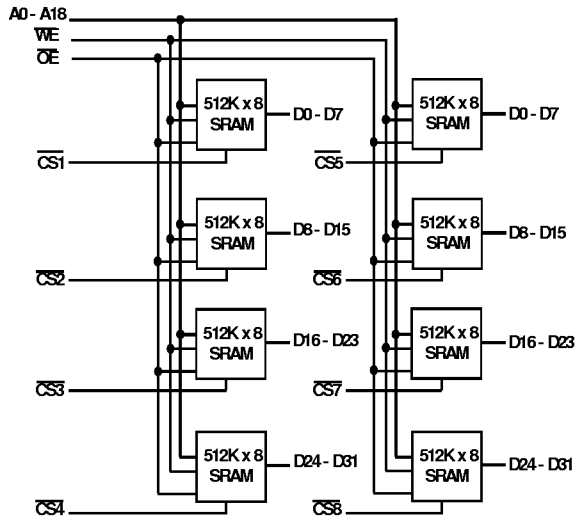
The PUMA 84S32000 is a 32Mbit CMOS High Speed Static RAM organised as 1M x 32 in a JEDEC 84 pin surface mount J-leaded PLCC, available with access times of 12, 15, and 20ns. The output width is user configurable as 8, 16 or 32 bits using eight Chip Selects ($\overline{CS1}$~8).

The device features low power standby, multiple ground pins for maximum noise immunity and TTL compatible inputs and outputs. The PUMA 84S32000 offers a dramatic space saving advantage over eight standard 512Kx8 devices.

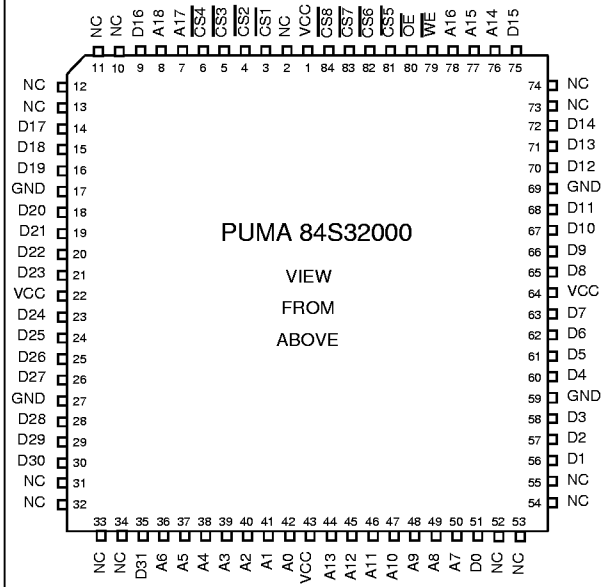
Features

- Very fast access times of 12/15/20 ns .
- JEDEC 84 'J' leaded plastic Surface Mount Package.
- Single 5V±10% Power supply.
- User Configurable as 8 / 16 / 32 bit wide output.
- Operating Power (32-BIT) 5.28 W (max)
  Low Power Standby CMOS 550 mW (max)
- Fully Static operation.
- Multiple ground pins for maximum noise immunity.

Block Diagram



Pin Definition



Pin Functions

Address Inputs	**A0 ~ A18**
Data Input/Output	**D0 ~ D31**
Chip Select	**$\overline{CS1}$ ~ 8**
Write Enable	**$\overline{WE}$**
Output Enable	**$\overline{OE}$**
No Connect	**NC**
Power (+5V)	**V_{cc}**
Ground	**GND**

Package Details

Plastic 84 J-Leaded JEDEC PLCC

DC OPERATING CONDITIONS

Absolute Maximum Ratings (1)

Parameter	*Symbol*	*Min*	*Typ*	*Max*	*Unit*
Voltage on any pin relative to V_{SS}	V_T (2)	-0.5	-	7.0	V
Power Dissipation	P_T	-	-	5.0	W
Storage Temperature	T_{STG}	-65	-	150	°C

Notes : (1) Stresses above those listed may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

(2) V_T can be -2.0V pulse of less than 8ns.

Recommended Operating Conditions

Parameter		*Symbol*	*Min*	*Typ*	*Max*	*Unit*	
Supply Voltage		V_{CC}	4.5	5.0	5.5	V	
Input High Voltage		V_{IH}	2.2	-	V_{CC}+0.5	V	
Input Low Voltage		V_{IL}	-0.3	-	0.8	V	
Operating Temperature	(Commercial)	T_A	0	-	70	°C	
	(Industrial)	T_{AI}	-40	-	85	°C	(Suffix I)

DC Electrical Characteristics (V_{CC}=5V±10%, -40 to 85 °C)

Parameter		*Symbol*	*Test Condition*	*Min*	*Typ*	*max*	*Unit*
I/P Leakage Current	Address,$\overline{OE}$,$\overline{WE}$	I_{LI}	0V ≤ V_{IN} ≤ V_{CC}	-20	-	20	µA
Output Leakage Current		I_{LO}	$\overline{CS}$ = V_{IH}, $V_{I/O}$ = GND to V_{CC}	-20	-	20	µA
Operating Supply Current	32-bit mode	I_{CC32}	Min. Cycle, $\overline{CS}$ = V_{IL}, f=f_{MAX}, I_{OUT} = 0mA	-	-	960	mA
	16-bit mode	I_{CC16}	As Above.	-	-	640	mA
	8-bit mode	I_{CC8}	As Above.	-	-	480	mA
Standby Supply Current	TTL levels	I_{SB1}	$\overline{CS}$ = V_{IH}, f=f_{MAX}	-	-	320	mA
	CMOS levels	I_{SB2}	$\overline{CS}$ ≥ V_{CC}-0.2V, 0.2≤V_{IN}≤V_{CC}-0.2V, f=0	-	-	100	mA
Output Voltage		V_{OL}	I_{OL} = 8.0mA	-	-	0.4	V
		V_{OH}	I_{OH} = -4.0mA	2.4	-	-	V

Notes :

1/ Typical values are at V_{CC}=5.0V, T_A=25°C and specified loading.

2/ $\overline{CS}$ above refers to $\overline{CS1}$~4 / $\overline{CS5}$~8 for 32 bit mode

3/ At f=f_{MAX} address and data inputs are cycling at maximum frequency.

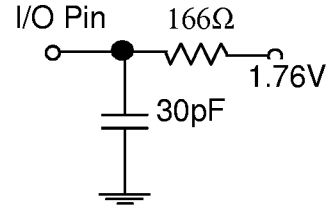
Capacitance (V_{CC}=5V±10%, T_A=25°C) Note: Capacitance calculated, not measured.

Parameter		*Symbol*	*Test Condition*	*max*	*Unit*
Input Capacitance	(Address,$\overline{OE}$,$\overline{WE}$)	C_{IN1}	V_{IN} = 0V	70	pF
I/P Capacitance	(Other)	C_{IN2}	V_{IN} = 0V	12	pF
I/O Capacitance	Worst case (8-bit)	$C_{I/O}$	$V_{I/O}$ = 0V	62	pF

AC Test Conditions

* Input pulse levels: 0V to 3.0V
* Input rise and fall times: 3ns
* Input and Output timing reference levels: 1.5V
* Output load: see diagram
* V_{CC}=5V±10%

Output Load



Operation Truth Table

$\overline{CS}$	$\overline{OE}$	$\overline{WE}$	*DATA PINS*	*SUPPLY CURRENT*	*MODE*
H	X	X	High Impedance	I_{SB1} , I_{SB2} , I_{SB3}	Standby
L	L	H	Data Out	I_{CC32} , I_{CC16} , I_{CC8}	Read
L	H	L	Data In	I_{CC32} , I_{CC16} , I_{CC8}	Write
L	L	L	Data In	I_{CC32} , I_{CC16} , I_{CC8}	Write
L	H	H	High-Impedance	I_{SB1} , I_{SB2} , I_{SB3}	High-Z

Notes : H = V_{IH} : L =V_{IL} : X = V_{IH} or V_{IL}

The above table reflects the operation of each of the RAM's on the module. Care should be taken to avoid bus contention on data lines using chip select signals.

AC OPERATING CONDITIONS

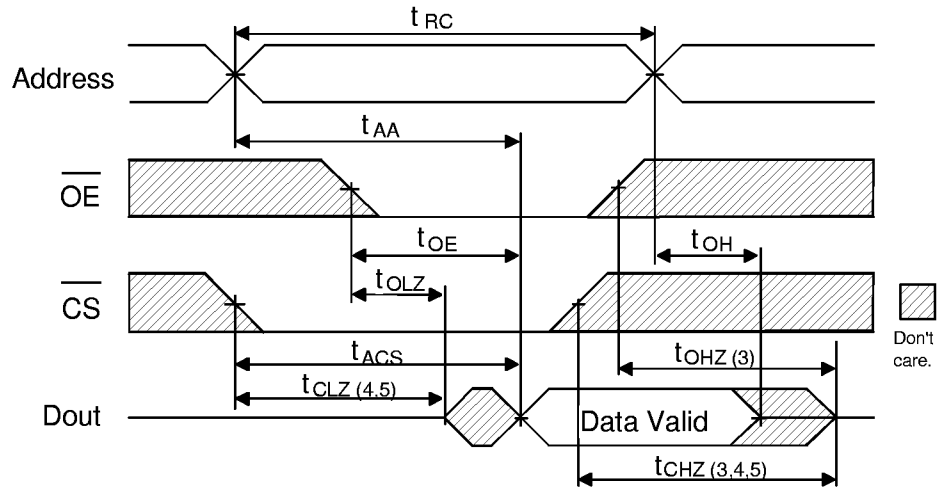
Read Cycle

		012		015		020		
Parameter	*Symbol*	*min*	*max*	*min*	*max*	*min*	*max*	*Unit*
Read Cycle Time	t_{RC}	12	-	15	-	20	-	ns
Address Access Time	t_{AA}	-	12	-	15	-	20	ns
Chip Select Access Time	t_{ACS}	-	12	-	15	-	20	ns
Output Enable to Output Valid	t_{OE}	-	6	-	7	-	9	ns
Output Hold from Address Change	t_{OH}	3	-	3	-	3	-	ns
Chip Selection to Output in Low Z	t_{CLZ}	3	-	3	-	3	-	ns
Output Enable to Output in Low Z	t_{OLZ}	0	-	0	-	0	-	ns
Chip Deselection to O/P in High Z	t_{CHZ}	0	6	0	7	0	9	ns
Output Disable to Output in High Z	t_{OHZ}	0	6	0	7	0	9	ns

Write Cycle

		012		015		020		
Parameter	*Symbol*	*min*	*max*	*min*	*max*	*min*	*max*	*Unit*
Write Cycle Time	t_{WC}	12	-	15	-	20	-	ns
Chip Selection to End of Write	t_{CW}	10	-	12	-	15	-	ns
Address Valid to End of Write	t_{AW}	10	-	12	-	15	-	ns
Address Setup Time	t_{AS}	0	-	0	-	0	-	ns
Write Pulse Width	t_{WP}	10	-	12	-	12	-	ns
Write Recovery Time	t_{WR}	0	-	0	-	0	-	ns
Write to Output in High Z	t_{WHZ}	0	6	0	7	0	9	ns
Data to Write Time Overlap	t_{DW}	6	-	7	-	9	-	ns
Data Hold from Write Time	t_{DH}	0	-	0	-	0	-	ns
Output active from end of write	t_{OW}	3	-	3	-	3	-	ns

Read Cycle Timing Waveform (1,2)



AC Read Characteristics Notes

(1) $\overline{WE}$ is High for Read Cycle.

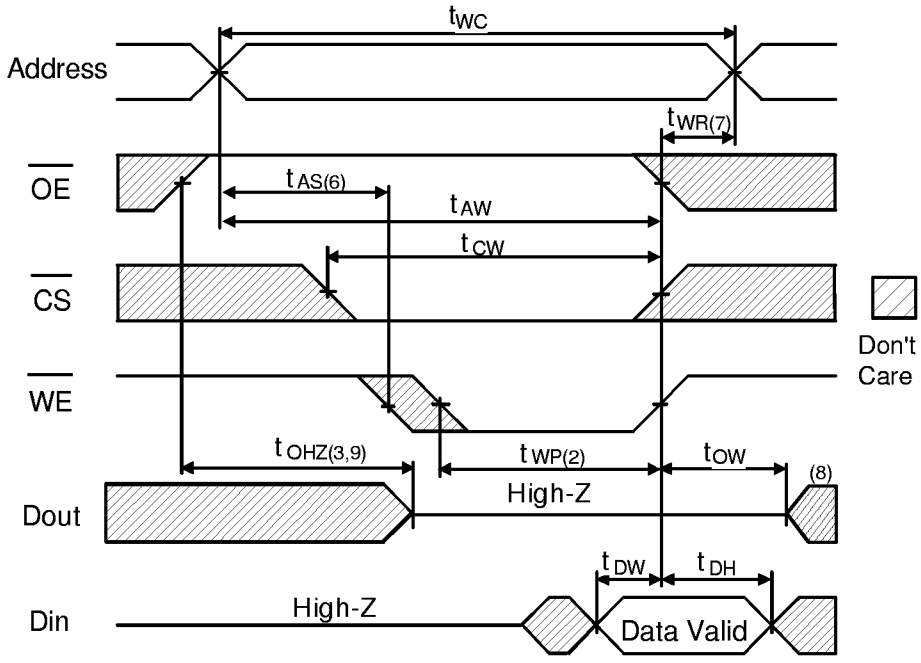
(2) All read cycle timing is referenced from the last valid address to the first transition address.

(3) t_{CHZ} and t_{OHZ} are defined as the time at which the outputs achieve open circuit conditions and are not referenced to output voltage levels.

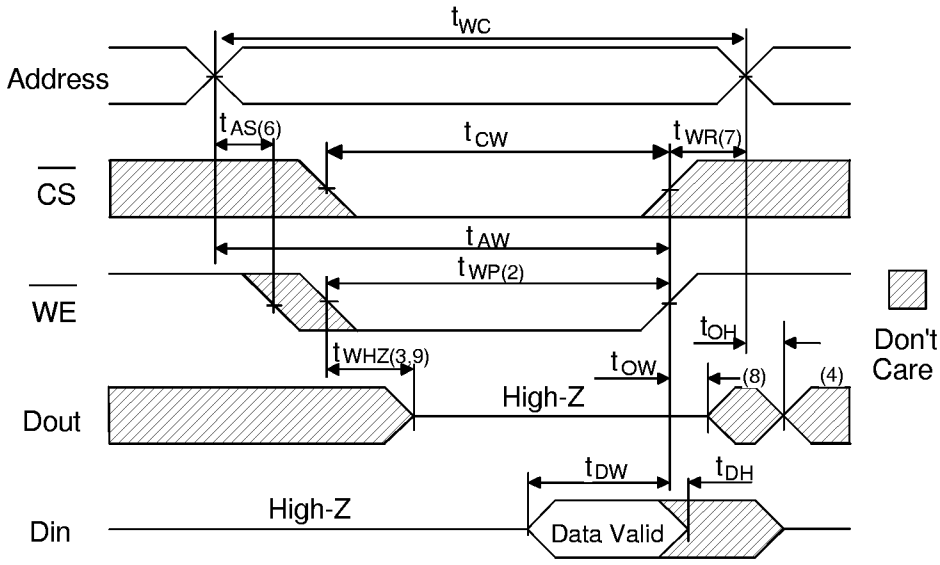
(4) At any given temperature and voltage condition, t_{CHZ} (max) is less than t_{CLZ} (min) both for a given module and from module to module.

(5) These parameters are sampled and not 100% tested.

Write Cycle No.1 Timing Waveform (1,4)



Write Cycle No.2 Timing Waveform (1,5)



AC Write Characteristics Notes

(1) All write cycle timing is referenced from the last valid address to the first transition address.

(2) All writes occur during the overlap of $\overline{CS}$ and $\overline{WE}$ low.

(3) If $\overline{OE}$, $\overline{CS}$, and $\overline{WE}$ are in the Read mode during this period, the I/O pins are low impedance state. Inputs of opposite phase to the output must not be applied because bus contention can occur.

(4) Dout is the Read data of the new address.

(5) $\overline{OE}$ is continuously low.

(6) Address is valid prior to or coincident with $\overline{CS}$ and $\overline{WE}$ low, too avoid inadvertant writes.

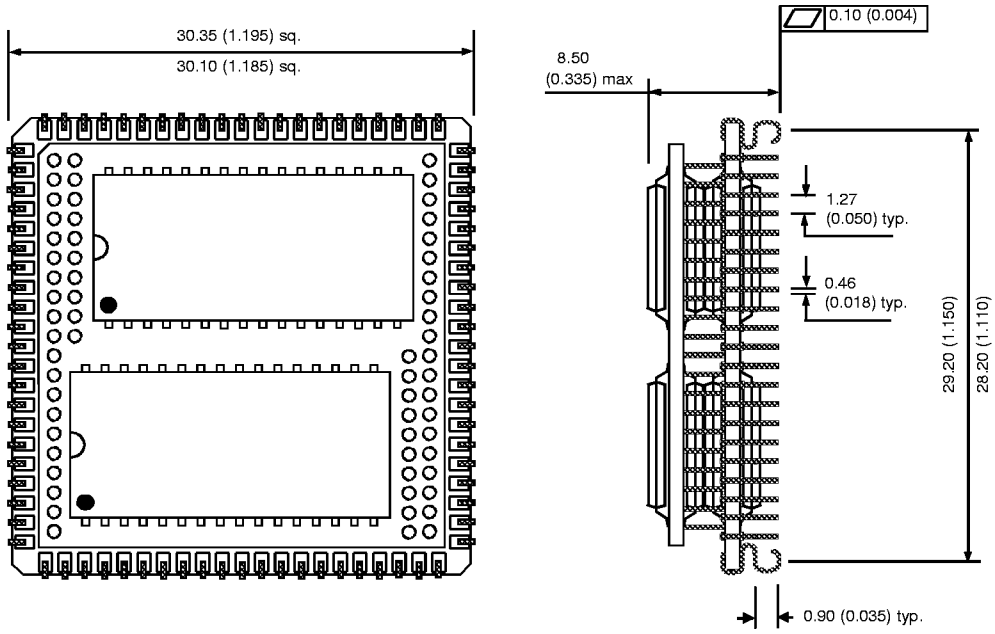
(7) $\overline{CS}$ or $\overline{WE}$ must be high during address transitions.

(8) When $\overline{CS}$ are low : I/O pins are in the output state. Input signals of opposite phase leading to the output should not be applied.

(9) Defined as the time at which the outputs achieve open circuit conditions and are not referenced to output voltage levels. These parameters are sampled and not 100% tested.

Package Information Dimensions in mm(inches)

Plastic 84 Pin JEDEC Surface mount PLCC



Ordering Information

PUMA 84S32000LI - 012

Speed	012	=	12 ns
	015	=	15 ns
	020	=	20 ns
Temperature Range	Blank	=	Commercial Temperature
	I	=	Industrial Temperature
Power Consumption	Blank	=	Standard
	L	=	Low Power
Organisation	32000	=	1M x 32 SRAM configurable as 2M x 16 and 4M x 8
Memory Type	S	=	Asynchronous SRAM 5V ± 10% V_{CC}
Package	PUMA 84	=	Memory Stack 84 pin 'J' Leaded

Note :

Although this data is believed to be accurate the information contained herein is not intended to and does not create any warranty of merchantibility or fitness for a particular purpose.
Our products are subject to a constant process of development. Data may be changed at any time without notice.
Products are not authorised for use as critical components in life support devices without the express written approval of a company director.