

Intelligent Subscriber Line Interface Circuit Am79R240 device

APPLICATIONS

- **Optimized for Voice over Broadband and related applications**
 - Cable telephony
 - Integrated Access Devices (IAD)
 - Smart Residential Gateways (SRG)
 - LAN Systems

FEATURES

- **Monitor of two-wire interface voltages and currents supports**
 - Voice transmission
 - Through chip ring generation
 - Programmable DC feed characteristics
 - Independent of battery
 - Current limited
 - Selectable off-hook and ground-key thresholds
 - Power cross and fault detection
- **Supports internal short loop ringing**
- **+5 V and battery supplies**
- **Dual battery operation for system power saving**
 - Automatic battery switching
- **Compatible with inexpensive protection networks**
 - Accommodates low tolerance fuse resistors or PTC thermistors
- **Metering capable**
 - 12 kHz and 16 kHz
- **Tip-open state supports ground start signaling**
- **5 REN with 15 V DC offset trapezoid.**

For US standard:

 - drives ring up to 4.4 kft of 26 gauge wire.

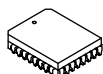
or

 - drives ring up to 7 kft of 24 gauge wire.

For European (British) standard:

 - drives ring up to 1.7 km of 0.5 mm copper cable.

ORDERING INFORMATION



An ISLAC™ device must be used with this part.

Device	Package
Am79R241JC	32-pin PLCC

DESCRIPTION

In combination with an ISLAC™ device, the Am79R240 device implements the telephone line interface function. This enables the design of a low cost, high performance, fully software programmable line interface for multiple country applications worldwide. All AC, DC, and signaling parameters are fully programmable via microprocessor or GCI interfaces on the ISLAC device. Additionally, the Am79R240 device has integrated self-test capabilities to resolve faults to the line circuit.

RELATED LITERATURE

- **080250 Am79Q2241/2242/2243 QISLAC Data Sheet**
- **080274 Am79D2251 DISLAC Data Sheet**
- **080262 Intelligent Access™ Voice Solutions Evaluation Board User's Guide**
- **080344 Am79R240/Am79Q224x ISLIC™/Quad ISLAC™ Technical Reference**
- **080345 Am79R240/Am79D2251 ISLIC™/Dual ISLAC™ Technical Reference**

BLOCK DIAGRAM

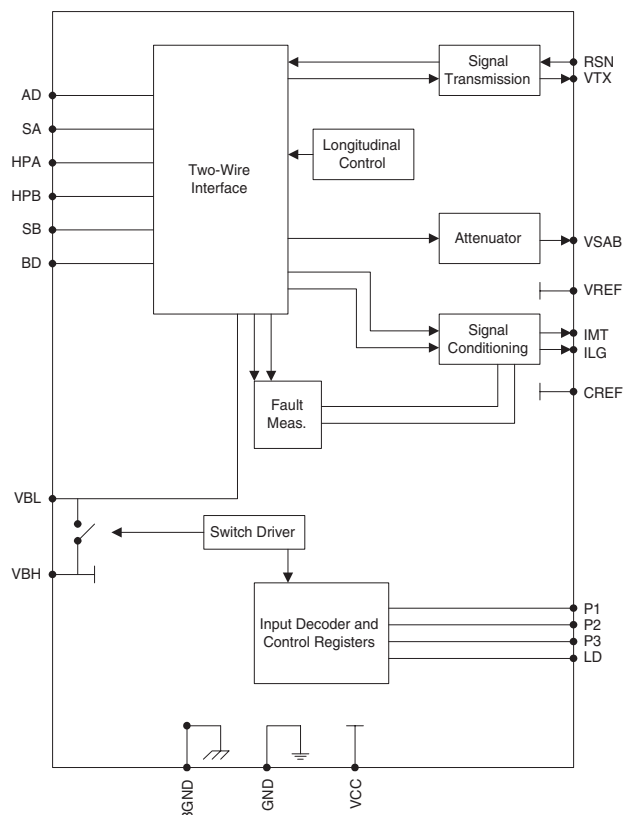


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PRODUCT DESCRIPTION

The Intelligent Access™ voice chip sets integrate all functions of the subscriber line. Two chip types are used to implement the line card — an Am79R240 device and an ISLAC device. Current ISLAC devices include the Am79Q2241/2242/2243 and the Am79D2251. These provide the following basic functions:

1. The Am79R240 device: A high voltage, bipolar device that drives the subscriber line, maintains longitudinal balance and senses line conditions.
2. The ISLAC device: A low voltage CMOS IC that provides conversion, control and DSP functions for the Am79R240 device.

A complete schematic of a line card using the Intelligent Access voice chip sets for internal ringing is shown in the “Chip Set Block Diagram - Two Channel Line Card Example” on page 6.

The Am79R240 device uses reliable, bipolar technology to provide the power necessary to drive a wide variety of subscriber lines. It can be programmed by the ISLAC device to operate in eight different modes that control power consumption and signaling. This enables it to have full control over the subscriber loop. The Am79R240 device is designed to be used exclusively with the ISLAC devices. The Am79R240 device requires only +5 V power and the battery supplies for its operation.

The Am79R240 device implements a linear loop-current feeding method.

The ISLAC device contains high-performance circuits that provide A/D and D/A conversion for the voice (codec), DC-feed and supervision signals. The ISLAC device contains a DSP core that handles signaling, DC-feed and supervision for all channels.

The DSP core selectively interfaces with three types of backplanes:

- Standard PCM/MPI
- Standard GCI
- Modified GCI with a single analog line per GCI channel

The Intelligent Access voice chip set provides a complete software configurable solution to the BORSCHT functions as well as complete programmable control over subscriber line DC-feed characteristics, such as current limit and feed resistance. In addition, these chip sets provide system level solutions for the loop supervisory functions and metering. In total, they provide a programmable solution that can satisfy worldwide line card requirements by software configuration.

Software programmed filter coefficients, DC-feed data and supervision data are easily calculated with the WinSLAC™ software. This PC software is provided free of charge, and allows the designer to enter a description of system requirements. WinSLAC then computes the necessary coefficients and plots the predicted system results.

The Am79R240 device includes circuitry to report Tip•Ring voltage and metallic and longitudinal currents to the ISLAC device. These inputs allow the ISLAC device to place several key Am79R240 device performance parameters under software control.

The main functions that can be observed and/or controlled through the ISLAC device backplane interface are:

- DC-feed characteristics
- Ground-key detection
- Off-hook detection
- Metering signal
- Subscriber line voltage and currents
- Ring-trip detection
- Abrupt and smooth battery reversal
- Subscriber line matching
- Ringing generation

To accomplish these functions, the ISLAC device collects the following information and feeds it in analog form to the ISLAC device:

- The metallic (IMT) and longitudinal (ILG) loop currents
- The AC (VTX) and DC (VSAB) loop voltage

The outputs supplied by the ISLAC device to the ISLAC device are then:

- A voltage (VHLi) that provides control for the following high-level ISLAC device outputs:
 - DC loop current
 - Internal ringing signal
 - 12 or 16 kHz metering signal
- A low-level voltage proportional to the voice signal (VOUTi)

The ISLAC device performs the codec and filter functions associated with the four-wire section of the subscriber line circuitry in a digital switch. These functions involve converting an analog voice signal into digital PCM samples and converting digital PCM samples back into an analog signal. During conversion, digital filters are used to band-limit the voice signals.

The user-programmable filters set the receive and transmit gain, perform the transhybrid balancing function, permit adjustment of the two-wire termination impedance and provide frequency attenuation adjustment (equalization) of the receive and transmit paths. Adaptive transhybrid balancing is also included. All programmable digital filter coefficients can be calculated using WinSLAC software and loaded into the ISLAC device registers using the system microprocessor. The PCM codes can be either 16-bit linear twos-complement or 8-bit companded A-law or μ -law.

Besides the codec functions, the Intelligent Access voice chip set provides all the sensing, feedback, and clocking necessary to completely control ISLIC device functions with programmable parameters. System-level parameters under programmable control include active loop current limits, feed resistance, and feed mode voltages.

The ISLAC device supplies complete mode control to the ISLIC device using the control bus (P1-P3) and tri-level load signal (LDi).

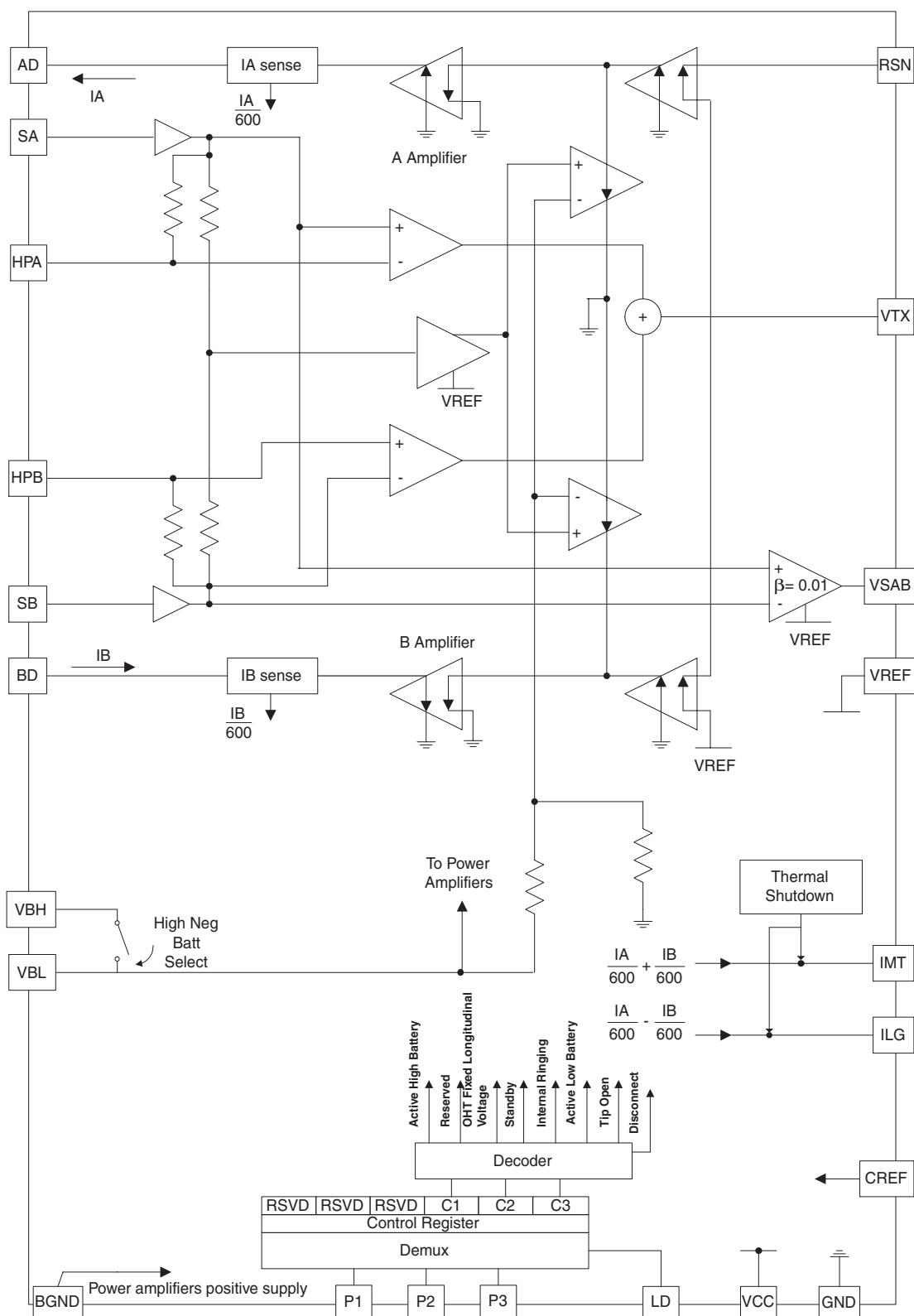
The Intelligent Access voice chipset provides extensive loop supervision capability including off-hook, ring-trip and ground-key detection. Detection thresholds for these functions are programmable. A programmable debounce timer is available that eliminates false detection due to contact bounce.

AC and DC fault detection is also provided.

Note:

i denotes channel number

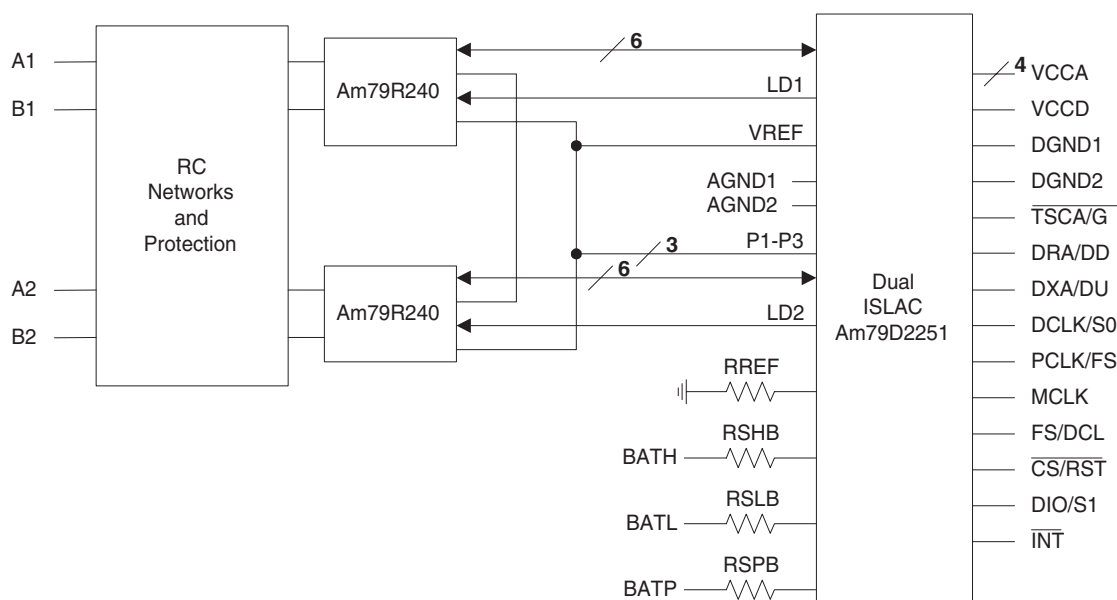
AM79R240 DEVICE INTERNAL BLOCK DIAGRAM



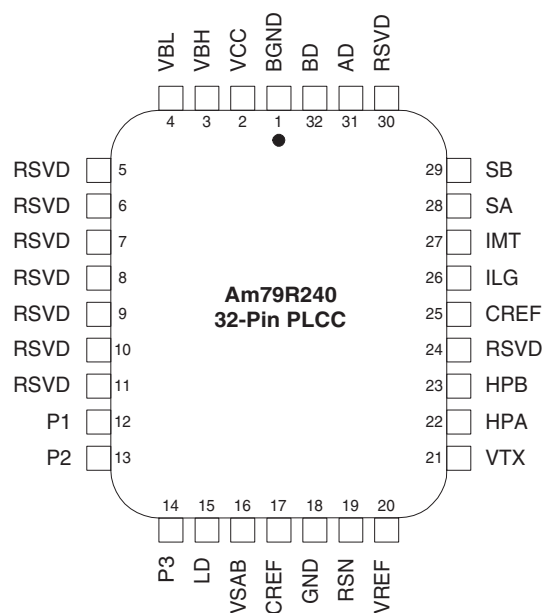
FEATURES OF THE INTELLIGENT ACCESS™ CHIP SET

- Performs all battery feed, ringing, signaling, hybrid and test (BORSCHT) functions
- Two chip solution supports high density, multi-channel architecture
- Single hardware design meets multiple country requirements through software programming of:
 - Ringing waveform and frequency
 - DC loop-feed characteristics and current-limit
 - Loop-supervision detection thresholds
 - Off-hook debounce circuit
 - Ground-key and ring-trip filters
 - Off-hook detect de-bounce interval
 - Two-wire AC impedance
 - Transhybrid balance
 - Transmit and receive gains
 - Equalization
 - Digital I/O pins
 - A-law/ μ -law and linear selection
- Supports internal balanced ringing with offset
 - Self-contained ringing generation and control
 - Integrated ring-trip filter and software enabled manual or automatic ring-trip mode
- Supports metering generation with envelope shaping
- Polarity reversal
- Supports both loop-start and ground-start signaling
- Exceeds central office requirements
- Selectable PCM or GCI interface
 - Supports most available master clock frequencies from 512 kHz to 8.192 MHz
- On-hook transmission
- Power/service denial mode
- Line-feed characteristics independent of battery voltage
- Only 5 V, 3.3 V and battery supplies needed
- Low idle-power per line
- Linear power-feed
- Compatible with inexpensive protection networks; Accommodates low-tolerance fuse resistors while maintaining longitudinal balance
- Monitors two-wire interface voltages and currents
- Power-cross and fault detection
- Integrated self-test features and built-in voice-path test modes
 - Echo gain, distortion, and noise
- Guaranteed performance over commercial temperature range.
- Small physical size

Chip Set Block Diagram - Two Channel Line Card Example



CONNECTION DIAGRAM



Note:

Pin1 is marked for orientation.

RSVD = Reserved. Do not connect to this pin.

PIN DESCRIPTIONS

Pin	Pin Name	I/O	Description
AD, BD	A, B Line Drivers	O	Provide the currents to the A and B leads of the subscriber loop.
BGND	Ground		Ground return for high and low battery supplies.
CREF	+3.3 VDC		VCCD reference. It is the digital high logic supply rail, used by the ISLIC device to ISLAC device interface.
GND	Ground		Analog and digital ground return for VCC.
HPA, HPB	High-Pass Filter Capacitor	O	These pins connect to CHP, the external high-pass filter capacitor that separates the DC loop-voltage from the voice transmission path.
ILG	Longitudinal Current Sense	O	ILG is proportional to the common-mode line current ($I_{AD} - I_{BD}$), except in disconnect mode, where ILG is proportional to the current into grounded SB.
IMT	Metallic Current Sense	O	IMT is proportional to the differential line current ($I_{AD} + I_{BD}$), except in disconnect mode, where IMT is proportional to the current into grounded SA. The Am79R240 device indicates thermal overload by pulling IMT to CREF.
LD	Register Load	I	The LD pin controls the input latch and responds to a 3-level input. When the LD pin is a logic 1 ($< (V_{REF} + 0.3 \text{ V})$), the logic levels on P1 – P3 latch into the Am79R240 device control register bits that operate the mode-decoder. When the LD pin level is at $< V_{REF} \pm 0.3 \text{ V}$, the control register contents are locked.
P1 – P3	Control Bus	I	Inputs to the latch for the operating-mode decoder and the relay-drivers.
RSN	Receive Summing Node	I	The metallic current between AD and BD is equal to 500 times the current into this pin. Networks that program receive gain and two-wire impedance connect to this node. This input is at a virtual potential of VREF.
RSVD	Reserved		This is used during Legerity testing. In the application, these pins must be left floating.
SA, SB	A, B Lead Voltage Sense	I	Sense the voltages on the line side of the fuse resistors at the A and B leads. External sense resistors, RSA and RSB, protect these pins from lightning or power-cross.
VBH	Battery (Power)		Connection to high-battery supply used for ringing and long loops. Connects to the substrate. When only a single battery is available, it connects to both VBH and VBL.
VBL	Battery (Power)		Connection to low-battery supply used for short loops. When only a single battery is available, this pin can be connected to VBH.
VCC	+5 V Power Supply		Positive supply for low voltage analog and digital circuits in the Am79R240 device.
VREF	1.4 V Analog Reference	I	The ISLAC chip provides this voltage which is used by the Am79R240 device for internal reference purposes. All analog input and output signals interfacing to the ISLAC chip are referenced to this pin.
VSAB	I_{LOOP} Voltage	O	Scaled-down version of the voltage between the sense points SA and SB on this pin.
VTX	4-Wire Transmit Signal	O	The voltage between this pin and VREF is a scaled down version of the AC component of the voltage sensed between the SA and SB pins. One end of the two-wire input impedance programming network connects to VTX. The voltage at VTX swings positive and negative with respect to VREF.

Absolute Maximum Ratings

Stresses greater than those listed under Absolute Maximum Ratings can cause permanent device failure. Functionality at or above these limits is not implied. Exposure to absolute maximum ratings for extended periods can affect device reliability.

Storage temperature	–55 to +150°C
Ambient temperature, under bias	0 to 70°C
Humidity	5% to 95%
V _{CC} with respect to GND	–0.4 to +7 V
V _{BH} , V _{BL} with respect to GND (See Note 2)	+0.4 to –95 V
BGND with respect to GND	–3 to +3 V
AD or BD to BGND: Continuous 10 ms (F = 0.1 Hz) 1 μs (F = 0.1 Hz) 250 ns (F = 0.1 Hz)	V _{BH} – 1 to BGND + 1 V _{BH} – 5 to BGND + 5 V _{BH} – 10 to BGND + 10 V _{BH} – 15 to BGND + 15
Current into SA or SB: 10 μs rise to I _{PEAK} 1000 μs fall to 0.5 I _{PEAK} 2000 μs fall to I = 0	I _{PEAK} = ±5 mA
Current into SA or SB: 2 μs rise to I _{PEAK} 10 μs fall to 0.5 I _{PEAK} 20 μs fall to I = 0	I _{PEAK} = ±12.5 mA
SA SB continuous	5 mA
Current through AD or BD	± 150 mA
P1, P2, P3, LD to GND	–0.4 to V _{CC} + 0.4 V
ESD Immunity (Human Body Model)	1500 V min
Maximum power dissipation (See Note 1)	T _A = 70°C 1.67 W

Note:

1. Thermal limiting circuitry on chip will shut down the circuit at a junction temperature of about 165°C. Operation above 145°C junction temperature may degrade device reliability.
2. Rise time of V_{BH} (dv/dt) must be limited to less than 27 v/μs.

Thermal Resistance

The junction to air thermal resistance of the Am79R240 device in a 32-pin, PLCC package is 45°C/W. The typical junction to case thermal resistance is 14°C/W. Measured under free air convection conditions and without external heat sinking.

Electrical Operating Ranges

Legerity guarantees the performance of this device over commercial (0°C to 70°C) temperature ranges by conducting a production test with single insertion coupled to periodic sampling. These characterization and test procedures comply with section 4.6.2 of Bellcore TR-TSY-000357 Component Reliability Assurance Requirements for Telecommunications Equipment.

Environmental Ranges

Ambient Temperature	0 to 70°C Commercial
Ambient Relative Humidity	15 to 85%

Electrical Ranges

Voltage at VCC	5 V ± 5%
Voltage at VBL	–15 V to VBH
Voltage at VBH	–42.5 V to –90 V
BGND with respect to GND	–100 mV to +100 mV
Load resistance on VTX to VREF	20 kΩ minimum
Load resistance on VSAB to VREF	20 kΩ minimum

SPECIFICATIONS

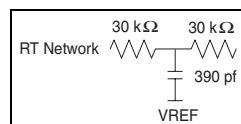
Power Dissipation

Loop resistance = 0 to ∞ unless otherwise noted (not including fuse resistors), 2 x 50 Ω fuse resistors, BATL = -24 V, BATH = -90 V, VCC = +5 V. For power dissipation measurements, DC-feed conditions are as follows:

- I_{LA} (active mode current limit) = 25 mA (I_{RSN} = 50 μ A)
- R_{FD} (feed resistance) = 500 Ω
- V_{AS} (anti-sat activate voltage) = 10 V
- V_{APP} (apparent battery voltage) = 48

Description	Test Conditions		Min	Typ	Max	Unit
Power Dissipation Normal Polarity	On-Hook Disconnect			55	80	mW
	On-Hook Standby			80	125	
	On-Hook Transmission Fixed Longitudinal Voltage	ISLIC		175	250	
	On-Hook Active High Battery	ISLIC		340	450	
	Off-Hook Active Low Battery R_L = 294 Ω	ISLIC		900	1050	
Power Supply Currents	On-Hook Disconnect	VBH		0.4	0.7	mA
		VBL		0.1		
		VCC		3.0	4.0	
	On-Hook Standby	VBH		0.75	1.2	
		VBL		0		
		VCC		3.1	4.0	
	On-Hook Transmission Fixed Longitudinal Voltage	VBH		1.85	3.0	
		VBL		0		
		VCC		5	6.5	
	On-Hook Active High Battery	VBH		3.6	5.0	
		VBL		0		
		VCC		7.3	8.5	
	Off-Hook Active Low Battery R_L = 294 Ω	VBH		0.9	2.0	
		VBL		26.9		
		VCC		7.5	10	

DC SPECIFICATIONS



Unless otherwise specified, test conditions are: $V_{CC} = 5\text{ V}$, $BATH = -90\text{ V}$, $BATL = -24\text{ V}$, $R_{RX} = 150\text{ k}\Omega$, $R_L = 600\text{ }\Omega$, $R_{SA} = R_{SB} = 200\text{ k}\Omega$, $R_{FA} = R_{FB} = 50\text{ }\Omega$, $C_{HP} = 22\text{ nF}$, $C_{AD} = C_{BD} = 22\text{ nF}$, $I_{RSN} = 50\text{ mA}$, Active low battery. DC-feed conditions are normally set by the ISLAC device. When the Am79R240 device is tested by itself, its operating conditions must be simulated as if it were connected to an ideal ISLAC device.

No.	Item	Condition	Min	Typ	Max	Unit	Note
1	Two-wire loop voltage (including offset)	Standby mode, open circuit, $ V_{BH} < 55\text{ V}$ $ V_{BH} > 55\text{ V}$ $GND - V_B$ Active mode, $R_L = 600\text{ }\Omega$, $I_{RSN} = 20\text{ }\mu\text{A}$	$V_{BH} - 8$ 48 13.5	$V_{BH} - 7$ 51 15	$V_{BH} - 6$ 55.5 56.5 16.5	V	2
2	Feed resistance per leg at pins AD & BD	Standby mode	130	250	375	W	2
3	Feed current limit	Standby mode, $R_L = 600\text{ }\Omega$	18	34	45	mA	
	IMT current	Standby mode, $R_L = 2200\text{ }\Omega$	44.6	56		μA	
	ILG current	Standby mode A to V_{BH} B to Ground	28 28				
4	Ternary input voltage boundaries for LD pin. Mid-level input source must be V_{ref} .	Low boundary High boundary Input high current Input low current Mid-level current	$C_{REF} - 1$	108 47 51	$V_{REF} + 0.3$	V V μA μA μA	2 2 2
5	Logic Inputs P1, P2, P3	Input high voltage Input low voltage Input high current Input low current	2.0 -20 -20	0 0	0.8 20 20	V V μA μA	
6	VTX output offset		-50	0	+50	mV	
7	VREF input current	$V_{REF} = 1.4\text{ V}$		50		μA	2
8	CREF input current	$C_{REF} = 3.3\text{ V}$	-3	0	3	μA	2
9	β , DC Ratio of V_{SAB} to loop voltage: $\beta = \frac{V_{SAB}}{V_{SA} - V_{SB}}$	$T_j < 145^\circ\text{C}$, $V_{SA} - V_{SB} = 22\text{ V}$	0.0088	0.0097	0.0106	V/V	
10	I_{LOOP}/I_{MT}	$I_{LOOP} = 10\text{ mA}$	275	300	325	A/A	
11	I_{LONG}/I_{LG}	$I_{LONG} = 10\text{ mA}$	560	605	650	A/A	
12	Input current, SA and SB pins	Active modes		1.0	3.0	μA	2
13	K1	Incremental DC current gain	462.5	500	537.5	A/A	2

Transmission Specifications

No.	Item	Condition	Min	Typ	Max	Unit	Note
1	RSN input impedance	f = 300 to 3400 Hz		1		Ω	2
2	VTX output impedance			3			
3	Max, AC + DC loop current	Active High Battery or Active Low Battery	50			mA	2
4	Longitudinal impedance, A or B to GND	Active mode		70	135	Ω	2
5	2-4 wire gain	-10 dBm, 1 kHz, 0 to 70°C	14.18	13.98	13.78	dB	
6	2-4 wire gain variation with frequency	300 to 3400 Hz, relative to 1 kHz	-0.15		+0.15		
7	2-4 wire gain tracking	+3 dBm to -55 dBm Reference: -10 dBm	-0.15		+0.15		5
8	4-2 wire gain	-10 dBm, 1 kHz	-0.20		+0.20		
9	4-2 wire gain variation with frequency	300 to 3400 Hz, relative to 1 kHz	-0.1		+0.1		
10	4-2 wire gain tracking	+3 dBm to -55 dBm Reference: -10 dBm	-0.15		+0.15		5
11	Total harmonic distortion level 2-wire	300 Hz to 3400 Hz 0 dBm			-50	dB	3
	4-wire	-14 dBm			-48	dB	2
	4-wire overload level at VTX OHT	$R_{LOAD} = 600 \Omega$ $V_{AB} = 50 V$ 0 dBm		± 1 -50		Vp	2
						dB	2
12	Idle channel noise C-message	Active modes, $R_L = 600 \Omega$					
		2-wire		+9	+12	dBrnC	2
	Psophometric Weighted	4-wire		-5		dBrnC	2
		2-wire		-8	-78	dBmp	
13	Longitudinal balance (IEEE method) Active	L - T 200 to 3400 Hz	52			dB	
		T - L 200 to 3400 Hz	40				
14	PSRR (VBH, VBL)	50 to 3400 Hz 3.4 to 50 kHz	25	45 40			3, 4 1, 2, 4
15	PSRR (VCC)	50 to 3400 Hz 3.4 to 50 kHz	25	45 35			3, 4 1, 2, 4
16	Longitudinal AC current per wire	F = 15 to 60 Hz Active mode	10			mArms	2
17	Metering distortion	Freq = 12 kHz 0.5 Vrms Freq = 16 kHz Metering load = 200 Ω	40			dB	2

Ringin Specifications

Item	Condition	Min	Typ	Max	Unit	Note
Ringin Voltage	Active internal ringin		VBH + 6		V	7

Current-Limit Behavior

SLIC Mode	Condition	Min	Typ	Max	Unit	Note
Disconnect	Applied fault between ground and T/R		1	100	μA	6
Tip Open	Ring Short to GND	24	35	46	mA	
Standby	Short Tip to VBH	20	38	47		
	Short Ring to GND	20	35	44		
Active Ringin	ISLAC device generating internal ringin		100			2

Thermal Shutdown Fault Indications

Fault	Indication
No Fault	IMT operates normally ($V_{REF} \pm 1$ V)
Thermal Shutdown	KG, IMT above 2.8 V

Note:

- These tests are performed with the following load impedances:
Frequency < 12 kHz – Longitudinal impedance = 500 Ω ; metallic impedance = 300 Ω
Frequency > 12 kHz – Longitudinal impedance = 90 Ω ; metallic impedance = 135 Ω
- Not tested or partially tested in production. This parameter is guaranteed by characterization or correlation to other tests.
- This parameter is tested at 1 kHz in production. Performance at other frequencies is guaranteed by characterization.
- When the Am79R240 device and ISLAC device is in the anti-sat operating region, this parameter is degraded. The exact degradation depends on system design.
- 55 dBm gain tracking level not tested in production. This parameter is guaranteed by characterization and correlation to other tests.
- This spec is valid from 0 V to V_{BL} or –50 V, whichever is lower in magnitude.
- Other ringing voltage characteristics are set by the ISLAC device.

Operating Modes

The Am79R240 device receives multiplexed control data on the P1, P2 and P3 pins. The LD pin then controls the loading of P1, P2, and P3 values into the proper bits in the Am79R240 device control register. When the LD pin is less than 0.3 V below V_{REF} ($V_{REF} - 0.3$ V), P1–P3 must be low. When the LD pin is more than 0.3 V above V_{REF} ($V_{REF} + 0.3$ V), P1–P3 must contain ISLIC device control data C1, C2, and C3, which are latched into the Am79R240 device control register. Connecting the LD pin to VREF locks the contents of the Am79R240 device control register.

The operating mode of the Am79R240 device is determined by the C1, C2, and C3 bits in the control register of the Am79R240 device. The following table defines the Am79R240 device operating modes set by these signals.

Table 1. Operating Modes

C3	C2	C1	Operating Mode	Battery Voltage Selection	Operating Mode
0	0	0	Standby (See Note)	High Battery (BATH) and BGND	(High ohmic feed): Loop supervision active, A and B amplifiers shut down
0	0	1	Tip Open (See Note)	High Battery (BATH) and BGND	Tip Open: AD at High-Impedance, Channel A power amplifier shut down
0	1	0	On-Hook Transmission, Fixed Longitudinal Voltage	High Battery (BATH) and BGND	Fixed longitudinal voltage of –28 V
0	1	1	Disconnect	Low Battery selection at VBL	AD and BD at High-Impedance, Channel A and B power amplifiers shut down
1	0	0	RSVD		Active feed, normal or reverse polarity
1	0	1	Active High Battery	High Battery (BATH) and BGND	
1	1	0	Active Low Battery	Low Battery (BATL) and BGND	
1	1	1	Active Internal Ringing	High Battery (BATH) and BGND	Active internal ringing

Note:

In these modes, the ring lead (B-lead) output has a –50 V internal clamp to battery ground (BGND).

Operating Mode Descriptions

Operating Mode	Description
Disconnect	This mode disconnects both A and B output amplifiers from the AD and BD outputs. The A and B amplifiers are shut down and the Am79R240 device selects the low battery voltage at the VBL pin. In the Disconnect state, the currents on IMT and ILG represent the voltages on the SA and SB pins, respectively. These currents are scaled to produce voltages across RMTi and RLGi of $\frac{V_{SA}}{400}$ and $\frac{V_{SB}}{400}$, respectively.
Standby	The power amplifiers are turned off. The AD output is driven by an internal 250 Ω (typical) resistor, which connects to ground. The BD output is driven by an internal 250 Ω (typical) resistor, which connects to the high battery (BATH) at the VBH pin, through a clamp circuit, which clamps to approximately –50 V with respect to BGND. For VBH values above –55 V, the open-circuit voltage, which appears at this output is $\sim$ VBH + 7 V. If VBH is below –55 V, the voltage at this output is –50 V. The battery selection for the balance of the circuitry on the chip is VBL. Line supervision remains active. Current limiting is provided on each line to limit power dissipation under short-loop conditions as specified in “Current-Limit Behavior” on page 12. In external ringing, the standby ISLIC device state is selected.
Tip Open	In this mode, the AD (Tip) lead is opened and the BD (Ring) lead is connected to a clamp, which operates from the high battery on VBH pin and clamps to approximately –50 V with respect to BGND through a resistor of approximately 250 Ω (typical). The battery selection for the balance of the circuitry on the chip is VBL.
Active High Battery	In the Active High Battery mode, battery connections are connected as shown in Table 1. Both output amplifiers deliver the full power level determined by the programmed DC-feed conditions. Active High Battery mode is enabled during a call in applications when a long loop can be encountered.
Active Low Battery	Both output amplifiers deliver the full power level determined by the programmed DC-feed conditions. VBL, the low negative battery, is selected in the Active Low Battery mode. This is typically used during the voice part of a call.
Active Internal Ringing	In the Internal Ringing mode, the Am79R240 device selects the battery connections as shown in Table 1. When using internal ringing, both the AD and BD output amplifiers deliver the ringing signal determined by the programmed ringing level.
On-Hook Transmission (OHT), Fixed Longitudinal Voltage	In the On-Hook Transmission, Fixed Longitudinal Voltage mode, battery connections are connected as shown in Table 1. The longitudinal voltage is fixed at the voltage (also in the table above) to allow compliance with safety specifications for some classes of products.

Thermal-Management Equations

Applies to all modes except Standby, which has no thermal management.

$$I_L < 5 \text{ mA}$$

$$P_{SLIC} = (S_{BAT} - I_L(R_L + 2R_{FUSE})) \cdot I_L + 0.3 \text{ W}$$

$$P_{RTMG} = 0$$

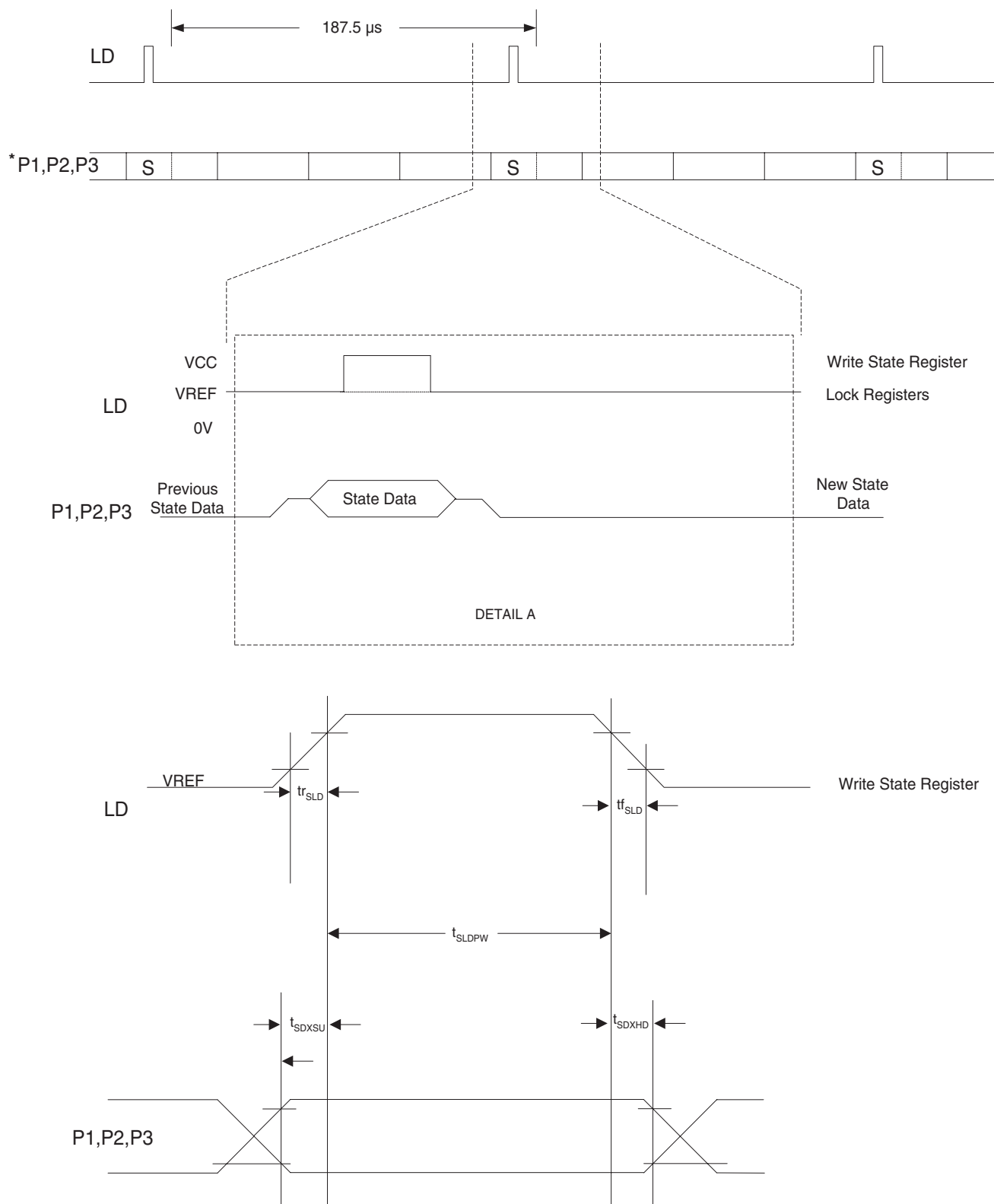
TIMING SPECIFICATIONS

Symbol	Signal	Parameter	Min	Typ	Max	Unit
t_{rSLD}	LD	Rise time Am79R240 device LD pin			2	μs
t_{fSLD}	LD	Fall time Am79R240 device LD pin			2	
t_{SLDPW}	LD	LD minimum pulse width	3			
t_{SDXSU}	P1,P2,P3	P1–P3 data Setup time	4.5			
t_{SDXHD}	P1,P2,P3	P1–P3 data hold time	4.5			

Note:

1. The P1–P3 pins are updated continuously during operation by the LD signal.
2. When writing to the ISLIC device registers, the sequence is:
 - a) Set LD pin to mid-state
 - b) Place appropriate data on the P1–P3 pins
 - c) Assert the LD pin to High to write the proper data
 - d) Return LD pin to mid-state
3. Am79R240 device registers are refreshed at 5.33 kHz when used with an ISLAC device.
4. If the clock or MPI becomes disabled, the LD pins and P1–P3 returns to 0 V state, thus protecting the Am79R240 device and the line connection.
5. Not tested in production. Guaranteed by characterization.

WAVEFORMS

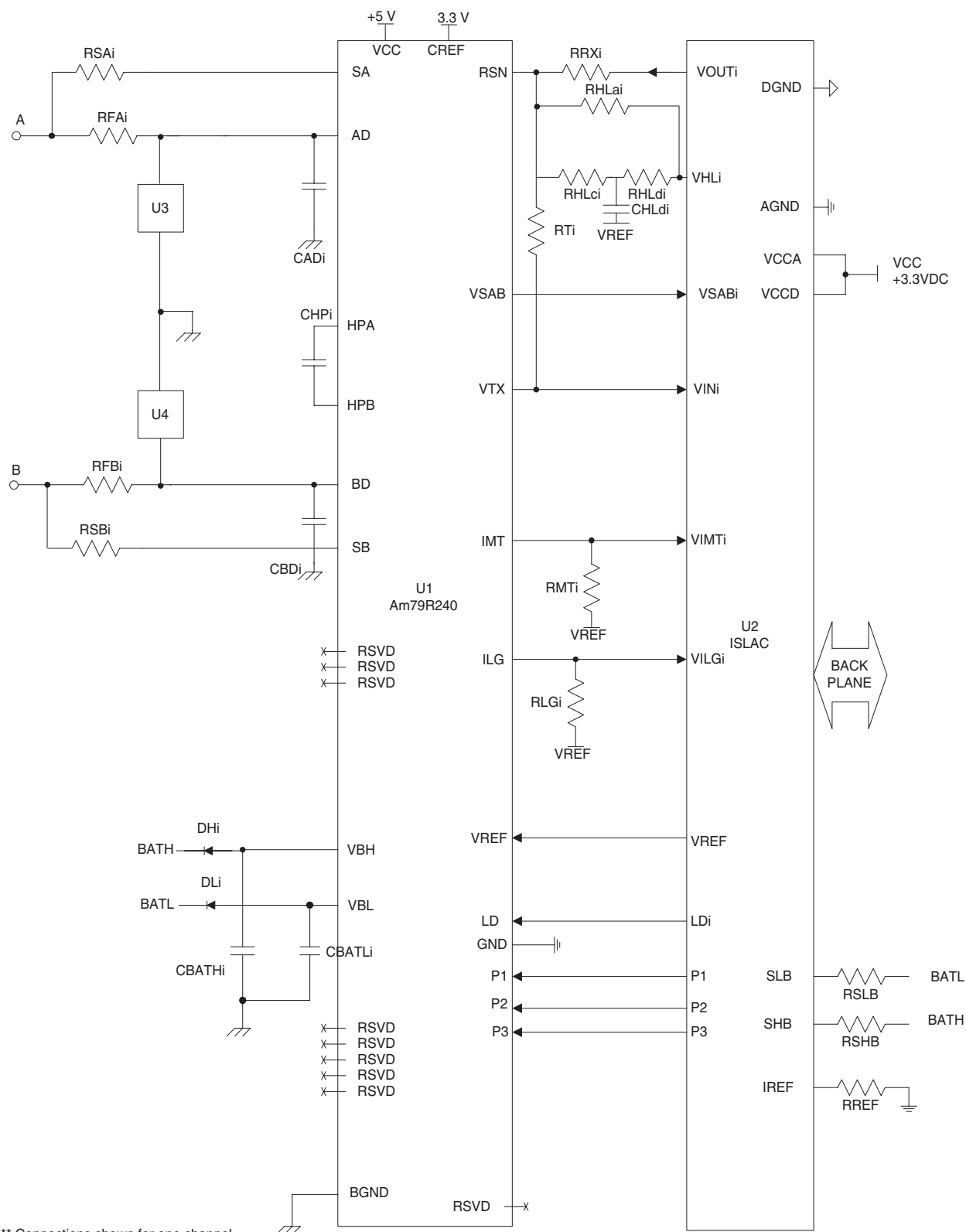


***Note:**

When the LD pin is less than 0.3 V below V_{REF} P1-P3 must be low.

APPLICATION CIRCUIT

Internal Ringing



** Connections shown for one channel

LINE CARD PARTS LIST

The following list defines the parts and part values required to meet target specification limits for channel i of the line card ($i = 1, 2$).

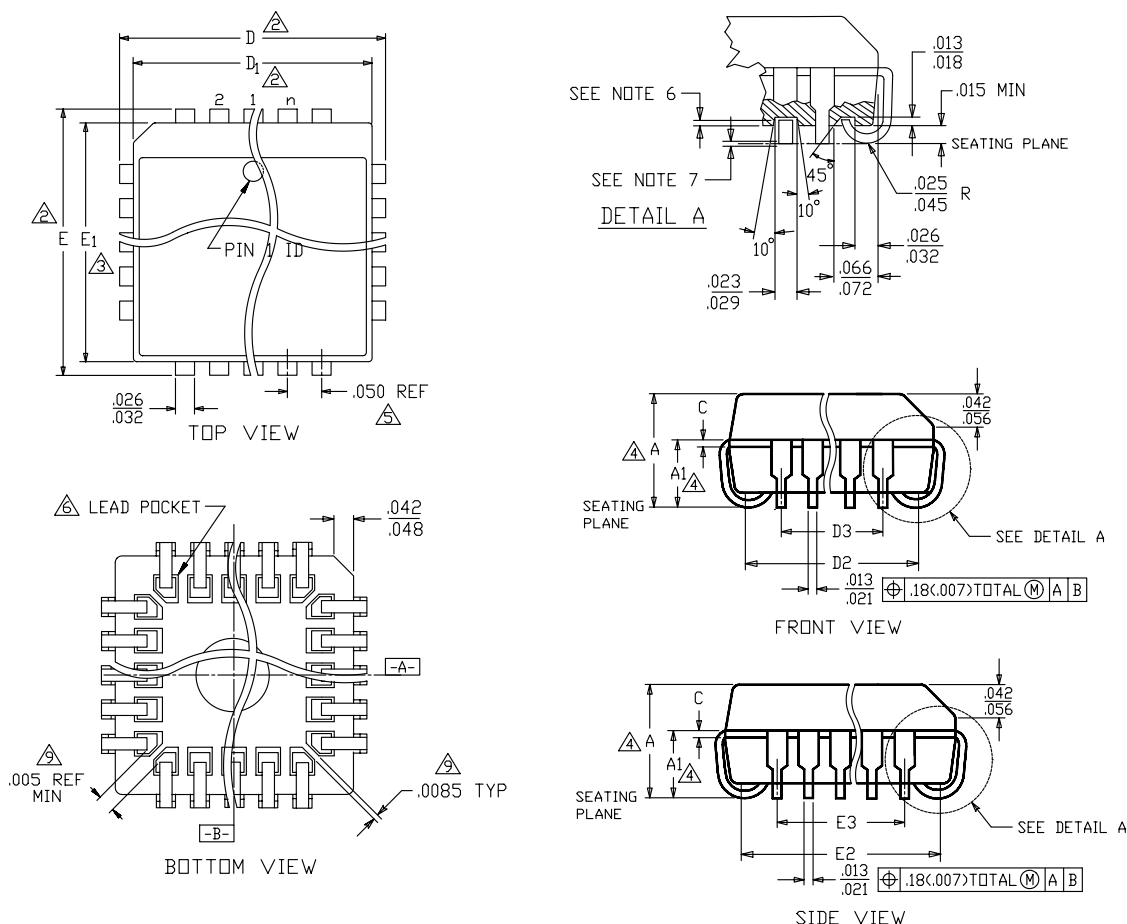
Item	Type	Value	Tol.	Rating	Comments
U1	Am79R240				ISLIC device
U2	Am79D22xx				ISLAC device
U3, U4	P0741SA				TECCOR protector
DHi, DLi	Diode	100 mA		100 V	50 ns
RFAi, RFBi	Resistor	50 Ω	5%	2 W	Fusible PTC protection resistors
RSAi, RSBi	Resistor	200 k Ω	2%	1/4 W	Sense resistors
RTi	Resistor	80.6 k Ω	1%	1/10 W	
RRXi	Resistor	100 k Ω	1%	1/10 W	
RREF	Resistor	69.8 k Ω	1%	1/10 W	Current reference
RSHB, RSLB, RSPB	Resistor	750 k Ω	1%	1/8 W	
RHLai	Resistor	40.2 k Ω	1%	1/10 W	
RHLci	Resistor	2.87 k Ω	1%	1/10 W	
RHLdi	Resistor	2.87 k Ω	1%	1/10 W	
CHLdi	Capacitor	0.82 μ F	10%	10 V	Ceramic
RMTi	Resistor	3.01 k Ω	1%	1/8 W	
RLGi	Resistor	6.04 k Ω	1%	1/8 W	
CADi, CBDi	Capacitor	22 nF	10%	100 V	Ceramic, not voltage sensitive
CBATHi, CBATLi	Capacitor	100 nF	20%	100 V	Ceramic
CHPi	Capacitor	22 nF	20%	100 V	Ceramic
CVC	Capacitor	100 nF	20%	50 V	Ceramic

Note:

1. Value can be adjusted to suit application.
2. Can be looser for relaxed ring-trip requirements.

PHYSICAL DIMENSIONS

PL 032



PACKAGE	PL 032	
JEDEC	MO-052(A)AE	
SYMBOL	MIN	MAX
A	.125	.140
A1	.080	.095
D	.485	.495
D1	.447	.453
D2	.390	.430
D3	.300	REF
E	.585	.595
E1	.547	.553
E2	.490	.530
E3	.400	REF
C	.009	.015

NOTES:

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- ALL DIMENSIONS ARE IN INCHES.
- DIMENSIONS "D" AND "E" ARE MEASURED FROM OUTERMOST POINT.
- DIMENSIONS D1 AND E1 DO NOT INCLUDE CORNER MOLD FLASH. ALLOWABLE CORNER MOLD FLASH IS .010"
- DIMENSIONS "A", "A1", "D2" AND "E2" ARE MEASURED AT THE POINTS OF CONTACT TO BASE PLANE
- LEAD SPACING AS MEASURED FROM CENTERLINE TO CENTERLINE SHALL BE WITHIN $\pm .005$ ".
- J-LEAD TIPS SHOULD BE LOCATED INSIDE THE "POCKET".
- LEAD COPLANARITY SHALL BE WITHIN .004" AS MEASURED FROM SEATING PLANE. COPLANARITY IS MEASURED PER AMD 06-500.
- LEAD TWEEZE SHALL BE WITHIN .0045" ON EACH SIDE AS MEASURED FROM A VERTICAL FLAT PLANE. TWEEZE IS MEASURED PER AMD 06-500.
- LEAD POCKET MAY BE RECTANGULAR (AS SHOWN) OR OVAL. IF CORNER LEAD POCKETS ARE CONNECTED THEN 5 MILS MINIMUM CORNER LEAD SPACING IS REQUIRED.

REVISION HISTORY

Revision B to C

- Applied new format.
- Added 5 REN statement and sub-bullets to “Distinctive Characteristics”
- Corrections to “Internal Ringing Application Circuit”
- Changed limits for *On-Hook Standby, Power Dissipation Normal Polarity* in “Power Dissipation” table.
- New value for VBL in “Electrical Ranges” table.
- Added V_{RING} condition to row 1 in “DC Specifications” table. Also provided min values for row 3, and created rows 15 and 16.
- Added max value for row 4 in “Transmission Specifications” table. Also changed min and max for row 6.
- Supplied ringing voltage in “Ringing Specifications” table.
- Supplied max values in “Current-Limit Behavior” table.
- Imported correct graphics for “Physical Dimensions.”

Revision C to D

- “Distinctive Characteristics changed to “Features.” 5 REN bullet changed from 9.2 to 9.55 kft and from 14.6 to 15.2 kft. Diameter information deleted from 5 REN bullet.
- “Environmental Ranges,” and “Chip Set Features” new temperature statement.
- Updated “Internal Ringing” Application Circuit for component “CBATLi” circuitry.
- “Waveforms,” new image.

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