Preliminary

Am82525

High-Level Serial Communications Controller Extended (HSCX)

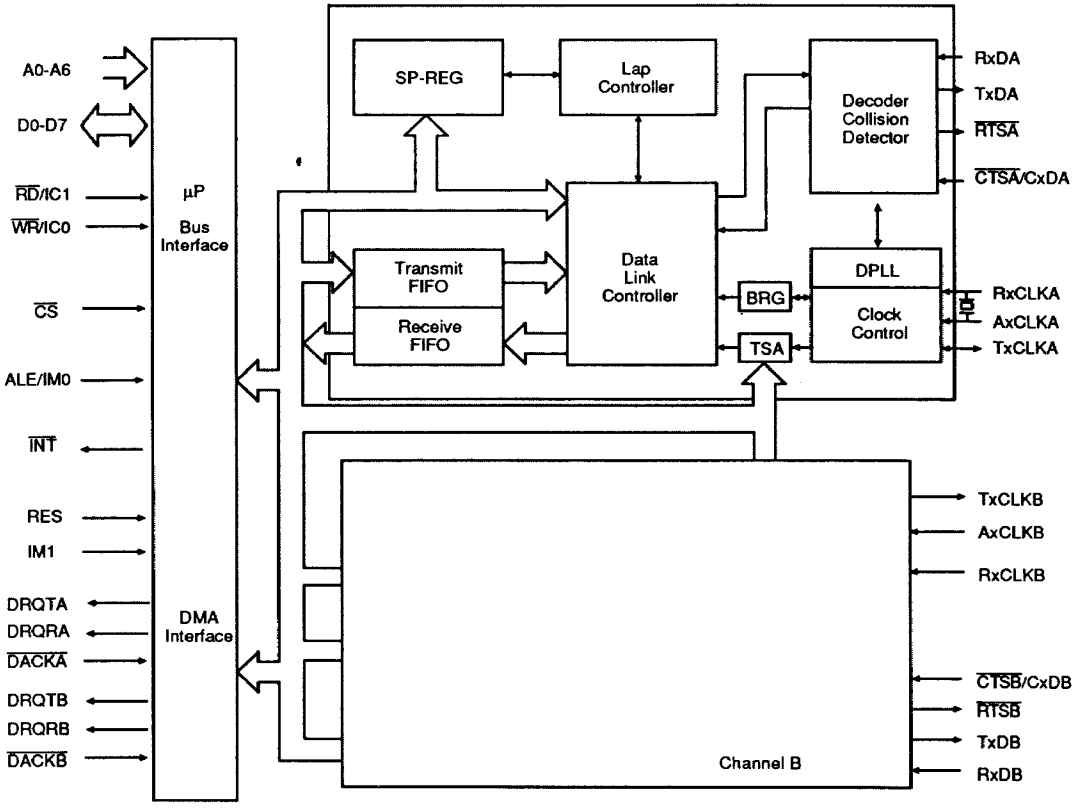
Advanced Micro Devices

DISTINCTIVE CHARACTERISTICS

Serial Interface

- Two independent full-duplex HDLC channels
- On-chip clock generation or external clock source
- On-chip DPLL for clock recovery for each channel
- On-chip baud rate generators for each channel
- Independent time slot assignment for each channel with programmable time slot length (1–256 bit)
- Different modes of data encoding (NRZI, NRZ)
- Modem control lines ($\overline{RTS}$, $\overline{CTS}$, $\overline{CD}$)
- Support of bus configuration by collision resolution

BLOCK DIAGRAM



11139–001B

Publication # 11139 Rev. B Amendment /0
Issue Date: May 1989

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DISTINCTIVE CHARACTERISTICS (Continued)

- Programmable bit inversion
- Transparent receive/transmit of data without HDLC framing
- Cyclic transmission mode (1 to 32 bytes possible)
- Data rate up to 4 Mbps

Protocol Support

- Auto mode
- Non-auto mode
- Transparent mode
- Handling of bit-oriented functions in all modes
- LAPB/LAPD/SDLC/HDLC procedural support in auto mode (I- and S-frame handling)
- Modulo 8 or modulo 128 operation
- Programmable timeout and retry conditions
- Programmable maximum packet size checking

Microprocessor Interface

- 64-byte FIFOs per channel and direction
- Storage capacity of up to 17 short frames in receive direction
- Efficient transfer of data blocks from/to system memory by DMA or interrupt request
- 8-bit demultiplexed or multiplexed bus interface
- Intel or Motorola type microprocessor interface

General

- Compatible to Am82520 (HSCC)
- Advanced CMOS technology
- Low power consumption
  - active 25 mW at 4 MHz
  - standby 4 mW

GENERAL DESCRIPTION

The Am82525 HSCX is a High-Level Serial Communications Controller with extended features and functionality. The HSCX is compatible to the Am82520 HSCC.

The HSCX has been designed to implement high-speed communication links using HDLC protocols and to reduce the hardware and software overhead needed for serial synchronous communications.

Due to its 8-bit adaptive bus interface it fits into every AMD/Siemens/Intel or Motorola 8- or 16-bit microcontroller or microprocessor system. The data throughput from/to system memory is optimized for transferring blocks of data (up to 32 bytes) by means of DMA or interrupt request. Together with the storing capacity of up to 64 bytes in on-chip FIFOs, the serial interfaces are effectively decoupled from the system bus which drastically reduces the dynamic load and reaction time of the CPU.

The HSCX directly supports the X.25 LAPB, the ISDN LAPD, and SDLC (Normal Response Mode) protocols and is capable of handling a large set of OSI layer 2 protocol functions independently from the host processor. Furthermore, the HSCX opens a wide area for applications which use time division multiplex methods; e.g, time-slot oriented PCM systems, systems designed for packet switching, and ISDN applications, by its programmable telecom-specific features.

The HSCX is available in a 44-pin PLCC package.

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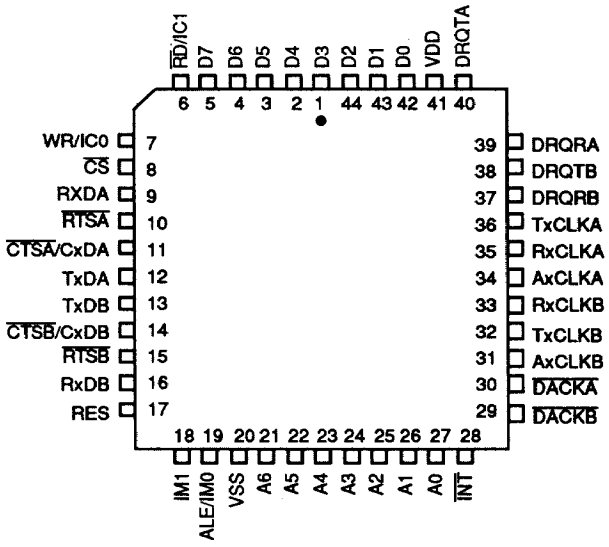
CONNECTION DIAGRAM
Top View

44-Pin PLCC



Note: Pin is marked for orientation.

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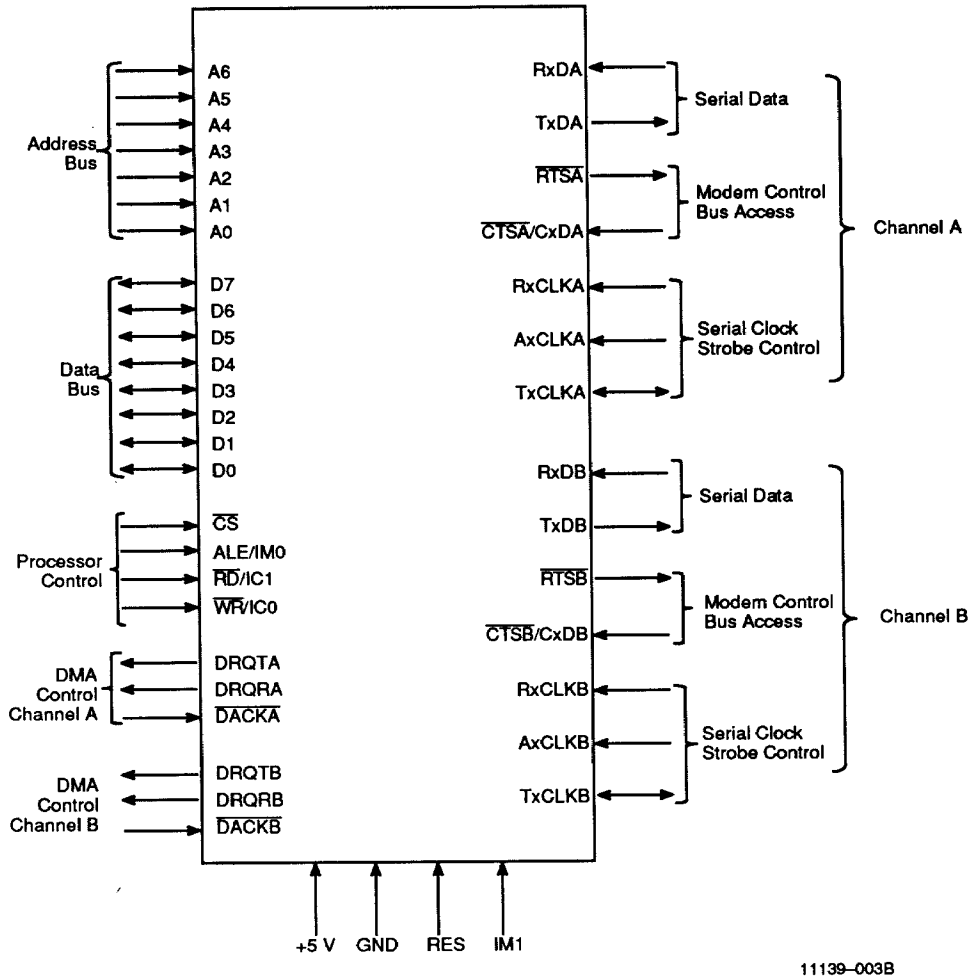
LOGIC SYMBOL



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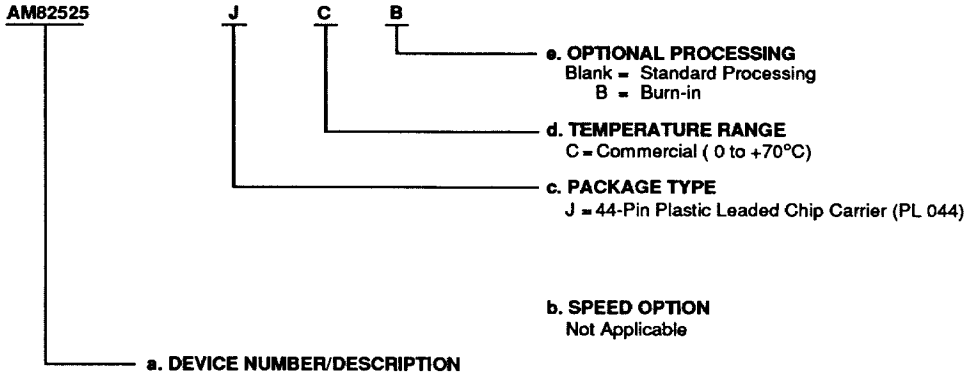
ORDERING INFORMATION
Standard Products

AMD standard products are available in several packages and operating ranges. The ordering number (Valid Combination) is formed by a combination of:

a. Device Number
b. Speed Option (if applicable)
c. Package Type
d. Temperature Range
e. Optional Processing



Valid Combinations	
AM82525	JC, JCB

Valid Combinations

Valid Combinations list configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations, to check on newly released combinations, and to obtain additional data on AMD's standard military grade products.

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PIN DESCRIPTION

D0–D7

Data Bus (Input/Output)

The Data Bus lines are bi-directional three-state lines which interface with the system's Data Bus. These lines carry data and commands status to and from the HSCX.

$\overline{RD}$/IC1

Read, Intel Bus Mode (IM1 connected to LOW) (Input)

This signal indicates a Read operation. When the HSCX is selected via $\overline{CS}$, the $\overline{RD}$ enables the bus driver to put data from an internal register addressed by A0–A6 on the Data Bus.

When the HSCX is selected for DMA transfers with $\overline{DACK}$, the $\overline{RD}$ signal enables the bus drivers to put data from the respective Receive FIFO on the Data Bus, and Inputs to A0–A6 are ignored.

INPUT CONTROL 1, Motorola Bus Mode (IM1 connected to HIGH.)

If Motorola Bus Mode has been selected, this pin serves as one of the following inputs (depending on the selection with IM0) to control Read/Write operations:
E = Enable, active HIGH (IM0 tied LOW) or
$\overline{DS}$ = Data Strobe, active LOW (IM0 tied HIGH)

$\overline{WR}$/IC0

Write, Intel Bus Mode (Input)

This signal indicates a Write operation. When $\overline{CS}$ is active the HSCX loads an internal register with data provided from the Data Bus. When $\overline{DACK}$ is active for DMA transfers, the HSCX loads data from the Data Bus on the top of the respective transmit FIFO.

INPUT CONTROL 0, Motorola Bus Mode

In Motorola Bus Mode, this pin serves as the R/W input to distinguish between Read or Write operations.

$\overline{CS}$

Chip Select (Input)

A LOW signal selects the HSCX for a Read/Write operation.

RXDA, RXDB

Receive Data (Channel A/Channel B) (Input)

Serial data is received on these pins at standard TTL or CMOS levels.

$\overline{RTSA}$, $\overline{RTSB}$

Request to Send (Channel A/Channel B) (Input)

When the $\overline{RTS}$ bit in the MODE register is set, the $\overline{RTS}$ pin goes LOW. When the $\overline{RTS}$ bit is reset, $\overline{RTS}$ goes HIGH if the transmitter has finished and there is no further request for transmission.

In the bus configuration, this pin can be programmed using CCR2 to:

–go LOW during the actual transmission of a frame shifted by one clock period, excluding collision bits.
–go LOW during the reception of data frame.
–stay always HIGH ($\overline{RTS}$ disabled).

$\overline{CTSA}$/CXDA

Clear to Send (Channel A/Channel B) (Input)

A LOW on the $\overline{CTS}$ input pin enables the respective transmitter. Additionally, an interrupt may be issued if a state transition occurs at the $\overline{CTS}$ pin. If no "Clear to Send" function is required, the $\overline{CTS}$ pins should be connected directly to GND.

$\overline{CTSB}$/CXDB

Collison Data (Channel A/Channel B) (Input)

In a bus configuration, the external serial bus must be connected to the respective CxD pin for collision detection.

TXDA, TXDB

Transmit Data (Channel A/Channel B) (Output)

Transmit Data is shifted out through these pins at standard TTL or CMOS levels. These pins can be programmed to work either as push-pull, or open drain outputs supporting bus configurations.

RES

Reset (Input)

A HIGH signal on this input forces the HSCX into the reset state. The HSCX is in power-up mode during reset and in power-down mode after reset. The minimum pulse which is 1.8 µs.

IM1

Input Mode 1 (Input)

By connecting this pin to either V_{SS} or V_{DD}, the bus interface can be adapted to either an AMD/Siemens/Intel or Motorola environment.
IM1 = LOW: Intel Bus Mode
IM1 = HIGH: Motorola Bus Mode

ALE/IM0

Address Latch Enable (Intel Bus Mode) (Input)

A HIGH on this line indicates an address on the external address/data bus, which will select one of the HSCX's internal registers. The address is latched by the HSCX with the falling edge of ALE. This allows the HSCX to be directly connected to a CPU with a multiplexed address/data bus compatible to Am82520 HSCC. The address input pins A0–A6 must be exernally connected to a CPU with a multiplexed address/data bus compatible to Am82520 HSCC. The address input pins A0–A6 must be externally connected to the data bus pins (D0–D6 for 8-bit CPUs, D1–D7 for 16-bit CPUs; that is, multiply all internal register addresses by 2).

Input Mode 0, Motorola Bus Mode

In Motorola bus mode, the level at this pin determines the function of the IC1 pin (see description of pin 6).

V_{SS}

Ground (Input)

0 V

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A0–A6

Address Bus (Input)

These inputs interface with seven bits of the system's address bus A3 to select one of the internal registers for read or write. They are usually connected at A0–A6 in 8-bit systems or at A1–A7 in 16-bit systems.

$\overline{INT}$

Interrupt Request (Output)

This signal is activated when the HSCX requests an interrupt. The CPU may determine the particular source and cause of the interrupt by reading the HSCX interrupt status registers (ISTA, EXIR).

$\overline{INT}$ is an open drain output; therefore, the interrupt request outputs of several HSCXs can be connected to one interrupt input in a "wired-or" combination. This pin must be connected to a pull-up register.

$\overline{DACKA}$/$\overline{DACKB}$

Acknowledge (Channel A/Channel B) (Input)

When LOW, this input signal from the DMA controller notifies the HSCX that the requested DMA cycle controlled via DRQxx (pins 37–40) is in progress; that is, the DMA controller has achieved bus mastership from the CPU and will start data transfer cycles (either Read or Write).

Together with $\overline{RD}$, if DMA has been requested from the receiver or with $\overline{WR}$, if DMA has been requested from the transmitter, this input works like $\overline{CS}$ to enable a data byte to be read from or written to the top of the receive or transmit FIFO of the specified channel.

IF $\overline{DACK}$n is active, the input pin A0–A6 is ignored and the FIFOs are implicitly selected. If the $\overline{DACK}$n signals are not used, these pins must be connected to V_{DD}.

AxCLKA, AxCLKB

Alternate Clock (Channel A/Channel B) (Input)

These pins realize several input functions. Depending on the selected clock mode, they may supply either a:

–CD (carrier detect) modem control or general purpose input. This pin can be programmed to function as receiver enable if the "auto start" feature is selected (CAS bit in XBCH set). The state at this pin can be read from the VSTR register, or

–a receive strobe signal (clock mode 1), or

–a frame synchronization signal in time-slot oriented operation mode (clock mode 5), or

–together with RxCLK, a crystal connection for the internal oscillator (clock mode 4, 6, 7).

TxCLKA, TxCLKB

Transmit Clock (Channel A/Channel B) (Input/Output)

The functions of these pins depend on the programmed clock clock, provided that the TSS bit in the CCR2 register is reset. Programmed as inputs (if the TIO bit in CCR2 is reset), they may supply either:

–the transmit clock for the respective channel (clock mode 0, 2, 6), or

–a transmit strobe signal (clock mode 1).

Programmed as outputs (if the TIO bit in CCR2 is set), the TxCLK pins supply either the:

–transmit clock of the respective channel which is generated either

- from the baud rate generator (clock mode 2, 6; TSS bit in CCR2 set), or
- from the DPLL circuit (clock mode 3, 7), or
- from the crystal oscillator (clock mode 4), or

–a tri-state control signal indicating the programmed transmit time slot (clock mode 5).

RxCLKA, RxCLKB

Receive Clock (Channel A/Channel B) (Input)

The function of these pins also depend on the programmed clock mode. In each channel, RxCLK may supply either:

–the receive clock (clock mode 0), or

–the receive and transmit clock (clock mode 1, 5), or

–the clock for the baud rate generator (clock mode 2, 3), or

–crystal connection for the internal oscillator (clock mode 4, 6, 7, together with AxCLKA).

DRQRA, DRQRB

DMA Request Receiver (Channel A/Channel B) (Output)

The receiver of the HSCX requests a DMA data transfer by activating this line. DRQRn remains HIGH as long as the receive FIFO requires data transfers, thus blocks of data (32, 16, 8, or 4 bytes) are transferred.

DRQRn is activated immediately following the falling edge of the last read cycle.

DRQTA, DRQTB

DMA Request Transmitter (Channel A/Channel B) (Output)

The transmitter of the HSCX requests a DMA data transfer by activating this line.

The DRQTn remains HIGH as long as the transmit FIFO requires data transfers.

The amount of data bytes to be transferred from system memory to the HSCX (byte count) must be written first to the XBCH, XBCL registers.

Blocks of data (n · 32 bytes + REST, n = 0, 1, . . .) are transferred until the byte count is reached.

DRQTn is deactivated immediately following the falling edge of the last $\overline{WR}$ cycle.

V_{DD}

Power (Input)

+5 V power supply.

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FUNCTIONAL DESCRIPTION

The HSCX comprises two completely independent full-duplex HDLC channels, Channel A and Channel B, supporting various layer 1 functions by means of an internal oscillator, baud rate generator (BRG), digital phase locked loop (DPLL), and time slot assignment (TSA) circuits.

Furthermore, layer 2 functions are performed by an on-chip LAP (link access procedure) data link controller.

The data link controller handles all functions necessary to establish and maintain an HDLC data link, such as:

- Flag insertion and detection
- Bit stuffing (zero-bit insertion/deletion)
- CRC generation and checking
- Address field recognition

Associated with each serial channel is a set of independent command and status registers (SP-REG) and 64-byte-deep FIFOs for transmit and receive direction.

DMA capability has been added to the HSCX by means of a 4-channel DMA interface with one DMA request line for each transmitter and receiver of both channels.

General

The HSCX distinguishes from other low-level HDLC devices by its advanced characteristics. The most important are:

- Support of different link configurations.

  Beyond the point-to-point configurations, the HSCX directly enables point-to-multipoint or multimaster configurations without additional hardware or software expense.

  In point-to-multipoint configurations, the HSCX can be used as a master as well as a slave station. Even when working as a slave station, the HSCX can initiate the transmission of data at any time. An internal function block provides the means of idle and collision detection, and collision resolution, which are necessary if several stations start transmitting simultaneously. A multimaster configuration is also possible.

- Support of layer 2 functions by HSCX.

  Besides those bit-oriented functions usually supported with the HDLC protocol such as bit stuffing, CRC check, flag and address recognition, the HSCX provides a high degree of procedural support.

  In a special operating mode (auto mode), the HSCX processes the information transfer and the procedure handshaking (I-, and S-frames of HDLC protocol) autonomously. The only restriction is that the window size (number of outstanding unacknowledged frames) is limited to 1. This will be sufficient in most applications. The communication procedures are mainly processed between the communication controllers and not between the processors; therefore, the dynamic load of the CPU and the software expense is largely reduced.

  The CPU is informed about the status of the procedure and has mainly to manage the receive and transmit data. In order to maintain cost effectiveness and flexibility, such functions as link setup/disconnection and error recovery in case of protocol errors (U-frames of HDLC protocols) are not implemented in hardware and must be done by user's software.

- Telecom-specific features.

  In a special operating mode, the HSCX can transmit or receive data packets in one of up to 64 time slots of programmable width (clock mode 5). Furthermore, the HSCX can transmit or receive variable data portions within a defined window of one or more clock cycles, which has to be selected by an external strobe signal (clock mode 1). These features make the HSCX especially suitable for all applications using time division multiplex methods such as time slot oriented PCM systems, systems designed for packet switching, or in ISDN applications.

- FIFO buffers for efficient transfer of data packets.

  The FIFO buffers used for the temporary storage of data packets transferred between the serial communications interface and the parallel system bus are another feature of the HSCX. Also because of the overlapping input/output operation (dual-port behavior), the maximum message length is not limited by the size of the buffer. Together with the DMA capability, the dynamic load of the CPU is drastically reduced by transferring the data packets block by block via direct memory access. The CPU only has to initiate the data transmission by the HSCX and determine the status in case of completely received frames but is not involved in data transfers.

Operating Modes

The HDLC controller of each channel can be programmed to operate in various modes, which are different in the treatment of the HDLC frame in receive direction. Thus, the receive data flow and the address recognition features can be effected in a very flexible way, which satisfies almost every requirement. There are six different operating modes which can be set by the mode register.

Auto Mode (MODE: MDS1, MDS0 = 00) — Characteristics: window size 1, random message length, address recognition.

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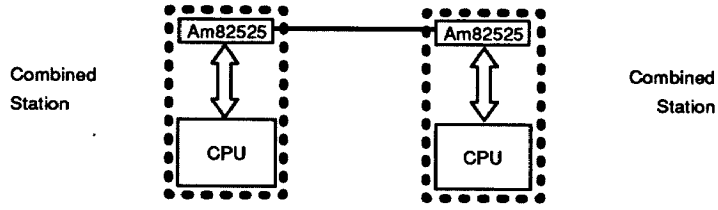
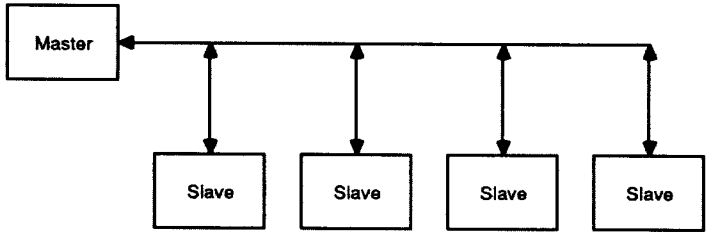
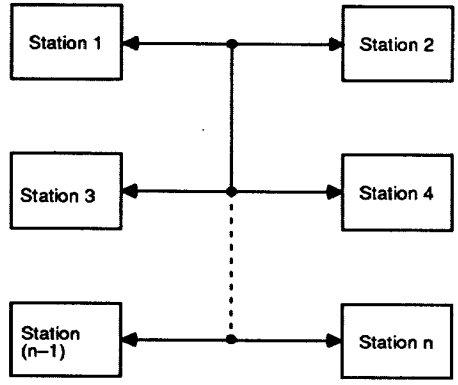


Point-to-Point Configuration



Point-to-Multipoint Configuration



Multimaster Configuration

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Figure 4. Link Configurations

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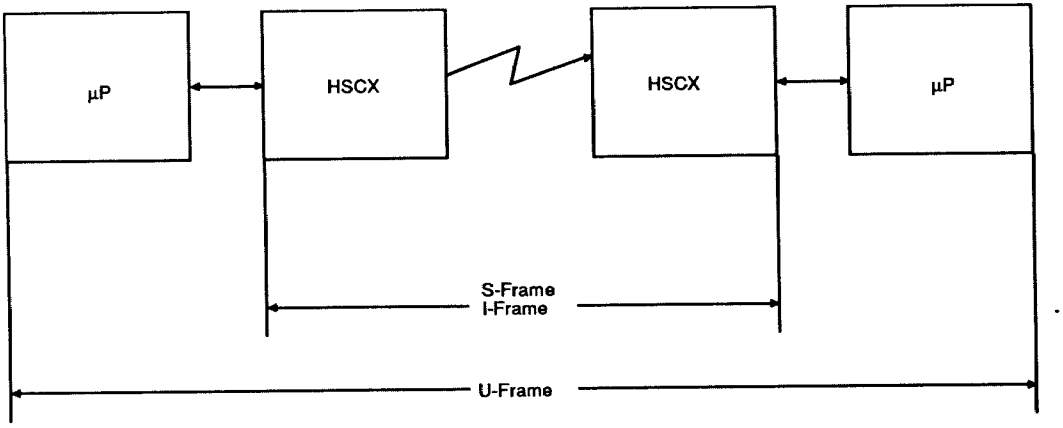

Figure 5. Procedural Support in Auto Mode

The HSCX processes autonomously all numbered frames (S-, I-frames) of an HDLC procedure. The HDLC control field, data in the I-field of the frames, and an additional status byte is temporarily stored in the RFIFO. The HDLC control field as well as additional information can also be read from special registers (RHCR, RSTA).

According to the selected address mode, the HSCX can perform a 2-byte or 1-byte address recognition. If a 2-byte address field is selected, the high address byte is compared with the fixed value FEH or FCH (group address) as well as with two individually programmable values in RAH1 and RAH2 registers. According to the ISDN LAPD protocol, bit 1 of the high byte address will be interpreted as command/response bit (C/R), depending on the setting of the CRI bit in RAH1, and will be excluded from the address comparison.

Similarly, two compare values can be programmed in special registers (RAL1, RAL2) for the low address byte. A valid address will be recognized in case the high and low byte of the address field correspond to one of the compare values. The HSCX can be called (addressed) with six different address combinations; however, only the logical connection identified through the address combination RAH1, RAL1 will be processed in the auto mode. All others will be processed in the non-auto mode. HDLC frames with address fields that do not match with any of the address combinations are ignored by the HSCX.

In case of a 1-byte address, RAL1 and RAL2 will be used as compare registers. According to the X.25 LAPB protocol, the value in RAL1 will be interpreted as command and the value in RAL2 as response.

Non-Auto Mode (MODE: MDS1, MDS0 = 01)—Characteristics: address recognition, random window size.

All frames with valid addresses (address recognition identical to auto mode) are forwarded directly to the system memory. The HDLC control field, data in the I-field and an additional status byte are temporarily stored in the RFIFO. The HDLC control field and additional information can also be read from special registers (RHCR, RSTA). In non-auto mode, all frames are treated similarly.

Transparent Mode 1 (MODE: MDS1, MDS0, ADM = 101)—Characteristics: address recognition high byte.

Only the high byte of a 2-byte address field will be compared. The whole frame except the first address byte will be stored in RFIFO. RAL1 contains the second and RHCR the third byte following the opening flag.

Transparent Mode 0 (Mode: MDS1, MDS0, ADM = 100)—Characteristics: no address recognition.

No address recognition is performed and each frame will be stored in the RFIFO. RAL 1 contains the first and RHCR the second byte following the opening flag.

Extended Transparent Modes 0, 1 (Mode: MDS1, MDS0 = 11)—Characteristics: fully transparent.

In extended transparent modes, fully transparent data transmission/reception without HDLC framing is performed; that is, without flag generation/recognition, CRC generation/check, bit-stuffing mechanism. This allows user-specific protocol variations or the usage of character oriented protocols (such as IBM BISYNC).

Data transmission is always performed out of the XFIFO. In extended transparent mode 0 (ADM = 0), data reception is done by the RAL1 register, which always contains the actual data byte assembled at the RxD pin. In extended transparent mode 1 (ADM = 1), the receive data is additionally shifted into the RFIFO.

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SYSTEM INTEGRATION

General Aspects

Figure 6 gives a general overview of the system integration of HSCX.

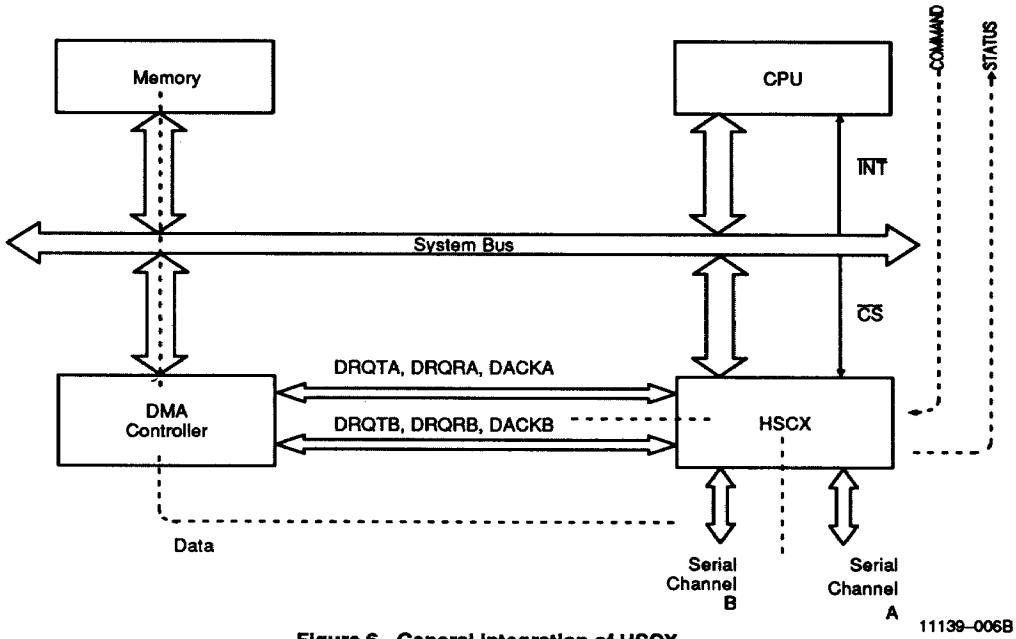

Figure 6. General Integration of HSCX

The HSCX's bus interface consists of an 8-bit bidirectional data bus (D0–D7), seven address line inputs (A0–A6), three control inputs ($\overline{RD}$ / DS, $\overline{WR}$ / R/W, $\overline{CS}$), one interrupt request output ($\overline{INT}$) and a 4-channel DMA interface (DRQTA, DRQRA, $\overline{DACKA}$, DRQTB, DRQRB, DACKB). Mode input pins (strapping options) allow the bus interface to be configured for either an AMD/Siemens/Intel, or Motorola environment.

Generally, there are two types of transfers occurring on the system bus:

- Command/Status transfers, which are always controlled by the CPU. The CPU sets the operation mode (initialization), controls function sequences and gets status information by writing or reading the HSCX's registers (using $\overline{CS}$, $\overline{WR}$, or $\overline{RD}$, and register address using A0–A6).
- Data Transfers, which are effectively performed by DMA without CPU interaction using the HSCX DMA interface (DMA Mode). Optionally, interrupt controlled data transfer can be done by the CPU (Interrupt Mode).

Specific Applications

HSCX with Am8051 Microcontroller

For cost-sensitive applications, the HSCX can be interfaced with an Am8051 microcontroller system (without DMA support) very easily as shown in Figure 7.

Although the HSCX provides a demultiplexed bus interface, it optionally can be connected directly to the local multiplexed bus of Am8051 because of the internal address latch function (using ALE, compatible to Am82520 HSCC).

The address lines A0–A6 must be wired externally to the data lines D0–D6 (direct connection) in this case.

Intel Bus Mode is selected connecting IM1 pin to LOW (GROUND). Since data transfer is controlled by interrupt, the DMA acknowledge inputs ($\overline{DACKA}$, $\overline{DACKB}$) are connected to V_{DD} (+5 V).

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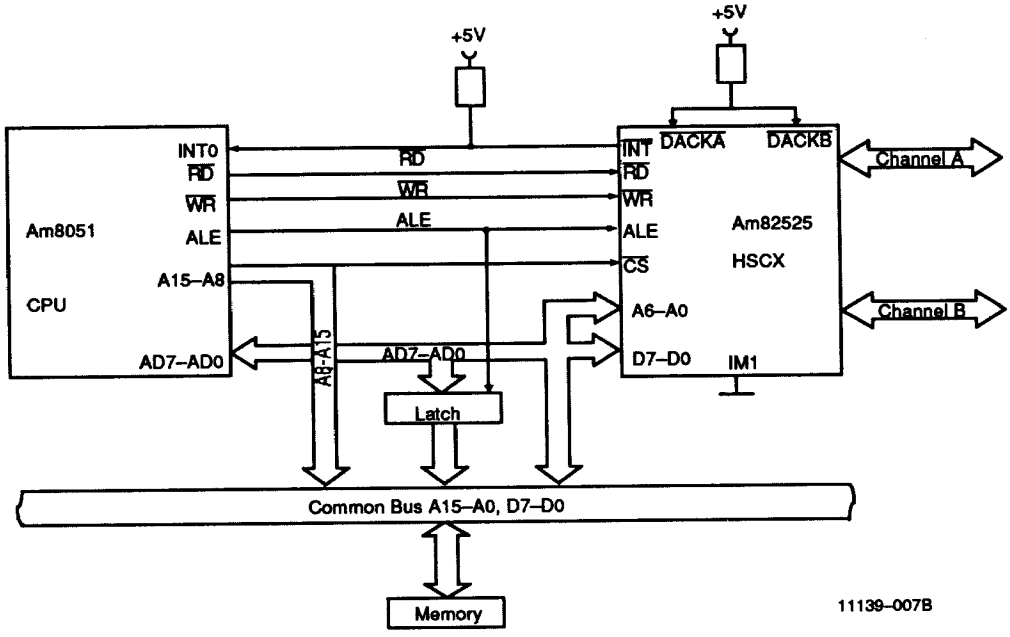

Figure 7. HSCX with Am8051 Microcontroller

HSCX with an Am80188 Microprocessor

A system with minimized additional hardware expense can be built up with an Am80188 microprocessor as shown in Figure 8.

The HSCX is connected to the demultiplexed system bus. Data transfer for one serial channel can be done by the 2-channel on-chip DMA controller of the Am80188; the other channel is serviced by interrupt. Since the Am80188 does not provide DMA acknowledge outputs, data transfer from/to HSCX is controlled with $\overline{CS}$, $\overline{RD}$, or $\overline{WR}$ address information (A0–A6), and the $\overline{DACKA}$, $\overline{DACKB}$ inputs are not used.

This solution supports applications with a high speed data rate in one serial channel with minimum hardware expense making use of the on-chip peripheral functions of the Am80188 (chip select logic, interrupt controller, DMA controller).

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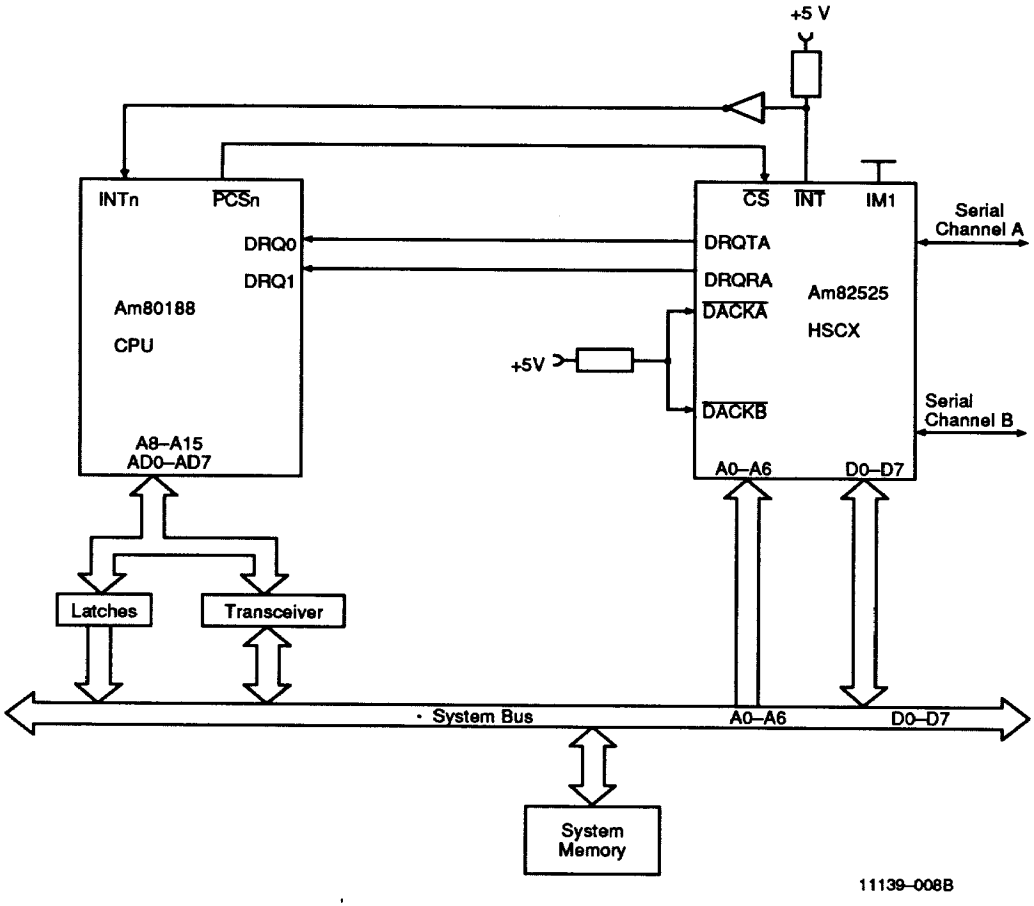

Figure 8. HSCX with 80188 CPU

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OPERATIONAL DESCRIPTION

Reset

The HSCX is forced into the reset state if a high signal is input to the RES pin for a minimum period of 1.8 µs. During RESET, the HSCX is temporarily in the power-up mode, and a subset of the registers is initialized with defined values.

After RESET, the HSCX is in power-down mode, and the following registers contain defined values:

Register	Reset Value	Meaning
CCR1	00 H	– power down mode Serial port configuration: pt-pt, NRZ coding, transmit data pins are open drain outputs – clock mode 0
CCR2	00 H	$\overline{RTS}$ pin normal function – $\overline{CTS}$ and $\overline{RTS}$ interrupts disabled no data inversion
MODE	00 H	auto-mode 1 byte address field external timer mode
	48 H	– receivers inactive $\overline{RTS}$ output controlled by HSCX, timer resolution: k = 32.768, no testloop
	00 H	XFIFO write enable receive line inactive no commands executing
	00 H	– no interrupts masked
	00 H	no commands
	00 H	– interrupt controlled data transfer (DMA disabled) – full-duplex LAPB/LAPD operation of LAP controller – carrier detect auto start of receiver disabled 1-bit timeslots

Operational Phase

After having performed the initialization, the CPU switches each individual channel of the HSCX into operational phase by setting the PU bit in the CCR1 register (power-up, if not already done during initialization).

Initially, the CPU should bring the transmitter and receiver to a defined state by issuing an XRES (transmitter reset) and RHR (receiver reset) command from the CMDR register. If data reception should be performed, the receivers must be activated by setting the RAC bit in Mode to 1.

If no "Clear to send" function is provided with a modem, the $\overline{CTS}$ pins of the HSCX must be connected directly to ground in order to enable data transmission.

Now the HSCX is ready to transmit and receive data. The control of the data transfer phase is done mainly by commands from CPU to HSCX via the CMDR register and by interrupt indications from HSCX to CPU.

Additional status information, which does not trigger an interrupt, is available in the STAR register. A complete description of every register is provided in the following paragraph. Additionally, the address of the respective registers is noted in the form: (ADDR Channel A/ADDR Channel B).

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ADDRESS (A0–A6) Channel		REGISTER		Comment Meaning
A	B	Read	Write	
00	40			
•	•	RIFO	XFIFO	Receive/Transmit FIFO
•	•			
1F	5F			
20	60	ISTA	MASK	Interrupt STAtus/MASK
21	61	STAR	CMDR	STAtus/CoMmanD
22	62	MODE		MODE
23	63	TIMR		TIMeR
24	64	EXIR	XAD1	EXtended Interrupt/Transmit ADdress 1
25	65	RBCL	XAD2	Receive Byte Count Low/Transmit ADdress 2
26	66	—	RAH1	Receive Address HIGH 1
27	67	RSTA	RAH2	Receive STAtus/Receive Address HIGH 2
28	68	RAL1		Receive Address LOW 1
29	69	RHCR	RAL2	Receive HDLC Control/Receive Address LOW 2
2A	6A	—	XBCL	Transmit Byte Count LOW
2B	6B	—	BGR	Baud Rate Generator Register
2C	6C	CCR2		Channel Configuration Register 2
2D	6D	RBCH	XBCH	Receive/Transmit Byte Count HIGH
2E	6E	VSTR	RLCR	Version STAtus/Receive Frame Length Check
2F	6F	CCR1		Channel Configuration Register 1
30	70	—	TSAX	Time Slot Assignment Transmit
31	71	—	TSAR	Time Slot Assignment Receive
32	72	—	XCCR	Transmit Channel Capacity
33	73	—	RCCR	Receive Channel Capacity

11139–009B

Figure 9. Layout of Register Addresses

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REGISTER DEFINITIONS

Receive FIFO (Read) RFIFO (00 . . . 1F/40 . . . 5F)

- Interrupt Controlled Data Transfer (Interrupt Mode). Selected if DMA bit in XBCH is reset. Up to 32 bytes of receive data can be read from the RFIFO following an RPF or an RME interrupt.

  RPF Interrupt: Exactly 32 bytes to be read.

  RME Interrupt: Number of bytes to be determined by reading the RBCL, RBCH registers.

- DMA Controlled Data Transfer (DMA Mode). Selected if DMA bit in XBCH is set.

  If the RFIFO contains 32 bytes, the HSCX autonomously requests a block data transfer by DMA activating the DRQR line as long as the start of the 32nd read cycle. This forces the DMA controller to continuously perform bus cycles until 32 bytes are transferred from the HSCX to the system memory (level triggered, demand transfer mode of DMA controller).

  If the RFIFO contains less than 32 bytes (one short frame or the last part of a long frame) the HSCX requests a block data transfer depending on the contents of the RFIFO according to the following table:

RFIFO Contents (Bytes)	DMA Request (Actual Bytes Transferred)
(1) 2,3	4
4–7	8
8–15	6
16–32	32

  Additionally, an RME interrupt is issued after the last byte has been transferred.

  As a result, the DMA controller may transfer more bytes as actually valid in the current received frame. The valid byte count must therefore be determined reading the RBCH, RBCL registers following the RME interrupt.

Transmit FIFO (WRITE) XFIFO (00 . . . 1F/40 . . . 5F)

- Interrupt Mode. Selected if DMA bit in XBCH is reset.

  Up to 32 bytes of transmit data can be written to the XFIFO following an XPR interrupt.

- DMA Mode. Selected if DMA bit in XBCH is set.

  Prior to any data transfer, the actual byte count of the frame to be transmitted must be written to the XBCH, XBCL registers by the user.

  If data transfer is then initiated via the CMDR register (command XTF or XIF), the HSCX autonomously requests the correct amount of block data transfers ($n \cdot 32 + REST$, $n = 0,1,\ldots$).

Note: Addresses within the address space of the FIFOs are interpreted equally; that is, the actual data byte can be accessed with any address within the valid scope.

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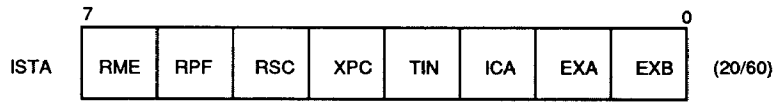
Interrupt Status Register (READ)–Value after RESET: 00H



Receive Message End (RME)—one message up to 32 bytes or the last part of a message greater than 32 bytes has been received and is now available in the RFIFO. The message is complete.

The actual message length can be determined reading the RBCH, RBCL registers. Additional information is available in the RSTA register.

Receive Pool Full (RPF)—a block of 32 bytes of a message is stored in the RFIFO. The message is not yet complete.

Note: This interrupt is generated only in Interrupt mode.

Receive Status Change (RSC) significant in auto mode only—a status change (receiver ready/receiver not ready) of the opposite station has been detected in auto mode; that is, the HSCX has received an RR/RNR supervisory frame according to the HDLC protocol. The current status can be read from the STAR register (RRNR bit).

Transmit Pool Ready (XPR)—a data block of up to 32 bytes can be written to the transmit FIFO.

Timer Interrupt (TIN)—the internal timer and repeat counter has expired. (See also description of TIMR register.)

Interrupt of Channel A (ICA) Channel B only—indicates that an interrupt is caused by Channel A and the interrupt source is indicated in the ISTA register of Channel A; that is, at least one bit of the ISTA register of Channel A is set.

Extended Interrupt of Channel A (EXA) Channel B only—an interrupt is caused by Channel A and the source is indicated in the EXIR register of Channel A.

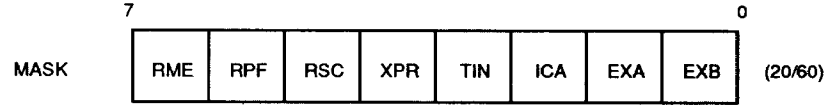
Extended Interrupt of Channel B (EXB) Channel B only—an interrupt is caused by Channel B and the source is indicated in the EXIR register of Channel B.

Note: The ICA, EXA, and EXB bits are present in Channel B only and point to the ISTA (Channel A), EXIR (Channel A), and EXIR (Channel B) registers.

After the HSCX has requested an interrupt by asserting its $\overline{INT}$ pin LOW, the CPU must first read the ISTA register of Channel B and check the state of these bits in order to determine which interrupt source of which channel has caused the interrupt. More than one interrupt source may be indicated by a single interrupt request.

After the respective register has been read, EXA, and EXB are reset. All other bits will be reset after reading ISTA. To prevent malfunctions, each bit is individually monitored and reset.

Mask Register (WRITE)—Value after RESET: 00H (all interrupts enabled)



Each interrupt source can be selectively masked by setting the respective bit in the Mask (bit positions corresponding to ISTA register). Masked interrupts are not indicated when reading ISTA. Instead, they remain internally stored and will be indicated after the respective Mask bit is reset.

Note: In the event of an extended interrupt, no interrupt request will be generated with a masked EXA, EXB bit, although this bit is set in ISTA.

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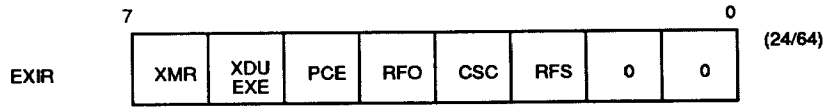
Extended Interrupt Register (READ)—Value after RESET: 00H



Transmit Message Repeat (XMR)—the transmission of the last message has to be repeated because:

- the HSCX has received a negative acknowledg ment in auto mode, or
- a collision has occurred after sending the 32nd data byte of a message in a bus configuration, or
- $\overline{CTS}$ (transmission enable) was withdrawn after sending the 32nd data byte of a message in a point-to-point configuration.

Transmit Data Underrun/Extended Transmission End (XDU/EXE) — the actual frame has been aborted with Idle, because the XFIFO holds no further data, but the frame is not yet complete. In extended transparent mode, this bit indicates the transmission-end condition.

Note: It is not possible to send transparent- or I-frames when an XMR or XDU interrupt is indicated.

Protocol Error (PCE) significant in auto mode only—the HSCX has detected a protocol error; that is, it has received:

- an S-, or I-frame with incorrect N (R)
- an S-frame containing an I-field

Receive Frame Overflow (RFO)—one frame could not be stored due to occupied RFIFO; that is, a whole frame has been lost. This interrupt can be used for statistical purposes and indicates that the CPU does not respond quickly enough to an incoming RPF or RME interrupt.

Clear To Send Status Change (CSC)—indicates that a state transition has occurred at the $\overline{CTS}$ pin. The actual state can be read from STAR register ($\overline{CTS}$ bit).

This interrupt must be enabled setting the CIE bit in CCR2.

Receive Frame Start (RFS)—this is an early receiver interrupt activated after the start of a valid frame has been detected; that is, after a valid address check in operation mode providing address recognition, otherwise after the opening flag (transparent mode 0), delayed by two bytes.

After an RFS interrupt, the contents of the following are valid and can be read by the CPU.

- RHCR
- RAL1
- RSTA—bit 3–0

This interrupt must be enabled setting the RIE bit in CCR2.

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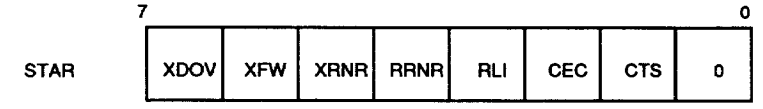
Status Register (READ)—Value after RESET: 48H



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Transmit Data Overflow (XDOV)—more than 32 bytes have been written to the XFIFO.

Transmit FIFO Write Enable (XFW)—data can be written to the XFIFO.

Transmit RNR (XRNR) significant in auto mode only—indicates the status of the HSCX.

0—receiver ready

1—receiver not ready

Received RNR (RRNR) significant in auto mode only — indicates the status of the remote station.

0—receiver ready

1—receiver not ready

Receive Line Inactive (RLI)—Neither flags as inter-frame time fill nor frames are received via the receive line.

Note: Significant only in point-to-point configurations.

Command Executing (CEC)

0—no command is currently executed; the CMDR register can be written to.

1—a command (written previously to CMDR) is currently executed, no further command can be temporarily written via CMDR register.

Clear To Send State ($\overline{CTS}$)—if the CIE bit in CCR2 is set, this bit indicates the state of the $\overline{CTS}$ pin.

0—$\overline{CTS}$ is inactive (HIGH signal at $\overline{CTS}$)

1—$\overline{CTS}$ is active (LOW signal at $\overline{CTS}$)

2

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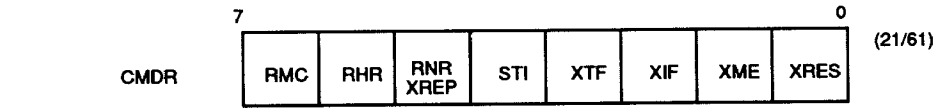
Command Register (WRITE)—Value after RESET: 00H.



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Receive Message Complete (RMC)—confirmation from CPU to HSCX that the actual frame or data block has been fetched following an RPF or RME interrupt, thus the occupied space in the RFIFO can be released.

Note: In DMA mode, this command is issued only once after an RME interrupt. The HSCX does not generate further DMA requests prior to the reception of this command.

Reset HDLC Receiver (RHR) all data in the RFIFO and the HDLC receiver is deleted.

In auto mode, the transmit and receive sequence number counters additionally are reset.

Receiver Not Ready/Transmission Repeat (RNR/XREP)—the function of this command depends on the selected operation mode (MDS1, MDS0, ADM bit in Mode):

- Auto mode: RNR

The status of the HSCX receiver is set. Determines whether a received frame is acknowledged via an RR or RNR supervisory frame in auto mode.

0—receiver ready (RR)

1—receiver not ready (RNR)

- Extended Transparent mode 0,1: XREP

Together with XTF and XME set (write 2AH to CMDR), the HSCX repeatedly transmits the contents of the XFIFO (1 . . . 32 bytes) without HDLC framing fully transparent, that is, without Flag, CRC insertion or Bit Stuffing.

The cyclic transmission is stopped with an XRES command.

Start Timer (STI)—the internal timer is started.

Note: The timer is stopped by rewriting the TIMR register after start.

Transmit Transparent Frame (XTF)

- Interrupt mode

After having written up to 32 bytes to the XFIFO, this command initiates the transmission of a transparent frame. An opening flag sequence is automatically added to the data by the HSCX.

- DMA mode

After having written the length of the frame to be transmitted to the XBCH, XBCL registers, this command initiates the data transfer from system memory to HSCX by DMA. Serial data transmission starts as soon as 32 bytes are stored in the XFIFO.

Transmit I-Frame (XIF) used in auto mode only—initiates the transmission of an I-frame in auto mode. In addition to the opening flag sequence, the address and control field of the frame are automatically added by HSCX.

Transmit Message End (XME) used in interrupt mode only—indicates that the data block written last to the transmit FIFO completes the actual frame. The HSCX can terminate the transmission operation properly by appending the CRC and the closing flag sequence to the data.

In DMA mode, the end of the frame is determined by the transmit byte count in XBCH, XBCL.

Transmit Reset (XRES)—the contents of the XFIFO are deleted and Idle is transmitted. This command can be used by the CPU to abort a frame currently in transmission.

Note: The maximum time between writing to the CMDR register and the execution of the command is 2,5 clock cycles. Therefore, if the CPU operates with a very high clock in comparison with the HSCX's clock, it's recommended that the CEC bit of the STAR register be checked before writing to the CMDR register to avoid any loss of commands.

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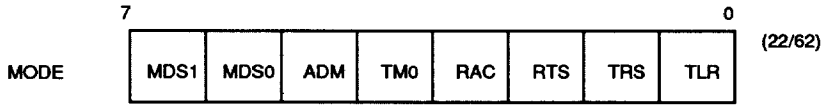
Mode Register (READ/WRITE)—Value after RESET: 00H



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Mode Select (MDS1, MDS0)—the operating mode of the HDLC controller is selected.

00—auto mode

01—non-auto mode

10—transparent mode

11—extended transparent mode

Address Mode (ADM)—the meaning of this bit varies depending on the selected operating mode:

- Auto mode, non-auto mode

  Defines the length of the HDLC address field.

  0—8-bit address field

  1—16-bit address field

In transparent modes, this bit differentiates between two sub-modes:

- Transparent mode

  0—transparent mode 0; no address recognition.

  1—transparent mode 1; high byte address recognition.

- Extended transparent mode; without HDLC framing.

  0—extended transparent mode 0

  1—extended transparent mode 1

Note: In extended transparent modes, the RAC bit must be reset to enable fully transparent reception.

Timer Mode (TMD)—the operation mode of the internal timer is set.

0—external mode

The timer is controlled by the CPU and can be started at any time setting the STI bit in CMDR.

1—internal mode

The timer is used internally by the HSCX for timeout and retry conditions in auto mode (refer to the description of the TIMR register).

Receiver Active (RAC)—switches the receiver to operational or inoperational state.

0—receiver inactive

1—receiver active

In extended transparent modes this bit must be reset to enable fully transparent reception.

Request To Send (RTS)—defines the state and control of the $\overline{\text{RTS}}$ pin.

0—The $\overline{\text{RTS}}$ pin is controlled by the HSCX autonomously.

$\overline{\text{RTS}}$ is activated when a frame transmission starts and is deactivated after the transmission operation is complete.

1—The $\overline{\text{RTS}}$ pin is controlled by the CPU.

If this bit is set, the $\overline{\text{RTS}}$ pin is activated immediately and remains active until this bit is reset.

Timer Resolution (TRS)—the resolution of the internal timer (factor k, see description of TIMR register) is selected.

0—k = 32.768

1—k = 512

Testloop (TLP)—Input and output of the HDLC channels are internally connected. (transmitter channel A—receiver channel A/transmitter channel B—receiver channel B).

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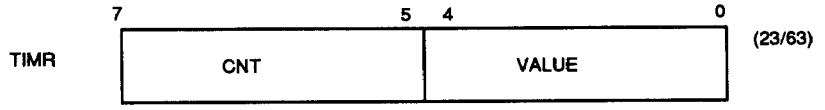
Timer Register (READ/WRITE)



VALUE—Sets the time period t1 as follows:

$$t1 = k \cdot (VALUE + 1) \cdot TCP$$

where k is the timer resolution factor which is either 32.768 or 512 clock cycles depending on the programming of TRS bit in Mode.

– TCP is the clock period of transmit data.

Interpreted differently depending on the selected timer mode (CNT) Bit TMD in MODE.

- Internal timer mode (MODE.TMD = 1)

– Retry Counter (in HDLC known as N2)

CNT indicates the number of S-commands (maximum six) which are transmitted autonomously by the HSCC after expiration of time period t1, in case an I-frame is not acknowledged by the opposite station.

If CTN is set to 7, the number of S-commands is unlimited.

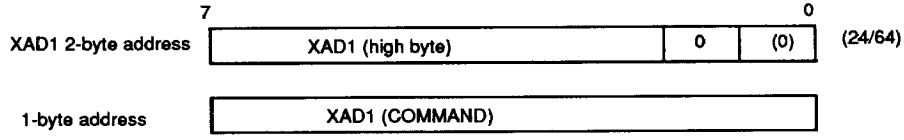
- External timer mode (MODE, TMD = 0)

CNT plus Value indicates the time period t2 after which a timer interrupt will be generated. The time period t2 is

$$t2 = 32 \cdot k \cdot CTN \cdot TCP + t1$$

If CTN is set to 7, a timer interrupt is periodically generated after the expiration of t1.

Transmit Address Byte 1 (WRITE)



XAD1 (and XAD2) can be programmed with one individual address byte which is appended automatically to the frame by HSCX in auto mode. The function depends on the selected address mode (bit ADM in Mode).

2-byte address field (MODE.ADM = 1)

XAD1 builds up the high byte of the 2-byte address field. Bit 1 must be set to 0. According to the ISDN LAPD protocol, bit 1 is interpreted as the C/R (Command/Response) bit. This bit is manipulated automatically by the HSCX depending on the setting of the CRI bit in RAH1:

4R Meaning	bit 1 (C/R)	
Commands transmit	1	0
Responses transmit	0	1
	CRI = 1	CRI = 1

(In the ISDN, the high address byte is known as SAPI.)

In accordance with the HDLC protocol, bit 0 should be set to 0, indicating the extension of the address field to two bytes.

1-byte address field (MODE.ADM = 0)

In accordance with the X.25 LAPB protocol, XAD1 indicates a command.

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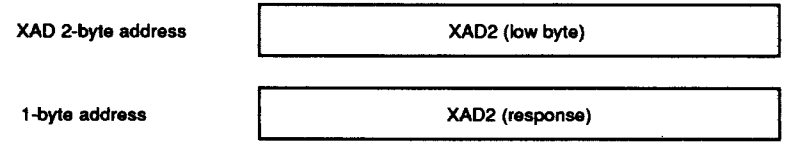
Transmit Address Byte 2 (WRITE)



Second individually programmable address byte.

2-byte address (MODE.ADM = 1)

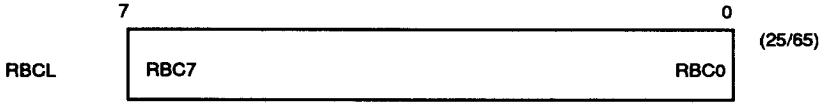
XAD2 builds up the low byte of the 2-byte address field. (In the ISDN, the low address byte is known as TEI.)

1-byte address (MODE.ADM = 0)

In accordance with the X.25 LAPB protocol, XAD2 indicates a response.

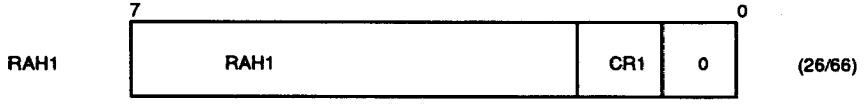
Note: XAD1, XAD2 registers are used only if the HSCX is operated in auto mode.

Receive Byte Count LOW (READ)



Together with RBCH (bits RBC11–RBC8), the length of the actual received frame (1... 4095 bytes) can be determined. These registers must be read by the CPU following an RME interrupt.

Receive Address Byte High Register 1 (WRITE)



In operating modes that provide high byte address recognition, the high byte of the received address is compared with the individual programmable values in RAH1 or RAH2.

RAH1—Value of the first individual high address byte

CRI—Command/Response Interpretation

The setting of the CRI bit affects the meaning of the C/R bit in RSTA as follows:

C/R Meaning	(C/R) Value	
Commands Received	0	1
Responses Received	1	0
	CRI = 1	CRI = 1

Important: If the 1-byte address field is selected in auto mode, RAH1 must be set to 00H.

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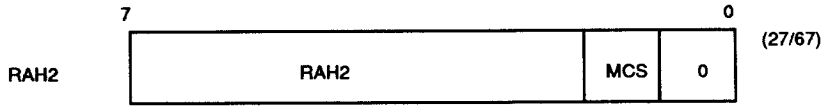
Receive Address Byte High Register 2 (WRITE)



RAH2 — Value of second individual programmable high address byte.

MCS — Modulo Count Select, valid in auto mode only.

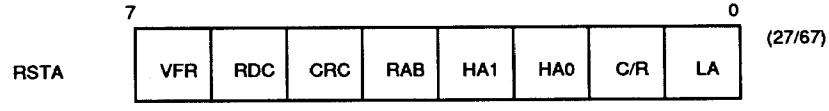
The MCS bit adjusts the control field format according to the HDLC (ISDN/LAPD).

0 – basic operation (modulo 8)

1 – extended operation (modulo 128)

Note: When modulo 128 is selected, in auto mode the "RHCR" register contains compressed information of the extended control field (see RHCR, register description). RAH1, RAH2 registers are used in auto and non-auto operating modes when a 2-byte address field has been selected (MODE.ADM = 1) and in the transparent mode 0.

Receive Status Register (READ)



VFR—Valid Frame—determines whether a valid frame has been received.

1. Valid

0. Invalid

An invalid frame is either

– a frame which is not an integer number of 8 bits (n · 8 bits) in length (e.g., 25 bit), or

– a frame which is too short depending on the selected operation mode via MODE (MDS1, MDS0, ADM) as follows:

- auto-/non-auto mode (16-bit address): 4 bytes
- auto-/non-auto mode (8-bit address): 3 bytes
- transparent mode 1: 3 bytes
- transparent mode 0: 2 bytes

Note: Shorter frames are not reported.

Receive Data Overflow (RDO)—a data overflow has occurred within the actual frame.

CRC Compare/Check (CRC)

0—CRC check failed; received frame contains errors.

1—CRC check okay; received frame is error-free.

Receive Message Aborted (RAB)—the received frame was aborted from the transmitting station.

According to the HDLC protocol, this frame must be discarded by the CPU.

High Byte Address Compare (HA1, HA0), significant only if 2-byte address mode has been selected—in operating modes that provide high byte address recognition, the HSCX compares the high byte of a 2-byte address with the contents of two individual programmable registers (RAH1, RAH2) and the fixed values FEH and FCH (group address).

Depending on the result of this comparison, the following bit combinations are possible:

10 — RAH1 has been recognized

00—RAH2 has been recognized

01—group address has been recognized

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Note: If RAH1, RAH2 contain the identical values, the combination 00 will be omitted.

Command/Response (C/R), significant only if 2-byte address mode has been selected—value of the C/R bit (bit of high address byte) in the received frame. The interpretation depends on the setting of the CRI bit in the RAH1 register. Refer also to the description of RAH1 register.

Low Byte Address Compare (LA), not significant in transparent and extended transparent operating mode—the low byte address of a 2-byte address field, or the single address byte of a 1-byte address field is compared with two individual programmable registers (RAL1, RAL2).

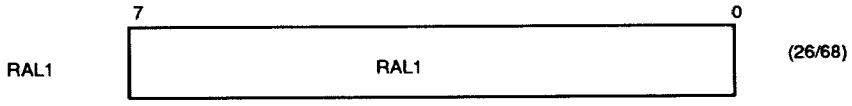
0—RAL2 has been recognized

1—RAL1 has been recognized

According to the X.25 LAPB protocol, RAL1 is interpreted as Command and RAL2 is interpreted as Response.

Note: RSTA corresponds to the last received HDLC frame; it is duplicated into RFIFO for every frame (last byte of frame).

Receive Address Byte Low Register 1 (READ/WRITE)



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The general function (READ/WRITE) and the meaning or contents of this register depend on the selected operating mode:

–auto-/non-auto mode (16-bit address)—WRITE:

RAL1 can be programmed with the value of the first individual low address byte.

– auto-/non-auto mode (8-bit address)—WRITE:

According to X.25 LAPB protocol, the address in RAL1 is recognized as command address.

– transparent mode 1 (high byte address recognition) —READ:

RAL1 contains the byte following the high byte of the address in the receive frame (that is, the second byte after the opening flag).

–transparent mode 0 (no address recognition)— READ:

RAL1 contains the first byte after the opening flag (first byte of received frame).

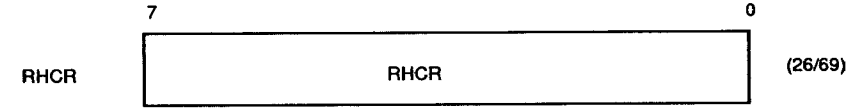
– extended transparent modes 0,1—READ:

RAL1 contains the actual data byte currently assembled at the RxD pin, by passing the HDLC receiver (fully transparent reception without HDLC framing).

Receive Address Byte Low Register 2 (WRITE)

Value of the second individual programmable low address byte. If a one-byte address field is selected, RAL2 is recognized as Response according to X.25 LAPB protocol.

Receive HDLC Control Register (READ)



(26/69)

Value of the HDLC control field of the last received frame.

Note: RHCR is duplicated into RFIFO for every frame.

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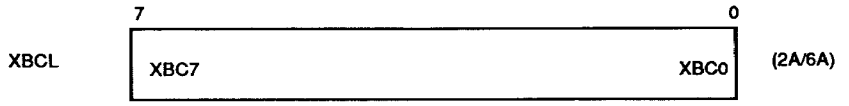
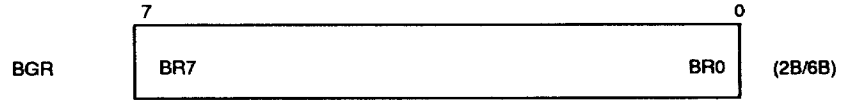
Transmit Byte Count Low (WRITE)



Together with XBCH (bits XBC11–XBC8) this register is used in DMA mode only to program the length (1–4095 bytes) of the next frame to be transmitted. This allows the HSCX to request the correct amount of DMA cycles after an XTF or XIF command via CMDR.

Baud Rate Generator Register (WRITE)



BR7–BR0 — Baud Rate, bit 7–0

Together with bits BR9, BR8 of CCR2, the division factor of the baud rate generator is adjusted. Depending on the programmed value N in BR9–BR0 (N = 0 – 1023), the division factor k results as follows:

$$k = (N + 1)\ 2$$

Channel Configuration Register 2 (READ/WRITE)—Value after RESET: 00H.

The meaning of the individual bits in CCR2 depends on the selected clock mode via CCR1 as follows:

CCR2 clock mode 0, 1	BCS1	BCS0	0	0	0	CIE	RIE	DIV	(2C/6C)
clock mode 2, 6	BR9	BR8	BDF	TSS	TIO	CIE	RIE	DIV	
clock mode 3, 4, 7	BR9	BR8	BDF	0	TIO	CIE	RIE	DIV	
clock mode 5	BCS1	BCS0	XCS0	RCS0	TIO	CIE	RIE	DIV	

BCS1, BCS0 — Bus Control Signal Selection—valid only in a bus configuration (selected via CCR1).

0 X $\overline{\text{RTS}}$ output is activated during the transmission of a frame, see also Mode register.

1 0 $\overline{\text{RTS}}$ output is always HIGH ($\overline{\text{RTS}}$ disabled).

1 1 $\overline{\text{RTS}}$ indicates the reception of a data frame (active LOW).

BR9, BR8—Baud Rate, Bit 9–8 (higher significant bits, refer to description of BGR register).

BD—Baud Rate Division Factor

0—The division factor of the baud rate generator is set to 1 (constant).

1—The division factor is adjusted with BR9–BR0 bits of CCR2 and BRG register.

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TSS—Transmit Clock Source Select

0—The transmit clock is input to the TxCLKA/TxCLKB pins.

1—The transmit clock is derived from the baud rate generator output clock divided by 16.

TIO—Transmit Clock Input Output Switch

0—TxCLKA, TxCLKB pins are inputs

1—TxCLKA, TxCLKB pins are outputs

CIE—Clear To Send Interrupt Enable—any state transition at the $\overline{CTS}$ input pin may cause an interrupt which is indicated in the EXIR register (CSC bit). The actual state at the $\overline{CTS}$ pin can be determined reading the $\overline{CTS}$ bit of the STAR register.

0—disable

1—enable

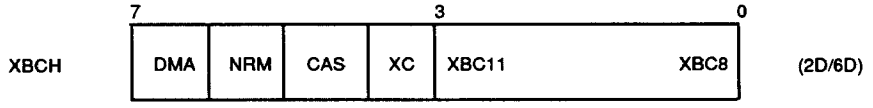
RIE—Receive Frame Start Interrupt Enable—When set, the RFS interrupt (via EXIR) is enabled.

DIV—Data Inversion—Valid only if NRZ data encoding is selected. Data is transmitted and received inverted.

XCS0, RCS0—Transmit/Receive Clock Shift, Bit 0—together with bits XCS2, XCS1 (RCS2, RCS1) in TSAX (TSAR) the clock shift relative to the frame synchronization signal of the transmit (receive) time slot can be adjusted.

A clock shift of 0–7 bits is programmable (clock mode 5 only).

Transmit Byte Count High (WRITE)—Value after RESET: 000xxxxx



DMA—DMA Mode—selects the data transfer mode of HSCX to System Memory.

0—Interrupt controlled data transfer (interrupt mode)

1—DMA controlled data transfer (DMA mode)

NRM—Normal Response Mode—valid in auto mode only. Determines the function of the LAP Controller:

0—full-duplex LAPB/LAPD operation

1—half-duplex NRM operation

CAS—Carrier Detect Auto Start—when set, a HIGH at the CD (AxCLK) pin enables the respective receiver, and data reception is started.

XC—Transmit Continuously—valid only if DMA mode is selected.

If the XC bit is set, the HSCX continuously requests for transmit data ignoring the transmit byte count programmed via XBCX, XBCL.

XBC11–XBC8—Transmit Byte Count (most significant bits)—valid only if DMA mode is selected.

Together with XBCL (bits XBC7–BC0) the length of the frame to be transmitted is programmed.

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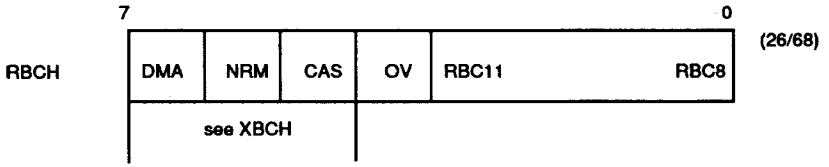
Received Byte Count High (READ)—Value after RESET: 000xxxxx

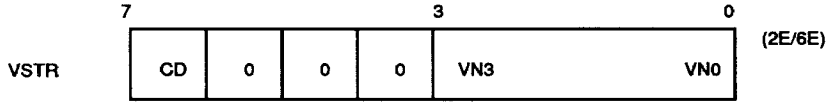


DMA, NRM, CAS—these bits represent the read-back value programmed in XBCH (see XBCH).

OV—Counter Overflow—more than 4095 bytes received. The received frame exceeded the byte count in RBC11 ... RBC0.

RBC11–RBC8—Receive Byte Count (most significant bits)—together with RBCL (bits RBC7–RBC0) the length of the received frame can be determined.

Version Status Register (READ)



CD—Carrier Detect—this bit represents the inverted state at the CD (AxCLK) pin.

1—CD active (LOW)

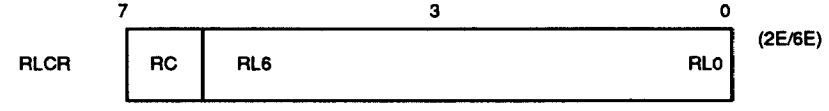
0—CD inactive (HIGH)

VN3 ... VN0 ... Version Number of Chip

0—Version A1

2—Version A2

Receive Length Check Register (WRITE)



RC—Receive Check (on/off)

0—Receive length check feature disabled

1—Receive length check feature enabled

RL—Receive Length—the maximum receive length after which data reception is suspended can be programmed here. Depending on the value RL programmed via RL6–RL0, the receive length is (RL + 1) · 32 bytes.

A frame exceeding this length is treated as if it were aborted by the opposite station (RME Interrupt, RAB bit set). In this case, the receive byte count (RBCH, RBCL) is greater than the programmed receive length.

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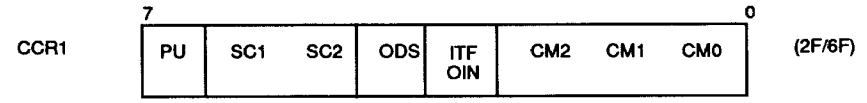
Channel Configuration Register 1 (READ/WRITE)—Value after RESET: 00H



PU—Switches Between Power Up and Power Down Mode

0—power down (standby)

1—power up (active)

SC1, SC0... Serial Port Configuration

00—NRZ data encoding

10—NRZI data encoding

01—bus configuration, timing mode 1

11—bus configuration, timing mode 2

Note: If bus configuration is selected, only NRZ coding is supported.

ODS...Output Driver Select—defines the function of the transmit data pins (TxDA, TxDB)

0—TxD pins are open drain outputs

1—TxD pins are push-pull outputs

ITF/OIN—Interframe Time Fill/One Insertion—the function of this bit depends on the selected serial port configuration (bit SC1):

- Point-to-point configurations: ITF

  Determines the idle (= no data to send) state of the transmit data pins (TxDA, TxDB)

  0—Continuous idle sequences are output (TxD pins remain in the "1" state)

  1—Continuous flag sequences are output ("01111110" bit patterns)

- Bus configurations: OIN

  In bus configurations, the ITF is implicitly set to "0"; that is, continuous "1"s are transmitted, and data encoding is NRZ.

  When this bit is set, a "ONE" insertion (deletion) mechanism is activated, inserting a "1" after seven consecutive "0"s in the transmit data stream or deleting a "1" in the receive data stream.

  Similar to the HDLC's bit-stuffing mechanism (inserting a "0" after five consecutive "1"s), this method proves to be advantageous when the receive clock is recovered from the receive data stream by means of DPLL, because it is guaranteed that at least after seven bits a transition occurs in the receive data as in case of long "0" sequences.

CM2, CM1, CM0—Clock Mode—selects one of the eight different clock modes:

000	clock mode 0
.	.
.	.
111	clock mode 7

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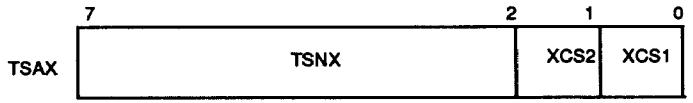
Time Slot Assignment Register Transmit (WRITE)



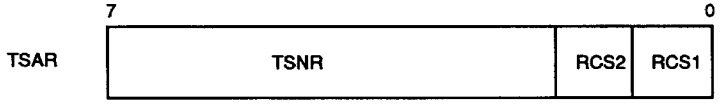
(30/70)

This register is used only in clock mode 5.

TSNX—Time Slot Number Transmit—selects one of up to 64 possible time slots (00H–3FH) in which data is transmitted. The number of bits per time slot can be programmed via XCCR.

XCS2, XCS1—Transmit Clock Shift, Bit 2–1—together with bit XCS0 in CCR2, the transmit clock shift can be adjusted.

Time Slot Assignment Register Receive (WRITE)



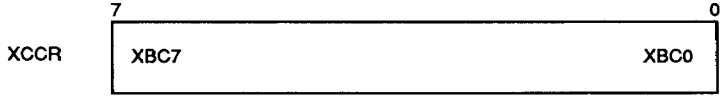
(31/71)

This register is used only in clock mode

TSNR—Time Slot Number Receive—defines one of up to 64 possible time slots (00H–3FH) in which data is received. The number of bits per time slot can be programmed via RCCR.

RCS2, RCS1—Receive Clock Shift, Bit 2–1—together with bit RCS0 in CCR2, the receive clock shift can be adjusted.

Transmit Channel Capacity Register (WRITE)—Value after RESET: 00H



(32/72)

XBC7–XBC0—Transmit Bit Count, Bit 7–0—defines the number of bits to be transmitted with a time slot:

Number of bits = XBC + 1 (1–256 bits/time slot)

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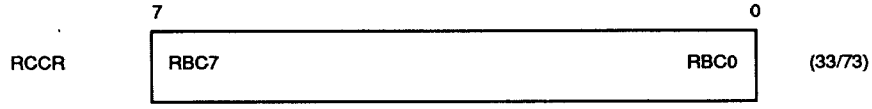
Receive Channel Capacity Register (WRITE)—Value after RESET: 00H



RBC7–RBC0—Receive Bit Count, Bit 7–0—defines the number of bits to be received within a time slot:

Number of bits = RBC + 1 (1–256 bits/time slot)

2

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ABSOLUTE MAXIMUM RATINGS

Ambient temperature under bias . . . . . –55 to +125°C

Voltage on any pin with
respect to ground . . . . . –0.25 to V_{DD} +0.25 V

Stresses above those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to absolute maximum ratings for extended periods may affect device reliability.

OPERATING RANGES

Commercial (C) Devices

Ambient Temperature (T_A) . . . . . 0 to +70°C

Supply Voltage (V_{CC}) . . . . . +4.75 to +5.25 V

Operating ranges define those limits between which the functionality of the device is guaranteed.

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DC CHARACTERISTICS

$T_A = 0$ to $+70°C$; $V_{DD} = 5\ V \pm 5\%$, $V_{SS} = 0\ V$.

Table 1. DC Characteristics

Symbol	Parameter	Limit Values Min.	Max.	Unit	Test Condition
V_{IL}	Input low voltage	–0.4	0.8	V	
V_{IH}	Input high voltage	2.0	$V_{CC} + 0.4$	V	
V_{OL}	Output low voltage		0.45	V	$I_{OL} = 2$ mA
V_{OH}	Output high voltage	2.4		V	$I_{OH} = -400\ \mu A$
V_{OH}	Output high voltage		$V_{DD} - 0.5$	V	$I_{OH} = -100\ \mu A$
I_{CC}	Power supply current operational		8	mA	$V_{DD} = 5$ V inputs at 0 V/V_{DD}, no output loads
	power down		1.5	mA	
I_{LI}	Input leakage current		10 µa		0 V < V_{IN} < V_{DD} to 0 V
I_{LO}	Output leakage current				0 V < V_{OUT} < V_{DD} to 0 V

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CAPACITANCES

$T_A = 25°C$, $V_{DD} = 5\ V \pm 5\%$, $V_{SS} = 0\ V$.

Table 2. Capacitances

Symbol	Parameter	Type	Limit Values Max	Unit	Test Condition
C_{IN}	Input capacitance	5	10	pF	
C_{OUT}	Output capacitance	10	20	pF	
C_{IO}	I/O	8	15	pF	

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SWITCHING CHARACTERISTICS

T_A = 0 to +70°C, V_{DD} = 5 V ±5%.

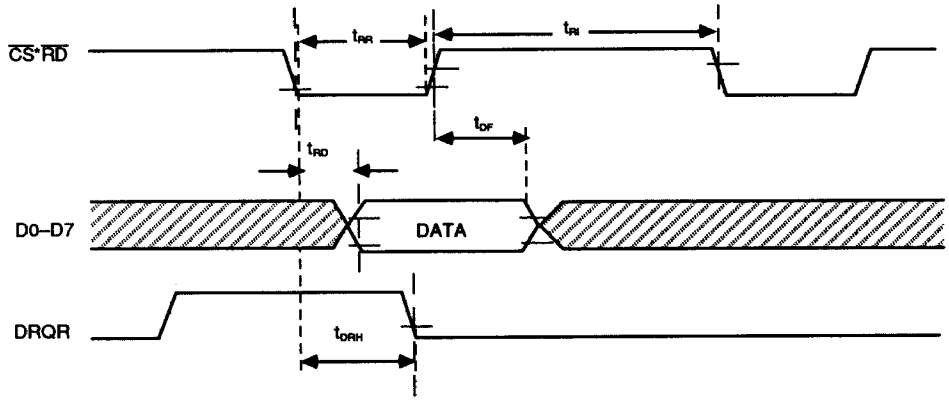
Inputs are driven to 2.4 V for a logical "1" and to 0.4 V for a logical '0'. Timing measurements are made at 2.0 V for a logical "1" and at 0.8 V for a logical "0".

The AC testing input/output waveforms are shown below.

11139-010B

Figure 10. Input/Output Waveform for AC Tests

Microcontroller Interface Timing



11139-011B

Figure 11. µP Read Cycle

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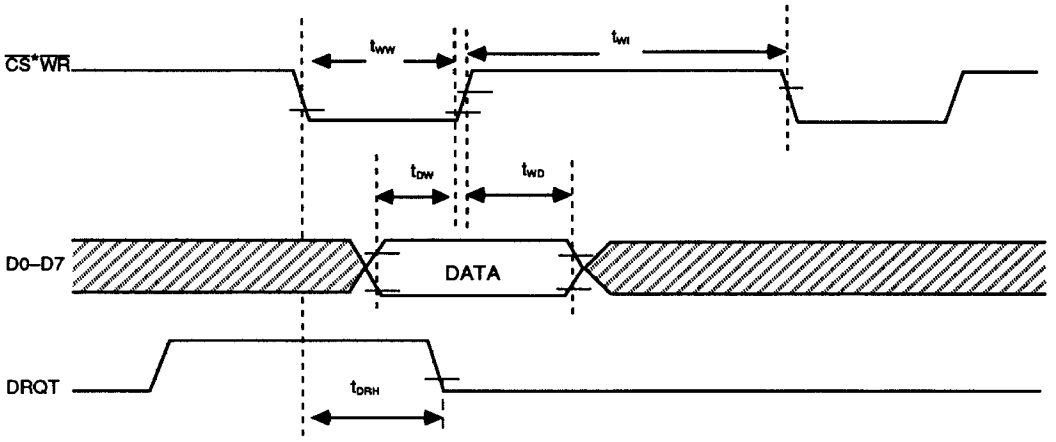

Figure 12. µP WriteCycle

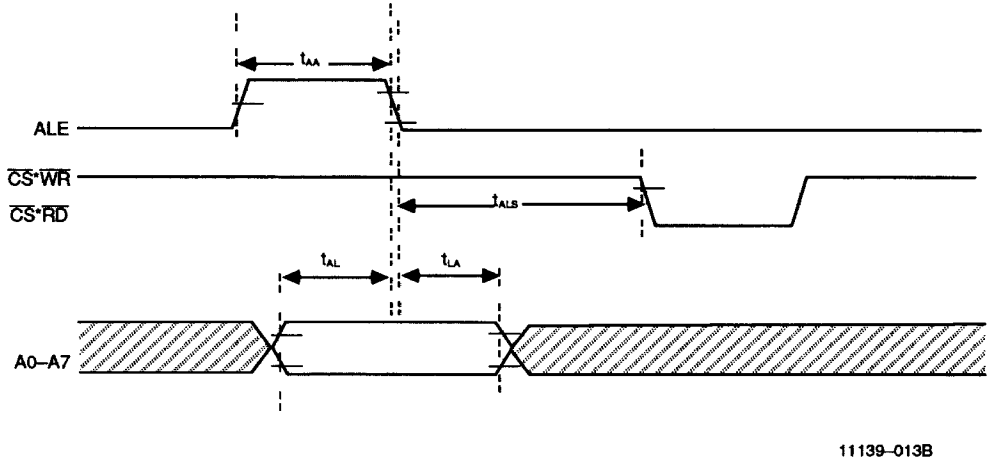

Figure 13. Multiplexed Address Timing

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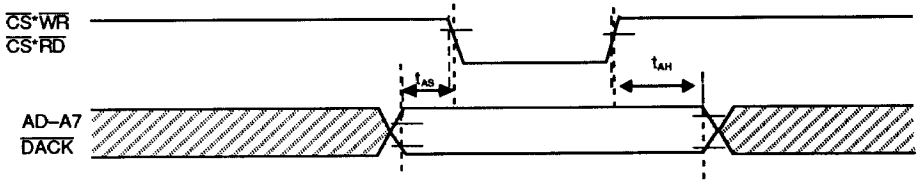
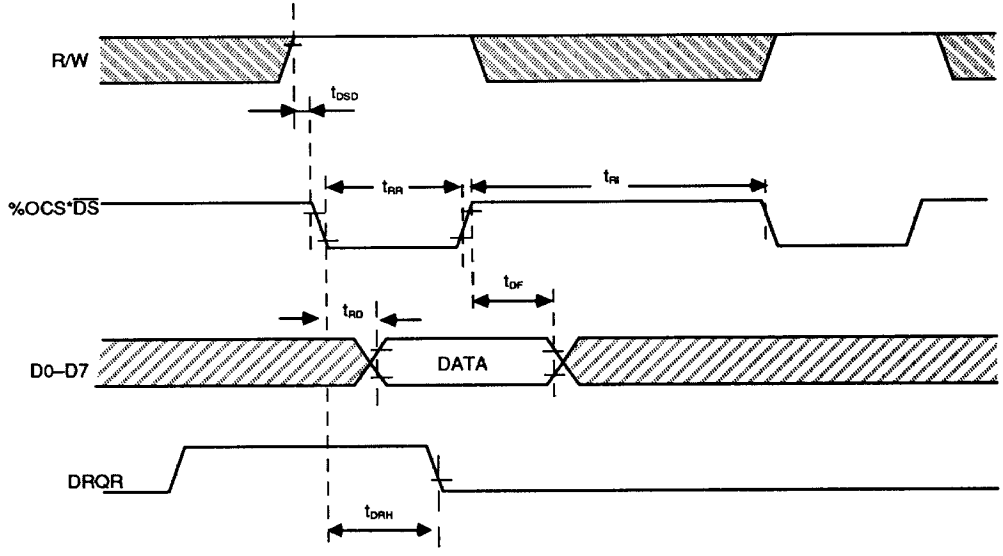


11139–014B

Figure 14. Address Timing

Motorola Bus Mode



11139–015B

Figure 15. µP Read Cycle

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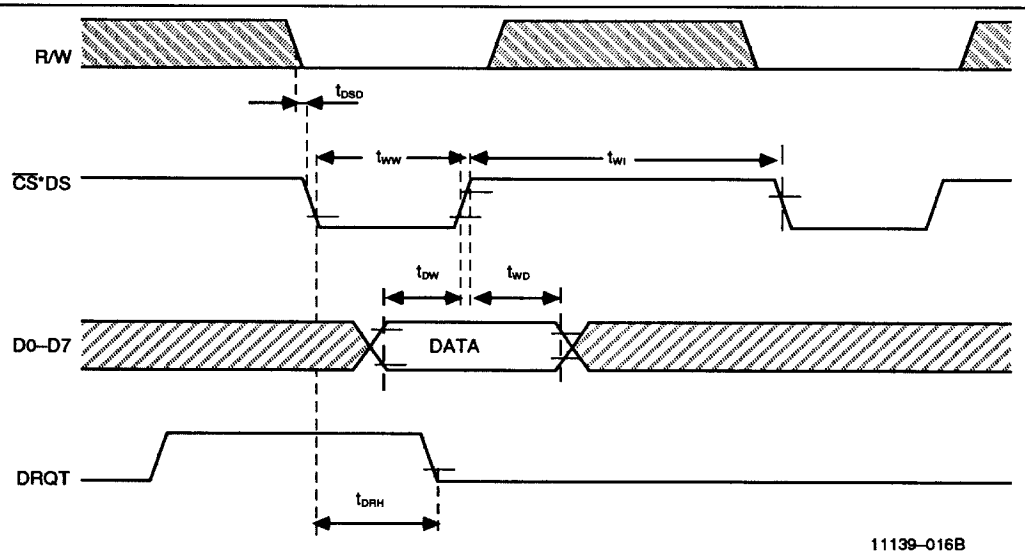

Figure 16. µP Write Cycle

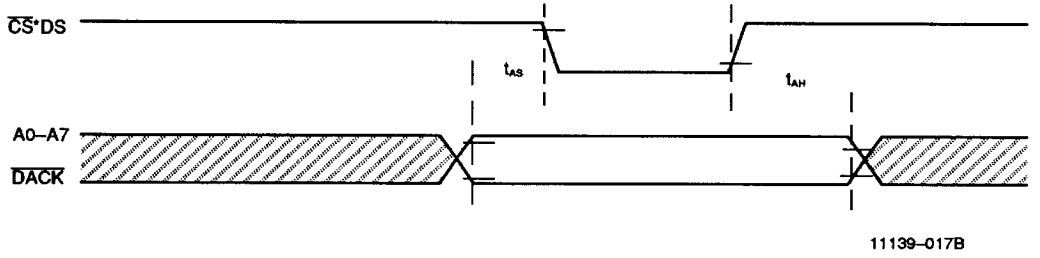

Figure 17. Address Timing

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Table 3. Microcontroller Interface Timing Characateristics

Parameter	Symbol	Limit Values Min.	Max.	Unit	Test Condition
ALE pulse width	t_{AA}	30	–	ns	–
Address setup time to ALE	t_{AL}	10	–	ns	–
Address hold time from ALE	t_{LA}	20	–	ns	–
Address latch setup time to $\overline{WR}$, $\overline{RD}$	t_{ALS}	0	–	ns	–
Address setup time to $\overline{WR}$, $\overline{RD}$	t_{AS}	10	–	ns	–
Address hold time from $\overline{WR}$, $\overline{RD}$	t_{AH}	20	–	ns	–
DMA request delay	t_{DRH}	–	75	ns	–
DS delay after R/W setup	t_{DSD}	0	–	ns	–
$\overline{RD}$ pulse width	t_{RR}	120	–	ns	–
Data output delay from $\overline{RD}$	t_{RD}	–	120	ns	–
Data float delay from $\overline{RD}$	t_{DF}	–	25	ns	–
$\overline{RD}$ control interval	t_{RI}	70	–	ns	–
$\overline{WR}$ pulse width	t_{WW}	60	–	ns	–
Data setup time to $\overline{WR}$+$\overline{CS}$	t_{DW}	30	–	ns	–
Data hold time from $\overline{WR}$+$\overline{CS}$	t_{WD}	10	–	ns	–
$\overline{WR}$ control interval	t_{WI}	70	–	ns	–

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Table 4. Serial Interface Timing

Parameter	Symbol	Limit Values Min.	Max.	Unit	Test Condition
Receive data setup	t_{RDS}	5		ns	
Receive data hold	t_{RDH}	30		ns	
Collision data setup	t_{CDS}	0		ns	
Data hold	t_{CDH}	20		ns	
Transmit data delay	t_{XDD}	20	70	ns	
Request to send delay 1	t_{RTD1}	30	120	ns	
Request to send delay 2	t_{RTD2}	20	85	ns	
Clock period	t_{CP}	240		ns	
Clock period Low	t_{CPL}	90		ns	
Clock period High	t_{CPH}	90		ns	

Table 5. Clock Mode 1

Parameter	Symbol	Limit Values Min.	Max.	Unit	Test Condition
Receive strobe delay	t_{RSD}	30		ns	
Receive strobe setup	t_{RSS}	60		ns	
Receive strobe hold	t_{RSH}	30		ns	
Transmit strobe delay	t_{XSD}	30		ns	
Transmit strobe setup	t_{XSS}	60		ns	
Transmit strobe hold	t_{XSH}	30		ns	
Transmit data delay	t_{XDD}		70	ns	
Strobe data delay	t_{SDD}		90	ns	
High impedance from clock	t_{XCZ}		50	ns	
High impedance from strobe	t_{XSZ}		50	ns	

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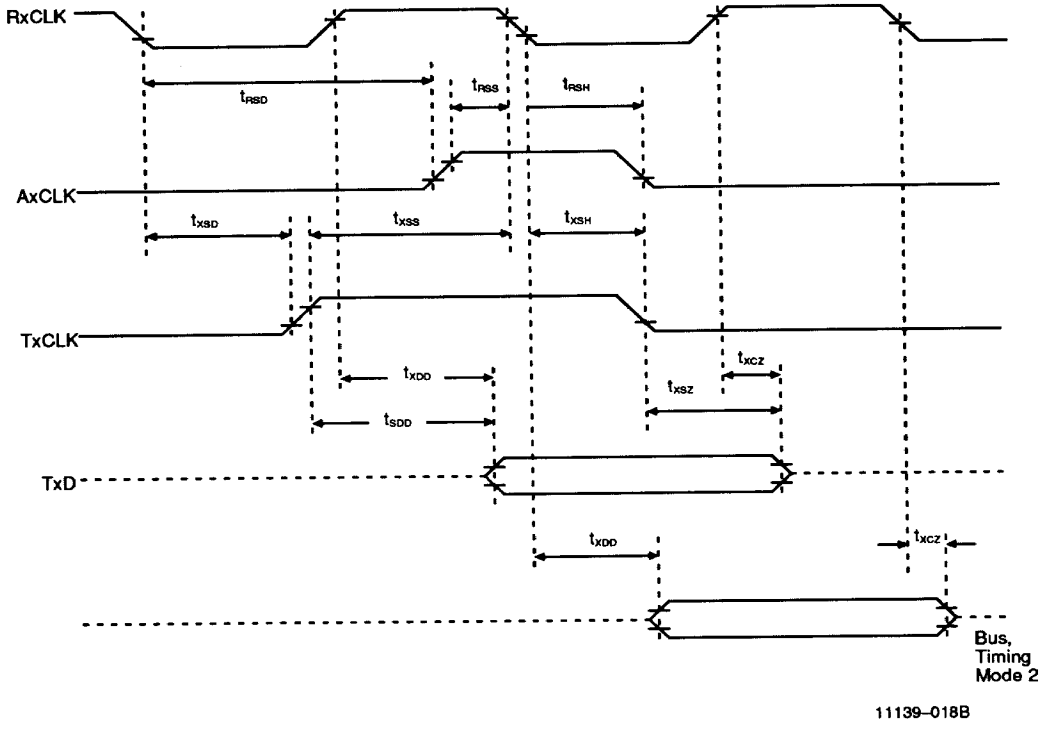

Figure 18. Strobe Timing

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Clock Mode 5

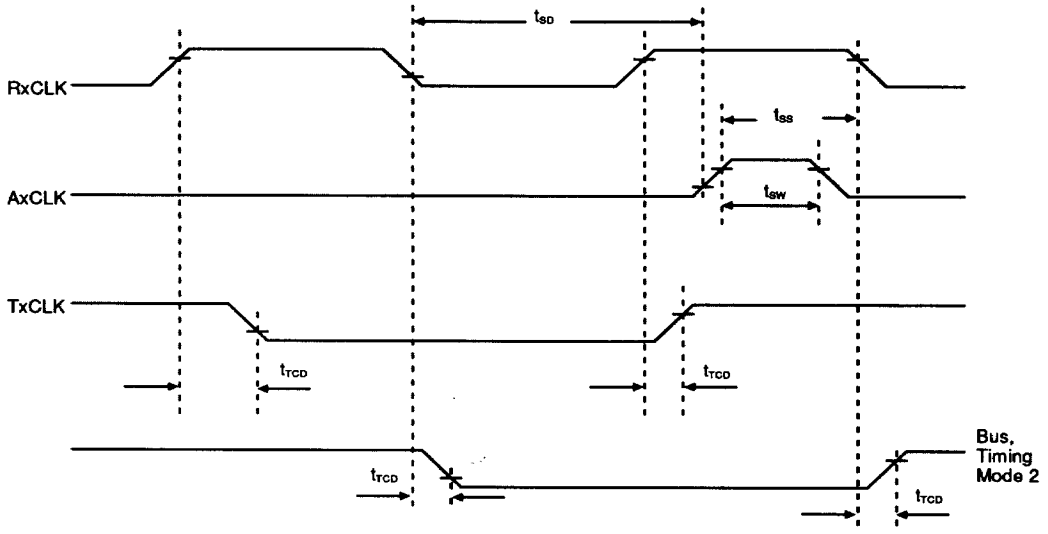

Figure 19. Synchronization Timing 11139–019B

Table 6. Clock Mode 5 Timing

Parameter	Symbol	Limit Values Min.	Max.	Unit
Sync pulse start early *	t_{SSE}	30		ns
Sync pulse start late **	t_{SSL}	0	30	ns
Sync pulse width	t_{SW}	40		ns
Time-slot control delay	t_{CD}	20	75	ns

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* If sync pulse starts before ↘ edge of RxCLK A/B first bit transmitted occurs on ↘ edge of RxCLK A/B.

** If sync pulse occurs after ↘ edge of RxCLK A/B first bit transmitted occurs on ↘ edge of sync pulse.

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Clock Mode 2, 3, 6, 7

Table 7. Internal Clocking

Description	Min.	Max.	Unit	Condition
Clock frequency		12	MHz	Baud rate generator used
Clock frequency		19.3	MHz	Baud rate generator not used

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Reset Timing

Table 8. RES Characteristics

Symbol	Description	Min.	Max.	Unit	Condition
t_{RWH}	RES High	1800		ns	

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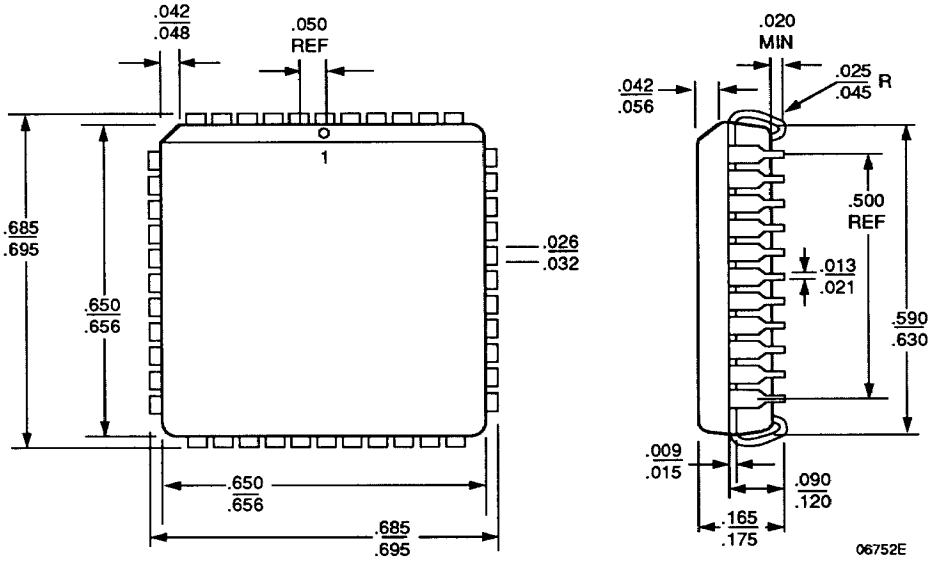
PHYSICAL DIMENSIONS

Plastic package, PLCC, 44 pins



2

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