Am9151

1024 x 4 Registered Static RAM with SSR™
— On-Chip Diagnostics Capability

DISTINCTIVE CHARACTERISTICS

- High Speed – 40 ns cycle time (25 ns Max. setup and 15 ns Max. clock-to-output)
- On-chip high-speed parallel register for pipelined systems
- On-chip high-speed "Shadow" register with serial shift mode for Serial Shadow Register (SSR) Diagnostics and for loading writable control stores
- Writable Initialize register for system interrupt or reset
- Synchronous or asynchronous output enable
- 24 mA output drive capability

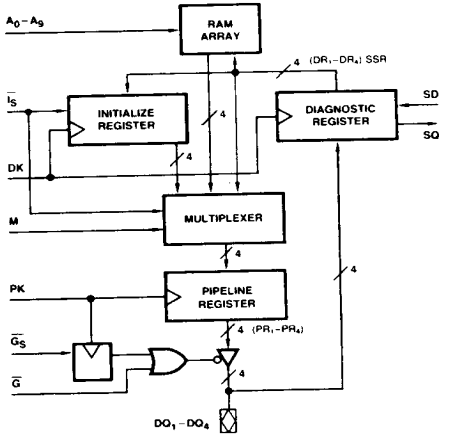
GENERAL DESCRIPTION

The Am9151 is a high-performance 1K x 4, n-channel, Registered Static RAM. The on-board registers are used for pipelined microprogrammed systems operation and for performing Serial Shadow Register (SSR) Diagnostics and Writable Control Store (WCS) loading.

The Am9151 contains three high-speed, 4-bit registers. The Pipeline register is a parallel data register in the memory array-to-output path intended for normal registered data operations. The Diagnostics register, also called a Serial Shadow Register (SSR), is used in a systematic way to control and observe the Pipeline register in order to exercise any desired system function during a diagnostic test mode. WCS loading can be accomplished by serially shifting an instruction word into the Shadow register and then clocking the data in parallel into memory. The Initialize register is used to generate any arbitrary microinstruction for system interrupt or reset.

The Am9151 operates from a single 5-volt supply and is fully TTL-compatible. The device is packaged in a slim 24-pin, 300-mil-wide DIP for the highest possible density.

BLOCK DIAGRAM



BD006270

PRODUCT SELECTOR GUIDE

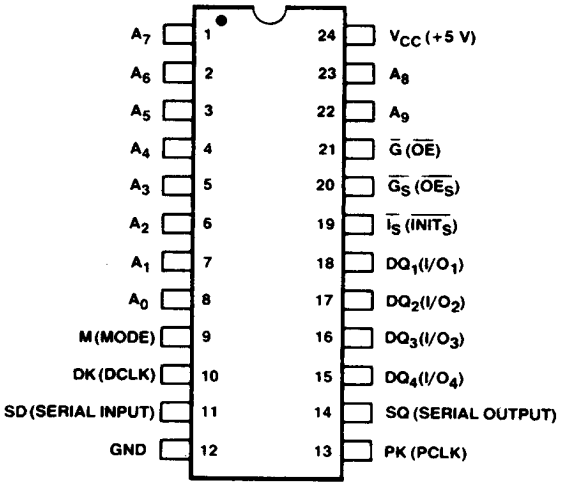
Part Number		Am9151-40	Am9151-50	Am9151-60
Minimum Cycle Time (ns)[1]		40	50	60
I_{CC} Max. (mA)	0°C to +70°C	180	180	180
	−55°C to +125°C	N/A	180	180

1. Cycle time = Address setup time plus clock to output time, including transition times.

SSR is a trademark of Advanced Micro Devices, Inc.

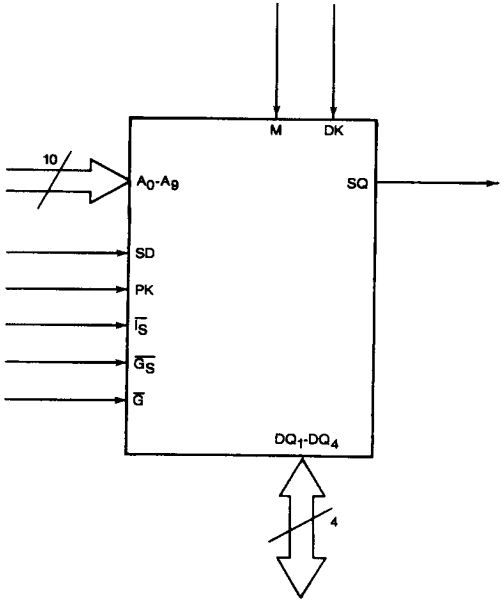
Publication # 05385 Rev. C Amendment /0
Issue Date: May 1986

CONNECTION DIAGRAM
Top View



CD009481

LOGIC SYMBOL



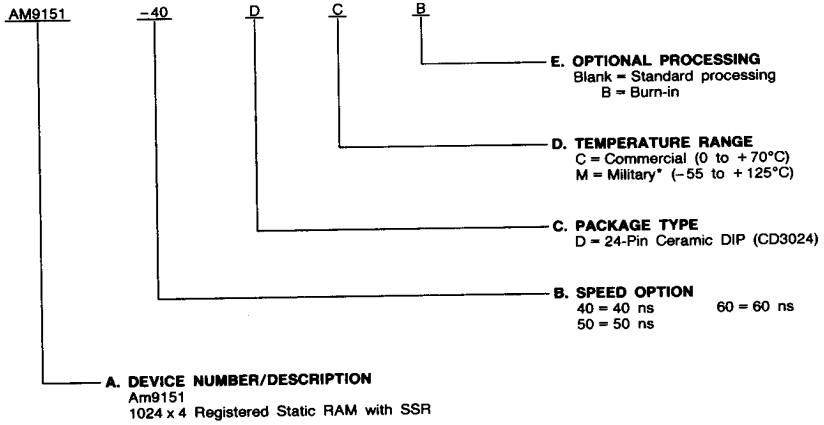
LS002440

ORDERING INFORMATION

Standard Products

AMD standard products are available in several packages and operating ranges. The order number (Valid Combination) is formed by a combination of:

A. Device Number
B. Speed Option (if applicable)
C. Package Type
D. Temperature Range
E. Optional Processing



*Military or Limited Military temperature range products are "NPL" (Non-Compliant Products List) or Non-MIL-STD-883C Compliant products only.

Valid Combinations	
AM9151-40	DC, DCB
AM9151-50	DC, DCB, DMB
AM9151-60	

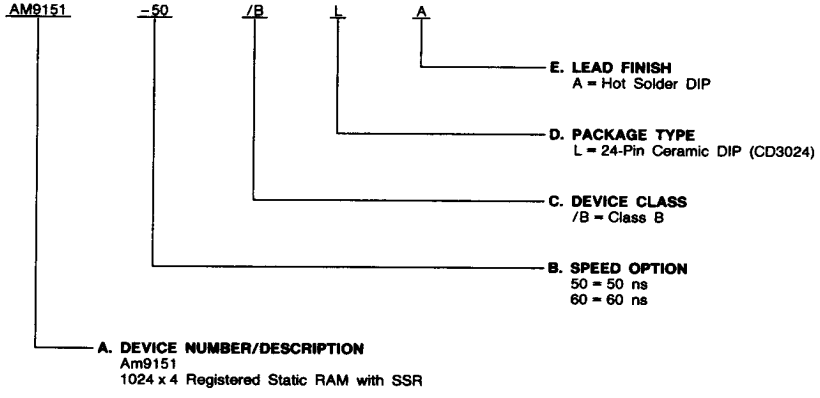
Valid Combinations

Valid Combinations list configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations, to check on newly released combinations, and to obtain additional data on AMD's standard military grade products.

ORDERING INFORMATION

APL Products

AMD products for Aerospace and Defense applications are available in several packages and operating ranges. APL (Approved Products List) products are fully compliant with MIL-STD-883C requirements. CPL (Controlled Products List) products are processed in accordance with MIL-STD-883C, but are inherently non-compliant because of package, solderability, or surface treatment exceptions to those specifications. The order number (Valid Combination) for APL products is formed by a combination of: **A. Device Number**
B. Speed Option (if applicable)
C. Device Class
D. Package Type
E. Lead Finish



Valid Combinations	
AM9151-50	/BLA
AM9151-60	

Valid Combinations

Valid Combinations list configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations or to check for newly released valid combinations.

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PIN DESCRIPTION

$A_0 - A_9$ Address (Inputs)
The 10-bit field presented at the address inputs selects one of the 1024 memory locations to be read from or written into.

M Mode (Input)
Control input for the pipeline register, multiplexer, shadow register, shadow register multiplexer, and initialize register.

DK Diagnostic Clock (Input)
The diagnostic clock is used to load or shift data into the shadow register. Also used to load data into the initialize register and the memory array. Transfer occurs on the LOW-to-HIGH transition of DK.

SD Serial Data Input (Input)
The input to the least significant bit of the shadow register when operating in the shift mode. SD is also a control input when it is not in the shift mode.

PK Pipeline Clock (Input)
The pipeline clock is used to load data into the pipeline register from the initialize register, shadow register, or the memory array.

SQ Serial Data Output (Output)
The output from the most significant bit of the shadow register. When mode is LOW SD feeds through to SQ.

$DQ_1 - DQ_4$ Data I/O Port (Input/Output)
Parallel data output from the pipeline register or parallel data input to the shadow register.

$\overline{IS}$ Synchronous Initialize (Input)
Control input for the initialize register. Used to load the pipeline register from the initialize register or load the initialize register from the shadow register. The initialize function can be used to generate any arbitrary microinstruction for system interrupt or reset.

$\overline{GS}$ Synchronous Output Enable (Input)
Controls the state of the DQ outputs in conjunction with PK.

$\overline{G}$ Asynchronous Output Enable (Input)
Controls the state of the DQ outputs independent of clock.

FUNCTIONAL DESCRIPTION

See the following function tables (Tables 1 and 2) for PK and DK operations.

TABLE 1. FUNCTION TABLE for PK OPERATIONS

PK transitions LOW-to-HIGH. DK stable at least 65 ns before PK transition, SD = Don't Care.

Inputs					Outputs	
PK	$\overline{IS}$	M	$\overline{GS}$	$\overline{G}$	$DQ_1 - DQ_4$	Operation
↑	L	L	L	L	$PR_1 - PR_4$	IREG → PREG
			H	X	Hi-Z	
			X	H	Hi-Z	
↑	H	L	L	L	$PR_1 - PR_4$	MEM → PREG
			H	X	Hi-Z	
			X	H	Hi-Z	
↑	X	H	L	L	$PR_1 - PR_4$	DREG → PREG
			H	X	Hi-Z	
			X	H	Hi-Z	

TABLE 2. FUNCTION TABLE for DK OPERATIONS

DK transitions LOW-to-HIGH, PK stable at least 65 ns before DK transition, $\overline{G}$ controls output impedance, otherwise Don't Care.

Inputs						Outputs	
DK	$\overline{IS}$	M	SD	$\overline{GS}$*	$\overline{G}$	$DQ_1 - DQ_4$	Operation
↑	L	H	H	L	L	$PR_1 - PR_4$	DREG → IREG
				H	X	Hi-Z	
				X	H	Hi-Z	
↑	X	L	X	L	L	$PR_1 - PR_4$	SHIFT DREG
				H	X	Hi-Z	
				X	H	Hi-Z	SD = DR_1, DR_4 = SQ
↑	X	H	L	L	L	$PR_1 - PR_4$	PDREG → DREG
				H	X	Hi-Z	DQ → DREG
				X	H	Hi-Z	$DQ_1 = DR_1$, $DQ_4 = DR_4$
↑	H	H	H	L	L	$PR_1 = PR_4$	
				H	X	Hi-Z	DREG → MEM
				X	H	Hi-Z	

*Set in a previous cycle by PK.

Note: If DK and PK transitions are within 65 ns of each other, the device will assume an unknown state.

APPLICATIONS

Applying Serial Shadow Register (SSR) Diagnostics In Sequential Logic Systems

Diagnostics

A diagnostics capability provides the necessary functionality as well as a systematic method for detecting and pin-pointing hardware related failures in a system. This capability must be able to both *observe* intermediate test points and *control* intermediate signals — address, data, control, and status — to exercise all portions of the system under test. These two capabilities, observability and controllability, provide the ability to establish a desired set of input conditions and state register values, sample the necessary outputs, and determine whether the system is functioning correctly.

Testing Combinational and Sequential Networks

The problem of testing a combinational logic network is well understood. Sets of input signals (test vectors) are applied to the network and the network outputs are compared to the set of computed outputs (result vectors). In some cases sets of test vectors and result vectors can be generated in a computer-aided environment, minimizing engineering effort. Additionally, fault coverage analysis can be automated to provide a measure of how efficient a set of test vectors is at pin-pointing hardware failures. For example, a popular measure of fault coverage computes the percentage of stuck-at-ones (nodes with outputs always HIGH) and stuck-at-zeros (nodes with outputs always LOW) a given set of test vectors will discover.

A sequential network (Figure 1) is much more difficult to test systematically. The outputs of a sequential network depend not only on the present inputs but also on the internal state of the network. Initializing the internal state register to the value necessary to test a given set of inputs is difficult at best, and not easily automated. Additionally, observing the internal state of a sequential network can be very difficult and time consuming if the state information is not directly available. For example, consider the problem of determining the value of an internal 16-bit counter if only a carry-out signal is available. The counter must be clocked until it reaches the carry-out state and the starting value computed. Up to 65,535 clock cycles may be necessary! An easier method must exist. Serial Shadow Register diagnostics provides this method.

Serial Shadow Register Diagnostics

Serial Shadow Register diagnostics provides sufficient observability and controllability to turn any sequential network into a combinational network. This is accomplished by providing the means to both initialize (control) and sample (observe) the state elements of a sequential network. Figure 2 shows the method by which Serial Shadow Register diagnostics accomplishes these two functions.

Serial Shadow Register diagnostics utilizes an extra multiplexer on the input of each state register and a duplicate or shadow of each state flip/flop in an additional register. The shadow register can be loaded serially via the serial data input (thus the name Serial Shadow Register diagnostics) for controllability. Once the desired state information is loaded into the serial register it can be transferred into the internal state register by selecting the multiplexer and clocking the state register with PCLK. This allows any internal state to be set to a desired state in a simple, quick, and systematic manner.

Internal state information can be sampled by loading the serial register from the state register outputs. This state information can then be shifted out via the serial data output to provide observability. Notice that the serial data inputs and outputs can be cascaded to make long chains of state information available on a minimum number of connections.

In effect, Serial Shadow Register diagnostics breaks the normal feedback path of the sequential network and establishes a logical path with which inputs can be defined and outputs sampled. This means that those techniques which have been developed to test combinational networks can be applied to any sequential network in which Serial Shadow Register diagnostics is utilized.

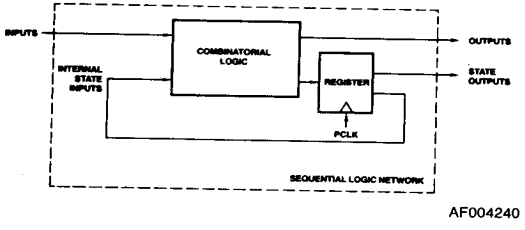

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Figure 1. Sequential Network

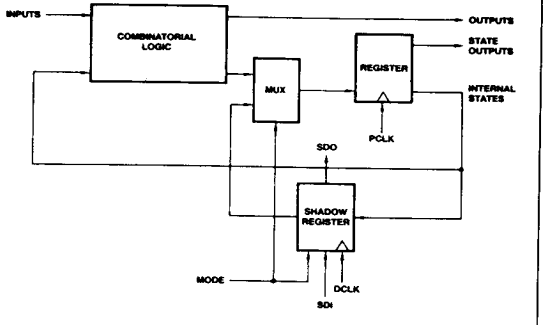

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Figure 2. Combinational Network

When normal pipeline registers are replaced by SSR diagnostics *pipeline registers, system debug and diagnostics are* easily implemented. State information which was inaccessible is now both observable and controllable. Figure 3 shows a typical computer system using Am29818's and Am9151's.

Serial paths have been added to all the important state registers (macroinstruction, data, status, address, and microinstruction registers). This extra path will make it easier to diagnose system failures by breaking the feed-back paths and turning sequential state machines into combinatorial logic blocks. For example, the status outputs of the ALU may be checked by loading the microinstruction register with the necessary microinstruction. The desired ALU function is then executed and the status outputs captured in the status register. The status bits can then be serially shifted out and checked for validity.

A single diagnostic loop was shown in Figure 3 for simplicity, but several loops can be employed in more complicated systems to reduce scan time. Additionally, the Am29818's can be used to sample intermediate test points not associated with normal state information. These additional test points can further ease diagnostics, testability and debug. The Am9151s' SSR format and functionality are identical to the Am29818.

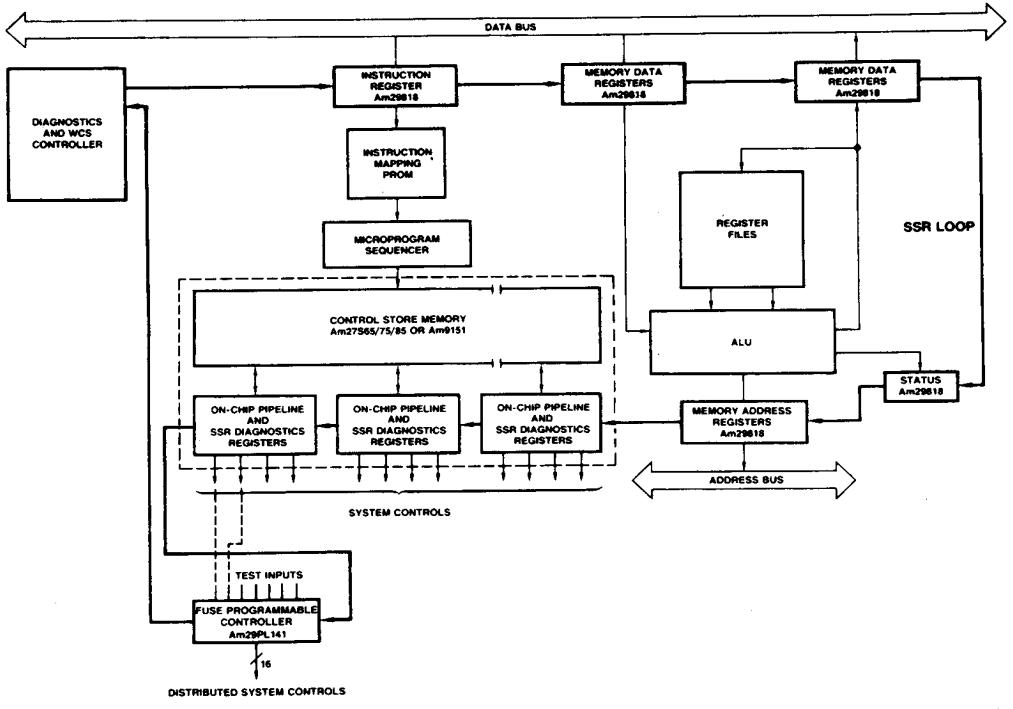


Figure 3. Typical System Configuration

ABSOLUTE MAXIMUM RATINGS (Note 1)

Storage Temperature ..... −65 to +150°C
Ambient Temperature with
Power Applied ..... −55 to +125°C
V_{CC} with Respect to GND ..... −0.5 to +7.0 V
All Signal Voltages with
Respect to GND ..... −3.5 to +7.0 V
Power Dissipation
(Package Limitation) ..... 1.2 W
DC Output Current ..... 20 mA

Stresses above those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to absolute maximum ratings for extended periods may affect device reliability.

OPERATING RANGES (Note 2)

Commercial (C) Devices
Temperature ..... 0 to +70°C
Supply Voltage ..... +4.5 to +5.5 V

Military (M) Devices*
Temperature ..... −55 to +125°C
Supply Voltage ..... +4.5 to +5.5 V

Operating ranges define those limits between which the functionality of the device is guaranteed.

*Military product 100% tested at T_C = +25°C, +125°C, and −55°C.

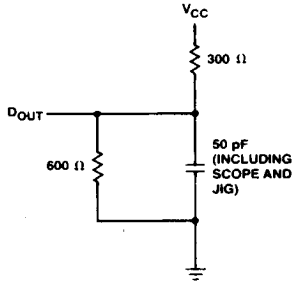
DC CHARACTERISTICS over operating range unless otherwise specified*

Parameter Symbol	Parameter Description	Test Conditions		Min.	Max.	Units
I_{OH} (DQ)	Parallel Output HIGH Current	V_{OH} = 2.4 V		−2		mA
I_{OL} (DQ)	Parallel Output LOW Current	V_{OL} = 0.4 V	T_A = +70°C	24		mA
			T_A = +125°C	18		
I_{OH} (SQ)	Serial Output HIGH Current	V_{OH} = 2.4 V		−0.5		mA
I_{OL} (SQ)	Serial Output LOW Current	V_{OL} = 0.5 V		4		mA
V_{IH}	Input HIGH Voltage			2.2	6.0	Volts
V_{IL}	Input LOW Voltage	(Note 6)		−0.5	0.8	Volts
I_{IX}	Input Load Corrent	$GND \leq V_I \leq V_{CC}$		−10	10	μA
I_{OZ}	Output Leakage Current	$GND \leq V_O \leq V_{CC}$		−50	50	μA
C_I	Input Capacitance	Test Frequency = 1.0 MHz T_A = 25°C, All Pins at 0 V, V_{CC} = 5 V (Note 8)			5	pF
$C_{I/O}$	Parallel Input/Output Capacitance				7	pF
C_O	Serial Output Capacitance				7	pF
I_{CC}	V_{CC} Operating Supply Current				180	mA
I_{OS} (DQ)	Parallel Output Short Circuit Current	V_O = 0 V (Notes 7, 8)			−225	mA
I_{OS} (SQ)	Serial Output Short Circuit Current	V_O = 0 V (Notes 7, 8)			−85	mA

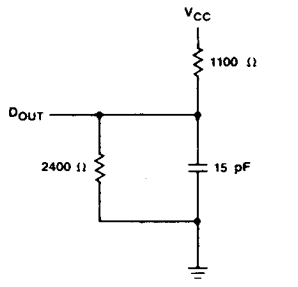
Notes:
1. Absolute Maximum Ratings are intended for user guidelines and are not tested.
2. For test and correlation purposes, operating temperature is defined as the "instant-ON" case temperature.
3. Test conditions assume signal transition time of 10 ns or less, timing reference levels of 1.5 V, input pulse levels of 0 to 3.0 V and output loading of the specified I_{OL}/I_{OH} and 50 pF load capacitance for $DQ_1 - DQ_4$ and 15 pF for SQ output; output timing reference is 1.5 V.
4. TGHDQZ and TPKHDQZ are measured to the V_{OH} −0.5 V and V_{OL} +0.5 V output levels using the load in C. under Switching Test Circuits.
5. All device test loads should be located within 2" of device outputs.
6. V_{IL} voltages of less than −0.5 V on $DQ_1 - DQ_4$ pins will cause the output current to exceed the maximum rating and thus should not exceed 30 seconds in duration.
7. For test purposes, not more than one output at a time should be shorted. Short circuit test duration should not exceed 30 seconds.
8. This parameter is not tested, but guaranteed by characterization.

*See the last page of this spec for Group A Subgroup Testing information.

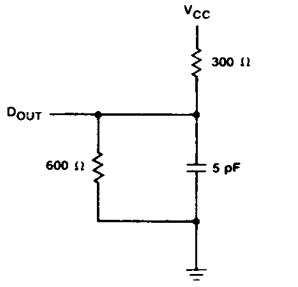
SWITCHING TEST CIRCUITS



A. Output Load for $DQ_1 - DQ_4$



B. Output Load for SQ



C. Output Load for TGHDQZ and TPKHDQZ (Note 4)

SWITCHING CHARACTERISTICS over operating range unless otherwise specified* (Cont'd.)

No.	Parameter Symbol	Parameter Description	Am9151-40		Am9151-50		Am9151-60		Units
			Min.	Max.	Min.	Max.	Min.	Max.	
PK-Controlled Operations									
1	TAVPKH	Address to PK HIGH Setup Time	25		30		35		ns
2	TPKHAX	Address from PK HIGH Hold Time	0		0		0		ns
3	TPKHDQV1	Delay from PK HIGH to Output Valid, if Outputs Were Not Hi-Z Initially		12		15		20	ns
4	TPKHDQV2	Delay from PK HIGH to Output Valid, if Outputs Were Hi-Z Initially		15		20		25	ns
5	TPKHPKL TPKLPKH	PK Pulse Width (LOW or HIGH)	15		20		25		ns
6	TGLDQV	Asynchronous Output Enable LOW to Output Valid		15		20		25	ns
7	TGHDQZ	Asynchronous Output Enable HIGH to Output Hi-Z (Note 4)		15		20		25	ns
8	TGSVPKH	$\overline{GS}$ to PK HIGH Setup Time	15		15		20		ns
9	TPKHGSX	$\overline{GS}$ from PK HIGH Hold Time	0		0		0		ns
10	TPKHDQZ	Delay from PK HIGH to Output in Hi-Z (Note 4)		15		20		25	ns
11	TMVPKH	Mode to PK HIGH Setup Time	35		35		40		ns
12	TPKHMX	Mode from PK HIGH Hold Time	5		5		5		ns
13	TIVPKH	Synchronous $\overline{I}$ to PK HIGH Setup Time	20		25		30		ns
14	TPKHIX	Synchronous $\overline{I}$ from PK HIGH Hold Time	5		5		5		ns
15	TDKSPKH	DK Stable to PK HIGH Setup Time	65		65		65		ns
16	TPKHDKX	DK from PK HIGH Hold Time	65		65		65		ns
		Address Input Rise and Fall Times		1		1		1	ns

SWITCHING CHARACTERISTICS over operating range unless otherwise specified*

No.	Parameter Symbol	Parameter Description	Am9151-40		Am9151-50		Am9151-60		Units
			Min.	Max.	Min.	Max.	Min.	Max.	
DK-Controlled Operations									
17	TPKSDKH	PK Stable to DK HIGH Setup Time	65		65		65		ns
18	TDKHPKX	PK from DK HIGH Hold Time	65		65		65		ns
19	TSDVDKH	Serial Data in to DK HIGH Setup Time	20		25		30		ns
20	TDKHSDX	Serial Data in from DK HIGH Hold Time	5		5		5		ns
21	TMVDKH	Mode to DK HIGH Setup Time	35		35		40		ns
22	TDKHMX	Mode from DK HIGH Hold Time	5		5		5		ns
23	TDQVDKH	Data in to DK HIGH Setup Time	20		25		30		ns
24	TDKHDQX	Data in from DK HIGH Hold Time	5		5		5		ns
25	TIVDKH	$\overline{IS}$ to DK HIGH Setup Time	20		25		30		ns
26	TDKHIX	$\overline{IS}$ from DK HIGH Hold Time	5		5		5		ns
27	TDKHSQV	Delay from DK HIGH to Serial Data Out Valid (Shifting)		35		35		40	ns
28	TDKHDKL TDKLDKH	DK Pulse Width (LOW or HIGH)	25		30		35		ns
29	TAVDKH	Address Valid to DK HIGH Setup Time for Memory Write	0		0		0		ns
30	TDKHAX	Address Hold from DK HIGH (Write)	40		50		60		ns
Non DK- or PK-Controlled Operations (DK = Stable, PK = Stable)									
31	TSDVSQV	Delay from Serial Data in Valid to Serial Data Out Valid (Mode HIGH)		25		30		35	ns
32	TMHSQV	Delay from Mode HIGH to Serial Data Out Valid		35		40		45	ns
33	TSDVMH	Serial Data in Valid to Mode HIGH Setup Time	0		0		0		ns
34	TMLSQV	Delay from Mode LOW to Serial Data Valid (SQ = DR4)		35		40		45	ns

*See the last page of this spec for Group A Subgroup Testing information.

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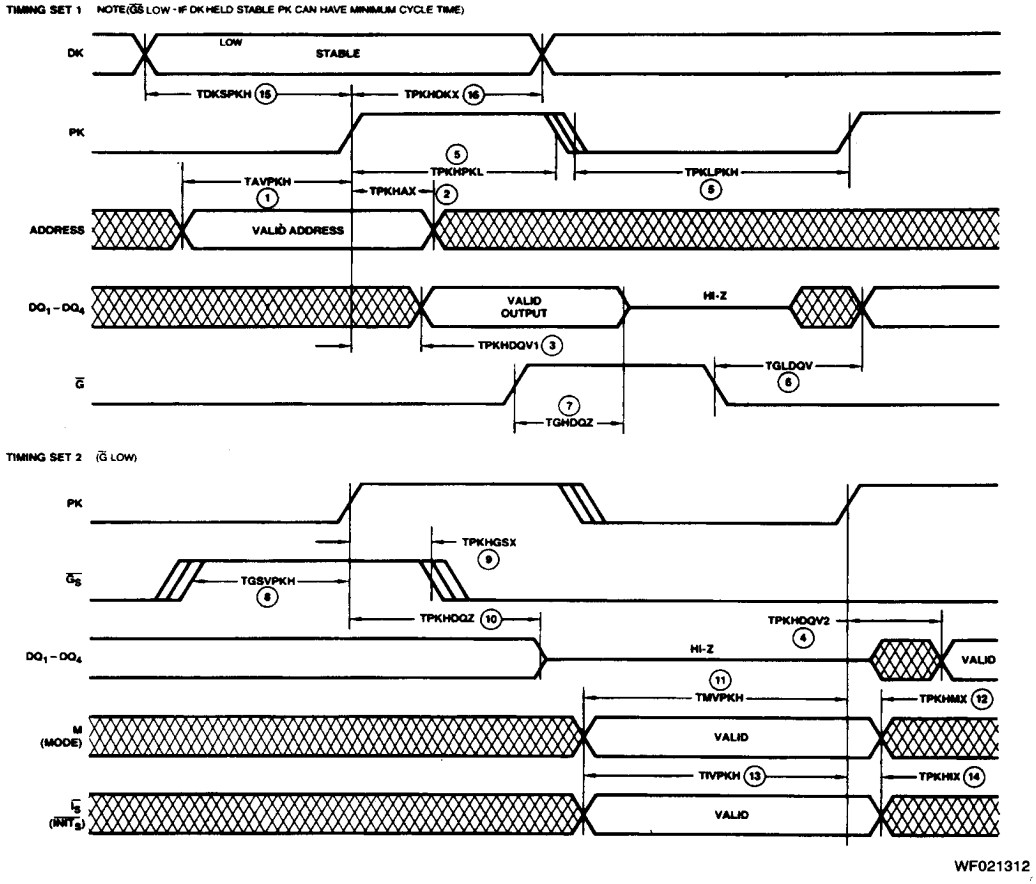
SWITCHING WAVEFORMS (Cont'd.)



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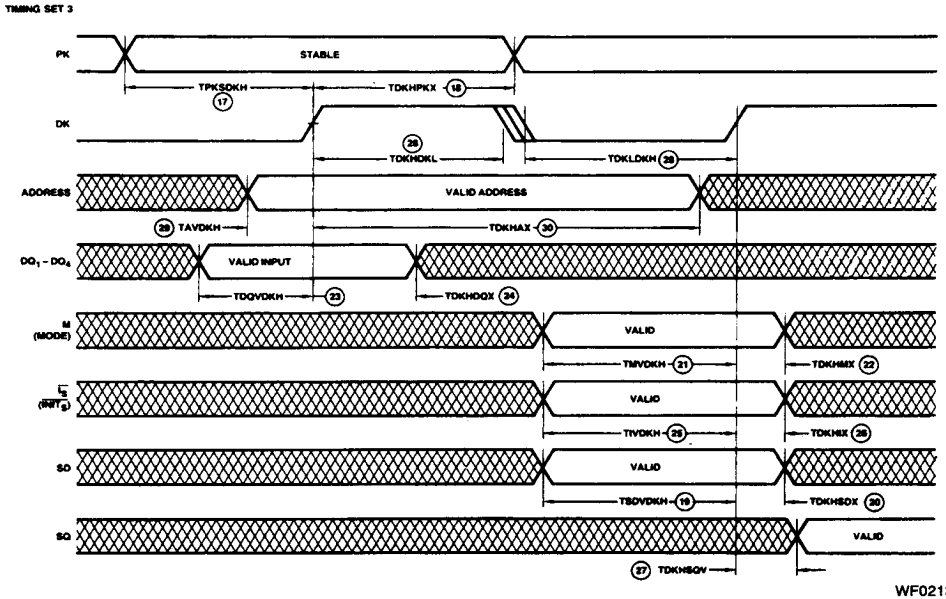
PK-Related

SWITCHING WAVEFORMS



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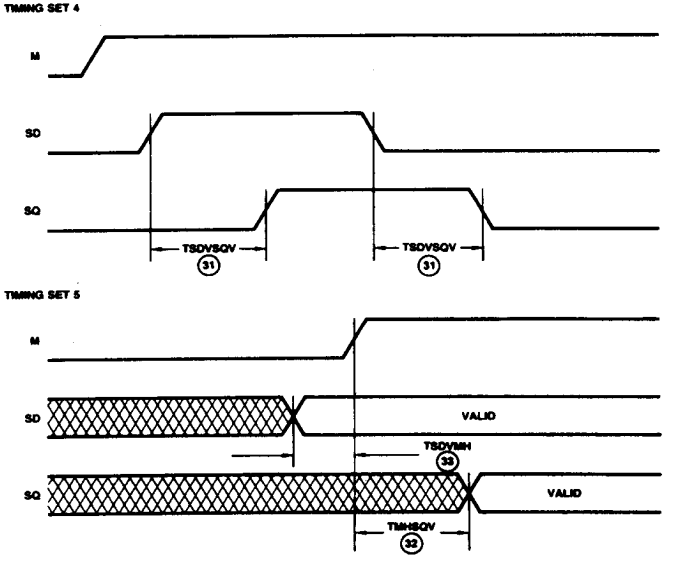
DK-Related



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Non DK- or PK-Related

GROUP A SUBGROUP TESTING

DC CHARACTERISTICS

Parameter Symbol	Subgroups
I_{OH} (DQ)	1, 2, 3
I_{OL}(DQ)	1, 2, 3
I_{OH} (SQ)	1, 2, 3
I_{OL}(SQ)	1, 2, 3
V_{IH}	7, 8
V_{IL}	7, 8
I_{IX}	1, 2, 3
I_{OZ}	1, 2, 3
I_{CC}	1, 2, 3

SWITCHING CHARACTERISTICS

No.	Parameter Symbol	Subgroups	No.	Parameter Symbol	Subgroups
1	TAVPKH	7, 8, 9, 10, 11	19	TSDVDKH	7, 8, 9, 10, 11
2	TPKHAX	7, 8, 9, 10, 11	20	TDKHSDX	7, 8, 9, 10, 11
3	TPKHDQV1	7, 8, 9, 10, 11	21	TMVDKH	7, 8, 9, 10, 11
4	TPKHDQV2	7, 8, 9, 10, 11	22	TDKHMX	7, 8, 9, 10, 11
5	TPKHPKL TPKHPKH	7, 8, 9, 10, 11	23	TDQVDKH	7, 8, 9, 10, 11
6	TGLDQV	7, 8, 9, 10, 11	24	TDKHDQX	7, 8, 9, 10, 11
8	TGSVPKH	7, 8, 9, 10, 11	25	TIVDKH	7, 8, 9, 10, 11
9	TPKHGSX	7, 8, 9, 10, 11	26	TDKHIX	7, 8, 9, 10, 11
11	TMVPKH	7, 8, 9, 10, 11	27	TDKHSQV	7, 8, 9, 10, 11
12	TPKHMX	7, 8, 9, 10, 11	28	TDKHDKL TDKLDKH	7, 8, 9, 10, 11
13	TIVPKH	7, 8, 9, 10, 11	29	TAVDKH	7, 8, 9, 10, 11
14	TPKHIX	7, 8, 9, 10, 11	30	TDKHAX	7, 8, 9, 10, 11
15	TDKSPKH	7, 8, 9, 10, 11	31	TSDVSQV	7, 8, 9, 10, 11
16	TPKHDKX	7, 8, 9, 10, 11	32	TMHSQV	7, 8, 9, 10, 11
17	TPKSDKH	7, 8, 9, 10, 11	33	TSDVMH	7, 8, 9, 10, 11
18	TDKHPKX	7, 8, 9, 10, 11	34	TMLSQV	7, 8, 9, 10, 11

MILITARY BURN-IN

Military burn-in is in accordance with the current revision of MIL-STD-883, Test Method 1015, Conditions A through E. Test conditions are selected at AMD's option.