APPLICATION NOTE AND DEVELOPMENT SYSTEM
AVAILABLE
AN67 • XK76

Password Access Security Supervisor

4K X76041 4 x 128 x 8 Bit

PASS™ E²

FEATURES

- 64-Bit Password Security
- Three Password Modes
  - —Secure Read Access
  - —Secure Write Access
  - —Secure Configuration Access
- Programmable Configuration
  - —Read, Write and Configuration Access Passwords
  - —Multiple Array Access/Functionality
  - —Retry Register/Counter
- 8 Byte Page Mode Write
- (4) 1K Memory Arrays
- ISO Response to Reset
- Low Power CMOS
  - —3V to 5.5V Power Supply
  - —50µA Standby Current
  - —3mA Active Current
- High Reliability
  - —Endurance: 100,000 Cycles Per Byte
  - —Data Retention: 100 Years
  - —ESD Protection: 2000V on All Pins

DESCRIPTION

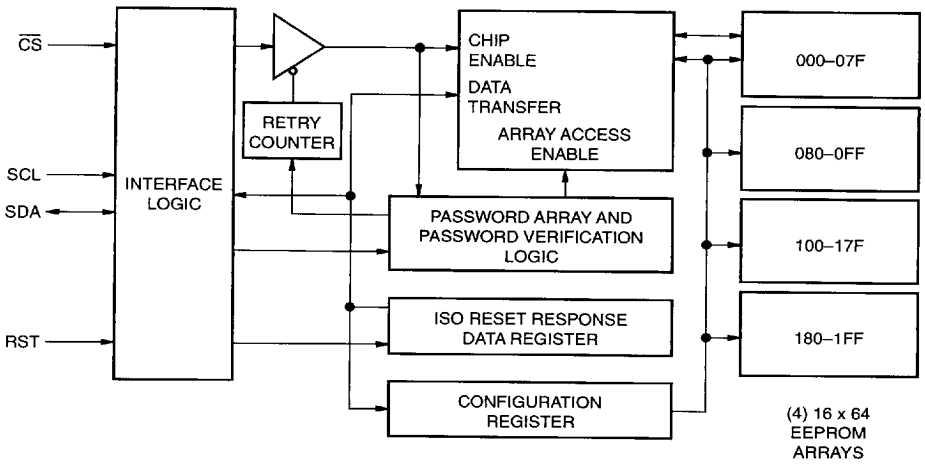
The X76041 is a password access security supervisor device, containing four 128 x 8 bit E²PROM arrays. Access can be controlled by three 64-bit programmable passwords, one for read operations, one for write operations and one for device configuration.

The X76041 features a serial interface and software protocol allowing operation on a simple two wire bus. The bus signals are a clock input (SCL) and a bidirectional data input and output (SDA). Access to the device is controlled through a chip select input ($\overline{CS}$), allowing any number of devices to share the same bus.

The X76041 also features a synchronous response to reset; providing an automatic output of a pre-configured 32-bit data stream conforming to the ISO standard for memory cards.

The X76041 utilizes Xicor's proprietary Direct Write™ cell, providing a minimum endurance of 100,000 cycles per byte and a minimum data retention of 100 years.

FUNCTIONAL DIAGRAM



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PIN DESCRIPTION

Serial Data Input/Output (SDA)

SDA is a true three state serial data input/output pin. During a read cycle, data is shifted out on this pin. During a write cycle, data is shifted in on this pin. In all other cases this pin is in a high impedance state.

Serial Clock (SCL)

The Serial Clock controls the serial bus timing for data input and output.

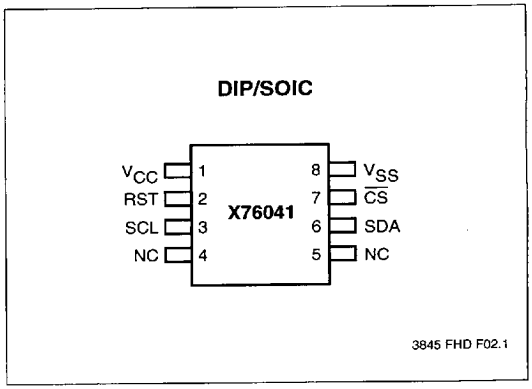
Chip Select ($\overline{CS}$)

When $\overline{CS}$ is HIGH, the X76041 is deselected and the SDA pin is at high impedance and unless an internal write operation is underway the X76041 will be in the standby power mode. $\overline{CS}$ LOW enables the X76041, placing it in the active power mode.

Reset (RST)

RST is a device reset pin. When RST is pulsed HIGH while $\overline{CS}$ is LOW the X76041 will output 32 bits of fixed data which conforms to the ISO standard for "synchronous response to reset". $\overline{CS}$ must remain LOW and the part must not be in a write cycle for the response to reset to occur. If at any time during the response to reset $\overline{CS}$ goes HIGH, the response to reset will be aborted and the part will return to the standby mode.

PIN CONFIGURATION



Symbol	Description
$\overline{CS}$	Chip Select Input
SDA	Serial Data Input/Output
RST	Reset Input
SCL	Serial Clock Input
V_{SS}	Ground
V_{CC}	Supply Voltage
NC	No Connect

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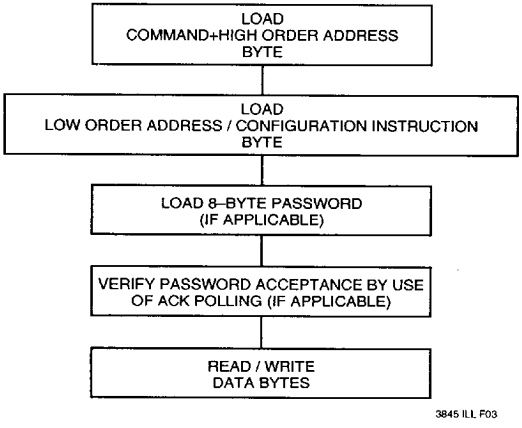
DEVICE OPERATION

There are three primary modes of operation for the X76041; READ, WRITE and CONFIGURATION. The READ and WRITE modes may be performed with or without an 8-byte password. The CONFIGURATION mode always requires an 8-byte password.

The basic method of communication is established by first enabling the device ($\overline{CS}$ LOW), generating a start condition and then transmitting a command and address field followed by the correct password (if configured to require a password). All parts will be shipped from the factory in the non-password mode. The user must perform an ACK Polling routine to determine the validity of the password and start the data transfer (see Acknowledge Polling). Only after the correct password is accepted and an ACK Polling has been performed can the data transfer occur.

To ensure correct communication, RST must remain LOW under all conditions except when initiating a "Response to Reset sequence".

Figure 1. X76041 Device Operation



Data is transferred in 8-bit segments, with each transfer being followed by an ACK, generated by the receiving device.

If the X76041 is in a nonvolatile write cycle a "no ACK" (SDA HIGH) response will be issued in response to loading of the command + high order address byte. If a stop condition is issued prior to the nonvolatile write cycle the write operation will be terminated and the part will reset and enter into a standby mode.

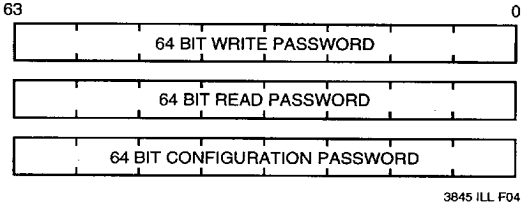
The basic sequence is illustrated in Figure 1.

After each transaction is completed, the X76041 will reset and enter into a standby mode. This will also be the response if an attempt is made to access any limited array.

Password Registers

The three passwords, Read, Write and Configuration are stored in three 64 bit Write Only registers as illustrated in figure 2.

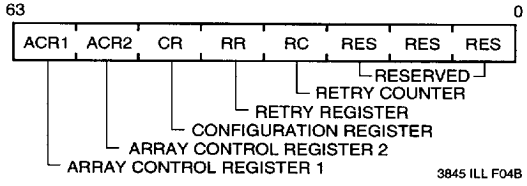
Figure 2. Password Registers



Device Configuration

Five 8-Bit configuration registers are used to configure the X76041. These are shown in figure 3.

Figure 3.Configuration Registers



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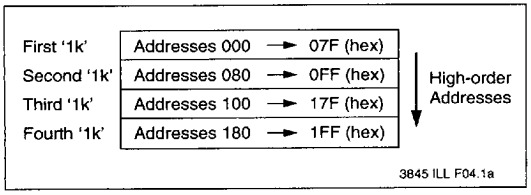
Array Control

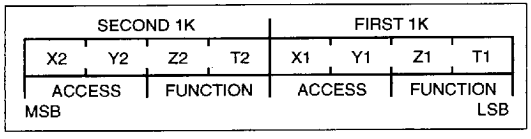
The four 1K arrays, are each programmable to different levels of access and functionality. Each array can be programmed to require or not require the read/write passwords. The functional options are:

- Read and Write Access.
- Read access with all write operations locked out.
- Read access and program only (writing a "1" to a "0"). If an attempt to change a "0" to a "1" occurs the X76041 will reset, issue a "no ACK" and enter the standby power mode.
- No read or write access to the memory. Access only through use of the configuration password.

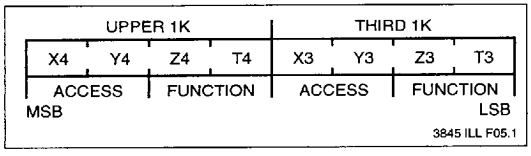
Array Map



8 Bit Array Control Register 1



8 Bit Array Control Register 2



Functional Bits

Z	T	FUNCTIONALITY
0	0	READ AND WRITE UNLIMITED
1	0	READ ONLY, WRITE LIMITED
0	1	PROGRAM & READ ONLY, ERASE LIMITED
1	1	NO READ OR WRITE, FULLY LIMITED

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Access Bits

X	Y	READ PASSWORD	WRITE PASSWORD
0	0	NOT REQUIRED	NOT REQUIRED
1	0	NOT REQUIRED	REQUIRED
0	1	REQUIRED	NOT REQUIRED
1	1	REQUIRED	REQUIRED

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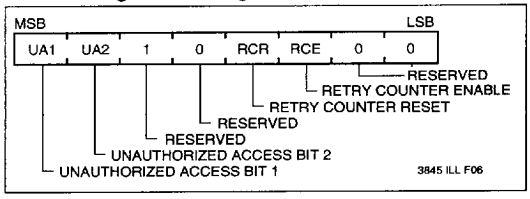
8-Bit Configuration Register



Unauthorized Access Bits (UA1, UA2):

1 0

Access is forbidden if retry register equals the retry counter (provided that the retry counter is enabled) and no further access of any kind will be allowed.

0 1, 0 0, 1 1

Only configuration operations are allowed if the retry register equals the retry counter (provided that the retry counter is enabled).

Retry Counter Reset Bit (RCR):

If the retry counter reset bit is a "1" then the retry counter will be reset following a correct password, provided the retry counter is enabled.

If the retry counter reset bit is a "0" then the retry counter will not be reset following a correct password, provided the retry counter is enabled.

Retry Counter Enable Bit (RCE):

If the Retry counter enable bit is a "1", then the retry counter is enabled. An initial comparison between the retry register and retry counter determines whether the number of allowed incorrect password attempts has been reached. If not, the protocol continues and in case of a wrong password, the retry counter is incremented by one. If the password is correct then the retry counter will either be reset or unchanged, depending on the reset bit.

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The retry register must have a higher value than the retry counter for correct device operation. If the retry counter value is larger than the retry register and the retry counter is enabled, the device will wrap around allowing up to an additional 255 incorrect access attempts.

If the Retry counter enable bit is a "0", then the retry counter is disabled.

Retry Register/Counter

Both the retry register and retry counter are accessible in the configuration mode and may be programmed with a value of 0 to 255.

The difference between the retry register and the retry counter is the number of access attempts allowed, therefore the retry counter must be programmed to a smaller value than the retry register to prevent wrap around.

DEVICE PROTOCOL

The X76041 supports a bidirectional bus oriented protocol. The protocol defines any device that sends data onto the bus as a transmitter, and the receiving device as the receiver. The device controlling the transfer is a master and the device being controlled is the slave. The master will always initiate data transfers, and provide the clock for both transmit and receive operations. Therefore, the X76041 will be considered a slave in all applications.

Start Condition

All commands except for response to reset are preceded by the start condition, which is a HIGH to LOW transition of SDA when SCL is HIGH. The X76041 continuously monitors the SDA and SCL lines for the start condition and will not respond to any command until this condition has been met.

Figure 2. Data Validity During Write

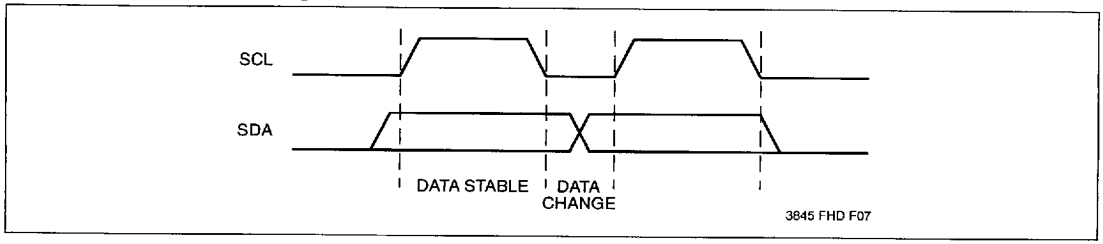
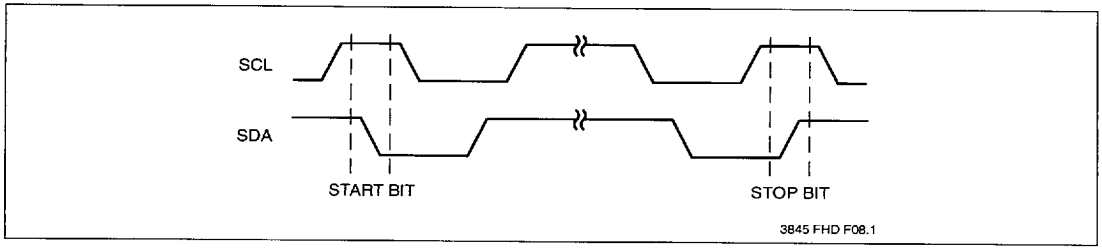


Figure 3. Definition of Start and Stop



NOTE: The part requires the SCL input to be LOW during non-active periods of operation. In other words, the SCL will need to be LOW prior to any START condition and LOW after a STOP condition. This is also reflected in the timing diagram.

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Stop Condition

All communications must be terminated by a stop condition, which is a LOW to HIGH transition of SDA when SCL is HIGH. A stop condition can only be issued after the transmitting device has released the bus.

Acknowledge

Acknowledge is a software convention used to indicate successful data transfer. The transmitting device, either master or slave, will release the bus after transmitting eight bits. During the ninth clock cycle the receiver will pull the SDA line LOW to acknowledge that it received the eight bits of data.

OPERATIONAL MODES

THE FIRST BYTE IN THE PROTOCOL	THE SECOND BYTE IN THE PROTOCOL	COMMAND DESCRIPTION	PASSWORD USED:
0 0 0XXXXA	Write address	Write (Byte / Page)	Write
0 0 1XXXXA	Read address	Read (Random / Sequential)	Read
0 1 0XXXXA	Write address	Write (Byte / Page)	Configuration
0 1 1XXXXA	Read address	Read (Random / Sequential)	Configuration
1 0 0XXXXX	0 0 0 0 0 0 0 0	Program write-password	Write
1 0 0XXXXX	0 0 0 1 0 0 0 0	Program read-password	Read
1 0 0XXXXX	0 0 1 0 0 0 0 0	Program configuration-password	Configuration
1 0 0XXXXX	0 0 1 1 0 0 0 0	Reset write password (all 0's)	Configuration
1 0 0XXXXX	0 1 0 0 0 0 0 0	Reset read password (all 0's)	Configuration
1 0 0XXXXX	0 1 0 1 0 0 0 0	Program configuration registers	Configuration
1 0 0XXXXX	0 1 1 0 0 0 0 0	Read configuration registers	Configuration
1 0 0XXXXX	0 1 1 1 0 0 0 0	Mass program	Configuration
1 0 0XXXXX	1 0 0 0 0 0 0 0	Mass erase	Configuration
All the rest		Reserved	

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NOTE: Illegal command codes will be disregarded. The part will respond with a "no-ACK" to the illegal byte and then return to the standby mode. All write/read operations may or may not require a password.

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WRITE OPERATIONS

Byte Write

The Byte Write mode requires issuing a 3-bit command followed by the address, password (if required) and then the data byte transfer as illustrated in Figure 4. After the data byte to be transferred is acknowledged a stop condition is issued which starts the nonvolatile write cycle. The nonvolatile write cycle starts with the falling edge of SCL following the stop condition.

Page Write

The Page Write mode requires issuing the 3-bit write command followed by the address, password if required and then the data bytes transferred as illustrated in Figure 5. Up to 8 bytes may be transferred. After the last byte to be transferred is acknowledged a stop condition is issued which starts the nonvolatile write cycle. If more than 8 bytes are transferred the data will wrap around and previous data will be overwritten. All data will be written to the same page as defined by A_8–A_3.

Figure 4. Byte Write

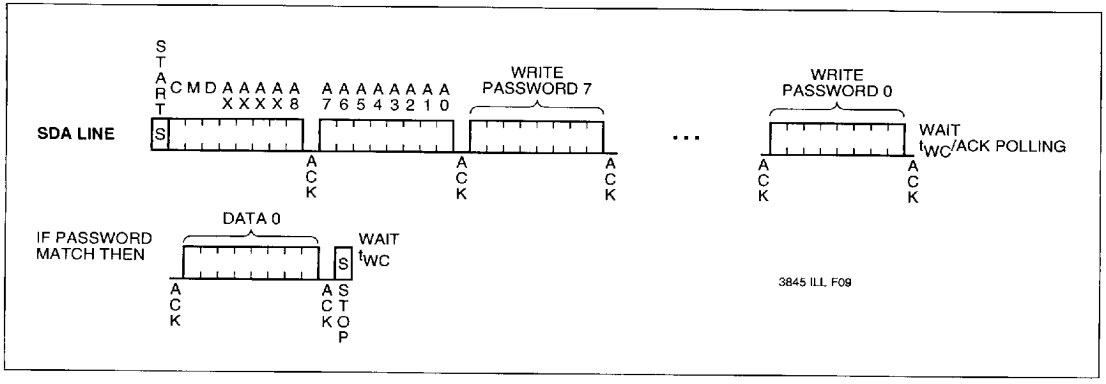
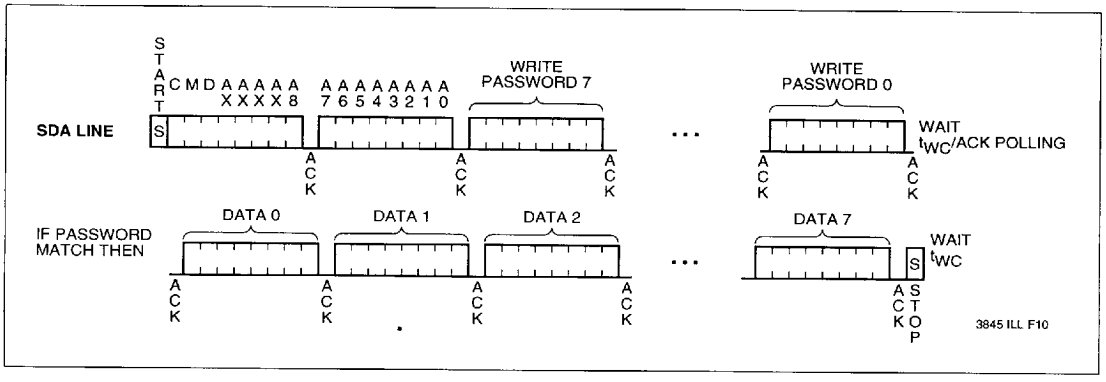


Figure 5. Page Write



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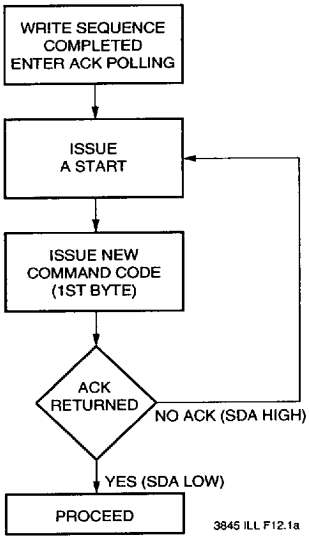
ACK Polling

Once a stop condition is issued to indicate the end of the host's write sequence, the X76041 initiates the internal nonvolatile write cycle. In order to take advantage of the typical 5ms write cycle, ACK polling can be initiated immediately. This involves issuing the Start condition followed by the new command code of eight bits (1st byte of the protocol). If the X76041 is still busy with the nonvolatile write operation, it will issue a "no ACK" in response. If the nonvolatile write operation has completed, an "ACK" will be returned and the host can then proceed with the rest of the protocol. Refer to the following flow:

ACK Polling Sequence



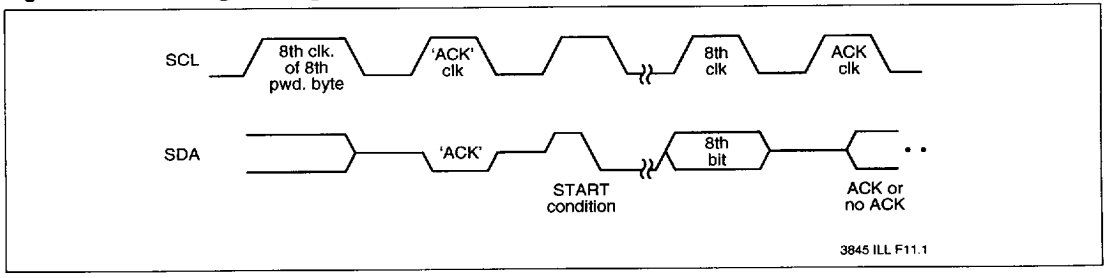
After a password sequence, there is always a nonvolatile write cycle. In order to continue the transaction, the X76041 requires the master to perform an ACK polling with the specific code of C0h. As with regular acknowledge polling the user can either time out for 10ms, and then issue the ACK polling once, or continuously loop as described in the flow.

As with regular acknowledge polling, if the user chooses to loop, then as long as the nonvolatile write cycle is active, a no ACK will be issued in response to each polling cycle.

If the password that was inserted was correct, then an "ACK" will be returned once the nonvolatile write cycle is over, in response to the ACK polling cycle immediately following it.

If the password that was inserted was incorrect, then a "no ACK" will be returned even if the nonvolatile write cycle is over. Therefore, the user cannot be certain that the password is incorrect until the 10ms write cycle time has elapsed.

Figure 6. Acknowledge Polling



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READ OPERATIONS

Read operations are initiated in the same manner as write operations but with a different command code.

Random Read

With random read, an address must be supplied with the read command. Once the password has been acknowledged and first byte has been read, another start can be issued followed by a new 8-bit address. Random reads are allowed only within the original 1K-bit array. Therefore the A7 bit that is given in the new address is actually a "don't care". To access another 1K-bit array, a stop must be issued followed by a new command/address/password sequence.

Sequential Read

Once past the password acceptance sequence (when required), the host can read sequentially within the originally addressed 1K-bit array. The data output is sequential, with the data from address n followed by the data from n+1. The address counter for read operations increments all address bits, allowing the 1K memory contents to be serially read during one operation. At the end of the address space (address 127), the counter "rolls over" to address 0 and the X76041 continues to output data for each acknowledge received. Refer to figure 8 for the address, acknowledge and data transfer sequence. An acknowledge must follow each 8-bit data transfer. After the last bit has been read, a stop condition is generated without a preceding acknowledge.

Figure 7. Random Read with Password

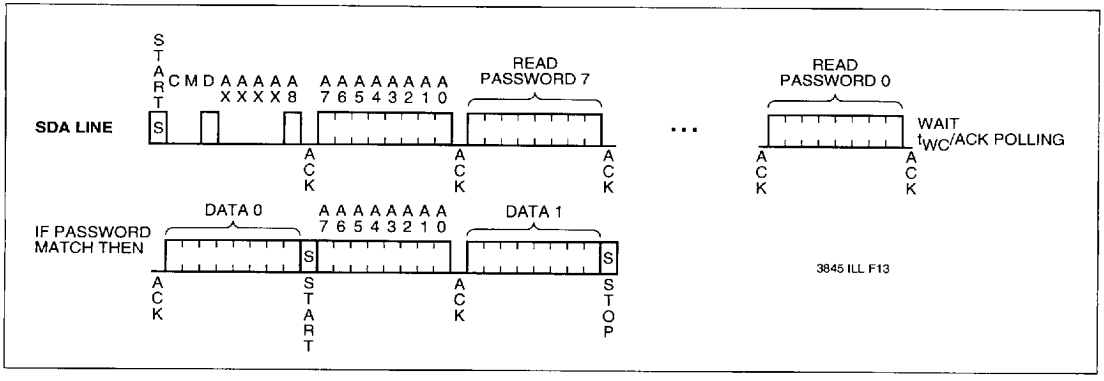
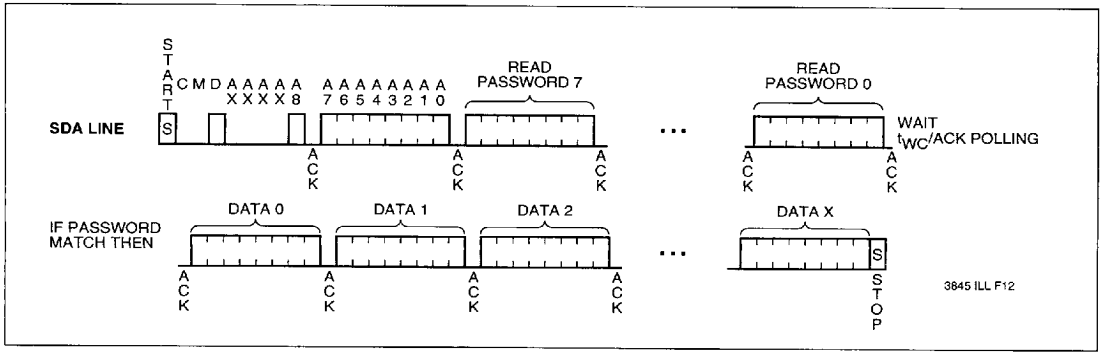


Figure 8. Sequential Read with Password



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CONFIGURATION OPERATIONS

Configuration commands generally require the configuration password. The exception is that programming a new read/write password requires the old read/write password and not the configuration password. In most cases these operations will be performed by the equipment manufacturer or end distributor of the equipment or card.

Configuration Read/Write

Configuration read/write allows access to all of the nonvolatile memory arrays regardless of the contents of the configuration registers. Access includes byte and page mode writes, random and sequential reads using the same format as normal reads and writes.

In general, the configuration read/write operation enables access to any memory location that may otherwise be limited. The configuration password, in this sense, is like a master key that can override the limits caused by the control partitioning of the arrays.

Figure 9. Configuration Write

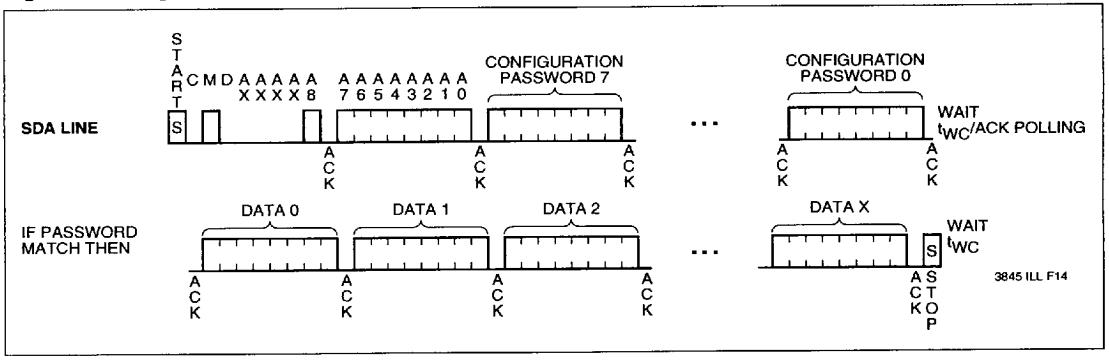

Figure 10. Configuration Sequential Read

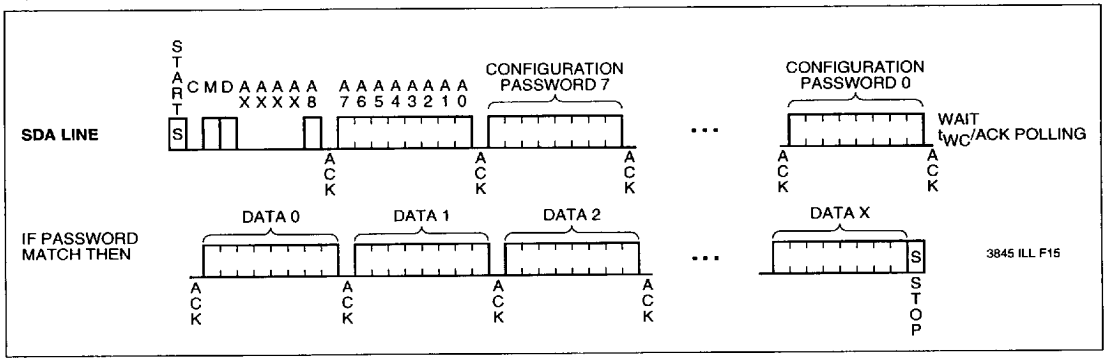

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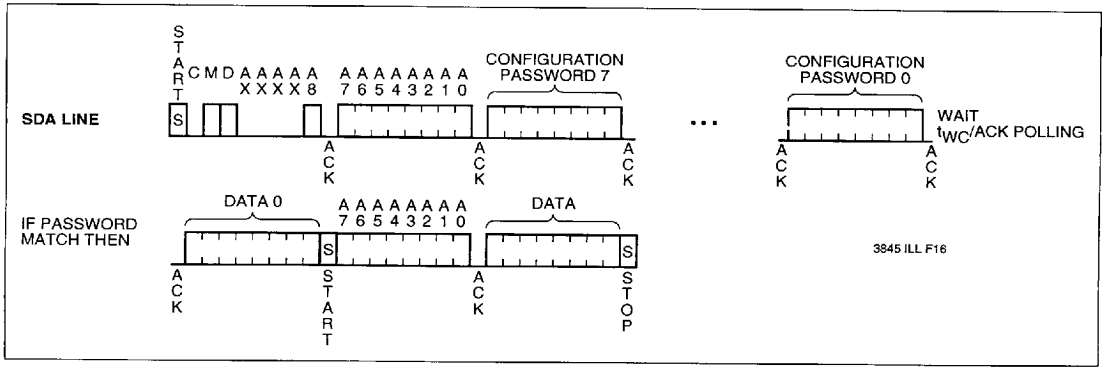
Figure 11. Configuration Random Read

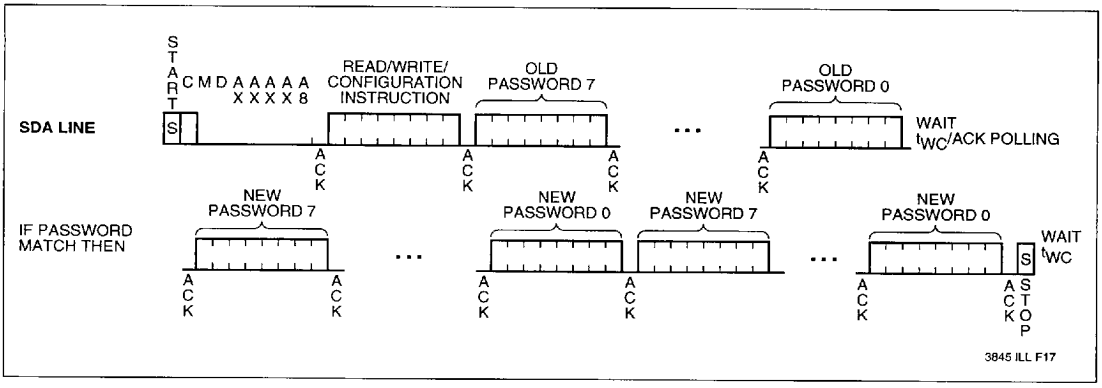


Configuration of Passwords

The sequence in figure 12 will change (program) the write, read and configuration passwords. The programming of passwords is done twice prior to the nonvolatile write cycle in order to verify that the new password is consistent. After the eight bytes are entered in the second pass, a comparison takes place. A mismatch will cause the part to reset and enter into the standby mode and a "no ACK" will be issued.

There is no way to read the Read/Write/Configuration passwords.

Figure 12. Program Passwords



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Program Configuration Registers

This mode allows programming of the five configuration/control registers using the configuration password. The retry counter must be programmed with a value less than the retry register. If it is programmed with a value larger than the retry register there will be a wrap around.

Read Configuration Registers

This mode allows reading of the 5 configuration/control registers with the configuration password. It may be useful for monitoring purposes.

Read Password Reset

This mode allows resetting of the READ password to all "0"s in case re-programming is needed and the old password is not known.

Write Password Reset

This mode allows resetting of the WRITE password to all "0"s in case re-programming is needed and the old password is not known.

Mass Program

This mode allows mass programming of the array, configuration registers and password to all "0"s using a special configuration command. All parts are shipped mass programmed.

Mass Erase

This mode allows mass erase of the array, configuration register and password to all "1"s using a special configuration command.

Figure 13. Program Configuration Registers

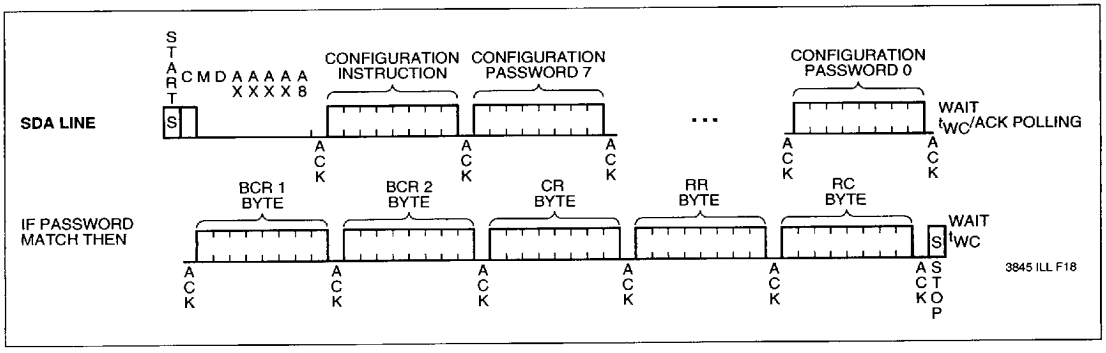

Figure 14. Read Configuration Registers

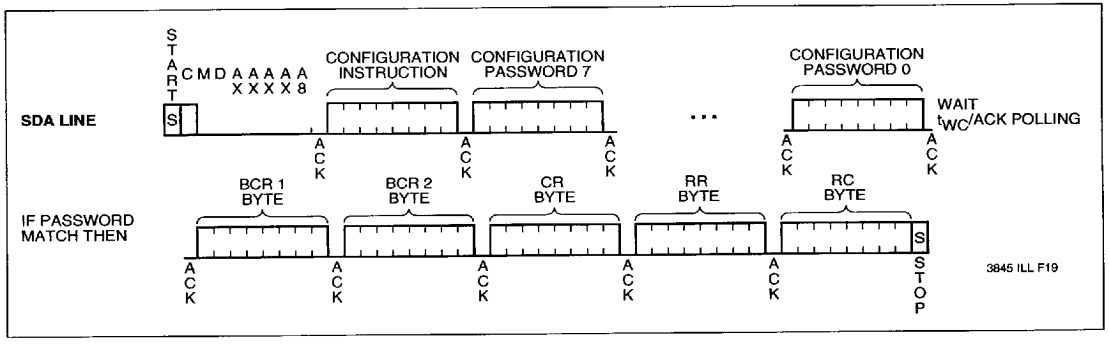

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Figure 15. Read/Write Password Reset

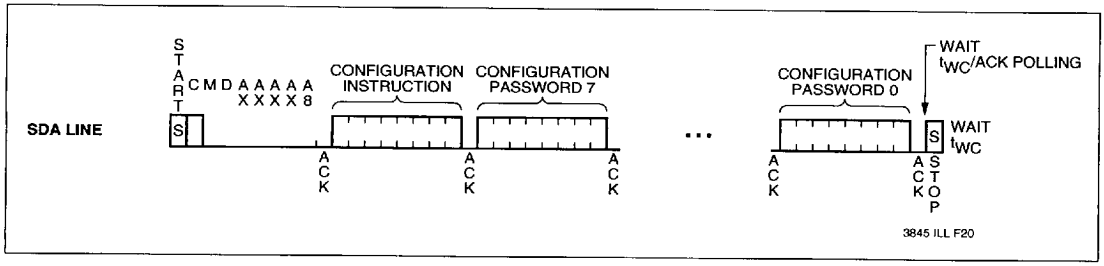
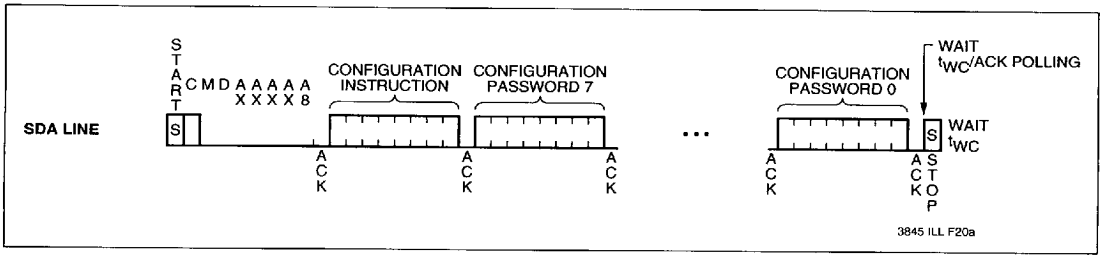


Figure 16. Mass Program/Erase



SYMBOL TABLE

WAVEFORM	INPUTS	OUTPUTS
	Must be steady	Will be steady
	May change from LOW to HIGH	Will change from LOW to HIGH
	May change from HIGH to LOW	Will change from HIGH to LOW
	Don't Care: Changes Allowed	Changing: State Not Known
	N/A	Center Line is High Impedance

ABSOLUTE MAXIMUM RATINGS*

Temperature under Bias ..... –65°C to +135°C
Storage Temperature ..... –65°C to +150°C
Voltage on any Pin with
Respect to V_{SS} ..... –1V to +7V
D.C. Output Current 5mA
Lead Temperature
(Soldering, 10 seconds) ..... 300°C

***COMMENT**

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and the functional operation of the device at these or any other conditions above those listed in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

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RECOMMENDED OPERATING CONDITIONS

Temp	Min.	Max.
Commercial	0°C	+70°C
Industrial	–40°C	+85°C
Military	–55°C	+125°C

3845 PGM T05.1

Supply Voltage	Limits
X76041	4.5V to 5.5V
X76041 – 3	3V to 5.5V

3845 PGM T06.1

D.C. OPERATING CHARACTERISTICS (Over the recommended operating conditions unless otherwise specified.)

Symbol	Parameter	Limits Min.	Limits Max.	Units	Test Conditions
I_{CC1}	V_{CC} Supply Current (Read)		2	mA	$f_{SCL} = V_{CC}x0.1/V_{CC}x0.9$ Levels @ 1MHz, SDA = Open, RST = $\overline{CS}$ = V_{SS}
I_{CC2}	V_{CC} Supply Current (Write)		3	mA	$f_{SCL} = V_{CC}x0.1/V_{CC}x0.9$ Levels @ 1MHz, SDA = Open, RST = $\overline{CS}$ = V_{SS}
I_{SB1}(1)	V_{CC} Supply Current (Standby)		100	µA	SCL = V_{SS}, $\overline{CS}$ = V_{CC} – 0.3V, SDA = Open, RST = V_{CC} = 5.5V
I_{SB2}(1)	V_{CC} Supply Current (Standby)		50	µA	SCL = V_{SS}, $\overline{CS}$ = V_{SS}, V_{CC} – 0.3V, SDA = Open, RST = V_{SS}, V_{CC} = 3V
I_{LI}	Input Leakage Current		10	µA	$V_{IN} = V_{SS}$ to V_{CC}
I_{LO}	Output Leakage Current		10	µA	$V_{OUT} = V_{SS}$ to V_{CC}
V_{IL}(2)	Input LOW Voltage	–1	V_{CC} x 0.3	V	
V_{IH}(2)	Input HIGH Voltage	V_{CC} x 0.7	V_{CC} + 0.5	V	
V_{OL}	Output LOW Voltage		0.4	V	I_{OL} = 2mA
V_{OH}	Output HIGH Voltage	V_{CC}–0.8		V	I_{OH} = –1mA

3845 PGM T07.3

CAPACITANCE T_A = +25°C, f = 1MHz, V_{CC} = 5V

Symbol	Test	Max.	Units	Conditions
C_{OUT}(3)	Output Capacitance (SDA)	10	pF	$V_{I/O}$ = 0V
C_{IN}(3)	Input Capacitance (RST, SCL, $\overline{CS}$)	10	pF	V_{IN} = 0V

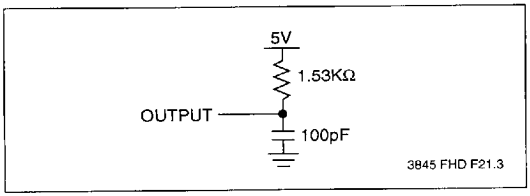
3845 PGM T08.1

NOTES: (1) Must perform a stop command after a read command prior to measurement

(2) V_{IL} min. and V_{IH} max. are for reference only and are not tested.

(3) This parameter is periodically sampled and not 100% tested.

EQUIVALENT A.C. LOAD CIRCUIT



3845 FHD F21.3

A.C. TEST CONDITIONS

Input Pulse Levels	V_{CC} x 0.1 to V_{CC} x 0.9
Input Rise and Fall Times	10ns
Input and Output Timing Level	V_{CC} x 0.5
Output Load	100pF

3843 PGM T09

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A.C. CHARACTERISTICS (Over recommended operating conditions, unless otherwise specified)

Read & Write Cycle Limits

Symbol	Parameter	Min.	Max.	Units
f_{SCL}	SCL Clock Frequency		1	MHz
TI	Noise Suppression Time Constant at SCL & SDA Inputs		20	ns
t_{DV}	SCL HIGH to SDA Data Valid		450	ns
t_{LOW}	CLock LOW Period	500		ns
t_{HIGH}	Clock HIGH Period	500		ns
t_{STAS1}	Start Condition Setup Time to Rising Edge of SCL	150		ns
t_{STAS2}	Start Condition Setup time to Falling Edge of SCL	150		ns
t_{STAH1}	Start Condition Hold Time to Rising Edge of SCL	50		ns
t_{STAH2}	Start Condition Hold Time to Falling Edge of SCL	50		ns
t_{STPS1}	Stop Condition Setup Time to Rising Edge of SCL	150		ns
t_{STPS2}	Stop Condition Setup time to Falling Edge of SCL	150		ns
t_{STPH1}	Stop Condition Hold Time to Rising Edge of SCL	50		ns
t_{STPH2}	Stop Condition Hold Time to Falling Edge of SCL	50		ns
$t_{HD:DAT}$	Data in Hold Time	10		ns
$t_{SU:DAT}$	Data in Setup Time	150		ns
t_{RSCL}(4)	SCL Rise Time		90	ns
t_{FSCL}(4)	SCL Fall Time		90	ns
t_{R}(4)	SDA, $\overline{CS}$, RST Rise Time		90	ns
t_{F}(4)	SDA, $\overline{CS}$, RST Fall Time		90	ns
t_{DH}	Data Out Hold Time	0		ns
t_{HZ1}	SCL LOW to High Impedance		150	ns
t_{LZ}	SCL HIGH to Output Active	0		ns
t_{VCCS}	V_{CC} to $\overline{CS}$ Setup Time	5		ms
$t_{SU:CS}$	$\overline{CS}$ Setup Time	200		ns
$t_{HD:CS}$	$\overline{CS}$ Hold Time	100		ns
t_{HZ2}	$\overline{CS}$ Deselect Time		150	ns
$t_{SU:SCL}$	SCL Setup Time to $\overline{CS}$ LOW after Power Up	200		ns
t_{RST}	RST HIGH Time	1500		ns
$t_{SU:RST}$	RST Setup Time	500		ns
$f_{SCL:RST}$	SCL Frequency During Response to Reset		1	MHz
$t_{LOW:RST}$	SCL LOW Time During Response to Reset	500		ns
$t_{HIGH:RST}$	SCL HIGH Time During Response to Reset	500		ns
t_{PD}	SCL LOW to SDA Valid During Response to Reset		450	ns
t_{NOL}	RST to SCL Non-Overlap	500		ns
t_{WC}	Nonvolatile Write Cycle		10	ms

NOTES: (4) This parameter is periodically sampled and not 100% tested.

3845 PGM T10.2

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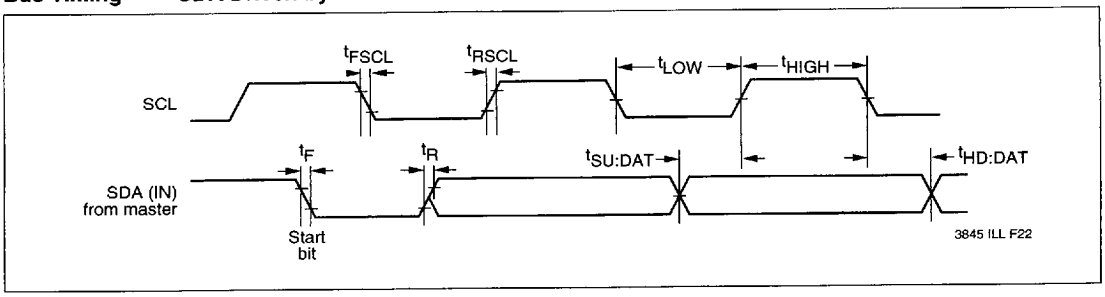
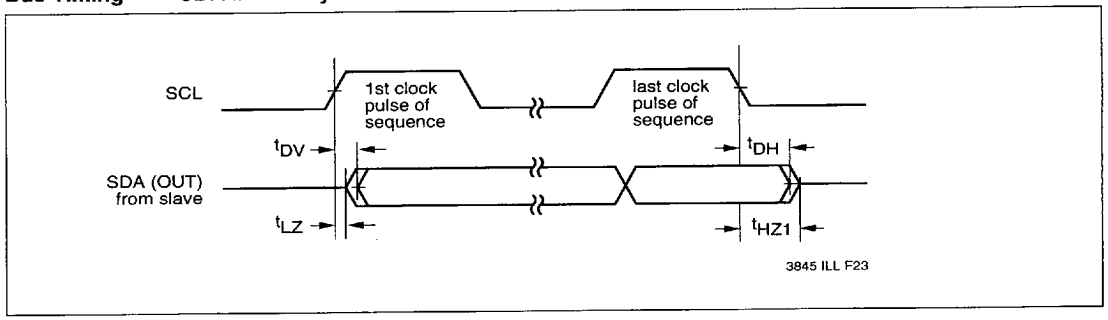
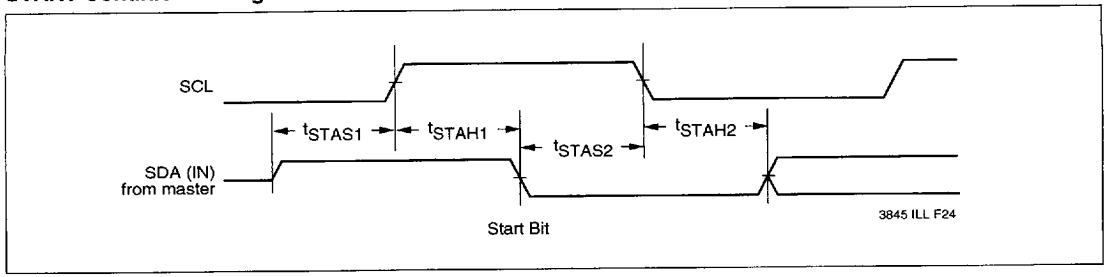
Bus Timing[1] — SDA Driven by the Bus Master



Bus Timing[2] — SDA Driven by the Slave



START Condition Timing



NOTES: (1) The master may issue a STOP condition at any given time in which it is driving the SDA line. In other words, when the part is sending ACK or data the master may NOT issue a STOP condition. The part will not respond to any such attempt which also causes bus contention. At any other time, a STOP condition will cause the part to reset and stop (enter a stand-by mode). Write operations will terminate prior to entering the stand-by mode.

(2) When the part drives the SDA line, it will tri-state the bus only after the last bit of the sequence. In other words, after the 8th bit of a byte that is read or after ACK between incoming bytes. In all other cases when the part drives the bus (between successive bits) it will continue to drive the bus also during the clock LOW periods.

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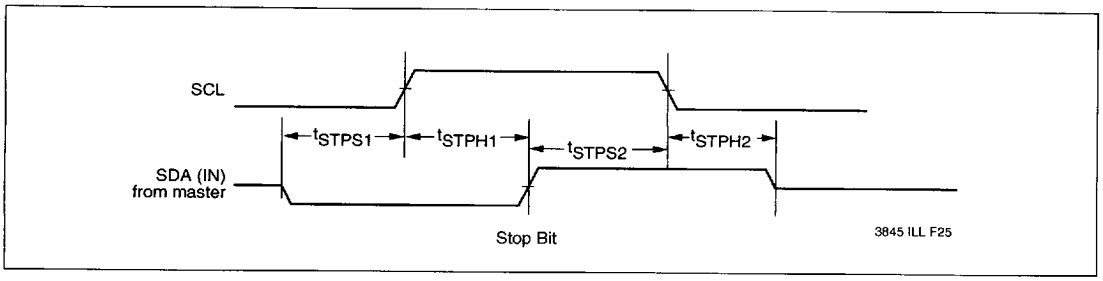
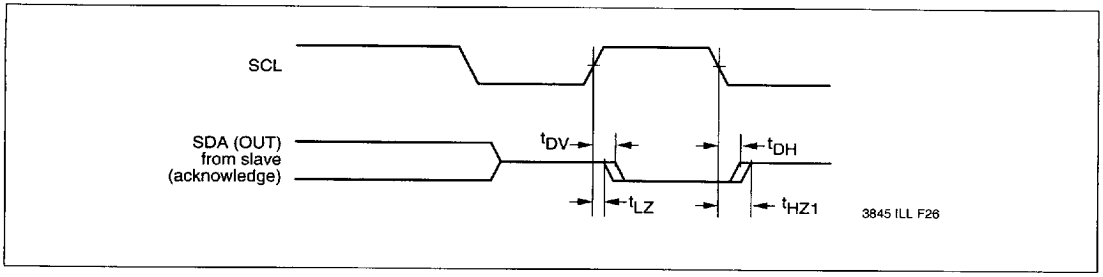
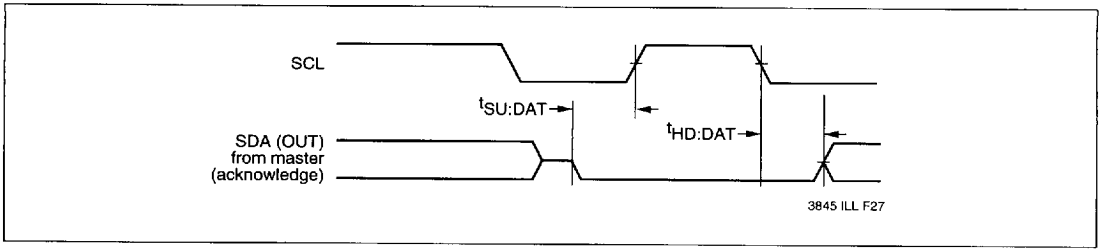
STOP Condition Timing



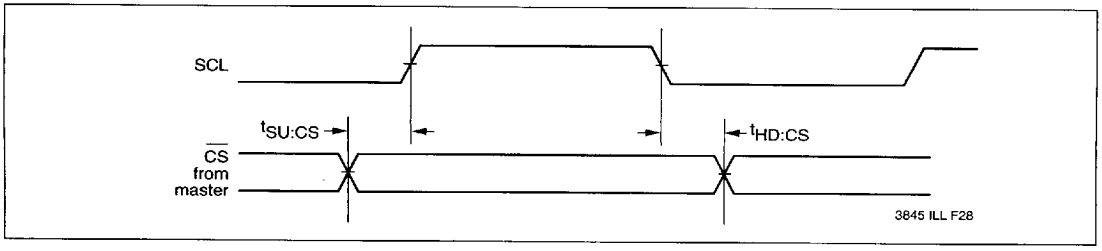
Acknowledge Response from Slave (Same Timing as Data Out)



Acknowledge Response from Master



$\overline{CS}$ Timing Diagram (Selecting/Deselecting the Part)



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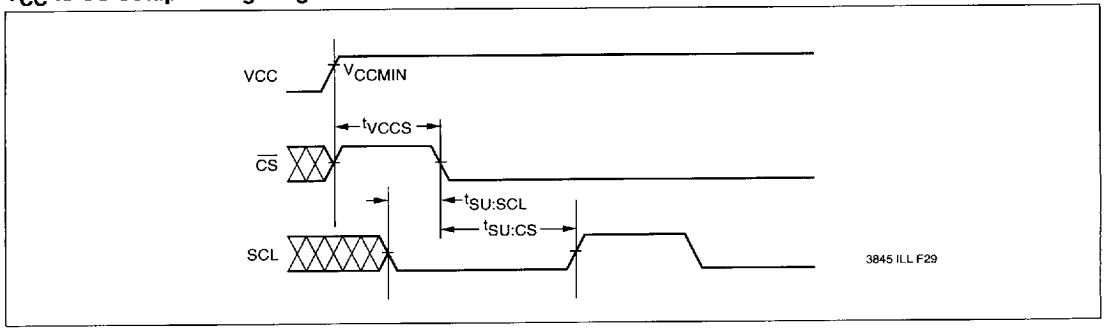
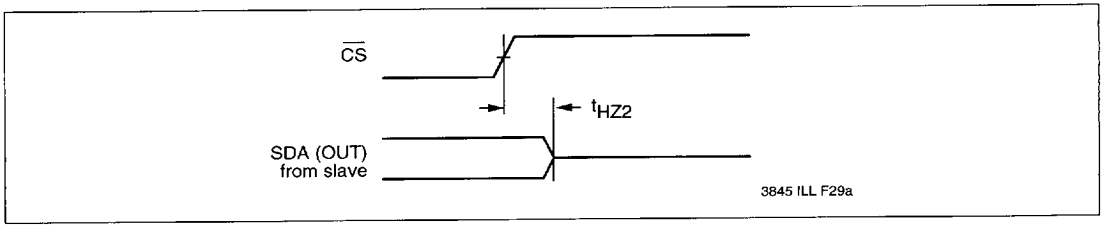
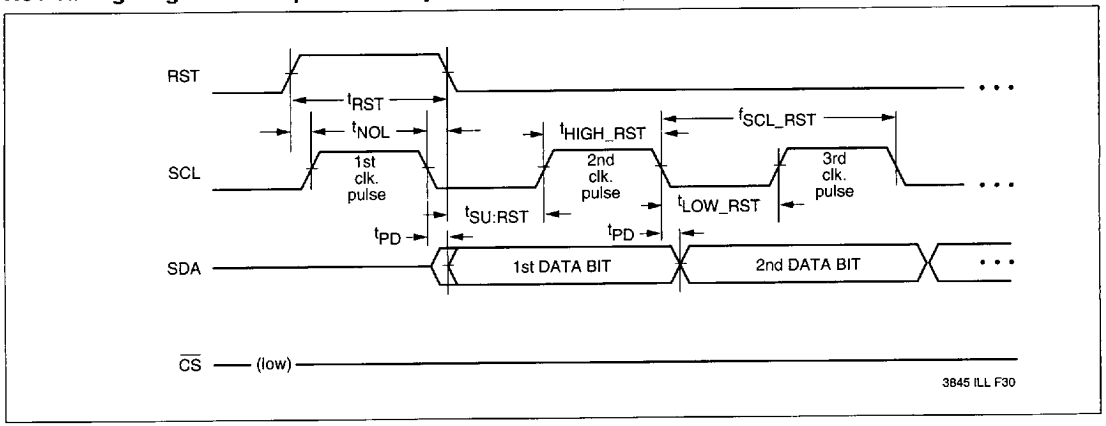
V_{CC} to $\overline{CS}$ Setup Timing Diagram



$\overline{CS}$ Deselect



RST Timing Diagram — Response to a Synchronous Reset (ISO)



NOTES: (1) The reset operation results in an answer from the part containing a header transmitted from the part to the master. The header has a fixed length of 32 bits and begins with two mandatory fields of eight bits : H1 and H2.

(2) The chronological order of transmission of the information bits shall correspond to bit identification b1 to b32 with the LEAST significant bit transmitted first.

(3) The current values are:

H1 : 19 h
H2 : 55 h
H3 : AA h
H4 : 55 h

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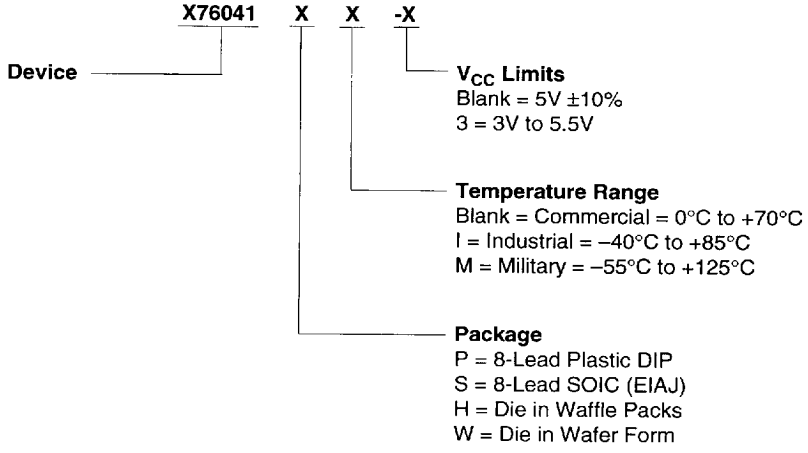
ORDERING INFORMATION



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