Product Specification

PE4263 DIE

SP6T UltraCMOS™ 2.6 V Switch 100 – 3000 MHz

Figure 1. Functional Diagram

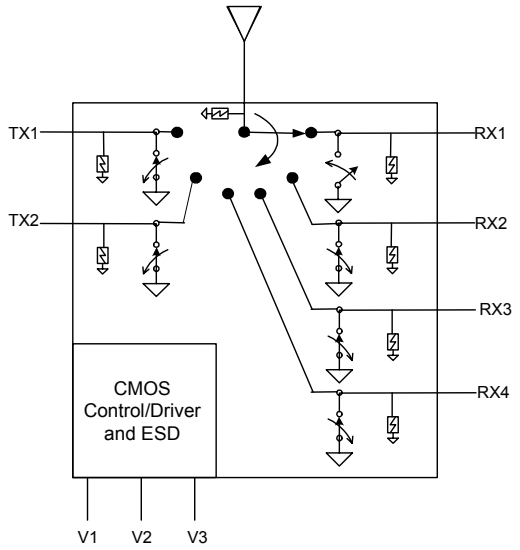
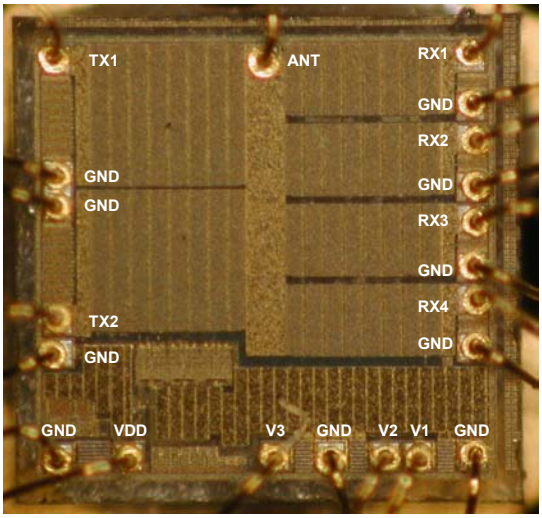


Figure 2. Die Top View



Features

- Three pin CMOS logic control with integral decoder/driver
- Low TX insertion loss: 0.55 dB at 900 MHz, 0.65 dB at 1900 MHz
- TX – RX Isolation of 48 dB at 900 MHz, 40 dB at 1900 MHz
- Low harmonics: $2f_o$ = -85 dBc and $3f_o$ = -72 dBc
- 1500 V HBM ESD tolerance all ports
- 41 dBm P1dB
- No blocking capacitors required

Product Description

The PE4263 SP6T RF UltraCMOS™ Switch addresses the specific design needs of the Quad-Band GSM Handset Antenna Switch Module Market. On-chip CMOS decode logic facilitates three-pin low voltage CMOS control. High ESD tolerance of 1500 V at all ports, no blocking capacitor requirements and on-chip SAW filter over-voltage protection devices make this the ultimate in integration and ruggedness.

The PE4263 UltraCMOS™ RF Switch is manufactured in Peregrine's patented Ultra Thin Silicon (UTSi®) CMOS process, offering the performance of GaAs with the economy and integration of conventional CMOS.

Table 1. Electrical Specifications @ +25 °C, V_{DD} = 2.6 V (Z_S = Z_L = 50 Ω)

Parameter	Conditions	Typical	Units
Operational Frequency			MHz
Insertion Loss	ANT - TX - 850 / 900 MHz	0.55	dB
	ANT - TX - 1800 / 1900 MHz	0.65	dB
	ANT - RX - 850 / 900 MHz	0.90	dB
	ANT - RX - 1800 / 1900 MHz	1.00	dB
Isolation	TX - RX - 850 / 900 MHz	48	dB
	TX - RX - 1800 / 1900 MHz	40	dB
	TX - TX - 850 / 900 MHz	29	dB
	TX - TX - 1800 / 1900 MHz	25	dB
	ANT - TX - 850 / 900 MHz	31	dB
	ANT - TX - 1800 / 1900 MHz	25	dB
Return Loss	850 / 900 MHz	22	dB
	1800 / 1900 MHz	23	
2nd Harmonic	35 dBm TX Input - 850 / 900 MHz	-85	dBc
	33 dBm TX Input - 1800 / 1900 MHz	-81	
3rd Harmonic	35 dBm TX Input - 850 / 900 MHz	-72	dBc
	33 dBm TX Input - 1800 / 1900 MHz	-66	
Switching Time	(10-90%) (90-10%) RF	2	µs

Table 2. Pin Descriptions

Pin No.	Pin Name	Description
1[2]	ANT	RF Common – Antenna
2[2]	TX1	RF I/O - TX1
3[1]	GND	Ground (Requires two bond wires)
4[2]	TX2	RF I/O – TX2
5[1]	GND	Ground
6[1]	GND	Ground
7	V_{DD}	Supply
8	V3	Switch control input, CMOS logic level
9[1]	GND	Ground
10	V2	Switch control input, CMOS logic level
11	V1	Switch control input, CMOS logic level
12[1]	GND	Ground
13[1]	GND	Ground
14[2]	RX4	RF I/O – RX4
15[1]	GND	Ground
16[2]	RX3	RF I/O – RX3
17[1]	GND	Ground
18[2]	RX2	RF I/O – RX2
19[1]	GND	Ground
20[2]	RX1	RF I/O – RX1

Notes: 1. Bond wires should be physically short and connected to ground plane for best performance.
2. Blocking capacitors needed only when non-zero DC voltage present.

Figure 3. Pin Configuration (Top View)

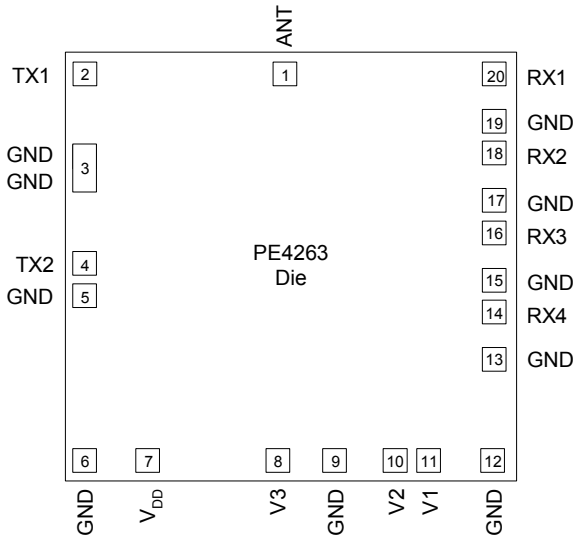


Table 3. Absolute Maximum Ratings

Symbol	Parameter/Conditions	Min	Max	Units
V_{DD}	Power supply voltage	-0.3	4.0	V
V_I	Voltage on any input	-0.3	V_{DD}+ 0.3	V
T_{ST}	Storage temperature range	-65	+150	°C
T_{OP}	Operating temperature range	-40	+85	°C
P_{IN}	TX input power (50 Ω)[1]		+38	dBm
	RX input power (50 Ω)[1]		+23	
V_{ESD}	ESD Voltage (HBM, MIL_STD 883 Method 3015.7)		1500	V
	ESD Voltage (MM, JEDEC, JESD22-A114-B)		100	V
	ESD Voltage (CDM, JEDEC, JESD22-C101-A)		2000	V
	ESD Voltage at ANT Port (IEC 61000-4-2)		1700	V

Note: 1. Max RF specified with V_{DD} applied

Absolute Maximum Ratings are those values listed in the above table. Exceeding these values may cause permanent device damage. Functional operation should be restricted to the limits in the DC Electrical Specifications table. Exposure to absolute maximum ratings for extended periods may affect device reliability.

Table 4. DC Electrical Specifications

Parameter	Min	Typ	Max	Units
V_{DD} Supply Voltage	2.4	2.6	2.8	V
I_{DD} Power Supply Current (V_{DD} = 2.6V)		13	20	µA
Control Voltage High	0.7 x V_{DD}			V
Control Voltage Low			0.3 x V_{DD}	V

Table 5. Truth Table

Path	V3	V2	V1
ANT – RX1	0	0	0
ANT – RX2	0	0	1
ANT – RX3	0	1	0
ANT – RX4	0	1	1
ANT - TX1	1	0	x
ANT - TX2	1	1	x

Electrostatic Discharge (ESD) Precautions

When handling this UltraCMOS™ device, observe the same precautions that you would use with other ESD-sensitive devices. Although this device contains circuitry to protect it from damage due to ESD, precautions should be taken to avoid exceeding the specified rating.

Latch-Up Avoidance

Unlike conventional CMOS devices, UltraCMOS™ devices are immune to latch-up.

Table 6. Ordering Information

Order Code	Die ID	Description	Package	Shipping Method
4263-92	C9797_3	PE4263-DIE-D	Film Frame	Wafer (Gross Die / Wafer Quantity)
4263-98	C9797_3	PE4263-DIE-400G	Waffle Pack	400 Dice / Waffle Pack
4263-10	C9797_3	PE4263-DIE-1H	Evaluation Kit	1/ box

Sales Offices

The Americas

Peregrine Semiconductor Corp.
9450 Carroll Park Drive
San Diego, CA 92121
Tel 858-731-9400
Fax 858-731-9499

Europe

Peregrine Semiconductor Europe
Commercial Products:
Bâtiment Maine
13-15 rue des Quatre Vents
F- 92380 Garches, France
Tel: +33-1-47-41-91-73
Fax : +33-1-47-41-91-73
Space and Defense Products:
180 Rue Jean de Guiramand
13852 Aix-En-Provence cedex 3, France
Tel: +33(0) 4 4239 3361
Fax: +33(0) 4 4239 7227

North Asia Pacific

Peregrine Semiconductor K.K.
5A-5, 5F Imperial Tower
1-1-1 Uchisaiwaicho, Chiyoda-ku
Tokyo 100-0011 Japan
Tel: +81-3-3502-5211
Fax: +81-3-3502-5213

South Asia Pacific

Peregrine Semiconductor
28G, Times Square,
No. 500 Zhangyang Road,
Shanghai, 200122, P.R. China
Tel: +86-21-5836-8276
Fax: +86-21-5836-7652

For a list of representatives in your area, please refer to our Web site at: ***www.psemi.com***

Data Sheet Identification

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Product Specification

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