



Am95C94

Advanced Burst Error Processor

DISTINCTIVE CHARACTERISTICS

- Implements Reed-Solomon code for the proposed X3B11 and ISO Continuous Servo standard.
- Supports:
 - 5-way and 10-way interleaving
 - 512-byte and 1024-byte sectors
 - Alternative sector sizes up to 2550 bytes
 - Layered CRC (optional)
- Performs fast correction vector computation, entirely in hardware; there is no need for external software to reduce syndromes to vectors.
- Parallel operation on two contiguous sectors; checkbytes for the second sector accumulate while correction vectors for first sector are computed. This allows "on-the-fly" correction.
- Data and EDAC interface is byte-wide parallel; operates at speeds up to 10 Mbytes per second.
- Microprocessor-compatible 8-bit data bus with optional parity.
- Correction vector generation performance with a 20 MHz system clock is such that up to 80 correction vectors can be generated in under 400 μ secs for a 1024 byte sector.

GENERAL DESCRIPTION

The Am95C94 Advanced Burst Error Processor (ABEP) performs error detection and correction in optical disk systems. The ABEP implements the proposed ANSI X3B11 Standard Continuous Composite Servo Reed-Solomon Error Detection and Correction (EDAC) algorithm. It interfaces directly with AMD's disk data controller for optical systems, the Am95C96 Optical Disk Data Controller (ODC).

The ABEP simultaneously performs syndrome generation for the sector being read, and correction vector generation for the previously read sector. This allows "on-the-fly" correction of data transferred from the disk at a high rate. This feature is extremely critical for optical disk systems, where read errors can be very frequent.

The ABEP works closely with the Am95C96 disk data controller. The ABEP resides on the buffer interface bus alongside the buffer memory. It functions as a slave peripheral on this bus, supporting high-speed disk data transfer operations. Parity can be generated and checked on this 8-bit bus.

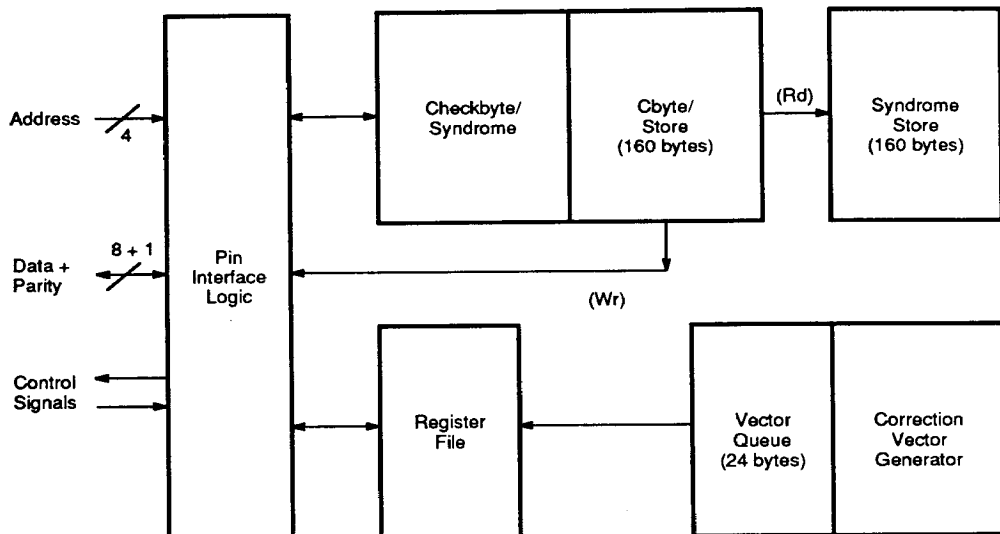
During a disk write operation, the data controller transfers a sector of data bytes from the buffer memory to the

disk and simultaneously to the ABEP. The ABEP generates checkbytes for this sector, and the data controller writes these checkbytes to the disk after the sector data.

During a disk read operation, the data controller transfers a sector of data bytes from the disk to the buffer memory and simultaneously to the ABEP. Using the checkbytes read from the disk, the ABEP determines whether there are any errors, and, if so, how to correct them. If correction is required, correction vector generation takes place while the data and checkbytes of the next sector are being read from the disk and written to the ABEP. The disk data controller performs any necessary corrections to data during disk sector transfers by using the correction vectors computed by the ABEP. This ensures that errors can be corrected "on the fly," allowing high-speed, zero-sector-interleave read operations.

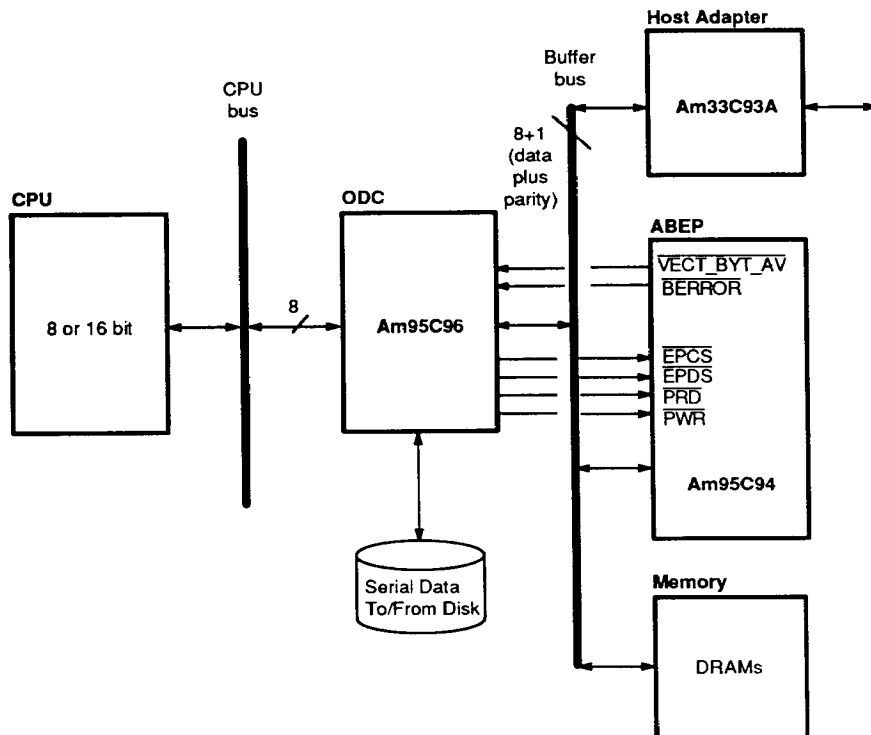
Unlike earlier error-processing chips, the Am95C94 ABEP may be treated as a black-box error processor; no software assistance is required for error checking or correction vector generation.

BLOCK DIAGRAM



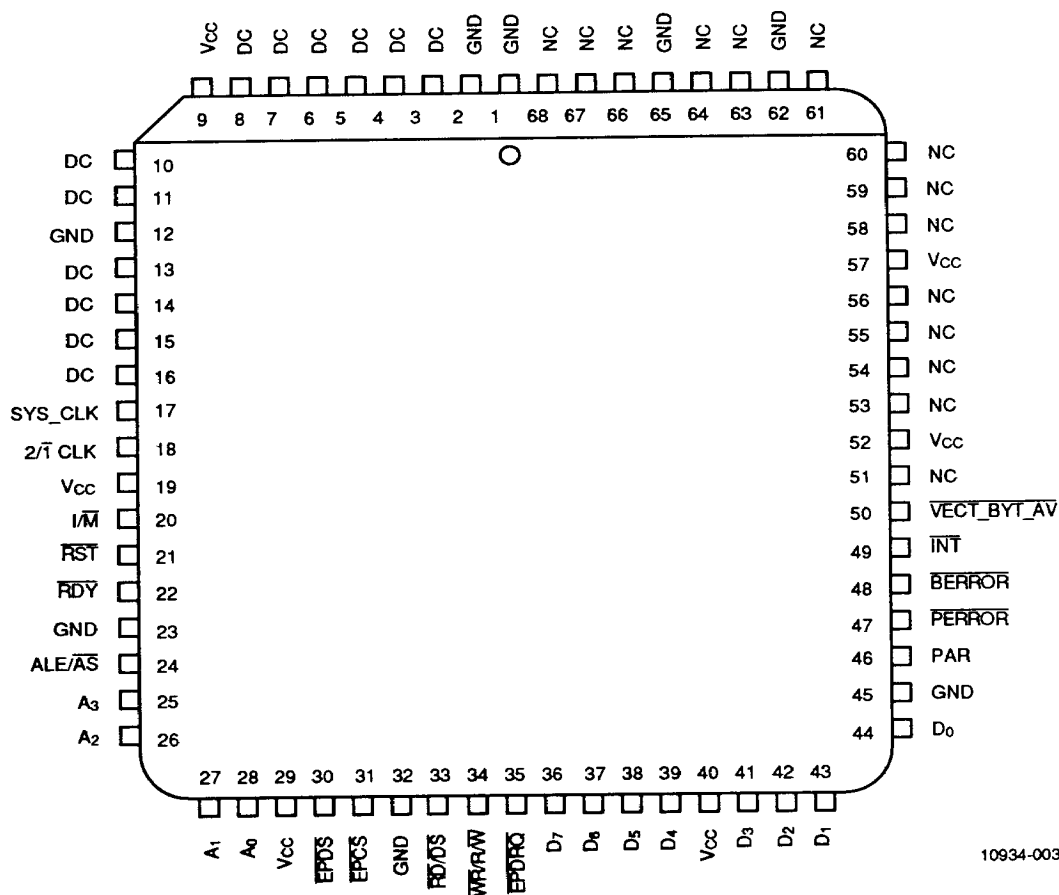
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SYSTEM DIAGRAM



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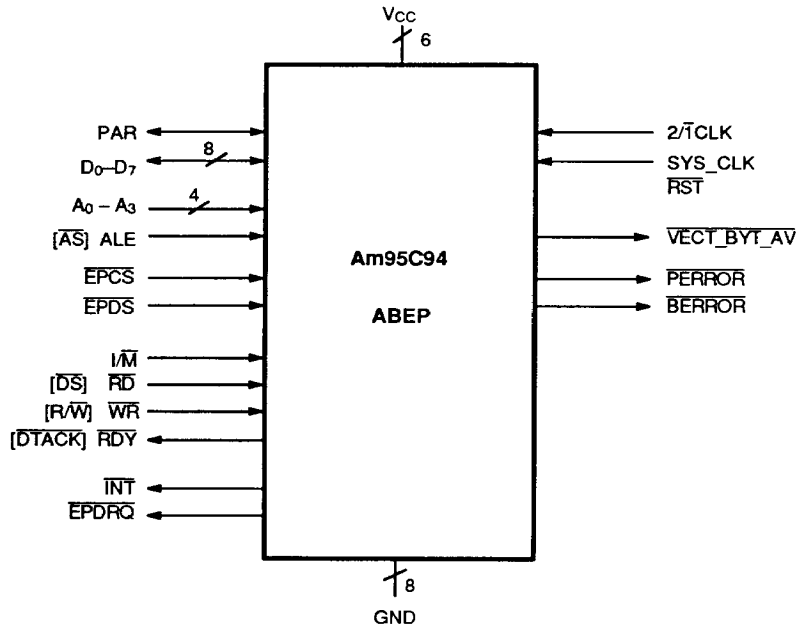
CONNECTION DIAGRAM



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Note: NC means No Connection to Die,
DC means Do Not Connect These Pins.

LOGIC SYMBOL



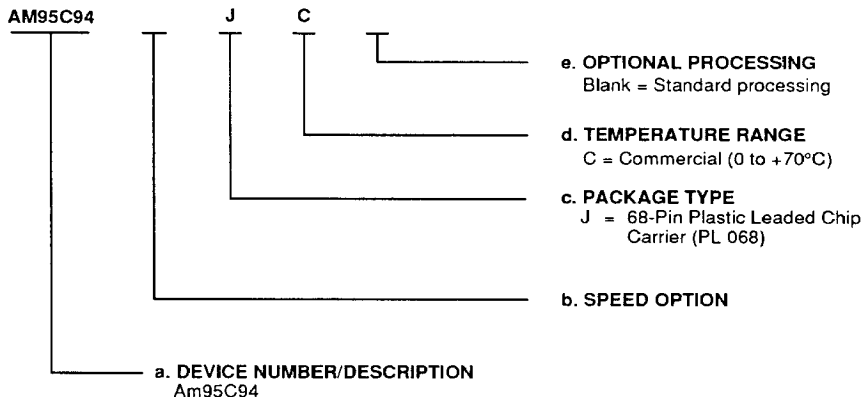
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ORDERING INFORMATION

Standard Products

AMD standard products are available in several packages and operating ranges. The ordering number (Valid Combination) is formed by a combination of:

- a. Device Number
- b. Speed Option (if applicable)
- c. Package Type
- d. Temperature Range
- e. Optional Processing



Valid Combinations	
AM95C94	JC

Valid Combinations

Valid Combinations list configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations, to check on newly released combinations, and to obtain additional data on AMD's standard military grade products.

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Advanced Micro Devices, Inc. 901 Thompson Place, P.O. Box 3453, Sunnyvale, CA 94088, USA
Tel: (408) 732-2400 • TWX: 910-339-9280 • TELEX: 34-6306 • TOLL FREE: (800) 538-8450
APPLICATIONS HOTLINE TOLL FREE: (800) 222-9323 • (408) 749-5703

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