T-46-13-27

Am9864

8192 x 8-Bit Electrically Erasable PROM

DISTINCTIVE CHARACTERISTICS

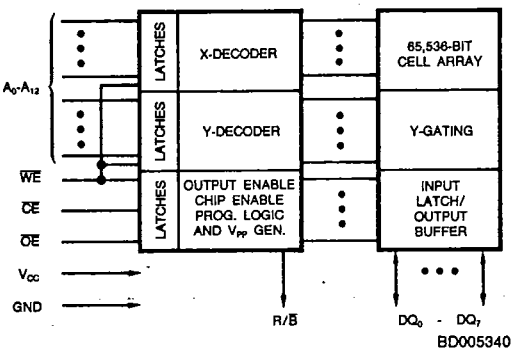
- 5 V only operation
- Self Timed Write Cycle with on chip latches
- Ready/$\overline{\text{Busy}}$ Pin for end of write indication
- Data Protection Features to prevent writes from occurring during V_{CC} power up/down
- Fast Read Access Time
  - Am9864-2/-20 : 200 ns
  - Am9864 /-25 : 250 ns
  - Am9864-30 : 300 ns
  - Am9864-3/-35 : 350 ns
- Minimum endurance of 10,000 write cycles per byte with a 10 year data retention (See 9864 Reliability Report Order #06891A for detailed information).

GENERAL DESCRIPTION

The Am9864 is a 65,536 bit Electrically Erasable Programmable Read Only Memory (EEPROM), organized as 8192 words by 8 bits per word. It operates from a single 5 volt supply and has a fully self timed write cycle with address, data and control lines latched during the write operation. The Am9864 is fabricated on AMD's highly manufacturable N-Channel Silicon gate process, and uses AMD's proprietary EEPROM technology to achieve the Electrically Alterable Nonvolatile Storage. This technology employs the industry accepted Fowler-Nordheim tunneling across a thin oxide.

The Am9864 provides on chip the logic necessary to interface with most microprocessors. The latched inputs and self timed write cycle free the microprocessor to perform other tasks during a write. A transparent automatic erase before write enhances system performance.

BLOCK DIAGRAM



BD005340

MODE SELECTION

Inputs			Outputs		Mode
$\overline{CE}$	$\overline{OE}$	$\overline{WE}$	R/$\overline{B}$	I/O	
L	L	H	H	Data Out	Read
L	H	⎍	⎍	Data In	Write
H	X	X	H	Hi Z	Standby
L	H	H	H	Hi Z	Read Inhibit
X	L	X	–	–	Write Inhibit

H = High
L = Low
X = Don't Care
⎍ = Pulse

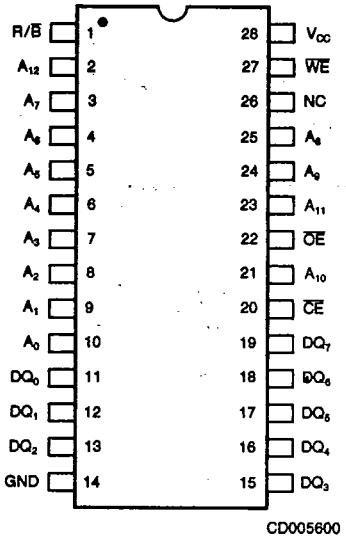
PRODUCT SELECTOR GUIDE

Part Number	Am9864-2	Am9864-20	Am9864	Am9864-25	Am9864-30	Am9864-3	Am9864-35
V_{CC} Supply tolerance	±5%	±10%	±5%	±10%	±10%	±5%	±10%
Access Time	200 ns		250 ns		300 ns	350 ns	
Chip Select Delay	200 ns		250 ns		300 ns	350 ns	
Output Enable Delay	75 ns		100 ns		120 ns	120 ns	

Publication # 05003 Rev. D Amendment /0
Issue Date: May 1986

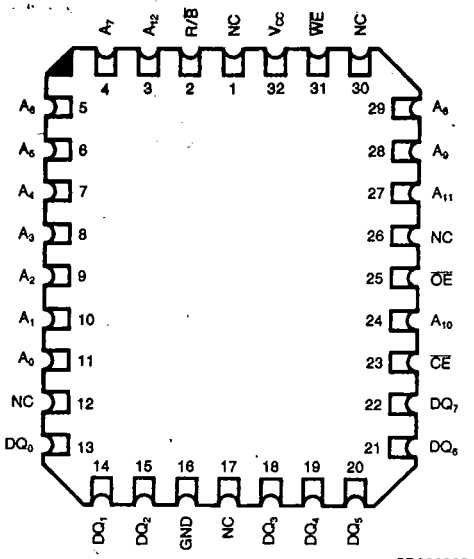
T-46-13-27

CONNECTION DIAGRAMS
Top View



CD005600

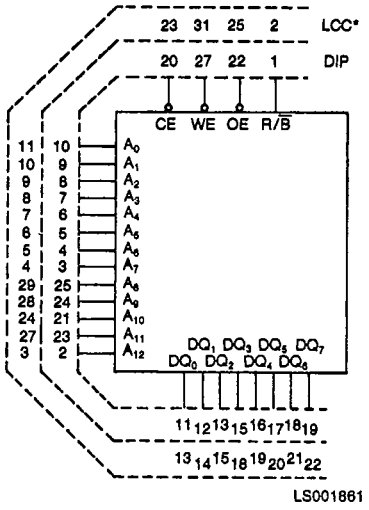
LCC*



CD006000

Note: Pin 1 is marked for orientation.

LOGIC SYMBOL



LS001861

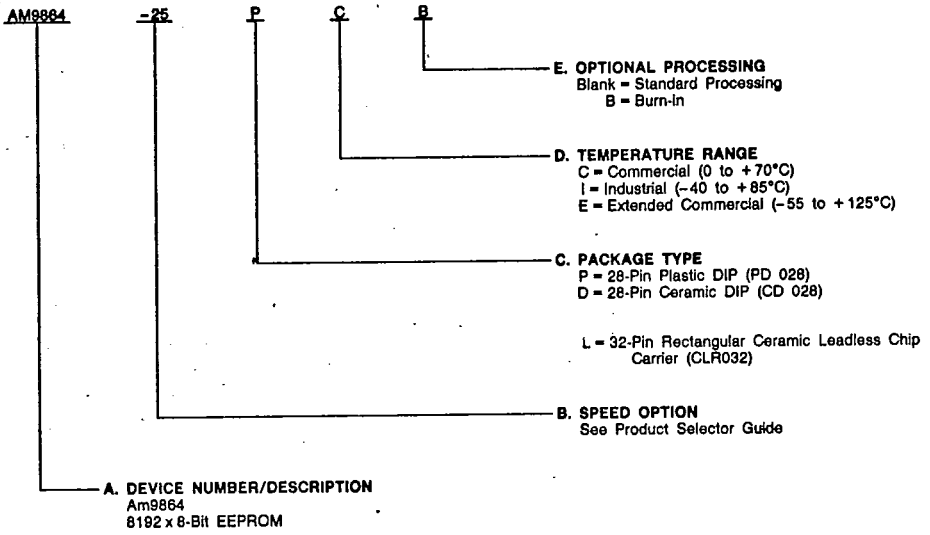
*Same pinouts apply to PLCC.

T-46-13-27

ORDERING INFORMATION

Standard Products

AMD standard products are available in several packages and operating ranges. The order number (Valid Combination) is formed by a combination of: **A. Device Number**
B. Speed Option (if applicable)
C. Package Type
D. Temperature Range
E. Optional Processing



Valid Combinations	
AM9864-2	PC, PCB, DC, DCB, DI, DIB, LI, LIB
AM9864-20	
AM9864	
AM9864-3	
AM9864-25	PC, PCB, DC, DCB, DI, DIB, DE, DEB, LC, LCB, LI, LIB, LE, LEB
AM9864-35	

Valid Combinations

Valid Combinations list configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations, to check on newly released combinations, and to obtain additional data on AMD's standard military grade products.

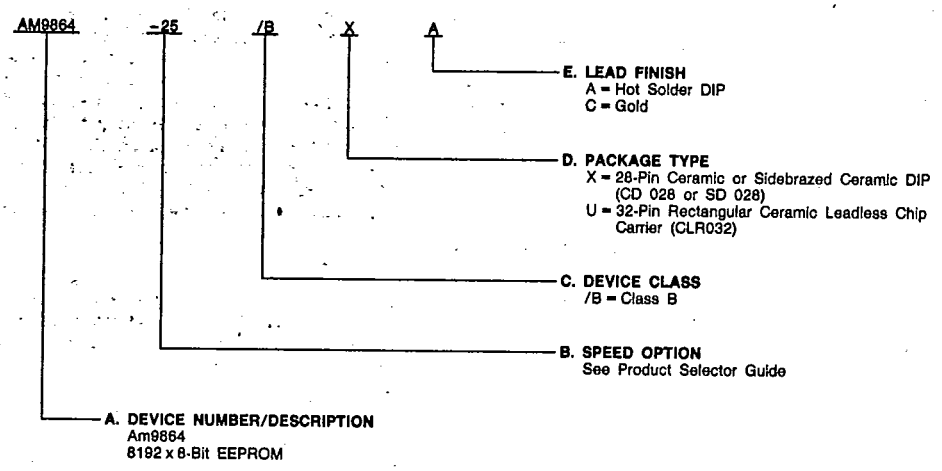
*To be announced.

T-46-13-27

ORDERING INFORMATION

APL Products

AMD products for Aerospace and Defense applications are available in several packages and operating ranges. APL (Approved Products List) products are fully compliant with MIL-STD-883C requirements. CPL (Controlled Products List) products are processed in accordance with MIL-STD-883C, but are inherently non-compliant because of package, solderability, or surface treatment exceptions to those specifications. The order number (Valid Combination) for APL products is formed by a combination of: **A. Device Number**
B. Speed Option (if applicable)
C. Device Class
D. Package Type
E. Lead Finish



Valid Combinations	
AM9864-25	/BXA, /BXC, /BUC
AM9864-30	
AM9864-35	

Valid Combinations

Valid Combinations list configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations or to check for newly released valid combinations.

5

FUNCTIONAL DESCRIPTION

Read Mode

The Am9864 has two control functions, both of which must be logically satisfied in order to obtain data at the outputs. Chip Enable ($\overline{CE}$) is the power control and should be used for device selection. Output Enable ($\overline{OE}$) is the output control and should be used to gate data to the output pins independent of device selection. Assuming that addresses are stable, address access time (t_{ACC}) is equal to the delay from $\overline{CE}$ to output (t_{CE}). Data is available at the outputs t_{OE} after the falling edge of $\overline{OE}$, assuming that $\overline{CE}$ has been low and addresses have been stable for at least t_{ACC}-t_{OE}.

Standby Mode

The Am9864 has a standby mode which reduces the active power dissipation by 60%, from 525 mW to 210 mW (V_{CC} ±5% values for 0 to 70°C). The Am9864 is placed in the standby mode by applying a TTL high signal to the $\overline{CE}$ input. When in the standby mode, the outputs are in a high-impedance state, independent of the $\overline{OE}$ input.

Data Protection

The Am9864 incorporates several features that prevent unwanted write cycles during V_{CC} power up and power down. These features protect the integrity of the stored data.

To avoid the initiation of a write cycle during V_{CC} power up and power down, a write cycle is locked out for V_{CC} less than 3.3 volts (typical 3.8 V). It is the users's responsibility to insure that the control levels are logically correct when V_{CC} is above 3.3 volts.

There is a $\overline{WE}$ lockout circuit that prevents WE pulses of less than 10 ns duration from initiating a write cycle.*

When the $\overline{OE}$ control is in logic zero condition, a write cycle cannot be initiated.

Write Mode

The Am9864 has a write cycle that is similar to that of a Static RAM. The write cycle is completely self timed, and initiated by a low going pulse on the $\overline{WE}$ pin. On the falling edge of $\overline{WE}$ the address information is latched. On the rising edge, the data and the control pins ($\overline{CE}$ and $\overline{OE}$) are latched. The Ready/$\overline{Busy}$ pin goes to a logic low level indicating that the Am9864 is in a write cycle which signals the microprocessor host that the system bus is free for other activity. When Ready/$\overline{Busy}$ goes back to a high the Am9864 has completed writing, and is ready to accept another cycle.

Output OR-Tieing

To accommodate multiple memory connections, a 2-line control function is provided to allow for:

1. Low memory power dissipation
2. Assurance that output bus contention will not occur.

It is recommended that $\overline{CE}$ be decoded and used as the primary device selecting function, while $\overline{OEW}$ be made a common connection to all devices in the array and connected to the READ line from the system control bus. This assures that all deselected memory devices are in their low-power standby mode and that the output pins are only active when data is desired from a particular memory device.

Ready/$\overline{Busy}$ Pin

T-46-13-27

The Ready/$\overline{Busy}$ is a totem-pole output. It can be tied to a system interrupt to allow a writing operation to be defined by one microprocessor cycle time. The state of this output is determined by the Am9864 and must not be externally forced. When not used this pin must be kept floating. This output cannot be or-tied.

APPLICATIONS

During the switch between active and standby conditions, transient current peaks are produced on the rising and falling edges of chip enable. The magnitude of these transient current peaks is dependent on the output capacitance loading of the device. A 0.1μF ceramic capacitor (high frequency, low inherent inductance) should be used on each device between V_{CC} and GND to minimize transient effects. In addition, to overcome the voltage drop caused by the inductive effects of the printed circuit board traces on EEPROM arrays, a 4.7μF bulk electrolytic capacitor should be used between V_{CC} and GND for each eight devices. The location of the capacitor should be close to where the power supply is connected to the array.

Endurance

Since endurance testing is a destructive test it is sampled and not 100% tested. To test for endurance, a sample of devices are written 10,000 times and checked for data retention capability.

There is one main failure mechanism associated with endurance failures in EEPROMs. This failure mechanism is due to charge trapping in the thin tunneling dielectric. At a point, when the amount of trapped charge creates an electric field that exceeds the dielectric breakdown of the oxide, the oxide becomes conductive, and reliable storage of charge on the floating gate is no longer possible. This results in the failure of a single bit to properly write and retain data.

There are three different failure rates associated with this failure mechanism, and the failure rates are a function of the number of write cycles. For less than a few hundred write cycles, the failure rate is relatively high. During AMD testing, each part is written hundreds of times to allow those cells that would be infant mortality failures to be screened out. For the next 10,000 write cycles the failure rate is low. It is in this region that AMD EEPROMs are operated. Somewhere above this region, typically well above 12,000 total write cycles, the failure rate again starts increasing.

The endurance failure rate is a function of the number of write cycles that the part has experienced. All parts that pass the AMD test screens will write a minimum of 10,000 times at every byte location with a maximum failure rate of 5%. In other words, 5% of a sample of devices will fail to write 10,000 times. Those devices that fail will have one single bit that fails to retain the correct data after being written. This failure rate is measured from a sample of devices, in the same manner that other reliability failure mechanisms are measured.

For more detailed information on how this data was obtained please refer to the Am9864 reliability report.

*This parameter is sampled and is not 100% tested.

ABSOLUTE MAXIMUM RATINGS

Storage Temperature ..... −65 to +150°C
Ambient Temperature with Power Applied ..... −65 to +135°C
Voltage on All Inputs with Respect to GND ..... +6.25 to −0.6 V

Stresses above those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to absolute maximum ratings for extended periods may affect device reliability.

OPERATING RANGES

Supply Voltage* (V_{CC} ±5%) ..... +4.75 to +5.25 V
Supply Voltage** (V_{CC} ±10%) ..... +4.5 to +5.5 V
*9864-2, 9864, 9864-3
**9864-20, 9864-25, 9864-35

Commercial (C) Device
Case Temperature ..... 0 to +70°C
Industrial (I) Device
Case Temperature ..... −40 to +85°C
Limited (L) Device
Case Temperature ..... −55 to +100°C
Extended Commercial (E) Device
Case Temperature ..... −55 to +125°C
Military (M) Device
Case Temperature ..... −55 to +125°C

Operating ranges define those limits between which the functionality of the device is guaranteed.

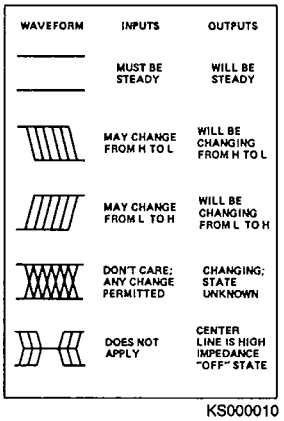
DC CHARACTERISTICS over operating range unless otherwise specified *

Parameter Symbol	Parameter Description	Test Conditions	Min.	Typ.	Max.	Units
I_{LI}	Input Leakage Current	V_{IN} = 0 to 5.5 V			10	µA
I_{LO}	Output Leakage Current	V_{OUT} = 0 to 5.5 V			10	µA
I_{CC1}	V_{CC} Current (Standby)	$\overline{CE}$ = V_{IH}, $\overline{OE}$ = V_{IL}			40	mA
I_{CC2}	V_{CC} Current (Active)	$\overline{OE}$ = $\overline{CE}$ = V_{IL}			100	mA
I_{CC}	V_{CC} Current (Write)	$\overline{WE}$ = ⎍, $\overline{CE}$ = V_{IL}, $\overline{OE}$ = V_{IH}			120	mA
V_{IL}	Input Low Voltage		−0.1		.8	Volts
V_{IH}	Input High Voltage		2.0		V_{CC}+1	Volts
V_{OL}	Output Low Voltage	I_{OL} = 2.1 mA			.45	Volts
V_{OH}	Output High Voltage	I_{OH} = −400 µA	2.4			Volts
C_{IN}	Input Capacitance (Notes 1, 2)	V_{IN} = 0 V		4	10	pF
C_{OUT}	Output Capacitance (Notes 1, 2)	$\overline{OE}$ = $\overline{CE}$ = V_{IH}, V_{OUT} = 0V		8	12	pF
V_{WI}	Write Inhibit Voltage		3.3	3.8		Volts
V_{RB}	R/$\overline{B}$ Output Low	I_{RB} = 2.1 mA			.45	Volts

Note 1. This parameter is sampled on a periodic basis and not 100% tested.
2. freq = 1 MHz @ 25°C.
3. Typical values are for nominal supply voltages.

*See the last page of this spec for Group A Subgroup Testing Information.

KEY TO SWITCHING WAVEFORMS



KS000010

5

SWITCHING CHARACTERISTICS over operating range unless otherwise specified* T-46-13-27

No.	Parameter Symbol	Parameter Description	Test Conditions		Am9864-2, -20 Min.	Am9864-2, -20 Max.	Am9864, -25 Min.	Am9864, -25 Max.	Am9864-30 Min.	Am9864-30 Max.	Am9864-3, -35 Min.	Am9864-3, -35 Max.	Units
READ													
1	t_{ACC}	Address to Output Delay	$\overline{WE} = V_{IH}$ Output Load: 1 TTL gate and C_L = 100 pF Input Rise and Fall Times: ≤20 ns Input Pulse Levels: 0.45 to 2.4 V Timing Measurement Reference Level Inputs: 0.8 V and 2 V Outputs: 0.8 V and 2 V	$\overline{CE} = \overline{OE} = V_{IL}$		200		250		300		350	ns
2	t_{CE}	$\overline{CE}$ to Output Delay		$\overline{OE} = V_{IL}$		200		250		300		350	ns
3	t_{OE}	Output Enable to Output Delay		$\overline{CE} = V_{IL}$		75		100		120		120	ns
4	t_{DF} (Note 1)	Output Enable High to Output Float		$\overline{CE} = V_{IL}$	0	60	0	60	0	60	0	60	ns
5	t_{OH} (Note 1)	Output Hold from Addresses, $\overline{CE}$ or $\overline{OE}$ Whichever Occurred First		$\overline{CE} = \overline{OE} = V_{IL}$	0		0		0		0		ns
WRITE													
6	t_{AS}	Address to Write Setup Time			20		20		20		60		ns
7	t_{CS}	$\overline{CE}$ to Write Setup Time			20		20		20		20		ns
8	t_{WP}	Write Pulse Width			100		100		100		150		ns
9	t_{AH}	Address Hold Time			80		80		80		100		ns
10	t_{DS}	Data Setup Time			50		50		50		70		ns
11	t_{DH}	Data Hold Time			20		20		20		20		ns
12	t_{CH}	$\overline{CE}$ Hold Time			50		50		50		50		ns
13	t_{OES}	$\overline{OE}$ Setup Time			20		20		20		20		ns
14	t_{OEH}	$\overline{OE}$ Hold Time			35		35		35		35		ns
15	t_{DB}	Time to Device Busy				100		100		100		100	ns
16	t_{WR}	Bytes Write Cycle				10		10		10		20	ms
17	t_{WPH}	Write Control Recovery			50		50		50		50		ns
18	t_{RE} (Note 4)	Write Recovery Time			0		0		0		0		ns
19	t_{RBO} (Notes 2, 4)	R/$\overline{B}$ to Output Time				50		50		50		50	ns
20	t_{WEH} (Note 4)	$\overline{WE}$ HIGH Recovery from R/$\overline{B}$			10		10		10		10		μs
	(Notes 1, 3)	Number of Writes per Byte			10		10		10		10		x1000

Notes: 1. This parameter is sampled on a periodic basis and is not 100% tested.
2. If $\overline{CE}$ and $\overline{OE} = V_{IL}$ when R/$\overline{B}$ is going to V_{OH}, then $DQ_0 - DQ_7$ becomes valid after $t_{RBO} + t_{ACC}$.
3. See 9864 reliability report.
4. This parameter is for information only. It is not tested or characterized.

*See the last page of this spec for Group A Subgroup Testing Information.

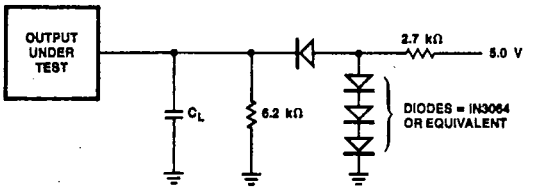
SWITCHING TEST CONDITIONS

Output load: 1 TTL gate and C_L = 100 pF
Input pulse levels: 0.45 V to 2.4 V

Timing Measurement Reference Levels

Input: 0.8 V and 2.0 V
Output: 0.8 V and 2.0 V

SWITCHING TEST CIRCUIT



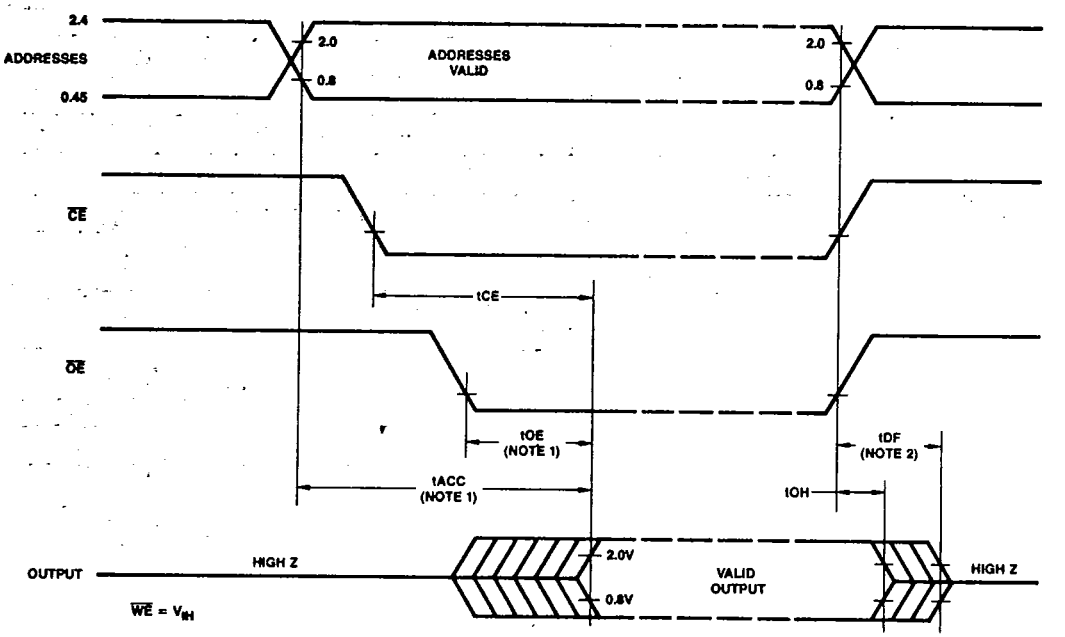
TC002491

C_L = 100pF, including jig capacitance.

SWITCHING WAVEFORMS

T-46-13-27

READ



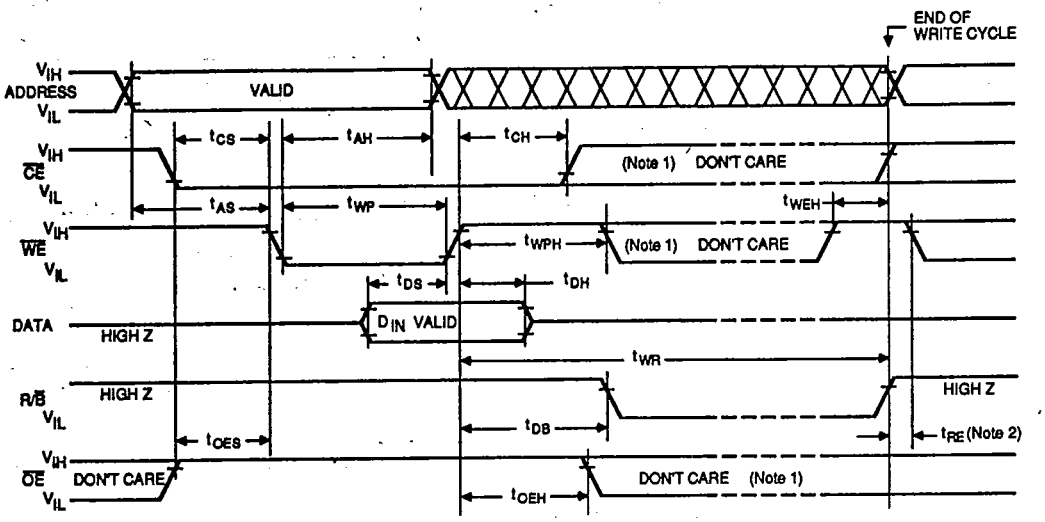
WF010280

Notes: 1. $\overline{OE}$ may be delayed up to t_{ACC}-t_{OE} after the falling edge of $\overline{CE}$ without impact on t_{ACC}.
2. t_{DF} is specified from $\overline{OE}$ or $\overline{CE}$, whichever occurs first.

5

T-46-13-27

WRITE



WF022260

Notes: 1. After t_{wph} and before the end of write cycle (R/$\overline{B}$ goes high), $\overline{WE}$, $\overline{CE}$ and $\overline{OE}$ are don't cares. However, in order to prevent an accidental write when R/$\overline{B}$ returns high, it is recommended that at least one of the following conditions are met after t_{wph}: $\overline{WE}$ high, $\overline{CE}$ high or an $\overline{OE}$ low.

2. After the write cycle is completed (R/$\overline{B}$ is high) the user must meet one of the following conditions to prevent an accidental write: $\overline{OE}$ low, $\overline{CE}$ high or $\overline{WE}$ high.

GROUP A SUBGROUP TESTING

T-46-13-27

DC CHARACTERISTICS

Parameter Symbol	Subgroups
I_{LI}	1, 2, 3
I_{LO}	1, 2, 3
I_{CC1}	1, 2, 3
I_{CC2}	1, 2, 3
I_{CC}	1, 2, 3
V_{IL}	1, 2, 3
V_{IH}	1, 2, 3
V_{OL}	1, 2, 3
V_{OH}	1, 2, 3
C_{IN}	4
C_{OUT}	4
V_{WI}	7, 8
V_{RB}	1, 2, 3

SWITCHING CHARACTERISTICS

No.	Parameter Symbol	Subgroups	No.	Parameter Symbol	Subgroups
1	t_{ACC}	9, 10, 11	9	t_{AH}	9, 10, 11
2	t_{CE}	9, 10, 11	10	t_{DS}	9, 10, 11
3	t_{OE}	9, 10, 11	11	t_{DH}	9, 10, 11
4	t_{DF}	9, 10, 11	12	t_{CH}	9, 10, 11
5	t_{OH}	9, 10, 11	13	t_{OES}	9, 10, 11
6	t_{AS}	9, 10, 11	14	t_{OEH}	9, 10, 11
7	t_{CS}	9, 10, 11	15	t_{DB}	9, 10, 11
8	t_{WP}	9, 10, 11	16	t_{WR}	9, 10, 11
			17	t_{wph}	9, 10, 11

5

MILITARY BURN-IN

Military burn-in is in accordance with the current revision of MIL-STD-883, Test Method 1015, Conditions A through E. Test conditions are selected at AMD's option.