Final | COM'L

AmPAL23S8-20/25

20-Pin PAL® Device-Based Sequencer

Advanced Micro Devices

DISTINCTIVE CHARACTERISTICS

- 14 Registers
  - 4 Output Logic Macrocells
  - 4 Output Registers
  - 6 Buried State Registers
- 23 possible array inputs and 8 outputs in a 20-pin package
- 33-MHz external/40-MHz internal cycle time
- Variable product term (PT) distribution for increased design flexibility
- Asynchronous and synchronous outputs supported for both Mealy- and Moore-type state-machine implementations
- Individually user-programmable Output Enable (OE) PTs with polarity control
- PTs for observing the buried registers on 6 of the output pins
- Separate PTs for common Synchronous PRESET and common Asynchronous RESET of all registers
- PRELOAD available on all registers for added test capability
- 99.9% post programming functional yield (PPFY)
- Platinum-Silicide fuse technology produces the most reliable bipolar programmable devices available today

GENERAL DESCRIPTION

The AmPAL23S8 is the first programmable array logic (PAL)-based sequencer device. It utilizes the familiar sum-of-products (AND-OR) logic structure, allowing users to customize logic functions by programming the device for specific applications. The AmPAL23S8 combines the ease of use of the familiar 20-pin PAL devices with the advanced "macrocell" concept introduced in the AmPAL22V10, as well as six Buried State Registers (BSRs).

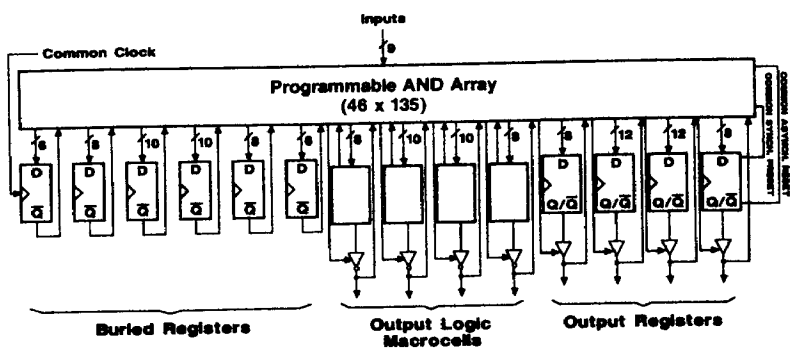
The AmPAL23S8 provides up to twenty-three array inputs and eight outputs. Four of the outputs are Output Logic Macrocells (OLMs) capable of being individually programmed as "combinatorial" or "registered," with active-HIGH or active-LOW polarity on each output. The other four are "registered" outputs, also capable of being programmed for active- HIGH or LOW polarity. All the flexibility on the outputs result in the simplification of logic design. The need to perform "DeMorgan's Law" on equations to have them fit into a PAL device is now a thing of the past. Each of the eight output registers can also be used dynamically as an input or output for greater design flexibility.

The AmPAL23S8 also offers designers increased flexibility and control over Output Enable (OE) functions. Each output is logically controlled by an OE product term (PT), with programmable OE polarity control. This allows the designer to use more complex control than previously available.

The six BSRs provide designers with enhanced logic power for sequencer applications. These registers are not only available to the system designer for use in sequencer applications (without the expense of a valuable I/O pin), but they may also be observed on the output pins during test. The observability of these registers on a programmable-logic sequencer adds to the list of features which make this device unique, simple to design with, and simple to debug.

System operation has been enhanced by the addition of Synchronous PRESET and Asynchronous RESET PTs. The AmPAL23S8 also incorporates the unique capability of PRELOADing the eight output registers and the BSRs to any desired state during testing. This is essential to permit full logical verification during test.

BLOCK DIAGRAM

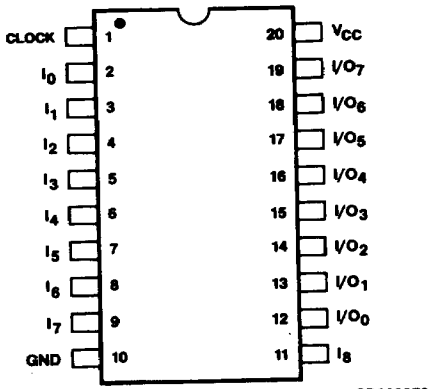


PAL is a registered trademark of Advanced Micro Devices.
This part is covered by various U.S. and foreign patents owned by Advanced Micro Devices.

Publication # 08207 Rev. E Amendment /0
Issue Date: January 1990

CONNECTION DIAGRAM
Top View

DIP



CD009870

Note: Pin 1 is marked for orientation.

Pin Description

V_{CC} = Supply Voltage

GND = Ground

CLOCK = Clock Pin

$I_0 - I_8$ = Dedicated Input Pins (9)

$I/O_0 - I/O_7$ = Bidirectional I/O Pins (8)

2

ORDERING INFORMATION
Standard Products

AMD standard products are available in several packages and operating ranges. The order number (Valid Combination) is formed by a combination of:

A. Device Number
B. Speed
C. Package Type
D. Operating Conditions
E. Optional Processing

AMPAL23S8 –20 P C

E. OPTIONAL PROCESSING
Blank = Standard processing

D. OPERATING CONDITIONS
C = Commercial (0 to + 75° C)

C. PACKAGE TYPE
P = 20-Pin Plastic DIP (PD 020)
D = 20-Pin Ceramic DIP (CD 020)

B. SPEED
–20 = 20 ns
–25 = 25 ns

A. DEVICE NUMBER/DESCRIPTION
AmPAL23S8
20-Pin IMOX PAL-Based Sequencer

Valid Combinations	
AMPAL23S8-20	PC, DC
AMPAL23S8-25	PC, DC

Valid Combinations list configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations and to check on newly released combinations.

Note: Marked with AMD logo.

FUNCTIONAL DESCRIPTION

The AmPAL23S8 is an advanced bipolar programmable array logic (PAL)-based sequencer. It contains a programmable array organized in the familiar sum-of-products structure. The structure of this device makes it particularly ideal for state machine applications. Any design which employs the use of complex state functions is a prime candidate for the AmPAL23S8.

The block diagram on the first page shows the basic architecture of this device; a maximum of 23 array inputs and 8 outputs are available. The inputs are connected to a programmable AND array containing 135 product terms (PTs), of which 124 are logical PTs and 11 are control PTs. Before programming, the AND gates are connected to both the true and complement of every input. By selectively programming fuses, the AND gates may be connected to only the true input, the complement input, or to neither type of input, establishing a logical "don't care". When both the true and complement fuses are left intact, a logical FALSE results on the output of the AND gate. An AND gate with all fuses blown will assume the logical TRUE state. The outputs of the AND gates are connected to OR gates.

Variable Product Term (PT) Distribution

The number of AND gates assigned to each OR gate varies in a fixed manner for each output as shown in the logic diagram (Figure 5). The OR gate outputs feed dedicated registers and macrocells. Each OR gate averages approximately ten PTs for output registers and macrocells. This gives the capability of using from eight to twelve logical PTs on one output in a single clock cycle (no feedback necessary). Buried state registers (BSRs) have an average of eight PTs per OR gate, providing the capability of using from six to ten logical PTs in one BSR in a single clock cycle.

Variable Output Architecture: Output Logic Macrocells (OLMs)

An innovation in logic design is the implementation on the AmPAL23S8 of variable output architecture on four of the outputs. These Output Logic Macrocells (OLMs) are user programmable for a great deal of design flexibility. Each of the four OLMs can be independently programmed for eight distinct configurations. The outputs can be either "registered" or "combinatorial;" they can also be individually programmed for active-HIGH or active-LOW polarity. Finally, the feedback paths which feed through the multiplexer back to the AND array can be programmed so that they originate either from the register or from the I/O pin. From the feedback multiplexer both the true and complement of the output going back to the array are available. All possible configurations of the OLMs are illustrated in Figures 4-1 through 4-8. For maximum flexibility, selection of output polarity and feedback path are kept independent of each other.

Output Registers

In addition to the four OLMs on the AmPAL23S8, there are also four output registers. The data on the output registers may be fed back to the array. When the output is disabled, the pin may be used as an external input. Since each of the eight outputs can obtain feedback from the pins associated with them, all eight of them provide the advantage of being usable dynamically as either inputs or outputs, significantly increasing design flexibility and possibilities.

Buried State Registers (BSRs)

The six observable Buried State Registers are one of the key features of the AmPAL23S8. All BSR outputs are fed back to the AND array, but they do not use up an output pin. The state of each BSR is, however, observable on an associated output pin by activating the user-programmable Observability product term as well as the appropriate Output Enable product term.

The extensive user-programmable flexibility enhances the usefulness of this device for different types of state machine implementations. The possibility exists to create both the Mealy and Moore type of design in the same device.

Programmable Output Polarity

Each output has a user-programmable output polarity fuse which, when blown, indicates that the output will be active HIGH, and when intact, active LOW. The obvious benefit of this enhancement is the increased flexibility of design. With the choice of output polarity, there is no need to DeMorganize equations to fit the device, allowing for more efficient designs both in terms of the amount of time spent in design as well as effective utilization of the device.

For further enhancement of the increased logic power of the AmPAL23S8, each output has a PT to control Output Enable (OE) with programmable polarity.

PRESET/RESET

To improve functionality at the system level, the AmPAL23S8 has additional RESET and PRESET PTs. One PT controls Output Register and BSR PRESET, and one PT controls the RESET for these registers. When the Synchronous PRESET PT is asserted (HIGH), all registers are loaded with a HIGH on the next LOW-to-HIGH clock transition. When the Asynchronous RESET PT is asserted, all registers are immediately loaded with a LOW, independent of the clock. These functions are particularly useful for applications such as system power-up and RESET.

PRELOAD

In order to simplify testing, the AmPAL23S8 is designed with PRELOAD circuitry that provides an easy method for testing logical functionality. PRELOAD allows any arbitrary "present state" values to be loaded into the OLMs, BSRs and Output Registers of this device. OLM Registers and BSRs are PRELOADed in separate cycles, allowing them to be PRELOADed with different values. Logic verification sequences can be significantly shortened, and all possible state sequences tested, reducing test time and development costs, and guaranteeing proper functionality in system.

A typical functional test sequence would be to verify all possible state transitions for the device being tested. To verify these transitions requires the ability to set the state registers to an arbitrary "present state" value and to set the device inputs to any arbitrary "present input" value. Once this is done, the state machine is then clocked into a new state, or "next state," which can be checked to validate the transition from the "present state." In this way, any state transition can be checked.

It is obvious that to attempt the debugging of a design using BSRs without the benefit of PRELOAD capability would be quite difficult. The combination of this feature and the BSRs

being observable is virtually indispensible for efficient and trouble-free state machine design.

Observability

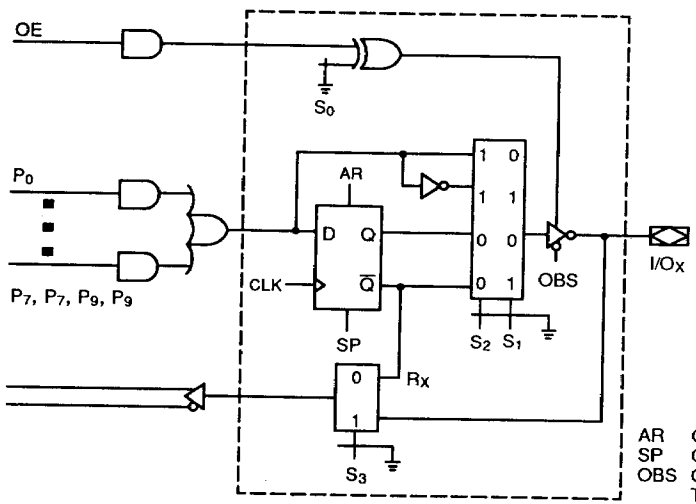
This extra ease of debugging the design comes from the use of the Observability (OBS) PT. The outputs must first be enabled according to the programmed pattern. When the OBS PT is selected, it disables all the Output Registers and Macrocell buffers, and enables the BSR buffers onto the output pins 13 through 18. When the OBS PT is not selected, the Output Registers and Macrocell buffers are enabled and the BSR buffers are disabled. When all the fuses for this PT are intact, (i.e., OBS is not selected), the data from the BSRs will not be visible on the output pins, and the Output Registers and OLMs will be enabled.

Processing and Fuse Technology

The AmPAL23S8 is manufactured using Advanced Micro Devices' IMOX oxide isolation process. This advanced process permits an increase in density and a decrease in internal capacitance resulting in the fastest possible programmable logic devices.

The AmPAL23S8 is fabricated with AMD's fast programming, highly reliable Platinum-Silicide fuse technology. Utilizing an easily implemented programming algorithm, these products can be rapidly programmed to any customized pattern. Extra test words are preprogrammed during manufacturing to ensure extremely high field programming yields (> 98%), and provide extra test paths to achieve excellent parametric correlation.

Platinum-Silicide was selected as the fuse link material to achieve a well controlled melt rate resulting in large, nonconductive gaps that ensure very stable, long term reliability. Extensive operating testing has proven that this low-field, large-gap technology offers high reliability for fusible link programmable logic.



AR Common Asynch Reset
SP Common Synch Preset
OBS Common Observability Term

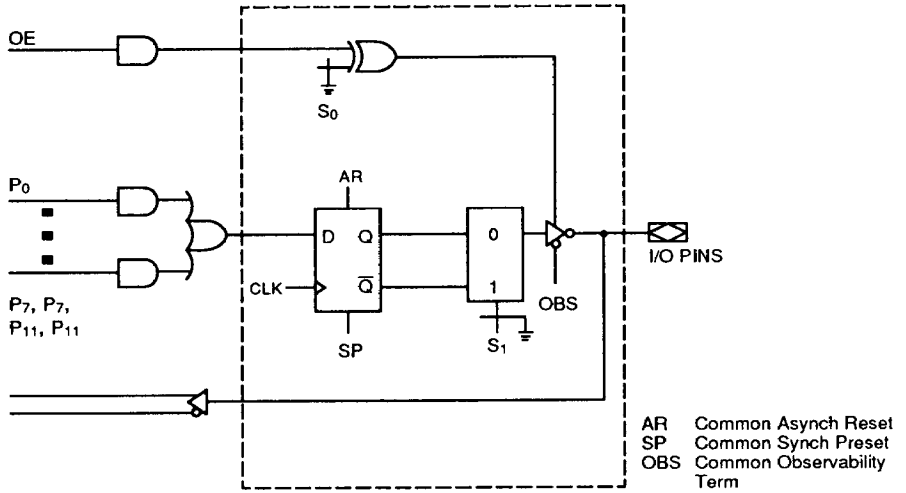
S0	OUTPUT ENABLE POLARITY
0	ENABLED HIGH
1	ENABLED LOW

08207-001A

S1	S2	S3	OUTPUT CONFIGURATION
0	0	0	ACTIVE LOW/REG/REG FEEDBACK
0	0	1	ACTIVE LOW/REG/IO FEEDBACK
0	1	0	ACTIVE LOW/COMB/REG FEEDBACK
0	1	1	ACTIVE LOW/COMB/IO FEEDBACK
1	0	0	ACTIVE HIGH/REG/REG FEEDBACK
1	0	1	ACTIVE HIGH/REG/IO FEEDBACK
1	1	0	ACTIVE HIGH/COMB/REG FEEDBACK
1	1	1	ACTIVE HIGH/COMB/IO FEEDBACK

0 = INTACT FUSE
1 = PROGRAMMED FUSE

Figure 1. Output Logic Macrocell (OLM)

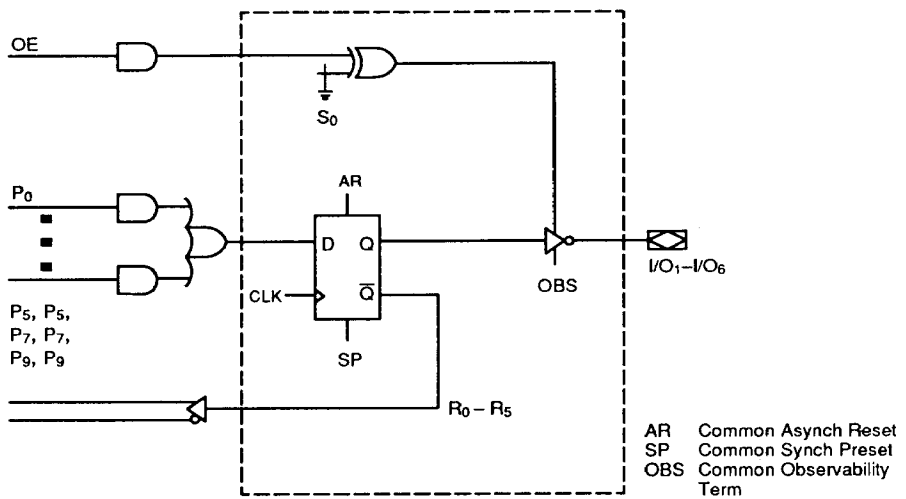


S0	OUTPUT ENABLE POLARITY
0	ENABLED HIGH
1	ENABLED LOW

S1	OUTPUT CONFIGURATION
0	ACTIVE LOW
1	ACTIVE HIGH

0 = INTACT FUSE
1 = PROGRAMMED FUSE

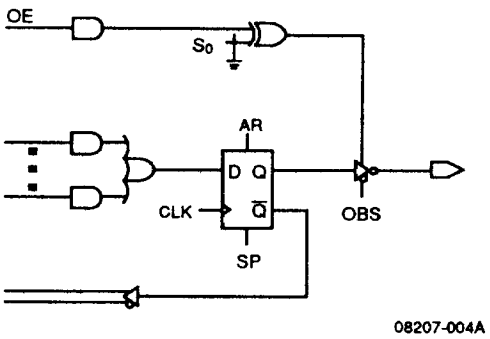
Figure 2. Output Register With Polarity



S0	OUTPUT ENABLE POLARITY
0	ENABLED HIGH
1	ENABLED LOW

0 = INTACT FUSE
1 = PROGRAMMED FUSE

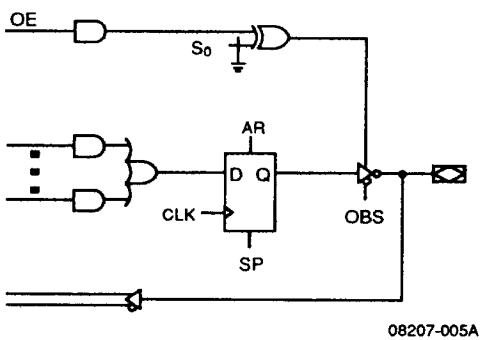
Figure 3. Buried State Register (BSR)



Output
Active Low $S_1 = 0$
Registered $S_2 = 0$

Feedback
Registered $S_3 = 0$

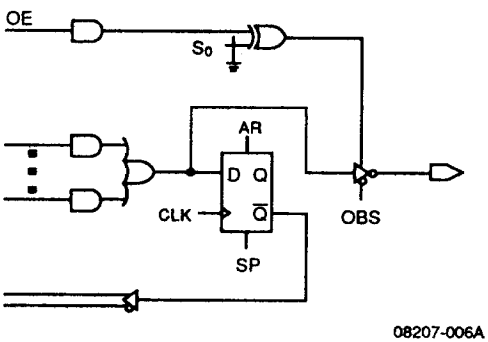
4-1



Output
Active Low $S_1 = 0$
Registered $S_2 = 0$

Feedback
I/O Pin $S_3 = 1$

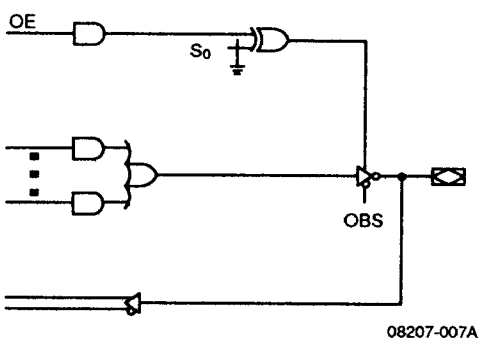
4-2



Output
Active Low $S_1 = 0$
Combinatorial $S_2 = 1$

Feedback
Registered $S_3 = 0$

4-3

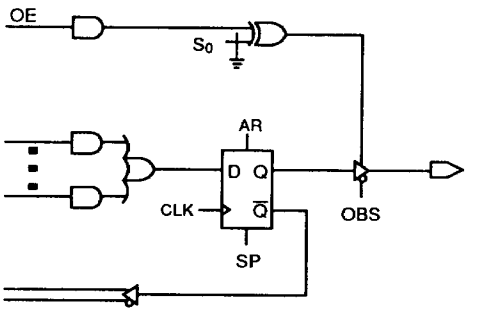


Output
Active Low $S_1 = 0$
Combinatorial $S_2 = 1$

Feedback
I/O Pin $S_3 = 1$

4-4

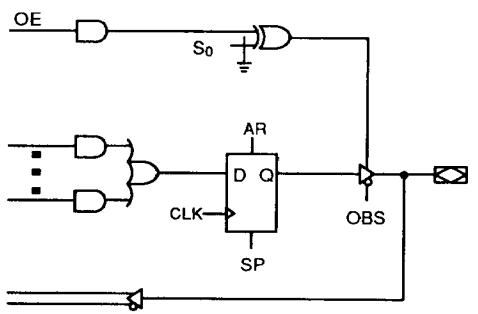
Figure 4. Possible Configurations of the Output Logic Macrocells (OLMs)



Output
Active High $S_1 = 1$
Registered $S_2 = 0$

Feedback
Registered $S_3 = 0$

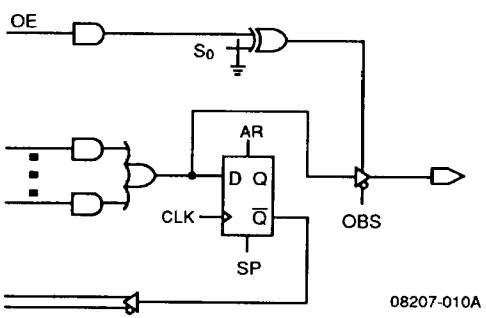
4-5



Output
Active High $S_1 = 1$
Registered $S_2 = 0$

Feedback
I/O Pin $S_3 = 1$

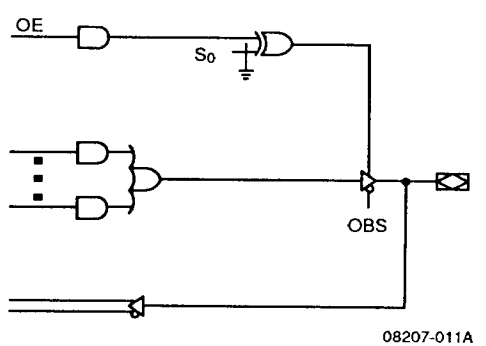
4-6



Output
Active High $S_1 = 1$
Combinatorial $S_2 = 1$

Feedback
Registered $S_3 = 0$

4-7



Output
Active High $S_1 = 1$
Combinatorial $S_2 = 1$

Feedback
I/O Pin $S_3 = 1$

4-8

Figure 4. Possible Configurations of the Output Logic Macrocells (OLMs) (Continued)

LOGIC DIAGRAM
AmPAL23S8

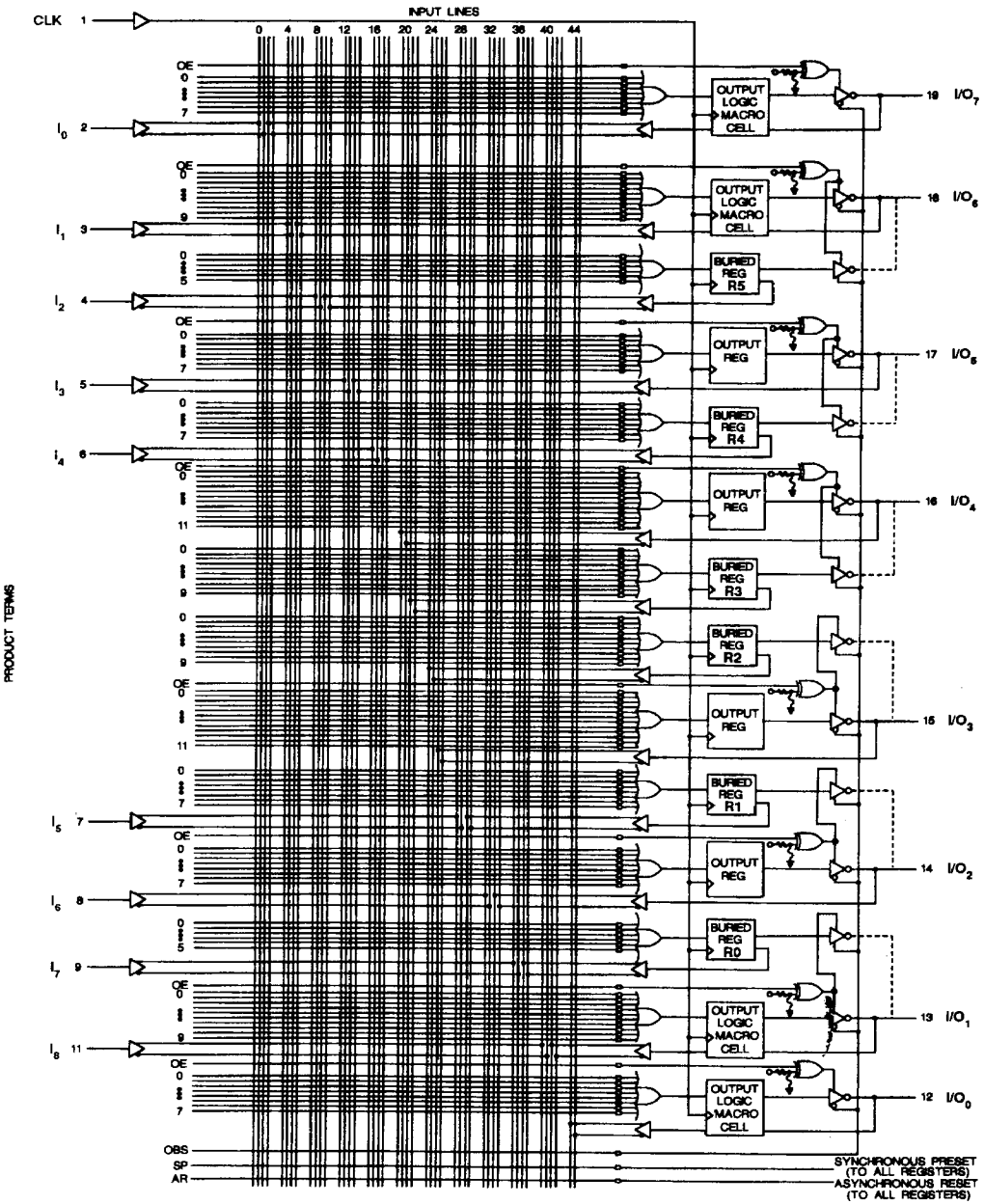


Figure 5.

LD000282

ABSOLUTE MAXIMUM RATINGS

Storage Temperature	–65°C to +150°C
Ambient Temperature with Power Applied	–55°C to +125°C
Supply Voltage with Respect to Ground	–0.5 V to +7.0 V
DC Input Voltage	–0.5 V to +5.5 V
DC Output or I/O Pin Voltage	–0.5 V to V_{CC} Max.
DC Input Current	–30 mA to +5 mA

Stresses above those listed under Absolute Maximum Ratings may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to Absolute Maximum Ratings for extended periods may affect device reliability. Programming conditions may differ.

OPERATING RANGES

Commercial (C) Devices

Ambient Temperature (T_A) Operating in Free Air	0°C to +75°C
Supply Voltage (V_{CC}) with Respect to Ground	+4.75 V to +5.25 V

Operating ranges define those limits between which the functionality of the device is guaranteed.

DC CHARACTERISTICS over COMMERCIAL operating ranges unless otherwise specified

Parameter Symbol	Parameter Description	Test Conditions	Min.	Max.	Unit
V_{OH}	Output HIGH Voltage	I_{OH} = –3.2 mA V_{IN} = V_{IH} or V_{IL}, V_{CC} = Min.	2.4		V
V_{OL}	Output LOW Voltage	I_{OL} = 16 mA V_{IN} = V_{IH} or V_{IL}, V_{CC} = Min.		0.5	V
V_{IH}	Input HIGH Voltage	Guaranteed Input Logical HIGH Voltage for all Inputs (Note 1)	2.0		V
V_{IL}	Input LOW Voltage	Guaranteed Input Logical LOW Voltage for all Inputs (Note 1)		0.8	V
V_I	Input Clamp Voltage	I_{IN} = –18 mA, V_{CC} = Min.		–1.2	V
I_{IH}	Input HIGH Current	V_{IN} = 2.7 V, V_{CC} = Max. (Note 2)		25	µA
I_{IL}	Input LOW Current	V_{IN} = 0.4 V, V_{CC} = Max. (Note 2)		–250	µA
I_I	Maximum Input Current	V_{IN} = 5.5 V, V_{CC} = Max.		1	mA
I_{OZH}	Off-State Output Leakage Current HIGH	V_{OUT} = 2.7 V, V_{CC} = Max. V_{IN} = V_{IH} or V_{IL} (Note 2)		100	µA
I_{OZL}	Off-State Output Leakage Current LOW	V_{OUT} = 0.4 V, V_{CC} = Max. V_{IN} = V_{IH} or V_{IL} (Note 2)		–100	µA
I_{SC}	Output Short-Circuit Current	V_{OUT} = 0.5 V, V_{CC} = Max. (Note 3)	–30	–90	mA
I_{CC}	Supply Current	V_{IN} = 0 V, Outputs Open (I_{OUT} = 0 mA) V_{CC} = Max.		210	mA

Notes:

1. These are absolute values with respect to device ground and all overshoots due to system and/or tester noise are included.
2. I/O pin leakage is the worst case of I_{IL} and I_{OZL} (or I_{IH} and I_{OZH}).
3. Not more than one output should be tested at a time. Duration of the short-circuit should not exceed one second. V_{OUT} = 0.5 V has been chosen to avoid test problems caused by tester ground degradation.

CAPACITANCE (Note 1)

Parameter Symbol	Parameter Description		Test Conditions		Typ.	Unit
C_{IN}	Input Capacitance	Pins 1,11	V_{IN} = 2.0 V	V_{CC} = 5.0 V	10	pF
		Others		T_A = +25°C	6	
C_{OUT}	Output Capacitance		V_{OUT} = 2.0 V	f = 1 MHz	9	

Note:

1. These parameters are not 100% tested, but are evaluated at initial characterization and at any time the design is modified where capacitance may be affected.

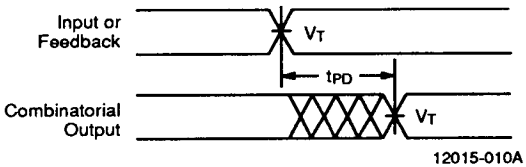
SWITCHING CHARACTERISTICS over COMMERCIAL operating ranges (Note 2)

Parameter Symbol	Parameter Description			-20		-25		Unit
				Min.	Max.	Min.	Max.	
t_{PD}	Input or Feedback to Combinatorial Output				20		25	ns
t_S	Setup Time from Input, Feedback, or SP to Clock			17		20		ns
t_H	Hold Time			0		0		ns
t_{CO}	Clock to Output				13		15	ns
t_{CF}	Clock to Feedback (Note 3)				8		10	ns
t_{AR}	Asynchronous Reset to Registered Output				25		30	ns
t_{ARW}	Asynchronous Reset Width			20		25		ns
t_{ARR}	Asynchronous Reset Recovery Time			20		25		ns
t_{WL}	Clock Width	LOW		12		15		ns
t_{WH}		HIGH		12		15		ns
f_{MAX}	Maximum Frequency (Note 4)	External Feedback	$1/(t_S + t_{CO})$	33		28.5		MHz
		Internal Feedback	$1/(t_S + t_{CF})$	40		33		MHz
t_{EA}	Input to Output Enable Using Product Term Control				25		28	ns
t_{ER}	Input to Output Disable Using Product Term Control				25		28	ns

Notes:

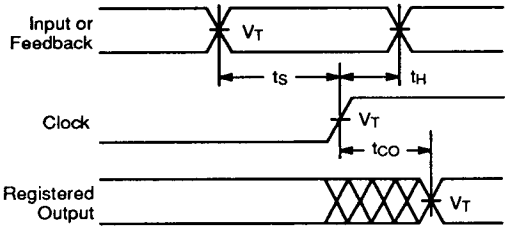
2. See Switching Test Circuit for test conditions.
3. Calculated from measured clock to combinatorial output.
4. These parameters are not 100% tested, but are calculated at initial characterization and at any time the design is modified where frequency may be affected.

SWITCHING WAVEFORMS



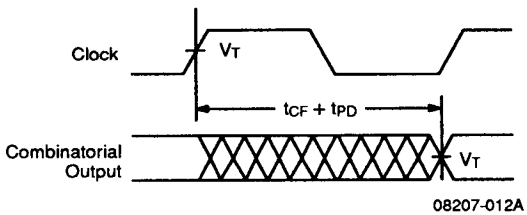
12015-010A

Combinatorial Output



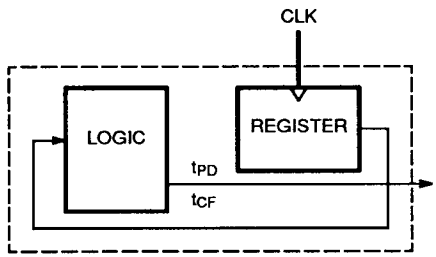
12015-012A

Registered Output

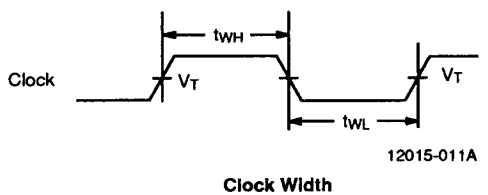


08207-012A

Clock to Feedback See Path at Right

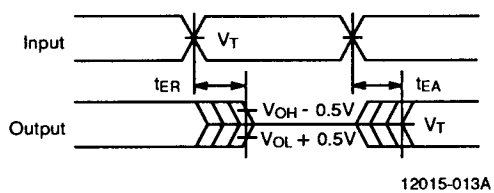


08207-013A



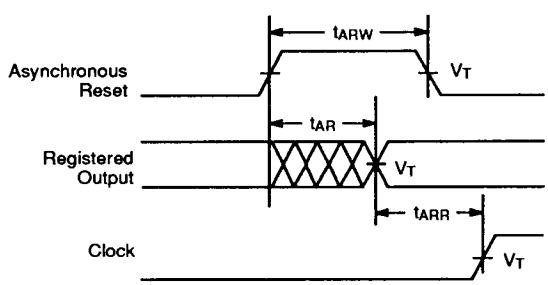
12015-011A

Clock Width



12015-013A

Input to Output Disable/Enable



08207-014A

Asynchronous Reset

Notes:

1. V_T = 1.5 V
2. Input pulse amplitude 0 V to 3.0 V
3. Input rise and fall times 2–5 ns typical.

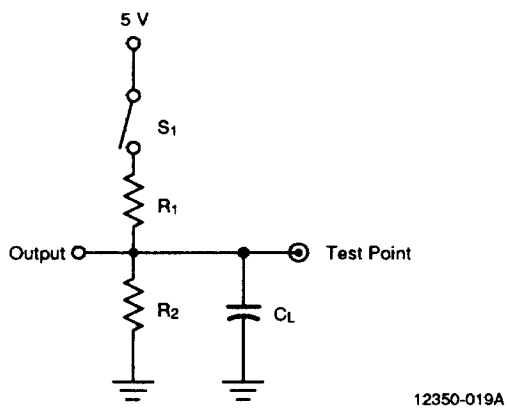
KEY TO SWITCHING WAVEFORMS

WAVEFORM	INPUTS	OUTPUTS
	Must be Steady	Will be Steady
	May Change from H to L	Will be Changing from H to L
	May Change from L to H	Will be Changing from L to H
	Don't Care; Any Change Permitted	Changing, State Unknown
	Does Not Apply	Center Line is High-Impedence "Off" State

KS000010-PAL

2

SWITCHING TEST CIRCUIT

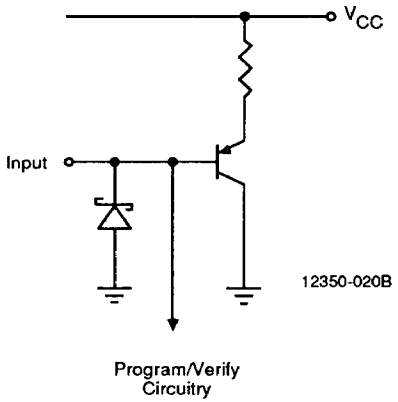


12350-019A

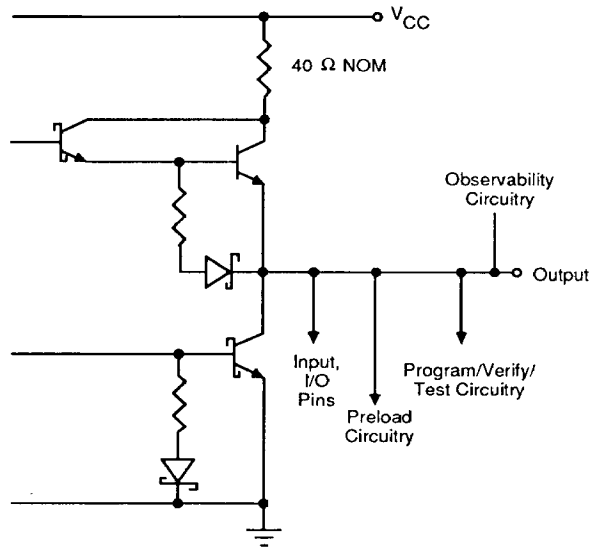
Specification	S_1	C_L	R_1	R_2	Measured Output Value
t_{PD}, t_{CO}, t_{CF}	Closed	50 pF	300 Ω	390 Ω	1.5 V
t_{EA}	Z → H: Open Z → L: Closed				1.5 V
t_{ER}	H → Z: Open L → Z: Closed	5 pF			H → Z: V_{OH} – 0.5 V L → Z: V_{OL} + 0.5 V

INPUT/OUTPUT EQUIVALENT SCHEMATICS

Typical Input

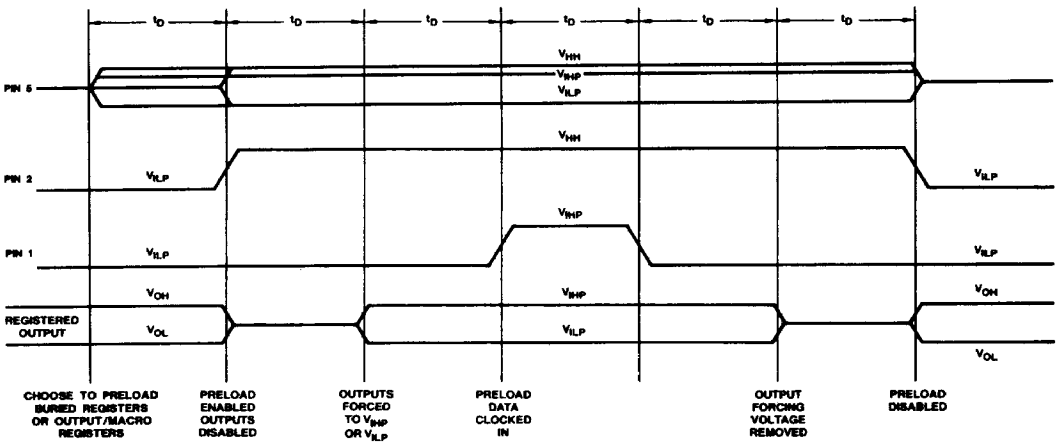


Typical Output



REGISTER PRELOAD

All AmPAL23S8 registers are provided with circuitry to allow loading each register synchronously with a HIGH or LOW. Output/macrocell registers and buried state registers are PRELOADed in separate cycles allowing output/macrocell registers and buried state registers to be PRELOADed with different values. PRELOAD will simplify testing since any state can be loaded into the registers to control testing sequences. The pin levels and timing necessary to perform the PRELOAD function are detailed below.



Par.	Min.	Max.
V_{HH}	10	12
V_{ILP}	0	0.5
V_{IHP}	2.4	5.5

Register Selection	Pin 5
Buried	V_{HH}
Output/Macro	$\leq V_{IHP}$

Level Forced on Register Output Pin During PRELOAD Cycle	Register State After Cycle
V_{IHP}	HIGH
V_{ILP}	LOW

WF022292

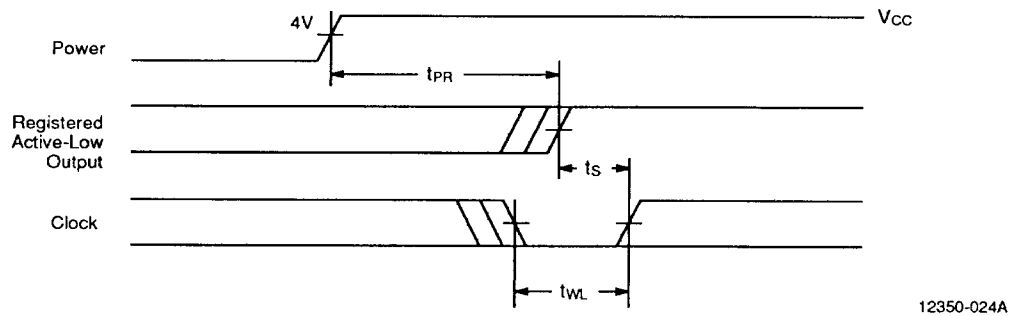
Output Register Preload Waveform

POWER-UP RESET

The power-up reset feature ensures that all flip-flops will be reset to LOW after the device has been powered up. The output state will depend on the programmed configuration. This feature is valuable in simplifying state machine initialization. A timing diagram and parameter table are shown below. Due to the synchronous operation of the power-up reset and the wide range of ways V_{CC} can rise to its steady state, two conditions are required to ensure a valid power-up reset. These conditions are:

1. The V_{CC} rise must be monotonic.
2. Following reset, the clock input must not be driven from LOW to HIGH until all applicable input and feedback setup times are met.

Parameter Symbol	Parameter Description	Max.	Unit
t_{PR}	Power-up Reset Time	1000	ns
t_S	Input or Feedback Setup Time	See Switching Characteristics	
t_{WL}	Clock Width LOW		



Power-Up Reset Waveform