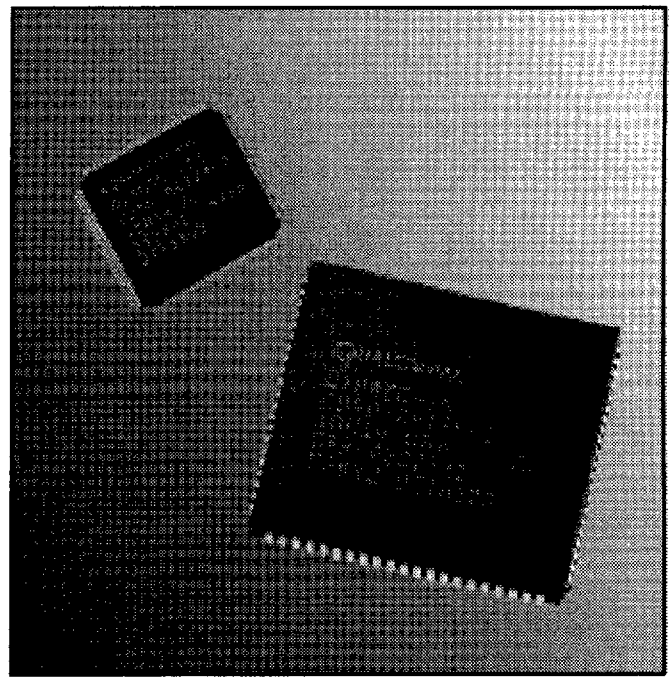
Q1900

VITERBI/TRELLIS DECODER



FEATURES

- Viterbi Mode Rates 1/3, 1/2, 3/4 and 7/8
- Trellis Mode Rates 2/3 and 3/4
- Full Duplex Encode and Decode in Both Viterbi and Trellis Modes
- Large Coding Gains at Eb/No of 10^{-5}
  - 5.5 dB for Rate 1/3 Viterbi Decoding
  - 5.2 dB for Rate 1/2 Viterbi Decoding
  - 3.2 dB for Rate 2/3 Trellis Decoding
  - 3.1 dB for Rate 3/4 Trellis Decoding
- Automatic Phase Synchronization for BPSK and QPSK in Viterbi Mode and for 8-PSK and 16-PSK in Trellis Mode
- Data Rates up to 30 Mbps for Viterbi Mode and 90 Mbps (16-PSK) for Trellis Mode
- 3-Bit Soft Decision or 1-Bit Hard Decision Decoder Inputs for Viterbi Mode
- Viterbi Mode On-chip Channel Bit Error Rate (BER) Monitor
- Easy Implementation of Additional Code Rates
- Processor Inferface Simplifies Control and Status
- Low-power CMOS Implementation
- Viterbi Mode Complies with INTELSAT IESS-308 and INTELSAT IESS-309
- Standard 84-Pin PLCC or 100-Pin VTQFP Package

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GENERAL DESCRIPTION

Forward Error Correction (FEC) improves the bit error rate (BER) performance of power-limited and/or bandwidth-limited channels by adding structured redundancy to the transmitted data. The type of additive noise experienced on the channel determines the class of FEC used on the channel. Tree codes are used for channels with Additive White Gaussian Noise (AWGN) and block codes are used for channels with additive burst noise. The Q1900 is based on a k=7 Viterbi decoder tree code, optimizing performance over channels with AWGN. The Q1900 supports encoding and decoding for Viterbi and Trellis Modes of operation. The Viterbi Mode is typically used for systems that are power-limited but not bandwidth-limited. The standard modulation types are Binary Phase Shift Keying (BPSK) and Quadrature Phase Shift Keying (QPSK). Trellis Mode is typically used for systems that are both power-limited and bandwidth-limited. The standard modulation types are 8-PSK and 16-PSK. Figure 1 shows a typical application of FEC techniques in a communication system.

Figures 2 and 3 show the encoder block diagrams for the Viterbi and Trellis Modes. Figures 4 and 5 show the decoder block diagrams for the Viterbi and Trellis Modes. The encoders are both based on a k=7 convolutional encoder and the decoders are both based on a k=7 Viterbi decoder.

The Viterbi Mode supports four code rates: 1/3, 1/2, 3/4 and 7/8. Additional code rates can be supported with external circuitry. The Viterbi Mode also supports built-in phase synchronization for standard BPSK, QPSK, and Offset Quadrature Phase Shift Keying (OQPSK) modulation techniques. Either 1 bit hard-decision or 3 bit soft-decision input data is supported. The Viterbi Mode also includes two powerful built-in techniques for monitoring synchronization status as well as performing channel BER measurements.

The Trellis Mode supports two codes rates: 2/3 for 8 PSK and 3/4 for 16 PSK. The Trellis Mode also supports built-in phase synchronization for 8-PSK and 16-PSK. The Viterbi and Trellis Modes include a processor interface to facilitate control and status monitoring functions while keeping device pinout to a minimum.

The Q1900 is packaged in a 84-pin PLCC package or a 100-pin VTQFP package and is implemented in fully static CMOS logic to reduce power consumption. It also uses fully parallel circuit architecture to negate the requirement for a higher speed computation clock.

The Q1900 is well suited for many commercial satellite communication networks, including INMARSAT and INTELSAT. The low-cost and high

Figure 1. Typical Application of FEC in a Communication System

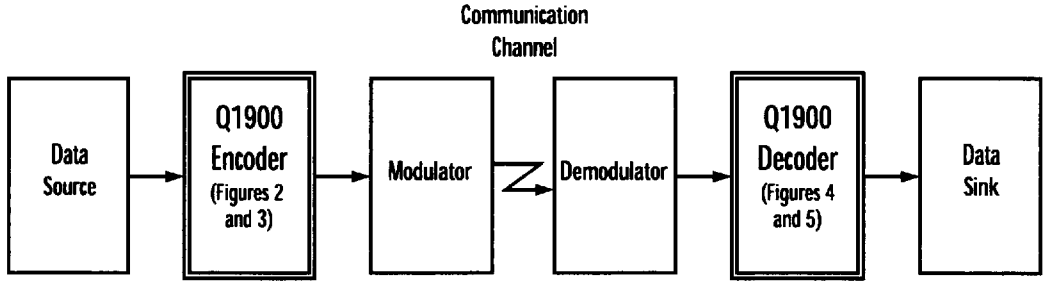

Figure 2. Viterbi Encoder Block Diagram

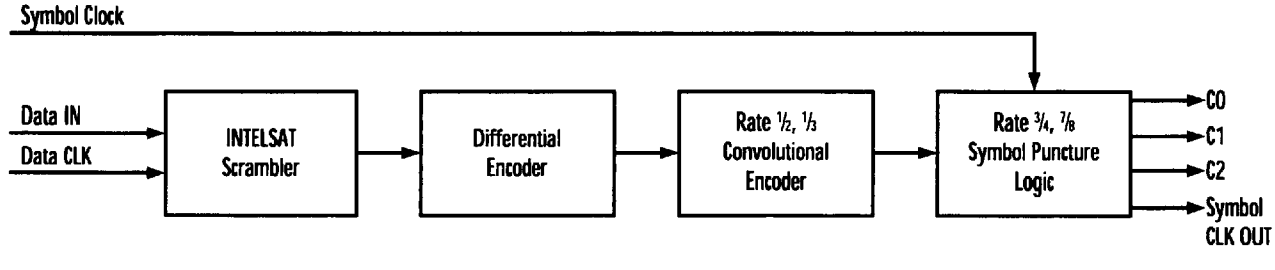

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Figure 3. Trellis Encoder Block Diagram

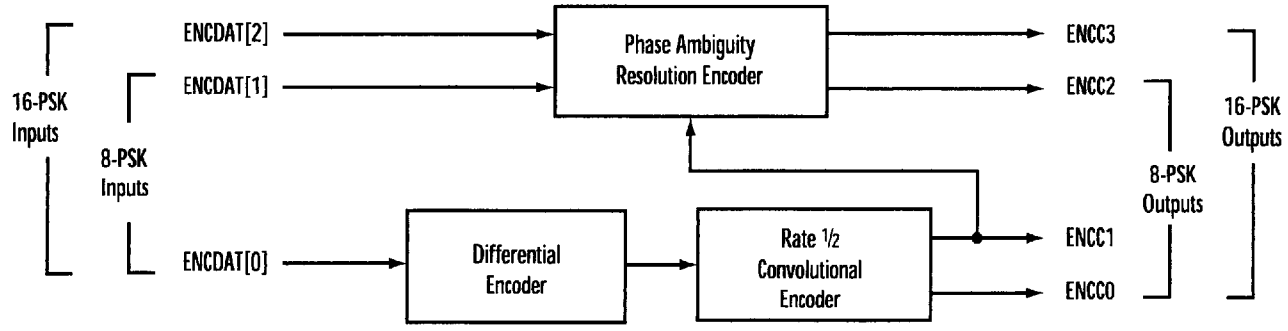


Figure 4. Viterbi Decoder Block Diagram

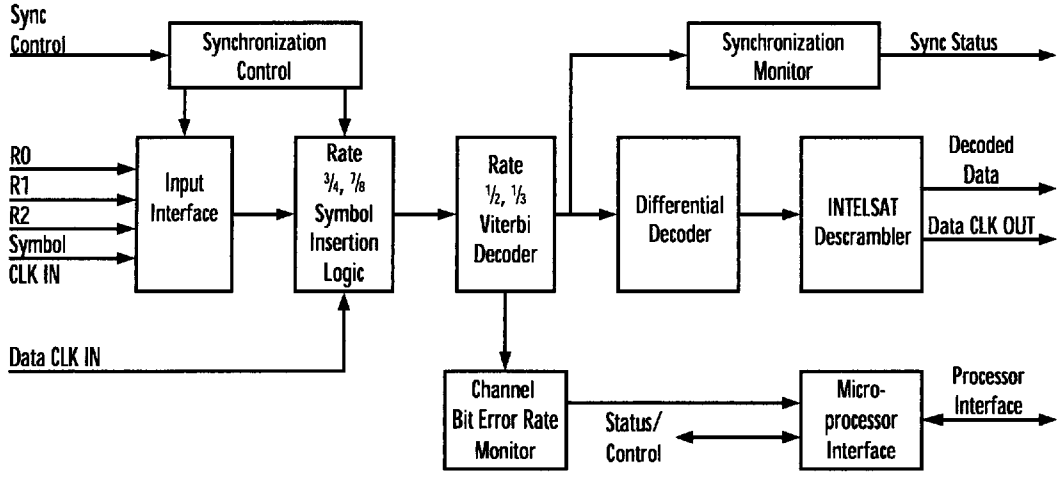
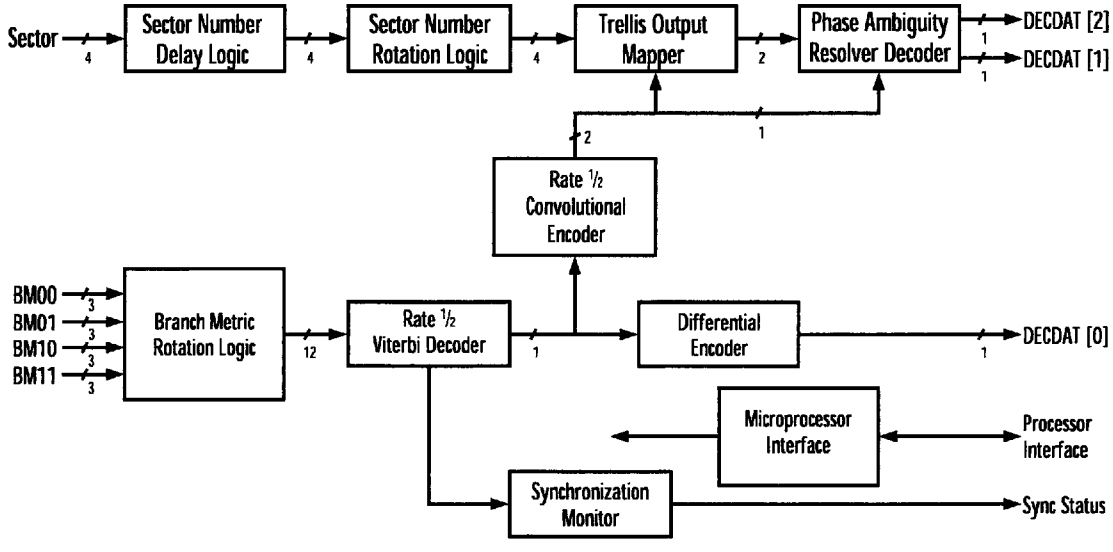


Figure 5. Trellis Decoder Block Diagram



performance of the Q1900 make it ideal for FEC requirements in systems such as direct broadcast satellites (DBS), microwave point-to-point data links, very small aperture terminals (VSAT), digital modems, digital video transmission systems, high-speed data modems and military and NASA communication systems.

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THEORY OF OPERATION

ENCODING

VITERBI MODE

The transformation from information bit to code word for the Viterbi Mode is shown in Figure 2. The number of functions involved in this process can range from one to four depending on which functions are enabled.

The first function is an INTELSAT specified scrambling algorithm. This algorithm is a slight modification to the CCITT V.35 algorithm. The details of this algorithm are described in the *Data Scrambling Applications Note* section of this data book. Scrambling is used in many communications systems to guarantee minimum transition densities in the transmitted signal for purposes such as timing loop synchronization.

A system consideration when using data scrambling is multiplication of output bit errors. Because the data scrambler output bits are affected by several input bits, error multiplication occurs. If the Viterbi decoder incorrectly decodes a bit and this single bit is input into the descrambler, it can generate up to three output errors. However, in actuality the error multiplication is a factor of 1.5 to 2. This equates to a coding gain loss of only 0.2 to 0.3 dB.

The second function is a differential encoder. The block diagrams for the differential encoder and decoder are shown in Figures 6 and 7. The differential encoder and decoder are used to resolve inverted data. The differential encoder actually transforms the input data stream into an indication of transitions rather than 1's or 0's. If a 0 is input into the encoder, the output stays the same. If a 1 is input, the output transitions either 0 to 1 or 1 to 0.

The third function is the industry standard k=7 rate ½ or rate ⅓ convolutional encoder, shown in Figure 8.

Figure 6. Differential Encoder

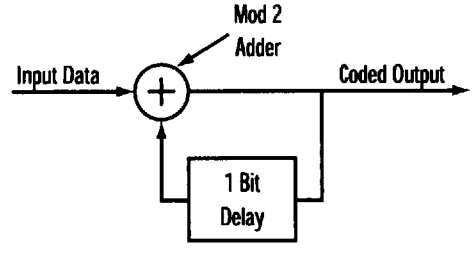


Figure 7. Differential Decoder

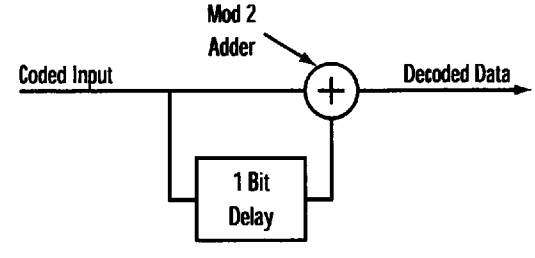
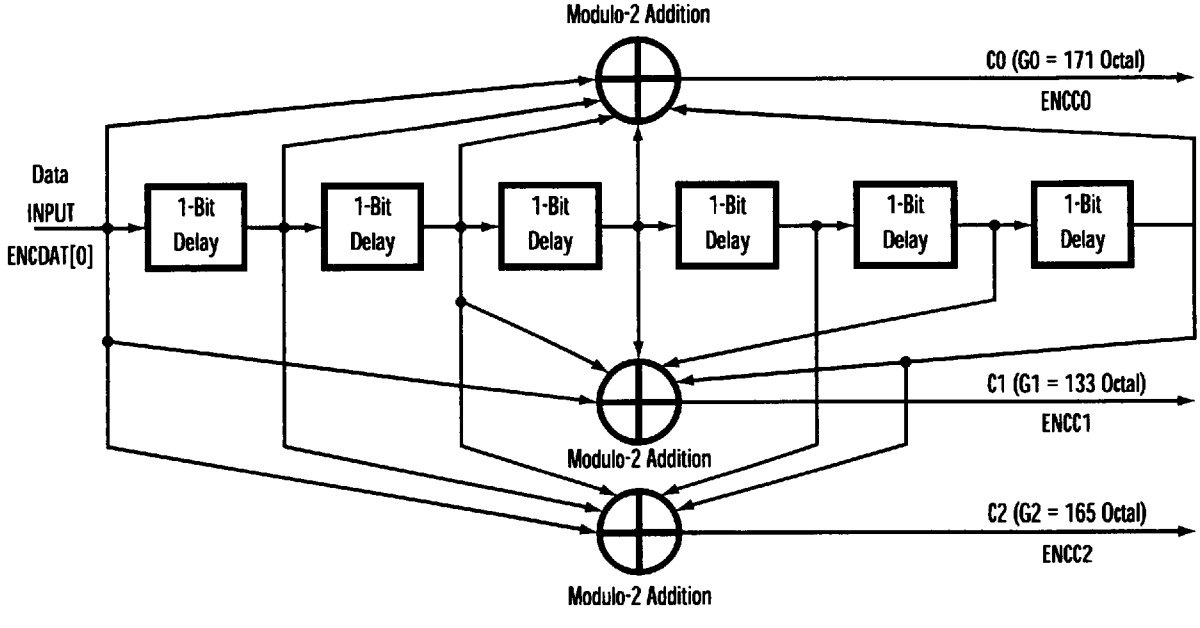


Figure 8. 64-State Convolutional Encoder



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It is used to encode the ENCDAT[0] input bit into two or three output bits ENCC0, ENCC1 and ENCC2.

The fourth function is the puncture logic. This step punctures the rate ½ data into either rate ¾ or rate ⅞. Figures 9a and 9b show how rate ½ data is punctured into rate ¾ or rate ⅞. The input data is encoded with a rate ½ encoder (B). Then certain bits of the rate ½ encoded data are punctured, or deleted, and not transmitted (C). For rate ¾, two out of six bits from the rate ½ encoder are deleted in a repeating pattern. Thus, for every three input bits, only four encoded bits are actually transmitted making this a rate ¾ code. For rate ⅞, six out of fourteen bits from the rate ½ encoder are deleted in a repeating pattern. Thus, for every seven input bits, only eight encoded bits are actually transmitted making this a rate ⅞ code.

At the receiver, the punctured bits are replaced with null bits prior to decoding with the rate ½ decoder (D). Insertion of the null bits is done automatically if the Q1900 is programmed for rate ¾ or ⅞. For punctured rates other than ¾ and ⅞, insertion of the null bits is done externally by asserting the erase input pins as appropriate for R0, R1, or R2. The decoder treats null bits as an input which is neither a received "1" nor "0", but is exactly between the "1" and "0".

The coding performance of a punctured rate ¾ code is equivalent to the coding performance of a classic non-punctured rate ¾ code. The major advantage of punctured coding with a standard rate convolutional encoder (½ or ⅓) is that a single code rate decoder can decode a wide range of codes. Specifically, any code rate of the form (n-1)/n can be efficiently implemented with this structure. Of course, the best performance is achieved with certain puncture patterns. The best punctured codes have been researched and are shown in Figure 10 for rates from ½ through 16/17. The chainback depth must increase as the code rate increases. A chainback memory depth of 35-40 states is adequate for rate ½ decoding. However, rate ¾ decoders require memory depths of at least 70 states, and rate ⅞ requires chainback depth of more than 90 states. The Q1900 decoder uses a minimum chainback memory depth of 96 states for puncture coding. Therefore, it is very effective at decoding code rates up to ⅞. Operation with code rates higher than ⅞ will result in a minor performance degradation in the coding gain when compared to the theoretical best.

During punctured coding, the decoder must synchronize the null symbol insertion pattern of the decoder to the symbol puncture pattern of the encoder. The Q1900 performs all the necessary symbol puncture (encoder), null symbol insertion (decoder) and synchronization functions required to implement rates ¾ and ⅞. The decoder also includes First-In-First-Out (FIFO) circuits which ease the frequent requirement of punctured code systems to re-align the punctured encoded stream to a channel clock, which is a non-integer multiple of the information data rate.

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Figure 9a. Punctured Coding for Rate 3/4

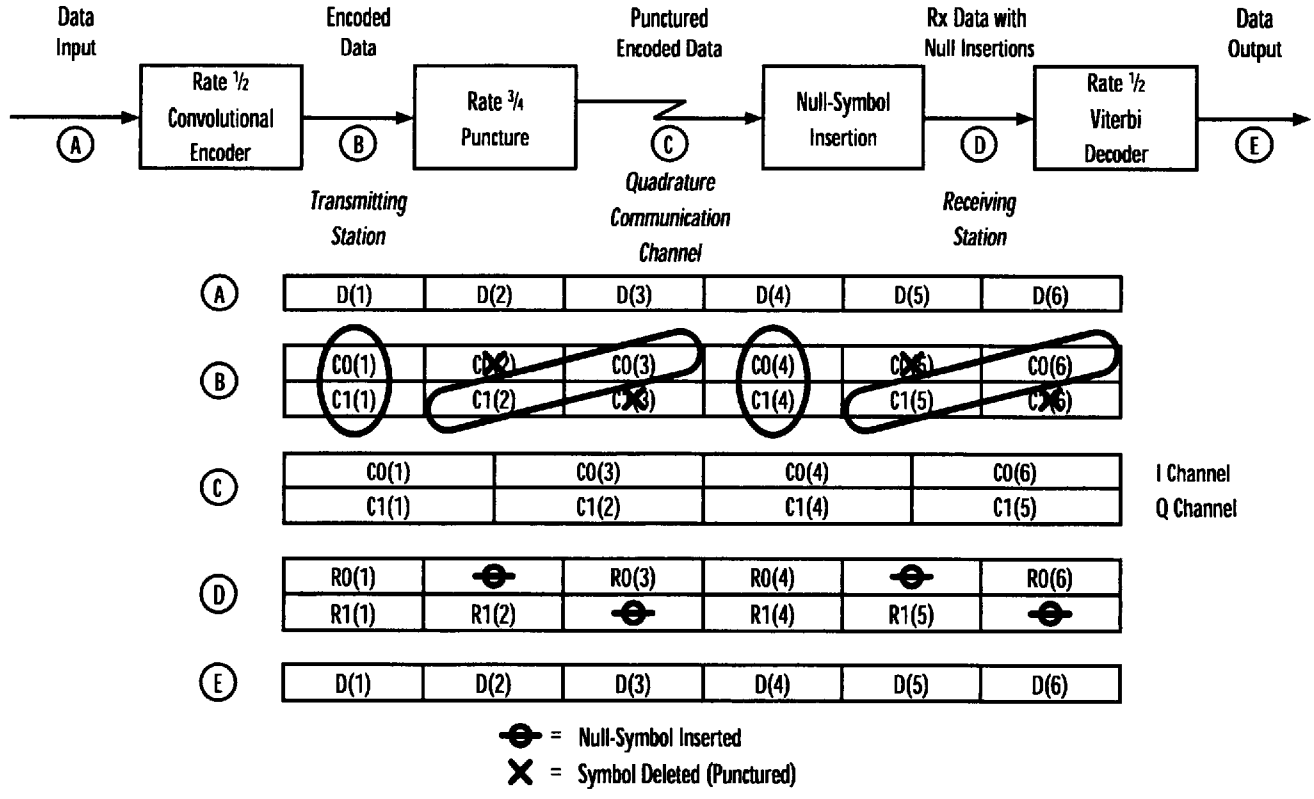

Figure 9b. Punctured Coding for Rate 7/8

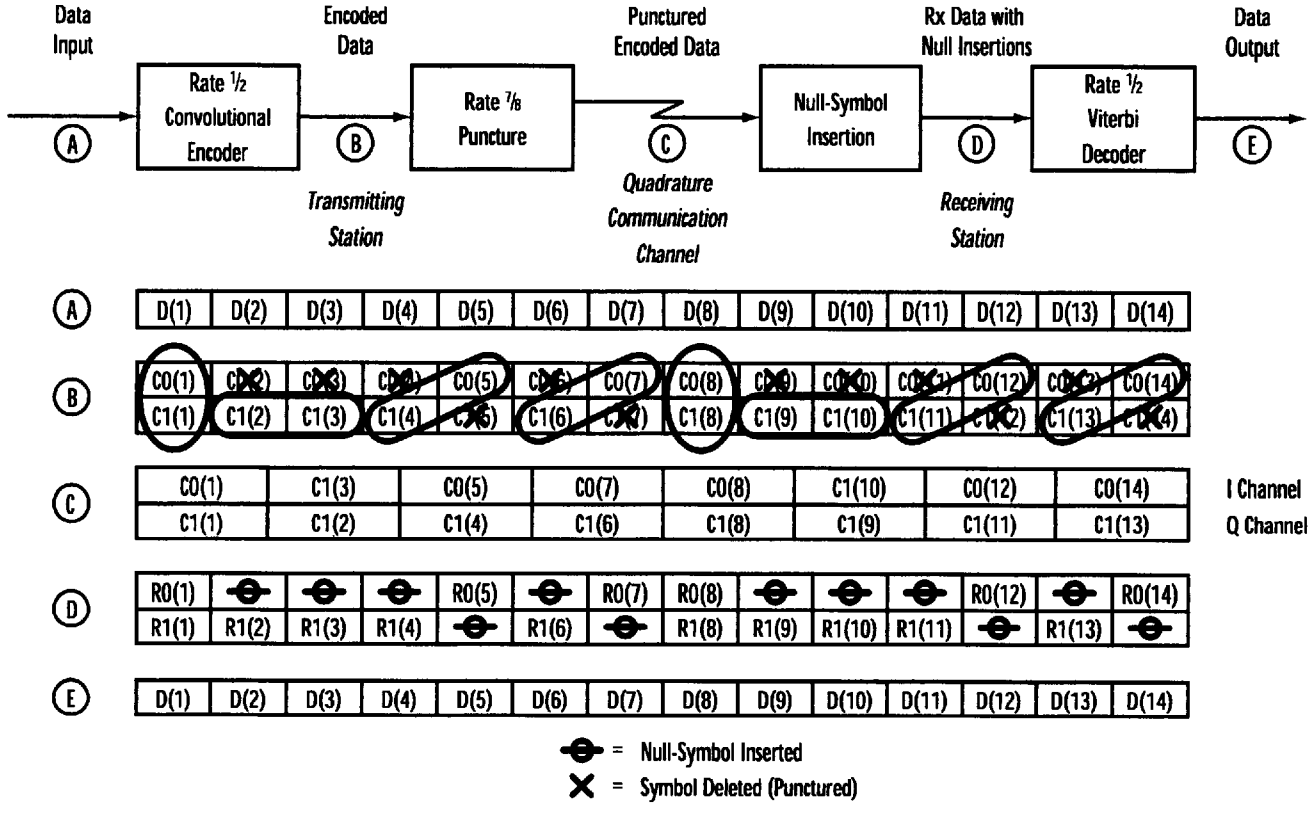

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Figure 10. Best Punctured Code Patterns

Code Rate	Puncture Pattern (0 = Deleted Code Bit)
1/2	C0: 1 C1: 1
2/3	C0: 1 0 C1: 1 1
3/4*	C0: 1 0 1 C1: 1 1 0
4/5	C0: 1 0 0 0 C1: 1 1 1 1
5/6	C0: 1 0 1 0 1 C1: 1 1 0 1 0
6/7	C0: 1 0 0 1 0 1 C1: 1 1 1 0 1 0
7/8*	C0: 1 0 0 0 1 0 1 C1: 1 1 1 1 0 1 0
11/12	C0: 1 0 0 0 1 0 0 0 0 0 1 C1: 1 1 1 1 0 1 1 1 1 1 0
12/13	C0: 1 0 0 0 0 0 0 0 1 0 1 0 C1: 1 1 1 1 1 1 1 1 0 1 0 1
15/16	C0: 1 0 0 1 1 0 1 0 0 1 0 1 1 0 1 C1: 1 1 1 0 0 1 0 1 1 0 1 0 0 1 0
16/17	C0: 1 0 1 0 1 0 1 1 0 1 1 1 1 0 1 0 C1: 1 1 0 1 0 1 0 0 1 0 0 0 0 1 0 1

* Two code bit groupings are shown for operation with code rates 3/4 and 7/8 in Parallel Data Mode. C0 and C1 code bits are output on the C0 and C1 signals, respectively, except for the second symbol in rate 7/8 pattern. In that case, the second of the two C1 code bits is output on the C0 signal.

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TRELLIS MODE

The transformation from information bits to code words for rate 2/3 8-PSK and rate 3/4 16-PSK is a three-step process (Figure 3). First, the ENCDAT[0] data bit is differentially encoded, if differential encoding is enabled. Next, the industry standard k=7 rate 1/2 convolutional encoder is used to encode the ENCDAT[0] input bit into two output bits, ENCC0 and ENCC1. The output bits, ENCC0 and ENCC1, become the Least Significant Bits (LSBs) of the transmitted phase. The third step applies phase ambiguity resolution encoding to the ENCDAT[1] bit for 2/3 8-PSK and to the ENCDAT[1] and ENCDAT[2] bits for 3/4 16-PSK.

The encoder phase ambiguity resolution functions for 8-PSK and 16-PSK are shown in Figures 11 and 12. The encoder phase ambiguity function uses the convolutional encoder output, ENCC1, to select one of two differential encoders for ENCDAT[1] (8-PSK), and for ENCDAT[1] and ENCDAT[2] (16-PSK). Table 1 shows the states of the four-phase differential encoder.

Table 1. Four-Phase Differential Encoder State Table

PRESENT INPUT		LAST INPUT		OUTPUT	
a(n)	b(n)	a(n-1)	b(n-1)	x(n)	y(n)
0	0	0	0	0	0
0	1	0	0	0	1
1	0	0	0	1	0
1	1	0	0	1	1
0	0	0	1	0	1
0	1	0	1	1	1
1	0	0	1	0	0
1	1	0	1	1	0
0	0	1	0	1	0
0	1	1	0	0	0
1	0	1	0	1	1
1	1	1	0	0	1
0	0	1	1	1	1
0	1	1	1	1	0
1	0	1	1	0	1
1	1	1	1	0	0

Figure 11. Phase Ambiguity Resolution Encoder for 8-PSK Modulation

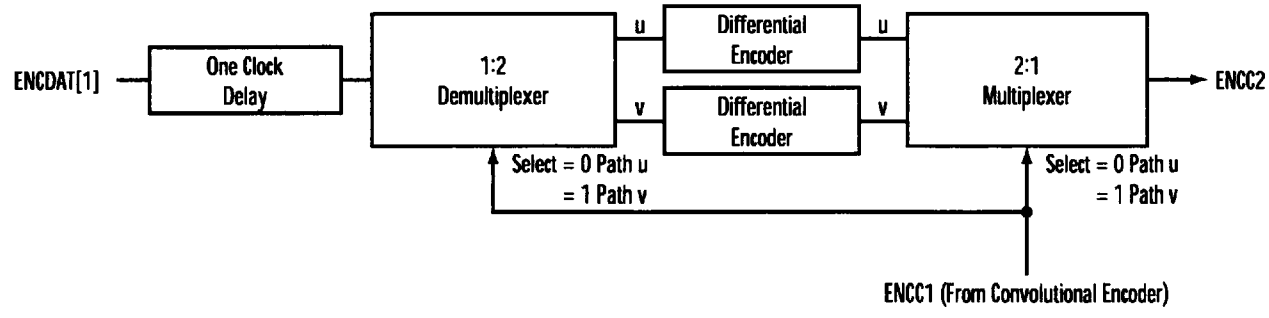
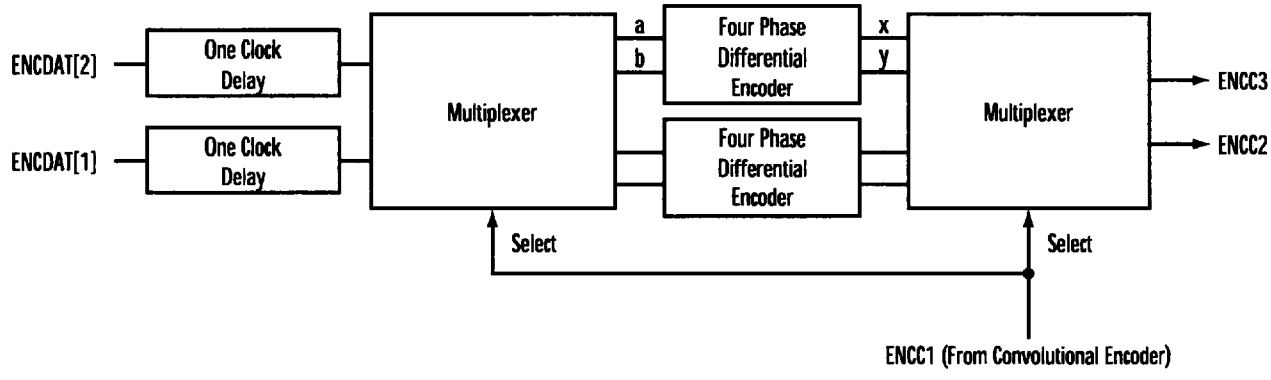


Figure 12. Phase Ambiguity Resolution Encoder for 16-PSK Modulation



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DECODING

While the implementation of the convolutional encoder functions for the Viterbi Mode and the Trellis Mode are straightforward and simple, the decoding of the data stream at the receiving node is complex.

VITERBI MODE

Viterbi decoding consists of three fundamental steps. The first step is to generate a set of correlation measurements, known as branch metrics, for each "m" grouping of code words input from the communication channel, where "m" is 2 for rate ½ codes, 3 for rate ⅓ codes, etc. These branch metric values indicate the correlation between the received code words and the 2"m" possible code word combinations.

The Viterbi decoder determines the state of the 7-bit memory at the encoder using a maximum likelihood technique. Once the value of the encoder memory is determined, the original information is known since the encoder memory is simply the information that has been stored. To determine the encoder state, the second step in the Viterbi algorithm generates a set of 2^{k-1} state metrics, where "k" is the constraint length (k=7 for the Q1900) which measures the occurrence probability for each of the 2^{k-1} possible encoder memory states. As the state metrics are computed, a binary decision is formed for each of the 2^{k-1} possible states, determining the probable path taken to arrive at that particular state. These binary decisions are stored in the path memory.

Step three computes the decoded output data. The path from the current state to some point in a finite past state is traced back by chaining the binary decisions stored in the path memory (step 2). The effects caused by noise are mitigated as paths to the correct result converge after some history. The greater the depth of the chainback process, the more likely that the final decoded result is error-free. As a result, higher code rates and constraint lengths require longer chainback depth for best performance.

TRELLIS MODE

The Trellis Mode also uses an industry standard k=7 Viterbi decoder along with supplementary circuitry to decode the trellis encoded data. This technique is called Pragmatic Trellis Coded Modulation (PTCM) decoding (U.S. patent No. 5,469,452 - foreign patents issued and pending).

Fundamentally, PTCM decoding consists of three steps. First, the received symbol or phase angle is converted to four branch metrics and a sector number. Second, the branch metrics are processed with a standard k=7 Viterbi decoder to decode the least significant output bit, DECDAT[0]. The third step decodes the most significant output bit(s) DECDAT[1] for 8-PSK and DECDAT[1] and DECDAT[2] for 16-PSK. The three steps are described in detail in the following paragraphs.

In the first step, the received phase angle is converted to four branch metrics and a sector number with an external lookup table. The branch metrics are based on the Euclidean distance of the received phase with respect to the four closest transmitted phase points. The branch metric and sector number for 8-PSK are given in Table 2. The branch metrics and sector number for 16-PSK are given in Tables 3a and 3b. The sector number tells the decoder on which portion of the I-Q plane the symbol was received. For 8-PSK modulation, sector numbers are assigned by dividing the signal constellation into eight equal sectors (Figure 13). Likewise, for 16-PSK modulation, the signal constellation is divided into sixteen equal sectors (Figure 14). The actual value input into the Q1900 PTCM decoder is the binary representation of the sector number. Note: A sector is defined from a signal point counterclockwise to the border of the next signal point. For example, sector 2 for 8-PSK modulation begins at the phase point 011 (90°) but ends just before phase point 010 (135°).

In the second step of the decoding process, the PTCM decoder processes the branch metrics with the standard k=7 Viterbi decoder algorithm. The decoded output DECDAT[0] becomes the least significant output bit.

The third step re-encodes the DECDAT[0] data bit to generate the best possible estimate of the transmitted LSBs, ENCC0 and ENCC1. For each combination given of ENCC0 and ENCC1, there are 2 possible transmitted

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phase angles for 8-PSK and 4 possible transmitted phase angles for 16-PSK. For example, if the received LSB is equal to 01, this corresponds to 45° or 225° for 8-PSK and to 22.5°, 112.5°, 202.5° and 292.5° for 16-PSK. To determine the MSBs, the received sector number is compared to the 2 or 4 possible phase angles. The phase angle closest to the sector number is chosen as the transmitted phase.

For example, if the received signal has a phase angle of 100° for 8-PSK, this corresponds to a sector number of 2. See Figure 13. If the re-encoded bit provides estimates of ENCC1=0 and ENCC0=1, the two possible transmitted phase points are 001 and 101. Since the received phase of 100° is located in a sector that is closer to phase point 001 than to phase point 101, the DECDAT[1] is determined to be 0.

Table 2. 8-PSK Modulation Phase to Branch Metric Conversion

Phase	B00 (OCT)	B01 (OCT)	B11 (OCT)	B10 (OCT)	Sector Number	Phase	B00 (OCT)	B01 (OCT)	B11 (OCT)	B10 (OCT)	Sector Number
$0.0 \le \varphi < 2.8$	0	4	7	4	0	$180.0 \le \varphi < 182.8$	0	4	7	4	4
$2.8 \le \varphi < 8.4$	0	3	7	4	0	$182.8 \le \varphi < 188.4$	0	3	7	4	4
$8.4 \le \varphi < 14.1$	0	2	6	4	0	$188.4 \le \varphi < 194.1$	0	2	6	4	4
$14.1 \le \varphi < 19.7$	0	1	5	4	0	$194.1 \le \varphi < 199.7$	0	1	5	4	4
$19.7 \le \varphi < 25.3$	0	0	4	4	0	$199.7 \le \varphi < 205.3$	0	0	4	4	4
$25.3 \le \varphi < 30.9$	1	0	4	5	0	$205.3 \le \varphi < 210.9$	1	0	4	5	4
$30.9 \le \varphi < 36.6$	2	0	4	6	0	$210.9 \le \varphi < 216.6$	2	0	4	6	4
$36.6 \le \varphi < 42.2$	3	0	4	7	0	$216.6 \le \varphi < 222.2$	3	0	4	7	4
$42.2 \le \varphi < 45.0$	4	0	4	7	0	$222.2 \le \varphi < 225.0$	4	0	4	7	4
$45.0 \le \varphi < 47.8$	4	0	4	7	1	$225.0 \le \varphi < 227.8$	4	0	4	7	5
$47.8 \le \varphi < 53.4$	4	0	3	7	1	$227.8 \le \varphi < 233.4$	4	0	3	7	5
$53.4 \le \varphi < 59.1$	4	0	2	6	1	$233.4 \le \varphi < 239.1$	4	0	2	6	5
$59.1 \le \varphi < 64.7$	4	0	1	5	1	$239.1 \le \varphi < 244.7$	4	0	1	5	5
$64.7 \le \varphi < 70.3$	4	0	0	4	1	$244.7 \le \varphi < 250.3$	4	0	0	4	5
$70.3 \le \varphi < 75.9$	5	1	0	4	1	$250.3 \le \varphi < 255.9$	5	1	0	4	5
$75.9 \le \varphi < 81.6$	6	2	0	4	1	$255.9 \le \varphi < 261.6$	6	2	0	4	5
$81.6 \le \varphi < 87.2$	7	3	0	4	1	$261.6 \le \varphi < 267.2$	7	3	0	4	5
$87.2 \le \varphi < 90.0$	7	4	0	4	1	$267.2 \le \varphi < 270.0$	7	4	0	4	5
$90.0 \le \varphi < 92.8$	7	4	0	4	2	$270.0 \le \varphi < 272.8$	7	4	0	4	6
$92.8 \le \varphi < 98.4$	7	4	0	3	2	$272.8 \le \varphi < 278.4$	7	4	0	3	6
$98.4 \le \varphi < 104.1$	6	4	0	2	2	$278.4 \le \varphi < 284.1$	6	4	0	2	6
$104.1 \le \varphi < 109.7$	5	4	0	1	2	$284.1 \le \varphi < 289.7$	5	4	0	1	6
$109.7 \le \varphi < 115.3$	4	4	0	0	2	$289.7 \le \varphi < 295.3$	4	4	0	0	6
$115.3 \le \varphi < 120.9$	4	5	1	0	2	$295.3 \le \varphi < 300.9$	4	5	1	0	6
$120.9 \le \varphi < 126.6$	4	6	2	0	2	$300.9 \le \varphi < 306.6$	4	6	2	0	6
$126.6 \le \varphi < 132.2$	4	7	3	0	2	$306.6 \le \varphi < 312.2$	4	7	3	0	6
$132.2 \le \varphi < 135.0$	4	7	4	0	2	$312.2 \le \varphi < 315.0$	4	7	4	0	6
$135.0 \le \varphi < 137.8$	4	7	4	0	3	$315.0 \le \varphi < 317.8$	4	7	4	0	7
$137.8 \le \varphi < 143.4$	3	7	4	0	3	$317.8 \le \varphi < 323.4$	3	7	4	0	7
$143.4 \le \varphi < 149.1$	2	6	4	0	3	$323.4 \le \varphi < 329.1$	2	6	4	0	7
$149.1 \le \varphi < 154.7$	1	5	4	0	3	$329.1 \le \varphi < 334.7$	1	5	4	0	7
$154.7 \le \varphi < 160.3$	0	4	4	0	3	$334.7 \le \varphi < 340.3$	0	4	4	0	7
$160.3 \le \varphi < 165.9$	0	4	5	1	3	$340.3 \le \varphi < 345.9$	0	4	5	1	7
$165.9 \le \varphi < 171.6$	0	4	6	2	3	$345.9 \le \varphi < 351.6$	0	4	6	2	7
$171.6 \le \varphi < 177.2$	0	4	7	3	3	$351.6 \le \varphi < 357.2$	0	4	7	3	7
$177.2 \le \varphi < 180.0$	0	4	7	4	3	$357.2 \le \varphi < 360.0$	0	4	7	4	7

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A similar example can be supplied for 16-PSK modulation. See Figure 14. If the received signal has a phase angle of 175°, this corresponds to a sector number of 7. If the re-encoded LSB provides estimates of ENCC1=0 and ENCC0=0, the four possible transmitted phase points are 0000, 0100, 1100, and 1000. See Figure 14. Since the received phase of 175° (sector 7) is located in a sector that is closest to phase point 1100 (sector 8), the DECDAT[1] and DECDAT[2] data bits are determined to be DECDAT[1]=1 and DECDAT[2]=1.

Table 3a. 16-PSK Modulation Phase to Branch Metric Conversion

Phase	B00 (OCT)	B01 (OCT)	B11 (OCT)	B10 (OCT)	Sector Number	Phase	B00 (OCT)	B01 (OCT)	B11 (OCT)	B10 (OCT)	Sector Number
$0.0 \le \varphi < 1.4$	0	4	7	4	0	$90.0 \le \varphi < 91.4$	0	4	7	4	4
$1.4 \le \varphi < 4.2$	0	3	7	4	0	$91.4 \le \varphi < 94.2$	0	3	7	4	4
$4.2 \le \varphi < 7.0$	0	2	6	4	0	$94.2 \le \varphi < 97.0$	0	2	6	4	4
$7.0 \le \varphi < 9.8$	0	1	5	4	0	$97.0 \le \varphi < 99.8$	0	1	5	4	4
$9.8 \le \varphi < 12.7$	0	0	4	4	0	$99.8 \le \varphi < 102.7$	0	0	4	4	4
$12.7 \le \varphi < 15.5$	1	0	4	5	0	$102.7 \le \varphi < 105.5$	1	0	4	5	4
$15.5 \le \varphi < 18.3$	2	0	4	6	0	$105.5 \le \varphi < 108.3$	2	0	4	6	4
$18.3 \le \varphi < 21.1$	3	0	4	7	0	$108.3 \le \varphi < 111.1$	3	0	4	7	4
$21.1 \le \varphi < 22.5$	4	0	4	7	0	$111.1 \le \varphi < 112.5$	4	0	4	7	4
$22.5 \le \varphi < 23.9$	4	0	4	7	1	$112.5 \le \varphi < 113.9$	4	0	4	7	5
$23.9 \le \varphi < 26.7$	4	0	3	7	1	$113.9 \le \varphi < 116.7$	4	0	3	7	5
$26.7 \le \varphi < 29.5$	4	0	2	6	1	$116.7 \le \varphi < 119.5$	4	0	2	6	5
$29.5 \le \varphi < 32.3$	4	0	1	5	1	$119.5 \le \varphi < 122.3$	4	0	1	5	5
$32.3 \le \varphi < 35.2$	4	0	0	4	1	$122.3 \le \varphi < 125.2$	4	0	0	4	5
$35.2 \le \varphi < 38.0$	5	1	0	4	1	$125.2 \le \varphi < 128.0$	5	1	0	4	5
$38.0 \le \varphi < 40.8$	6	2	0	4	1	$128.0 \le \varphi < 130.8$	6	2	0	4	5
$40.8 \le \varphi < 43.6$	7	3	0	4	1	$130.8 \le \varphi < 133.6$	7	3	0	4	5
$43.6 \le \varphi < 45.0$	7	4	0	4	1	$133.6 \le \varphi < 135.0$	7	4	0	4	5
$45.0 \le \varphi < 46.4$	7	4	0	4	2	$135.0 \le \varphi < 136.4$	7	4	0	4	6
$46.4 \le \varphi < 49.2$	7	4	0	3	2	$136.4 \le \varphi < 139.2$	7	4	0	3	6
$49.2 \le \varphi < 52.0$	6	4	0	2	2	$139.2 \le \varphi < 142.0$	6	4	0	2	6
$52.0 \le \varphi < 54.8$	5	4	0	1	2	$142.0 \le \varphi < 144.8$	5	4	0	1	6
$54.8 \le \varphi < 57.7$	4	4	0	0	2	$144.8 \le \varphi < 147.7$	4	4	0	0	6
$57.7 \le \varphi < 60.5$	4	5	1	0	2	$147.7 \le \varphi < 150.5$	4	5	1	0	6
$60.5 \le \varphi < 63.3$	4	6	2	0	2	$150.5 \le \varphi < 153.3$	4	6	2	0	6
$63.3 \le \varphi < 66.1$	4	7	3	0	2	$153.3 \le \varphi < 156.1$	4	7	3	0	6
$66.1 \le \varphi < 67.5$	4	7	4	0	2	$156.1 \le \varphi < 157.5$	4	7	4	0	6
$67.5 \le \varphi < 68.9$	4	7	4	0	3	$157.5 \le \varphi < 158.9$	4	7	4	0	7
$68.9 \le \varphi < 71.7$	3	7	4	0	3	$158.9 \le \varphi < 161.7$	3	7	4	0	7
$71.7 \le \varphi < 74.5$	2	6	4	0	3	$161.7 \le \varphi < 164.5$	2	6	4	0	7
$74.5 \le \varphi < 77.3$	1	5	4	0	3	$164.5 \le \varphi < 167.3$	1	5	4	0	7
$77.3 \le \varphi < 80.2$	0	4	4	0	3	$167.3 \le \varphi < 170.2$	0	4	4	0	7
$80.2 \le \varphi < 83.0$	0	4	5	1	3	$170.2 \le \varphi < 173.0$	0	4	5	1	7
$83.0 \le \varphi < 85.8$	0	4	6	2	3	$173.0 \le \varphi < 175.8$	0	4	6	2	7
$85.8 \le \varphi < 88.6$	0	4	7	3	3	$175.8 \le \varphi < 178.6$	0	4	7	3	7
$88.6 \le \varphi < 90.0$	0	4	7	4	3	$178.6 \le \varphi < 180.0$	0	4	7	4	7

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Table 3b. 16-PSK Modulation Phase to Branch Metric Conversion (cont.)

Phase	B00 (OCT)	B01 (OCT)	B11 (OCT)	B10 (OCT)	Sector Number	Phase	B00 (OCT)	B01 (OCT)	B11 (OCT)	B10 (OCT)	Sector Number
$180.0 \le \varphi < 181.4$	0	4	7	4	8	$270.0 \le \varphi < 271.4$	0	4	7	4	12
$181.4 \le \varphi < 184.2$	0	3	7	4	8	$271.4 \le \varphi < 274.2$	0	3	7	4	12
$184.2 \le \varphi < 187.0$	0	2	6	4	8	$274.2 \le \varphi < 277.0$	0	2	6	4	12
$187.0 \le \varphi < 189.8$	0	1	5	4	8	$277.0 \le \varphi < 279.8$	0	1	5	4	12
$189.8 \le \varphi < 192.7$	0	0	4	4	8	$279.8 \le \varphi < 282.7$	0	0	4	4	12
$192.7 \le \varphi < 195.5$	1	0	4	5	8	$282.7 \le \varphi < 285.5$	1	0	4	5	12
$195.5 \le \varphi < 198.3$	2	0	4	6	8	$285.5 \le \varphi < 288.3$	2	0	4	6	12
$198.3 \le \varphi < 201.1$	3	0	4	7	8	$288.3 \le \varphi < 291.1$	3	0	4	7	12
$201.1 \le \varphi < 202.5$	4	0	4	7	8	$291.1 \le \varphi < 292.5$	4	0	4	7	12
$202.5 \le \varphi < 203.9$	4	0	4	7	9	$292.5 \le \varphi < 293.9$	4	0	4	7	13
$203.9 \le \varphi < 206.7$	4	0	3	7	9	$293.9 \le \varphi < 296.7$	4	0	3	7	13
$206.7 \le \varphi < 209.5$	4	0	2	6	9	$296.7 \le \varphi < 299.5$	4	0	2	6	13
$209.5 \le \varphi < 212.3$	4	0	1	5	9	$299.5 \le \varphi < 302.3$	4	0	1	5	13
$212.3 \le \varphi < 215.2$	4	0	0	4	9	$302.3 \le \varphi < 305.2$	4	0	0	4	13
$215.2 \le \varphi < 218.0$	5	1	0	4	9	$305.2 \le \varphi < 308.0$	5	1	0	4	13
$218.0 \le \varphi < 220.8$	6	2	0	4	9	$308.0 \le \varphi < 310.8$	6	2	0	4	13
$220.8 \le \varphi < 223.6$	7	3	0	4	9	$310.8 \le \varphi < 313.6$	7	3	0	4	13
$223.6 \le \varphi < 225.0$	7	4	0	4	9	$313.6 \le \varphi < 315.0$	7	4	0	4	13
$225.0 \le \varphi < 226.4$	7	4	0	4	10	$315.0 \le \varphi < 316.4$	7	4	0	4	14
$226.4 \le \varphi < 229.2$	7	4	0	3	10	$316.4 \le \varphi < 319.2$	7	4	0	3	14
$229.2 \le \varphi < 232.0$	6	4	0	2	10	$319.2 \le \varphi < 322.0$	6	4	0	2	14
$232.0 \le \varphi < 234.8$	5	4	0	1	10	$322.0 \le \varphi < 324.8$	5	4	0	1	14
$234.8 \le \varphi < 237.7$	4	4	0	0	10	$324.8 \le \varphi < 327.7$	4	4	0	0	14
$237.7 \le \varphi < 240.5$	4	5	1	0	10	$327.7 \le \varphi < 330.5$	4	5	1	0	14
$240.5 \le \varphi < 243.3$	4	6	2	0	10	$330.5 \le \varphi < 333.3$	4	6	2	0	14
$243.3 \le \varphi < 246.1$	4	7	3	0	10	$333.3 \le \varphi < 336.1$	4	7	3	0	14
$246.1 \le \varphi < 247.5$	4	7	4	0	10	$336.1 \le \varphi < 337.5$	4	7	4	0	14
$247.5 \le \varphi < 248.9$	4	7	4	0	11	$337.5 \le \varphi < 338.9$	4	7	4	0	15
$248.9 \le \varphi < 251.7$	3	7	4	0	11	$338.9 \le \varphi < 341.7$	3	7	4	0	15
$251.7 \le \varphi < 254.5$	2	6	4	0	11	$341.7 \le \varphi < 344.5$	2	6	4	0	15
$254.5 \le \varphi < 257.3$	1	5	4	0	11	$344.5 \le \varphi < 347.3$	1	5	4	0	15
$257.3 \le \varphi < 260.2$	0	4	4	0	11	$347.3 \le \varphi < 350.2$	0	4	4	0	15
$260.2 \le \varphi < 263.0$	0	4	5	1	11	$350.2 \le \varphi < 353.0$	0	4	5	1	15
$263.0 \le \varphi < 265.8$	0	4	6	2	11	$353.0 \le \varphi < 355.8$	0	4	6	2	15
$265.8 \le \varphi < 268.6$	0	4	7	3	11	$355.8 \le \varphi < 358.6$	0	4	7	3	15
$268.6 \le \varphi < 270.0$	0	4	7	4	11	$358.6 \le \varphi < 360.0$	0	4	7	4	15

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Figure 13. Encoder Output Mapping for 8-PSK Modulation

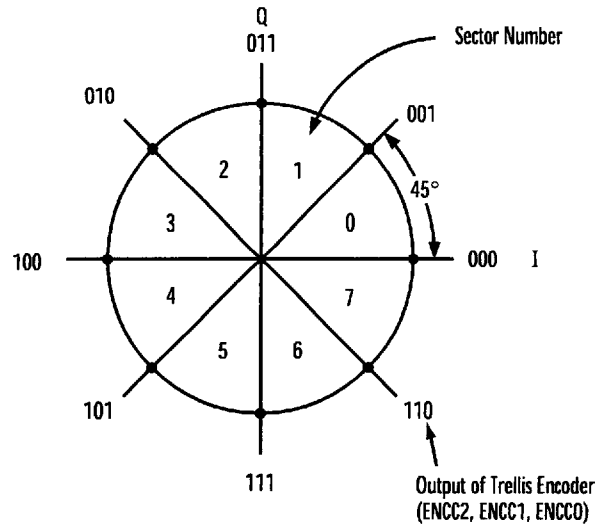
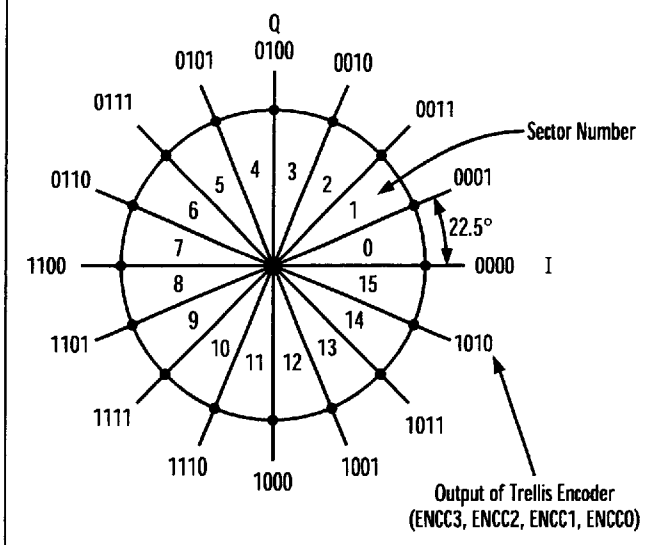


Figure 14. Encoder Output Mapping for 16-PSK Modulation



MEMORY CHAINBACK LENGTH

VITERBI MODE

Full or short chainback path depths can be selected in Viterbi Mode. Full chainback memory operation uses a minimum chainback depth of 96 states while short chainback memory operation uses a minimum chainback depth of 48 states. Near theoretical coding is achieved when either chainback depth is selected for code rates 1/3 or 1/2. However, when operating with code rates higher than rate 1/2 (rates 3/4 or 7/8), full chainback memory should be selected in order to provide maximum coding gain. The chainback depth is selected with bit 0 in the Decoder Control Register 3 (address 04H) of the processor interface.

TRELLIS MODE

Trellis Mode always uses the full chainback memory of a minimum 96 states.

CLOCKING SCHEME

Multiple code rate operation of the Q1900 encoder and decoder functions requires special timing circuits to provide for the various rates of operation.

CODING PERFORMANCE

VITERBI MODE

The coding performance for the Viterbi Mode at different rates (1/3, 1/2, 3/4, 7/8) are shown in Figure 15. A decoding gain of 5.5 dB is achieved when operating at a code rate of 1/3 with decoded BER of 10^{-5} for BPSK or QPSK modulation with soft-decision inputs. The decoding gain is 5.2 dB for the same conditions when operating with rate 1/2 coding.

TRELLIS MODE

The coding performance in Trellis Mode for rates 2/3 and 3/4 is shown in Figure 16. A coding gain of 3.2 dB is achieved for rate 2/3 8-PSK modulation with a decoded BER of 10^{-5}. A coding gain of 3.1 dB is achieved for rate 3/4 16-PSK modulation with a decoded BER of 10^{-5}.

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Figure 15. Viterbi Mode Coding Performance

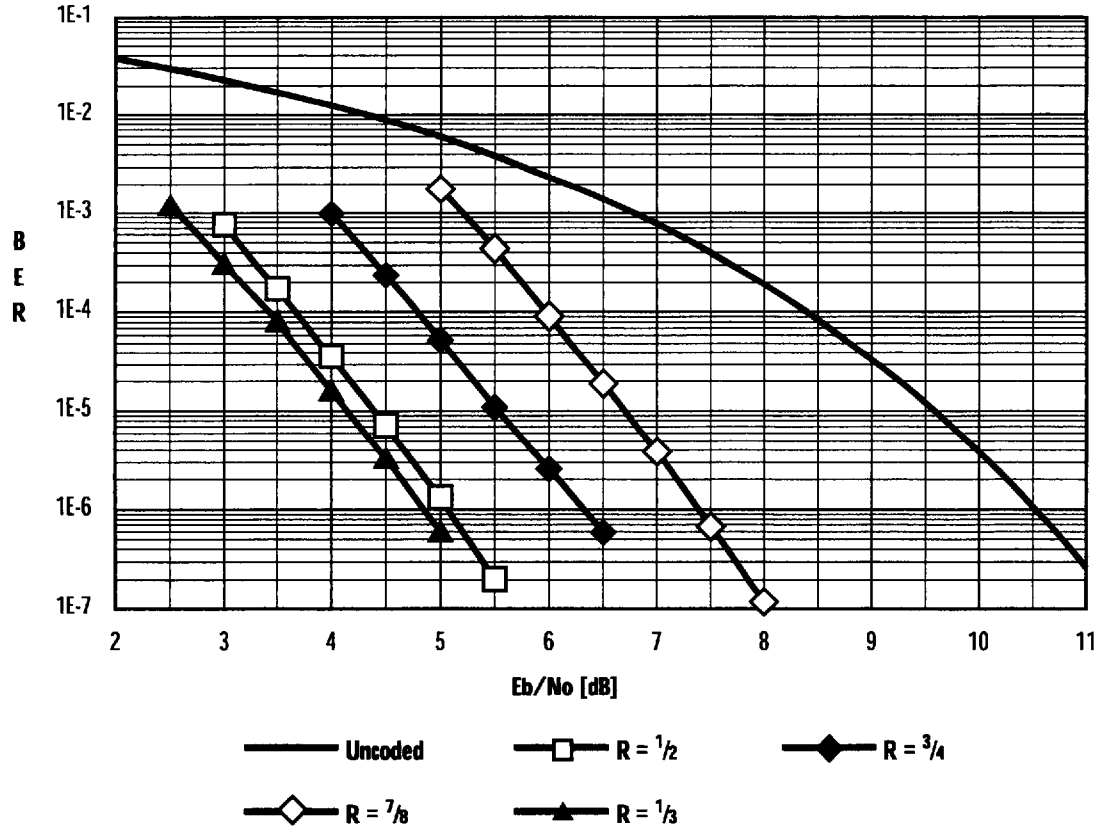
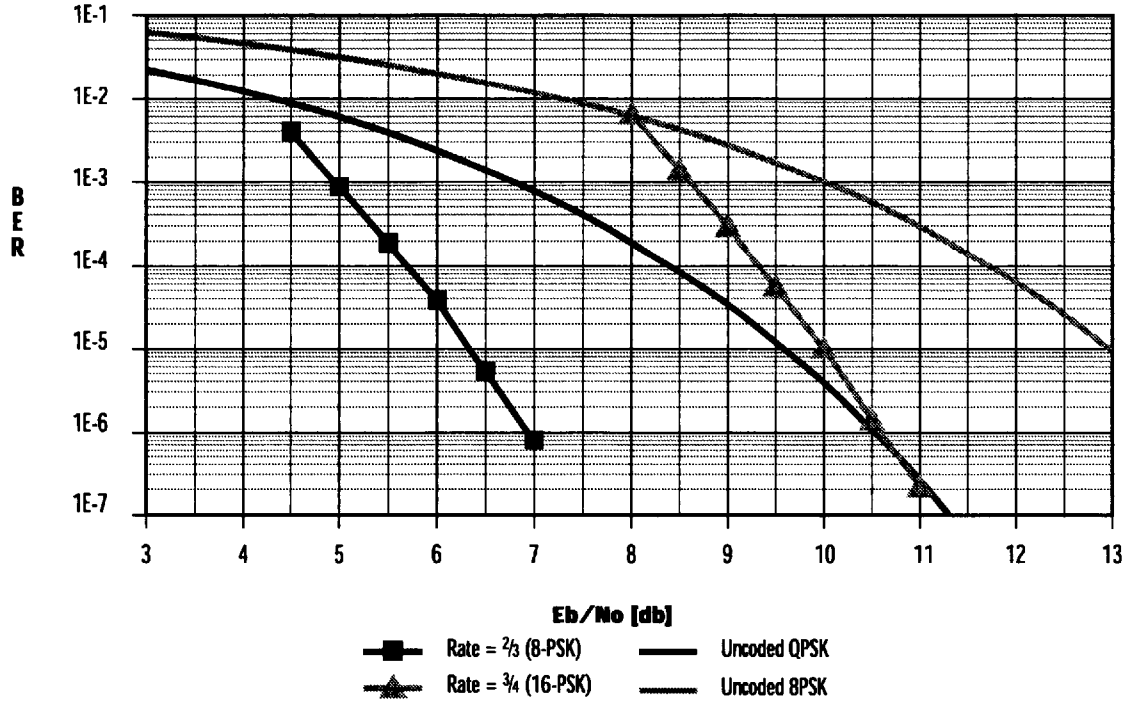


Figure 16. Trellis Mode Coding Performance



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CHANNEL BIT ERROR RATE MONITOR

VITERBI MODE

The Viterbi Mode BER monitor provides a powerful technique to monitor the performance of the Viterbi decoder. The BER works on a re-encode and compare principle, see Figure 17. The decoded data is re-encoded and compared to the delayed transmitted data A'. The BER monitor indicates an error whenever this comparison fails. It also indicates an error when the decoder fails to correct an information bit properly. However, the probability of the decoder incorrectly decoding a bit is at least two orders of magnitude below the probability of a channel bit error. Therefore, the effect of decoder errors on the accuracy of the BER measurement is minimal.

The bit error outputs of the re-encode and compare circuit can be monitored using the on-chip channel BER measurement circuit. See Figure 18. This circuit consists of two accumulators acting as counters. The first accumulator counts decoder input code bits (i.e., code bit count accumulator). The second accumulator counts code bit errors detected by the re-encode and compare circuit (i.e., code bit error accumulator). The valve programmed into the BER Input Registers is the

Figure 17. Re-Encode and Compare Circuit

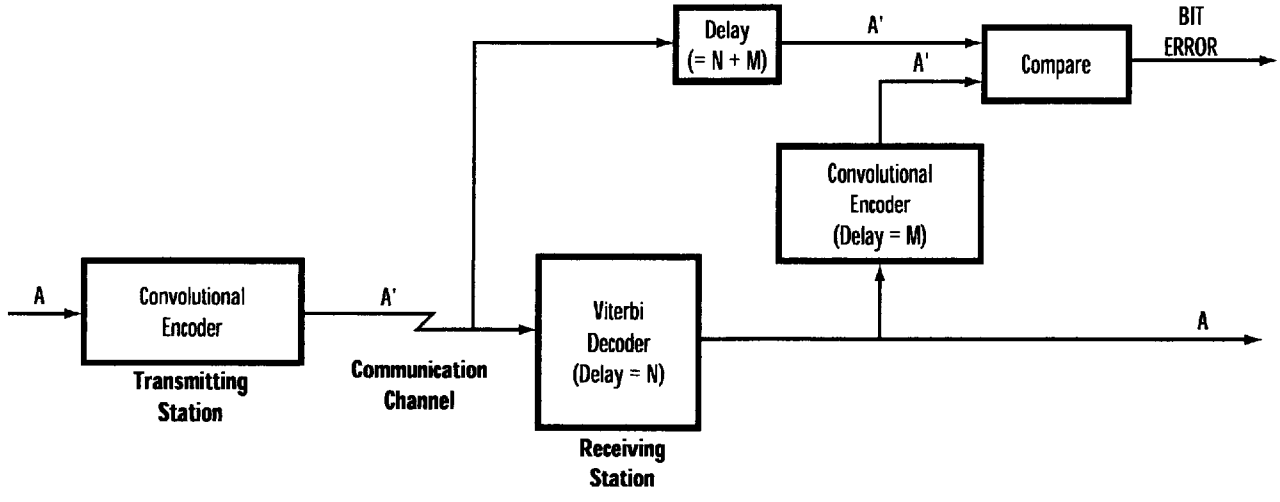
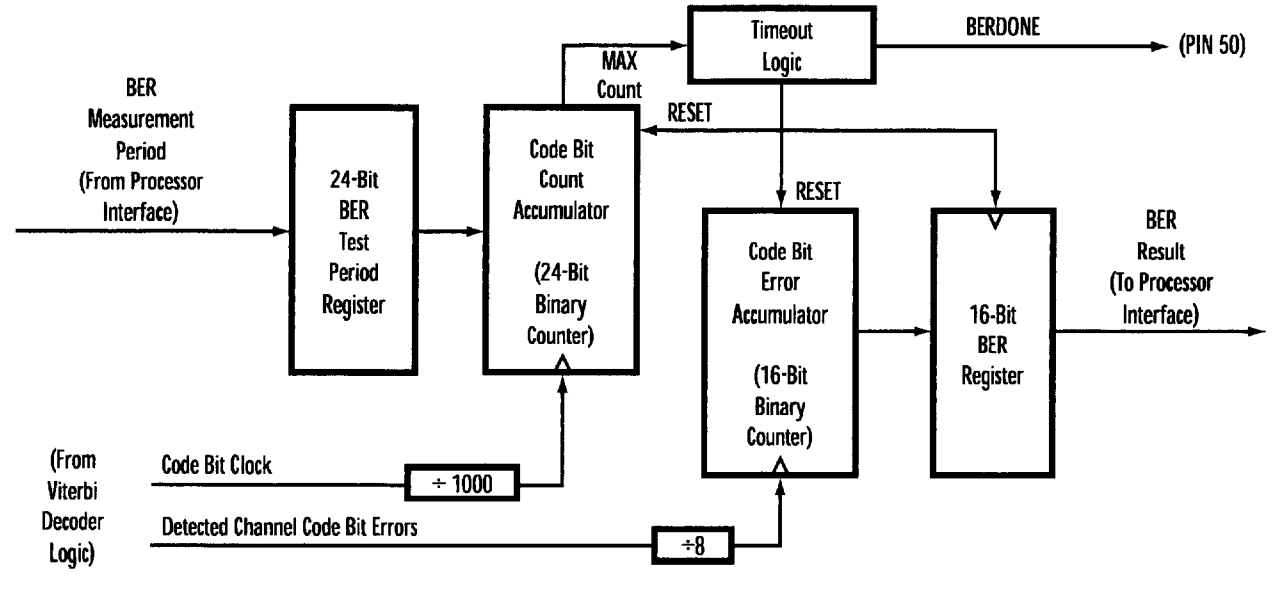


Figure 18. Channel Bit Error Rate Measurement Circuit



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two's complement of the BER Iput Register (Number of Decoder Input Bits/1000). For example if the number of decoder input code bits is 4000, this number is divided by 1000 resulting in 4. The two's complement of 4 is then programmed via the microprocessor interface into the BER Input Registers (write address 0A, 0B and 0CH).

The BER measurement operates whenever the clock signal DECOUTCLK (pin 23 PLCC and pin 39 VTQFP) is active (i.e., toggling). During the BER measurement period, the detected errors are accumulated in the code bit-error accumulator (also called the BER Measurement Output Register). This 16-bit binary accumulator is reset at the beginning of each BER measurement period. Once the 24-bit period of the BER measurement is entered, the loaded value is activated by writing any value to the BER Test Value Enable processor interface port (write address 18 H). The BER measurement is completed when the code bit-count accumulator completes its count. At this point, the number of detected errors recorded in the code bit-error accumulator is transferred to a parallel 16-bit buffer register.

The completion of the BER measurement period is indicated by BERDONE (pin 50 PLCC and pin 72 VTQFP), which goes to logic High for two periods of DECOUTCLK (pin 23 PLCC and pin 39 VTQFP). The BERDONE signal can be used as an interrupt or polled status bit to a controlling processor. The accumulated error value then can be read via the processor interface. The actual measured bit error count is derived by the following formula:

$$\text{Actual Error Count} = (\text{Register Value} - 1) \times 8$$

Where Register Value is the value read from the 16-bit BER measurement register (read address 03 and 04 H). That is, if no errors are recorded, the BER measurement register will have a value of "1" stored. If the number of errors exceeds the limit of the 16-bit register, the BER measurement will read as "0000H". The BER test continues running and stores the next test value in the 16-bit BER measurement register upon completion of each test.

The BER is computed by dividing the measured BER value by the number of bits in the test. This measurement division is facilitated if the measurement period is a power of 10, such as 10,000 or 100,000 code bits long. In this case, the binary number recorded by the error accumulator is the mantissa of the symbol BER, and the exponent of the BER value is determined by the measurement period. For example, if the test period is set to 100,000 (= 10^5) bits and 250 errors are recorded during the measurement period, the measured BER is 2.5 x 10-3.

In the event that more than 2^{19} errors are recorded in the measurement period, the code bit error accumulator saturates at an "all-zeros" value. If this condition is indicated at the completion of a BER measurement, the period of the measurement should be reduced until a value less than saturation is recorded.

For an accurate measurement of the BER, at least 100 errors should be detected within a given test period. If fewer than 100 errors are recorded, the statistical variance of such a measurement will be high. In this case, the measurement period should be increased until more than 100 errors are detected during the BER test.

The on-chip BER monitor can be used for measurements other than simply the BER. For example, by setting the measurement period to the output bit rate (output bits per second), the test period becomes equal to exactly one second in time. The BER monitor, therefore, becomes a straightforward means for monitoring error-free seconds, which is frequently a useful error statistic. If no errors are recorded during the one second period, this is an error free second. External hardware or software can record the percentage of error-free seconds for error statistics purposes.

TRELLIS MODE

Trellis Mode does not support a BER monitor.

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NORMALIZATION RATE MONITOR OPERATION (SYNCHRONIZATION STATUS MONITOR)

The normalization rate monitor is used during synchronization (phase ambiguity resolution) and during normal operation to monitor the performance of the decoder.

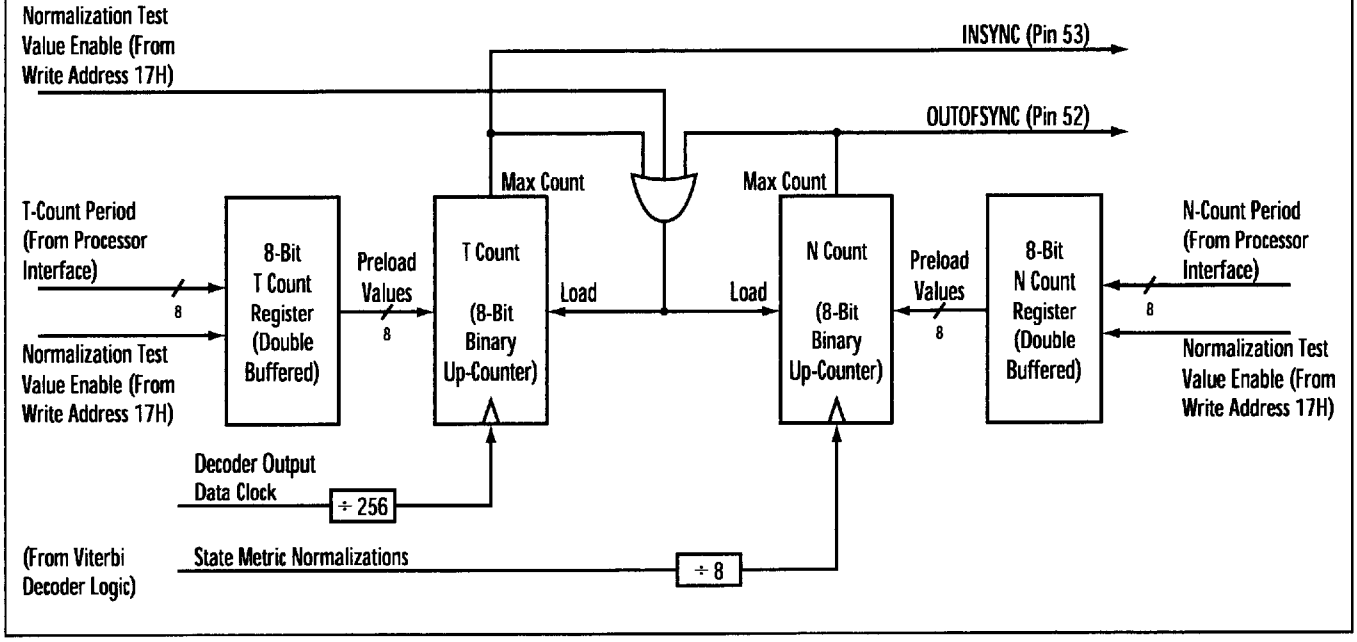
The system designer determines an acceptable normalization rate threshold and programs this threshold into the Q1900. The designer controls both the period of time in which the metric normalization is monitored and the number of normalizations allowed during that time. These two numbers, that provide for more than 65,000 possible settings, are programmed into the device using the microprocessor interface. If the threshold is not exceeded during any test period, a signal (INSYNC) indicates that the decoder is synchronized. If the threshold is exceeded during any test period, a signal (OUTOFSYNC) indicates the detected loss of synchronization. In many systems, this signal can be used with an external D flip-flop divider to provide a correction signal to a synchronization control input pin (SYNCCHNG). In this configuration, the decoder will attempt to correct the out of synchronization state by changing the synchronization state of the decoder. This technique provides a complete self-synchronizing decoder function for a variety of communication systems.

The on-chip normalization circuit, see Figure 19, consists of two accumulators acting as counters. The system designer controls the periods of these two counters. The first counter (T) measures the number of decoded bits. The second counter (N) measures the number of state metric normalizations. The normalization rate threshold is determined by taking the ratio of the count of normalizations (the N counter) and the time period (the T counter). Each 8-bit-wide binary counter is pre-loaded using the processor interface registers. Both the N and T counters are loaded with binary values that are the two's complements of the actual count value. The count value loaded into the T counter is multiplied by 256 to determine the actual number of decoded bits in the normalization test period. That is:

$$t = 256 * T$$

Where "t" is the actual number of decoded bits counted and "T" is the two's complement value of the 8-bit number loaded into the T counter (write address 08 H).

Figure 19. Normalization Rate Monitor Circuit



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The actual count of the N counter is determined by the following formula:

$$n = (N-1) * 8 + 4$$

Where "n" is the actual number of normalizations allowed, and "N" is the two's complement value of the 8-bit number loaded into the N counter (write address 09 H). With this programming capability, the system designer selects the normalization rate threshold for determining an in-sync or out-of-sync condition, as well as the period of the measurement.

VITERBI MODE EXAMPLE

When operating with rate ½ decoding, a normalization rate threshold of about 10% reliably detects a loss of synchronization.

To avoid false detection of synchronization loss due to a noise burst, the normalization measurement should detect at least 20-30 normalizations before declaring a loss of synchronization. For example, the system designer may specify 50 as the number of normalizations to be detected. By loading the 8-bit two's complement value of seven (i.e., F9 H) into the N counter register, the actual number of normalizations allowed in a test period without indicating a loss of synchronization would be:

$$(7 - 1) * 8 + 4 = 52$$

The value for the T counter must be approximately ten times the value in the N counter. Loading the T counter with the two's complement value of 2 (i.e., FE H) the actual count value for T counter will be:

$$(2 * 256) = 512$$

Therefore, the actual normalization rate threshold will be:

$$^{52}/_{512} = 10.2\%$$

This is an appropriate threshold for reliable synchronization when operating with rate ½ coding.

The threshold should be set to approximately 1.7% for rate ¾ coding and 0.8% for rate ⅞ coding. For rate ¾, programming the N counter to 7 (i.e., F9 H) and the T counter to 12 (i.e., F4 H) will give the desired normalization rate of 1.7%. Likewise, for rate ⅞, programming the N counter to 8 (i.e., F8 H) and the T counter to 29 (i.e., E3 H) will give the desired normalization rate of 0.8%.

TRELLIS MODE EXAMPLE

When operating with rate ⅔ 8-PSK or rate ¾ 16-PSK decoding, a normalization rate threshold of approximately 14% will reliably detect a loss of synchronization.

To avoid false detection of synchronization loss due to a noise burst, the normalization measurement should detect at least 20 to 30 normalizations before declaring a loss of synchronization. For example, the system designer may specify 108 as the number of normalizations to be detected. By loading the 8-bit, two's complement value of 14 (i.e., F2H) into the N counter register, the actual number of normalizations allowed in a test period without indicating a loss of synchronization would be:

$$(14 - 1) * 8 + 4 = 108$$

The value for the T counter must be approximately 7 times (1/0.14) the value in the N counter. Loading the Tcounter with the two's complement value of 3) (i.e., FDH), the actual count value for T will be:

$$(3 * 256) = 768$$

The actual normalization rate threshold will be $^{108}/_{768} = 14\%$. This is an appropriate threshold for reliable synchronization when operating with rate ⅔ and rate ¾ coding.

PHASE AMBIGUITY RESOLUTION

In a Phase Shift Keying (PSK) communication system, the received phase can be phase rotated from the transmitted phase. Table 4 gives the possible phase rotations for the following modulation types: BPSK, QPSK, 8-PSK and 16-PSK.

The Q1900 provides two methods for resolving the phase shifts between the transmitter and the receiver, differential encoding and phase ambiguity resolution. Table 4 specifies which phases are resolved with the two methods. Differential encoding is described in the

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Table 4. Modulation Type vs. Phase Shift

Modulation Type	Possible Phase Shifts	Resolved by Differential Encoders	Resolved by Phase Ambiguity
BPSK	0°, 180°	0°, 180°	—
QPSK	0°, 90°, 180°, 270°	0°, 180°	90°, 270°
8-PSK	0°, 45°, 90°, 135°, 180°, 225°, 270°, 315°	0°, 90°, 180°, 270°	45°, 135°, 225°, 315°
16-PSK	0°, 22.5°, 45°, 67.5°, 90°, 112.5°, 135°, 157.5°, 180°,202.5°, 225°, 247.5°, 270°, 292.5°, 315°, 337.5°	0°, 45°, 90°, 135°, 180°, 225°, 270°, 315°	22.5°, 67.5°, 112.5°, 157.5°, 202.5°, 247.5°, 292.5°, 337.5°

Theory of Operation section.

The phase ambiguity function uses the normalization rate monitor to determine if the decoder is out of phase synchronization. When the normalization rate threshold (number of normalizations/number of decoded bits) is exceeded, an out-of-sync pulse is output to pin 52 PLCC or pin 74 VTQFP (OUTOFSYNC). The effects of the out-of-sync condition can be compensated for either by a timing alignment or by a permutation of the decoder input data.

VITERBI MODE

For the standard Viterbi Mode, the Q1900 can be configured for automatic synchronization by using the OUTOFSYNC signal along with an external D-flip-flop divider as an input to the SYNCCHNG pin. In this configuration, the decoder attempts to correct the out of synchronization state by changing the synchronization state of the decoder.

The standard Viterbi synchronization modes are described in the *Modes of Operation* section.

TRELLIS MODE

For the Trellis Mode, the Q1900 can be configured for automatic synchronization by using the OUTOFSYNC signal along with an external D-flip-flop to drive the address line of the external branch metric PROMs. When the OUTOFSYNC is Low nothing happens. That is, B00 = B00, B01 = B01, B11 = B11, B10 = B10 and SN = SN. When the OUTOFSYNC is High, then B00 = B01, B01 = B11, B11 = B10, B10 = B00, and SN = (SN + 1) MOD7 (i.e. 0 = 1, 1 = 2, ..7 = 0). Figure 20 shows how the branch metrics are rotated and Figure 21 shows how the sector number (SN) is rotated.

INPUT DATA FORMATS

VITERBI MODE

The Viterbi Mode has two input formats: 3-bit soft decision and 1-bit hard decision. As seen in Figure 22, the Viterbi decoder provides the highest coding gain when using soft decision inputs.

The 3-bit soft decision values can be input to the Q1900 decoder inputs (R0, R1, and R2) in either sign-magnitude or offset-binary notation. The encoding of soft decision values for each of these two formats is given in Table 24D, Decoder Control Register 2. The selection of the input format is made via the microprocessor interface.

Figure 20. Branch Metric Rotation

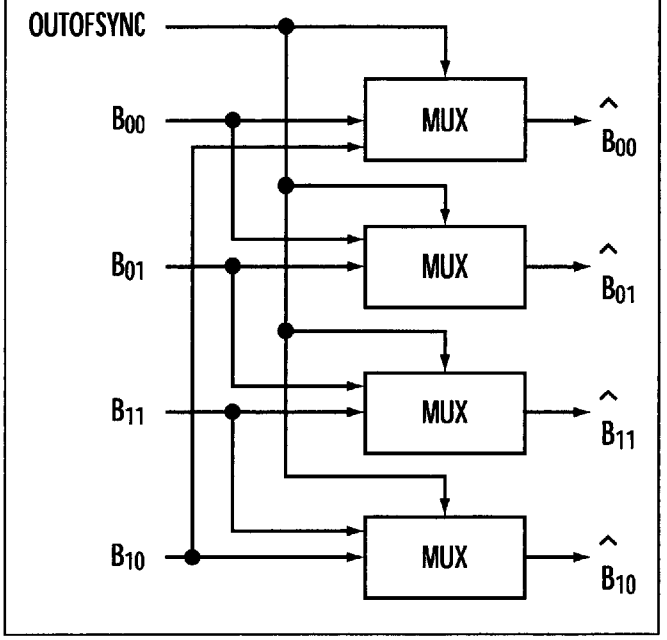

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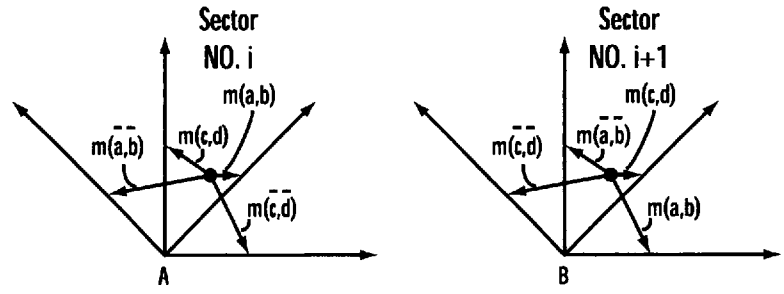
Figure 21. Sector Number Rotation



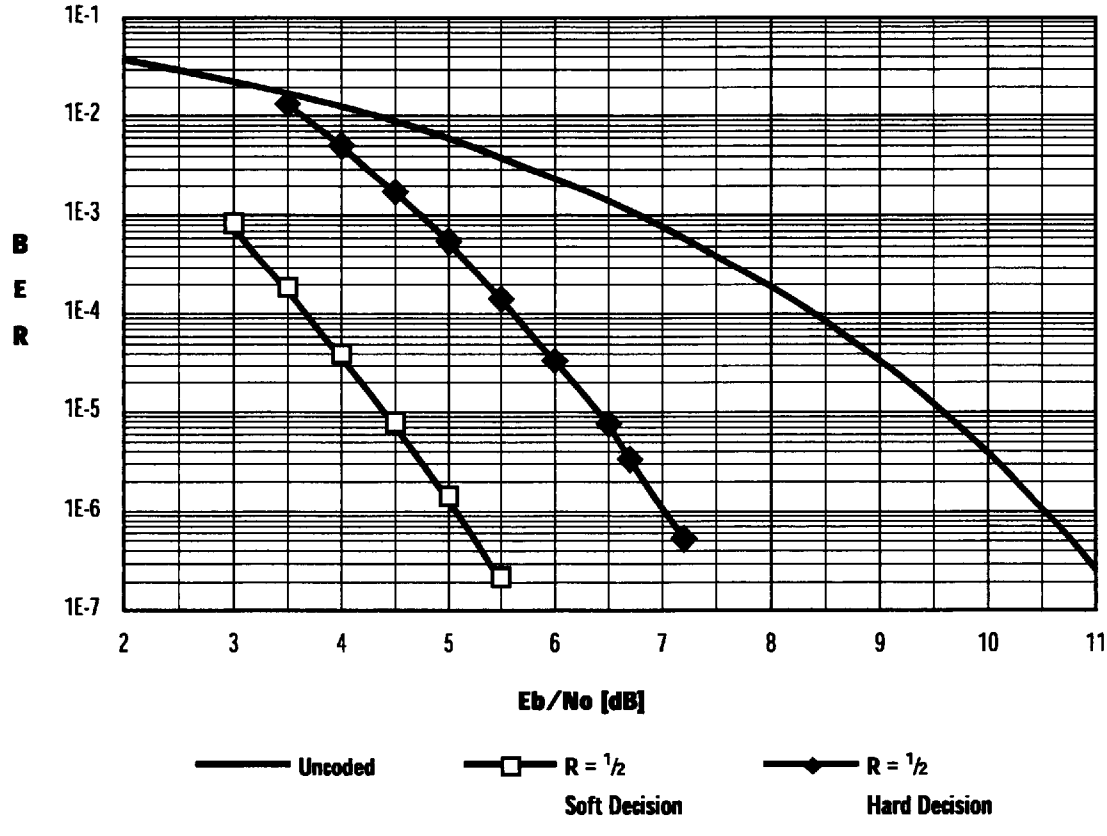
When using the Q1900 Viterbi decoder with hard decision (single-bit) values for R0, R1, and R2, the decoder input format should be set to sign-magnitude notation. The Rx[0] "magnitude" bits (R0[0], R1[0], and R2[0]) should be set to logic "1" (High). The Rx[1] "magnitude" bits (R0[1], R1[1], and R2[1]) should be set to logic "0" (Low).

The hard decision code bits should be input on the "sign" signal pins (R0[2], R1[2], and R2[2]) as appropriate.

TRELLIS MODE

The Trellis Mode has one type of input format, four 3-bit branch metrics and one 3-bit sector number. The branch metric and sector number are derived from the received symbol (phase angle) as shown in Table 2 for 8-PSK and Tables 3a and 3b for 16-PSK.

Figure 22. Hard Decision vs. Soft Decision Code Performance



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RESET CIRCUIT OPERATION

VITERBI MODE AND TRELLIS MODE

The Q1900 encoder and decoder functions have individual resets. A reset operation should be performed after the encoder or decoder is initially configured and when a change occurs in the mode of operation.

The reset operation can be performed using either the external input pins DECRESET (pin 13 PLCC or pin 27 VTQFP) and ENCRESET (pin 37 PLCC or pin 55 VTQFP) or reset bits in control registers of the processor interface. The operation of external input pins and processor controlled bits is identical. The encoder and decoder input clocks MUST be in operation PRIOR to reset.

When an encoder or decoder reset is asserted, either by setting the input pin to logic High or setting the processor interface bit to "1", the reset is latched synchronously into the Q1900. The reset operation is edge-triggered. The reset occurs during the first clock period after the reset line is asserted. Continuing to hold the reset line or bit to the logic High or "1" condition does not cause a continuous reset.

Resetting the encoder resets all the states of the convolutional encoder to logic "0". Resetting the decoder resets the internal states of the Viterbi puncture logic, the Viterbi and Trellis phase ambiguity logic and the Viterbi and Trellis synchronization logic. However, it does not set the internal states of the path memory to a fixed value. To initialize the decoder path memory, the decoder must be flushed with 183 zeros.

DEVICE THROUGHPUT DELAY

VITERBI MODE

The delay through the convolutional encoder or decoder functions depends on the mode and rate of operation. The only modes with fixed non-variable throughput delays are parallel rate ½ and rate ⅓.

The throughput delay through the encoder for rates ½ and ⅓ parallel operation is 10 ½ periods of ENCOUTCLK. The throughput delay through the decoder for rate ½ and ⅓ parallel operation is 102 ½ periods of DECOUTCLK for Short Memory Mode and 182 ½ periods of DECOUTCLK for Long Memory Mode.

The throughput delay through the decoder for rate ½ and ⅓ serial operation varies from the parallel modes by ± four clock period of DECOUTCLK. The variance is caused by the phasing of DECINCLK and the DECOUTCLK and the location of the RESET signal. If a fixed throughput delay is required for serial input data, two options exist. The first option is to use a serial-to-parallel converter and operate the Q1900 in Parallel Mode. The second option is to use external logic to reset the decoder and operate the Q1900 in Serial Mode. The external reset logic must guarantee that every time the reset occurs the phasing of the DECINCLK and DECOUTCLK is identical.

The throughput delay through the decoder for rate ¾ and rate ⅞ parallel operation varies from the Parallel Short and Long Memory Modes by ± four clock period of DECOUTCLK. This variance is caused by the Puncture Mode synchronization logic. Therefore, if a fixed throughput delay is required for rates ¾ and ⅞, external synchronization logic must be used.

TRELLIS MODE

When operating with either rate ⅔ 8-PSK coding or rate ¾ 16-PSK coding, the throughput delay of the encoder is 10 ½ periods of the ENCINCLK clock. The throughput delay of the decoder is 182 ½ periods of the DECINCLK clock.

DIRECT VS. PERIPHERAL DATA MODE

There are two interface modes for the Q1900, Direct Data Mode and Peripheral Data Mode. Direct Data Mode interfaces with all data via the dedicated pins. This mode is most commonly used with synchronous data channels. Peripheral Data Mode interfaces with all data signals via processor interface registers. This mode is most commonly used with asynchronous data channels.

When operating in Peripheral Data Mode, the Q1900 signals are provided by writing to the preprocessor register addresses described in Table 5 for Viterbi Mode and Table 6 for Trellis Mode. All the pins should be connected to logic "0". Direct or Peripheral Data Mode is selected by setting bit 3 in both Encoder Control

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Register 2 and Decoder Control Register 2 of the processor interface (0 = Direct, 1 = Peripheral). Peripheral operation is described in the *Peripheral Applications Note* section.

Table 5. Signal Register Address for Viterbi Mode

VITERBI SIGNALS	REGISTER ADDRESS DEC	REGISTER ADDRESS HEX	DATA BITS	DIRECT DATA PINS PLCC	DIRECT DATA PINS VTQFP
ENCINDATIN	05	05	0	33	51
ENCINCLK	17	11	0-7	36	54
ENCOUTCLK	18	12	0-7	44	66
ENCRESET	06	06	1	37	55
R0	00	00	4-6	18, 26, 29	32, 44, 47
R1	00	00	0-2	17, 22, 28	31, 38, 46
R2	01	01	4-6	16, 19, 27	30, 33, 45
R0ERASE	00	00	7	32	50
R1ERASE	00	00	3	31	49
R2ERASE	01	01	7	30	48
DECINCLK	14	0E	0-7	11	25
DECOUTCLK	15	0F	0-7	23	39
DECRESET	04	04	2	13	27

Table 6. Signal Register Address for Trellis Mode

TRELLIS SIGNALS	REGISTER ADDRESS DEC	REGISTER ADDRESS HEX	DATA BITS	DIRECT DATA PINS PLCC	DIRECT DATA PINS VTQFP
ENCDAT [0,1,2]	05	05	0-2	33, 34, 35	51, 52, 53
ENCINCLK	17	11	0-7	36	54
ENCOUTCLK	18	12	0-7	44	66
ENCRESET	06	06	1	37	55
BM00	00	00	0, 4	27, 28, 29	45, 46, 47
	01	01	4		
BM01	00	00	1, 5	16, 17, 18	30, 31, 32
	01	01	5		
BM10	00	00	2, 6	19, 22, 26	33, 38, 44
	01	01	6		
BM11	00	00	3, 7	30, 31, 32	48, 49, 50
	01	01	7		
SECTOR [0-3]	01	01	0-3	7, 8, 9, 10	21, 22, 23, 24
DECINCLK	14	0E	0-7	11	25
DECOUTCLK	15	0F	0-7	23	39
DECRESET	04	04	2	13	27

MODES OF OPERATION

The Q1900 can be operated in Serial or Parallel Mode with various data rates for each mode. Parallel and Serial Modes are shown in Figures 23 and 24 respectively. Viterbi Mode supports rate ½ serial, rate ½ parallel, rate ⅓ serial, rate ⅓ parallel, rate ¾ parallel and rate ⅞ parallel. Trellis Mode supports rate ⅔ parallel 8-PSK and rate ¾ parallel 16-PSK.

PARALLEL VS SERIAL DATA MODES

For each code rate R, the Q1900 encoder function outputs 1/R encoded bits for each input information bit. For instance, two encoded output bits are generated for each information bit when operating with code rate ½. As described below, these encoded bits can be output in either parallel or serial fashion.

In Parallel Mode, data is output on parallel output pins. The input data rate is the same as the output data rate. In Serial Mode, data is output on one output pin

Figure 23. Parallel Data Mode

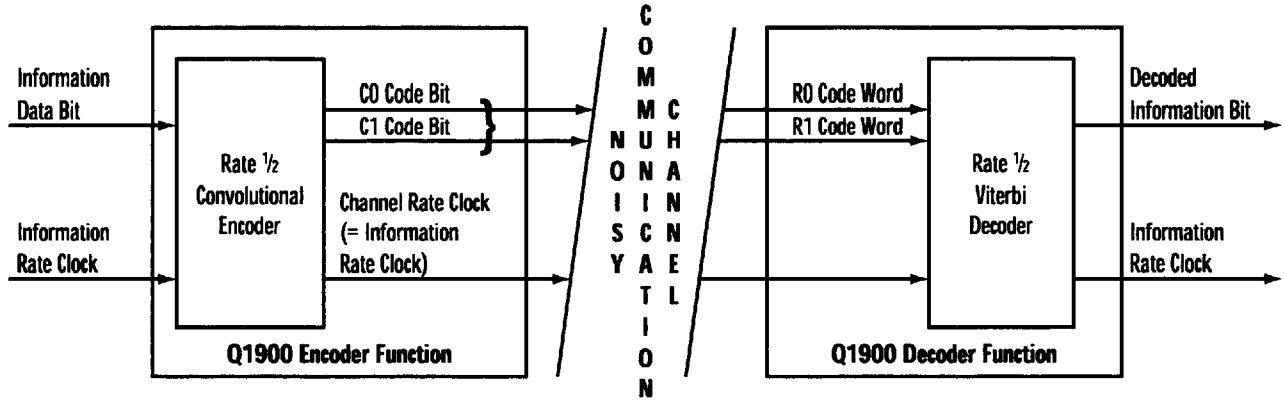

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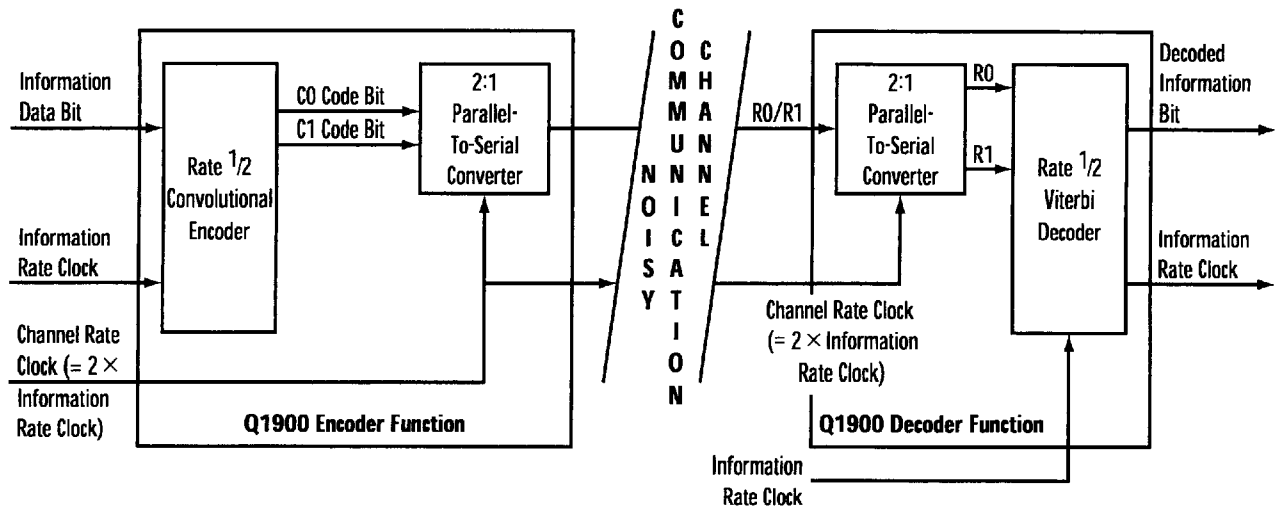
Figure 24. Serial Data Mode



in a serial manner. The input data rate is ½ or ⅓ the output data rate. To accommodate for both Parallel and Serial Output Mode, two clocks must be provided to the encoder during each period. The first clock is used to input information bits on the ENCDATIN pin, and the second clock is used to output data on the C0 pin (Serial Mode) or on the C0, C1 and C2 pins (Parallel Mode).

The ratio between the frequency of the input information clock and output encoded bit clock changes with changing code rate. The clocking schemes for the different Parallel and Serial Modes are described below.

The following sections also describe how to initialize and configure the Q1900 for the different rates of operation. The Q1900 supports various user-selected operation functions and modes in addition to the rate selection. The selection of these functions is made via the processor control registers. A detailed description of the processor register is presented in the *Technical Specification* section. Table 7 shows the Viterbi rates of operation and the synchronization parameters.

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Table 7. Viterbi Modes of Operation

MODE PARAMETERS			CONTROL REGISTER BITS								NOTE REFERENCES	
Code Rate	Format	Modulation	Rate 1/2	Rate 1/3	Rate 3/4	Rate 7/8	Serial Enable	OQPSK	Phase Sync	Swap Erase	Int Sync Method	Erase Bit Sync
1/2	Serial	BPSK	1	0	0	0	1	–	–	0	1	N/A
1/2	Parallel	QPSK	1	0	0	0	0	0	0	0	2	A
			1	0	0	0	0	0	0	1	2	B
			1	0	0	0	0	0	1	0	3	A
			1	0	0	0	0	0	1	1	3	B
1/2	Parallel	OQPSK	1	0	0	0	0	1	0	0	4	A
			1	0	0	0	0	1	0	1	4	C
			1	0	0	0	0	1	1	0	5	A
			1	0	0	0	0	1	1	1	5	C
1/3	Serial	BPSK	0	1	0	0	1	–	–	0	1	N/A
1/3	Parallel	–	0	1	0	0	0	–	–	0	6	N/A
3/4	Parallel	QPSK	0	0	1	0	0	0	0	0	7	A
			0	0	1	0	0	0	0	1	7	B
			0	0	1	0	0	0	1	0	3	A
			0	0	1	0	0	0	1	1	3	B
3/4	Parallel	OQPSK	0	0	1	0	0	1	0	0	8	A
			0	0	1	0	0	1	0	1	8	C
			0	0	1	0	0	1	1	0	5	A
			0	0	1	0	0	1	1	1	5	C
7/8	Parallel	QPSK	0	0	0	1	0	0	0	0	7	A
			0	0	0	1	0	0	0	1	7	B
			0	0	0	1	0	0	1	0	3	A
			0	0	0	1	0	0	1	1	3	B
7/8	Parallel	OQPSK	0	0	0	1	0	1	0	0	8	A
			0	0	0	1	0	1	0	1	8	C
			0	0	0	1	0	1	1	0	5	A
			0	0	0	1	0	1	1	1	5	C

Notes: Internal Synchronization Methods

1. Shifts input grouping pattern by one code word.
2. Edge actuation of SYNCCHNG signal toggles between alternate decoder input mapping states:
   State 1: $R0_N$ –> $R0_N$, $R1_N$ –> $R1_N$
   State 2: $R0_N$ –> $R1_N$/, $R1_N$ –> $R0_N$
3. Level activation of SYNCCHNG signal forces one of two decoder input mapping states:
   State 1 (SYNCCHNG = 1): $R0_N$ –> $R0_N$, $R1_N$ –> $R1_N$
   State 2 (SYNCCHNG = 0): $R0_N$ –> $R1_N$/, $R1_N$ –> $R0_N$
4. Edge actuation of SYNCCHNG signal toggles one of two decoder input mapping states:
   State 1: $R0_N$ –> $R0_N$, $R1_N$ –> $R1_N$
   State 2: $R0_N$ –> $R1_{N-1}$, $R1_N$ –> $R0_N$
5. Level actuation of SYNCCHNG signal forces one of two decoder input mapping states:
   State 1 (SYNCCHNG = 1): $R0_N$ –> $R0_N$, $R1_N$ –> $R1_N$
   State 2 (SYNCCHNG = 0): $R0_N$ –> $R1_N$/, $R1_{N-1}$ –> $R0_N$
6. No internal synchronization control is provided; SYNCCHNG signal should be tied to logic 0.
7. Edge actuation of SYNCCHNG performs the same operation as synchronization method 2. In addition, the puncture code pattern is shifted by one state every other activation of SYNCCHNG.
8. Edge actuation of SYNCCHNG performs the same operation as synchronization method 4. In addition, the puncture code pattern is shifted by one state every other activation of SYNCCHNG.

Erase Bit Synchronization

A. R0ERASE and R1ERASE inputs follow R0 and R1 data signal synchronization methods.
B. R0ERASE and R1ERASE inputs do not follow R0 and R1 data signal synchronization methods.
C. R0ERASE input is not affected by synchronization methods. R1ERASE is delayed by one input code word when in synchronization state 2.

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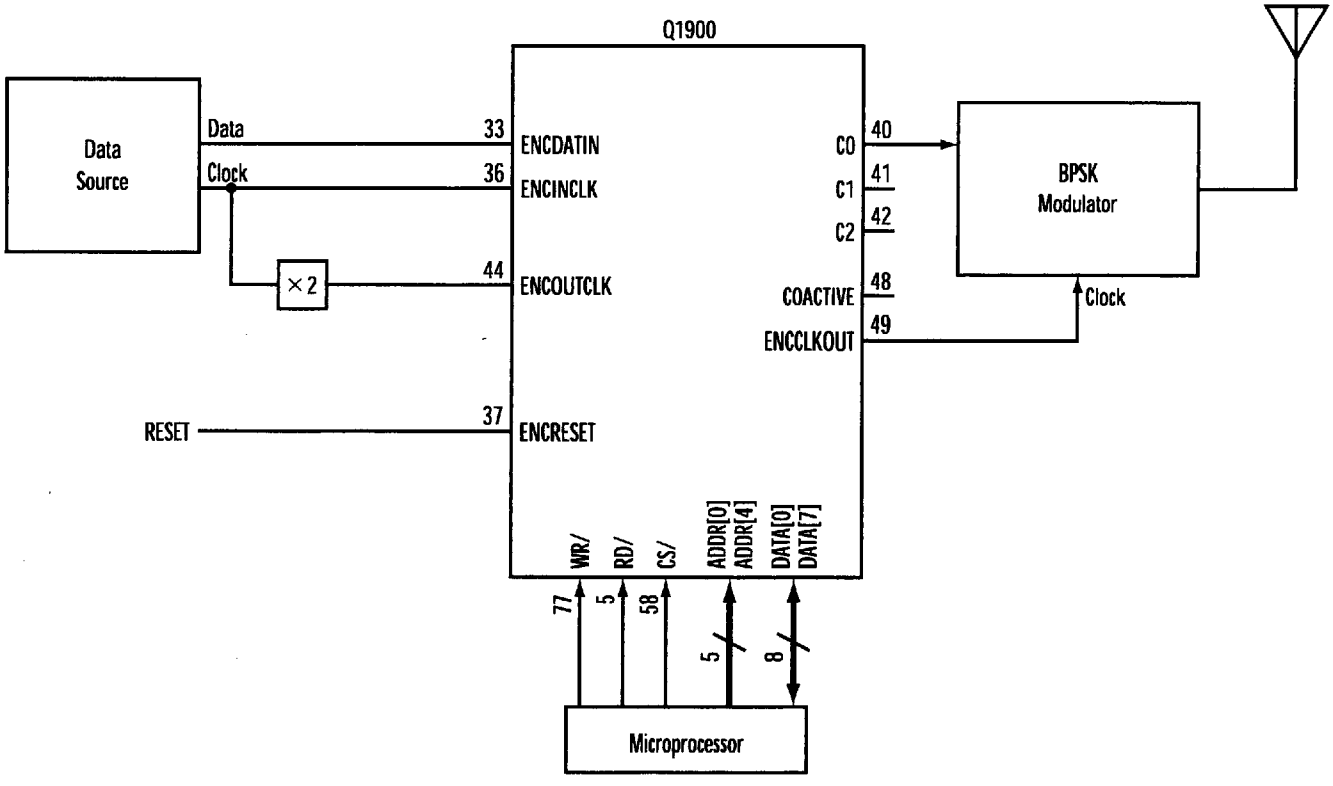
RATE ½ SERIAL VITERBI OPERATION

When operating with code rate ½ in Serial Data Mode, two encoded bits (C0 and C1) are generated by the encoder for every information bit. These encoded bits are serially output from the C0 pin at two times the frequency of the input information. Likewise, two coded words (R0 and R1) are serially input into the decoder for every information bit output from the decoder. These coded words are input into the decoder through the R0 input.

When operating with rate ½ coding in Serial Input Data Mode, the Q1900 decoder does not adjust for phase ambiguities, but simply the grouping of the input serial words. That is, since the two code words are input one at a time, the decoder must group the code words prior to the decoding process. The input word can be grouped or paired in one of two ways. Only one pairing sequence is correct, pairing the R0 input code word with the next input code word R1. However, if the decoder is not provided with explicit information as to which input is the R0 code word (i.e., if the optional signal R0ACTIVE/ is not used), the decoder may incorrectly group the R1 code word with the next input, which would be the R0 code word from the next symbol. In this case, the automatic synchronization circuit will detect the incorrect alignment, and the assertion of the SYNCCHNG signal will adjust the input stream by stopping the input grouping circuit for a single period of the DECINCLK signal. This will result in the correct pairing of code words. This technique requires that the C0 code word for a given encoded symbol always be transmitted immediately prior to the C1 code word of the same symbol.

A typical configuration of the Q1900 encoder operating in rate ½ Serial Mode is shown in Figure 25. Data is clocked into the encoder on the rising edge of ENCINCLK. ENCOUTCLK should be twice the frequency of ENCINCLK. Data is clocked out of the

Figure 25. Rate ½ Viterbi Serial Mode Encoder Example for 84-pin PLCC* Package



*Configuration for 100-pin VTQFP Package is the Same Except for Pin Numbers

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encoder on the rising edge of ENCCLKOUT which is the same frequency as ENCOUTCLK. An example of the decoder operating in rate ½ Serial Mode is shown in Figure 26. The demodulator output is quantized by a 3-bit Analog-to-Digital Converter (ADC) to generate the R0 soft decision input which is clocked into the decoder on the rising edge of DECINCLK. In this configuration, DECOUTCLK is one-half the frequency of DECINCLK. Decoded data is clocked out of the decoder on the rising edge of DECCLKOUT which is the same frequency as DECOUTCLK. In most cases, the DECCLKOUT signal should be used to clock the decoded data into subsequent processing stages.

The Q1900 is programmed for rate ½ Serial Mode operation by writing to the processor interface. An example initialization is shown in Table 8.

Figure 26. Rate ½ Serial Viterbi Mode Decoder Example for 84-pin PLCC* Package

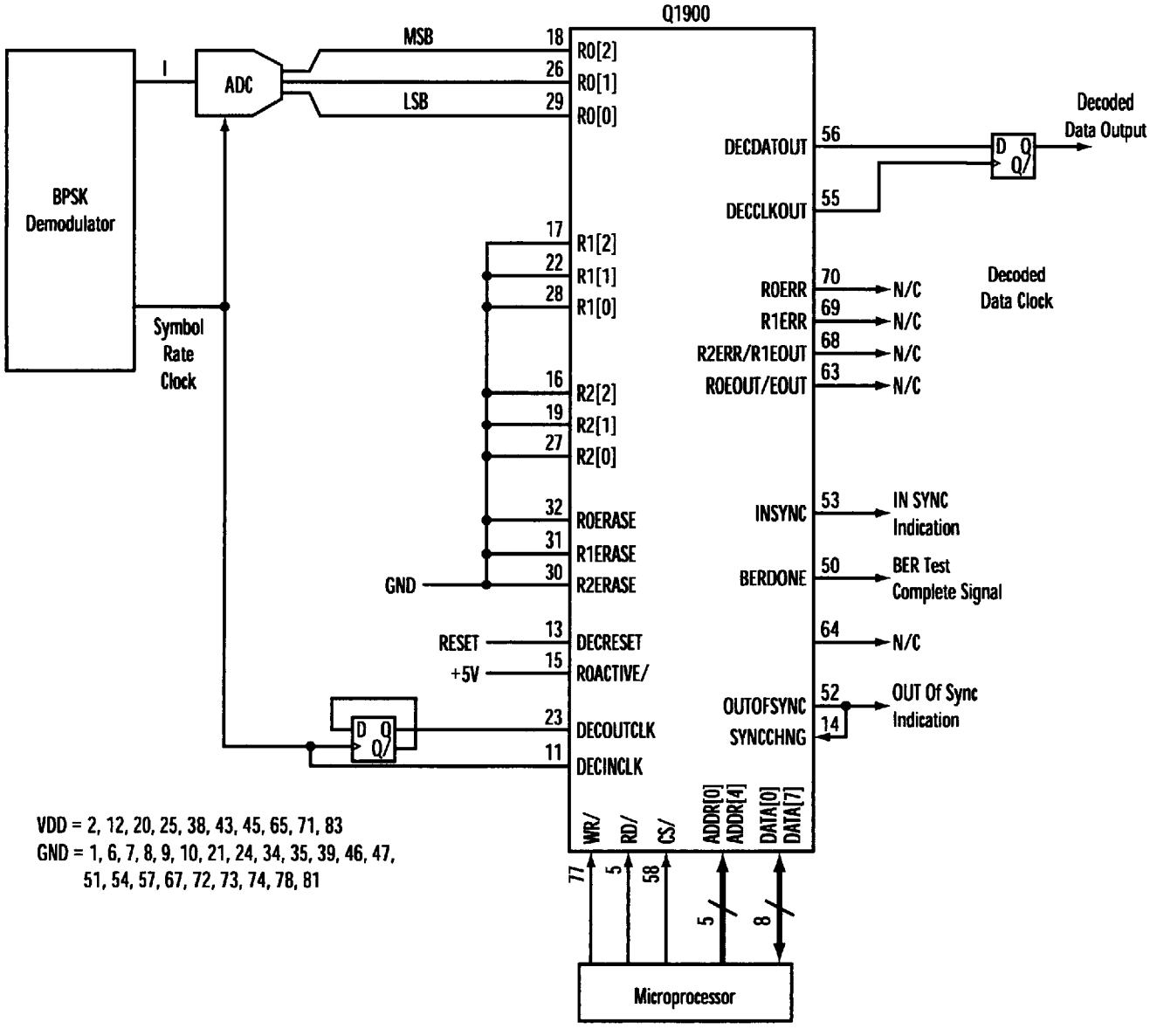

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Table 8. Rate 1/2 Serial Viterbi Mode Initialization Example

STEP	REGISTER NAME	ADDRESS	VALUE	COMMENTS
1	Reserved Register	15H	00H	Reserved Registers Must Be Set to 0 for Correct Operation
2	Reserved Register	16H	00H	
3	Decoder Control Register 1	02H	05H	Serial Mode, BPSK Demodulator, Rate 1/2 Selected
4	Decoder Control Register 2	03H	01H	Sign-magnitude, Direct Data Mode, No Differential Encoder or Descrambler
5	Decoder Control Register 3	04H	01H	Long Memory Mode, No Decoder Reset (Yet)
6	Normalization Test Bit Count Input Register	08H	FEH	T Count - Threshold Set for 10%
7	Normalization Test Normalize Count Input Register	09H	F9H	N Count - Threshold Set for 10%
8	BER Period Input Register LS Byte	0AH	FCH	LS Byte of 24-bit Value of Period of On-chip BER Monitor (Example Period is 4000 Symbols)
9	BER Period Input Register CS Byte	0BH	FFH	CS Byte of 24-bit Value of Period of On-chip BER Monitor
10	BER Period Input Register MS Byte	0CH	FFH	MS Byte of 24-bit Value of Period of On-chip BER Monitor
11	Normalization Test Value Enable Register	17H	00H	A Write of Any Value to This Register Begins the Normalization Test
12	BER Test Value Enable Register	18H	00H	A Write of Any Value to This Register Begins the BER Test
13	Encoder Control Register 1	06H	05H	Serial Mode, Rate 1/2, No Reset (Yet)
14	Encoder Control Register 2	07H	00H	Direct Data Mode, No Differential Encoder and No Scrambler
15	Decoder Control Register 3	04H	05H	Long Memory Mode, Reset Decoder
16	Encoder Control Register 1	06H	07H	Serial Mode, Rate 1/2, Reset Encoder
17	Decoder Control Register 3	04H	01H	Long Memory Mode, Clear Decoder Reset*
18	Encoder Control Register 1	06H	05H	Serial Mode, Rate 1/2, Clear Encoder Reset**

* After a Minimum of 2 DECINCLK and 2 DECOUTCLK Clock Periods

** After a Minimum of 2 ENCINCLK and 2 ENCOUTCLK Clock Periods

RATE 1/2 PARALLEL VITERBI OPERATION

When operating with code rate 1/2, two encoded bits (C0 and C1) are generated by the encoder for every information bit. Likewise, two coded words are input to the decoder for every information bit output from the decoder.

Synchronization states differ between the Parallel and Serial Input Modes of rate 1/2 operation. When operating with parallel input data, the synchronization states of the decoder function assume operation with a QPSK demodulation system. In these types of systems, the C0 code word of the rate 1/2 encoded output is commonly transmitted on the in-phase or quadrature channel of the QPSK modulator, while the C1 code word is transmitted on the remaining channel. In this case, the Q1900 synchronization state machine must resolve one of two possible states. The initial synchronization state, upon device reset, connects the R0 code word inputs to the internal R0 data lines, and the R1 code word inputs to the R1 data lines. This is the normal synchronization state. When the Q1900 synchronization state changes due to the assertion of the SYNCCHNG signal, the alternate synchronization state occurs in which the inverse of the R0 code word input is used internally as the R1 code word and vice versa.

The alternate synchronization state offsets the effects of a 90 degree phase ambiguity associated with QPSK demodulators. A QPSK demodulator actually can synchronize in one of four phase states. However, two of the four states are related to the other two in that they are inversions of both the R0 and R1 values. The effects of this data inversion can be offset by enabling the on-chip differential encoder and decoder circuits on this device.

Thus, the Q1900 decoder need only differentiate between normal and alternate synchronization states in order to provide synchronization to QPSK demodulators as long as the differential decoder function is enabled, or some other means is provided by the system to offset the effects of the inversion of the data. When operating in rate 1/2 Parallel Data Mode and

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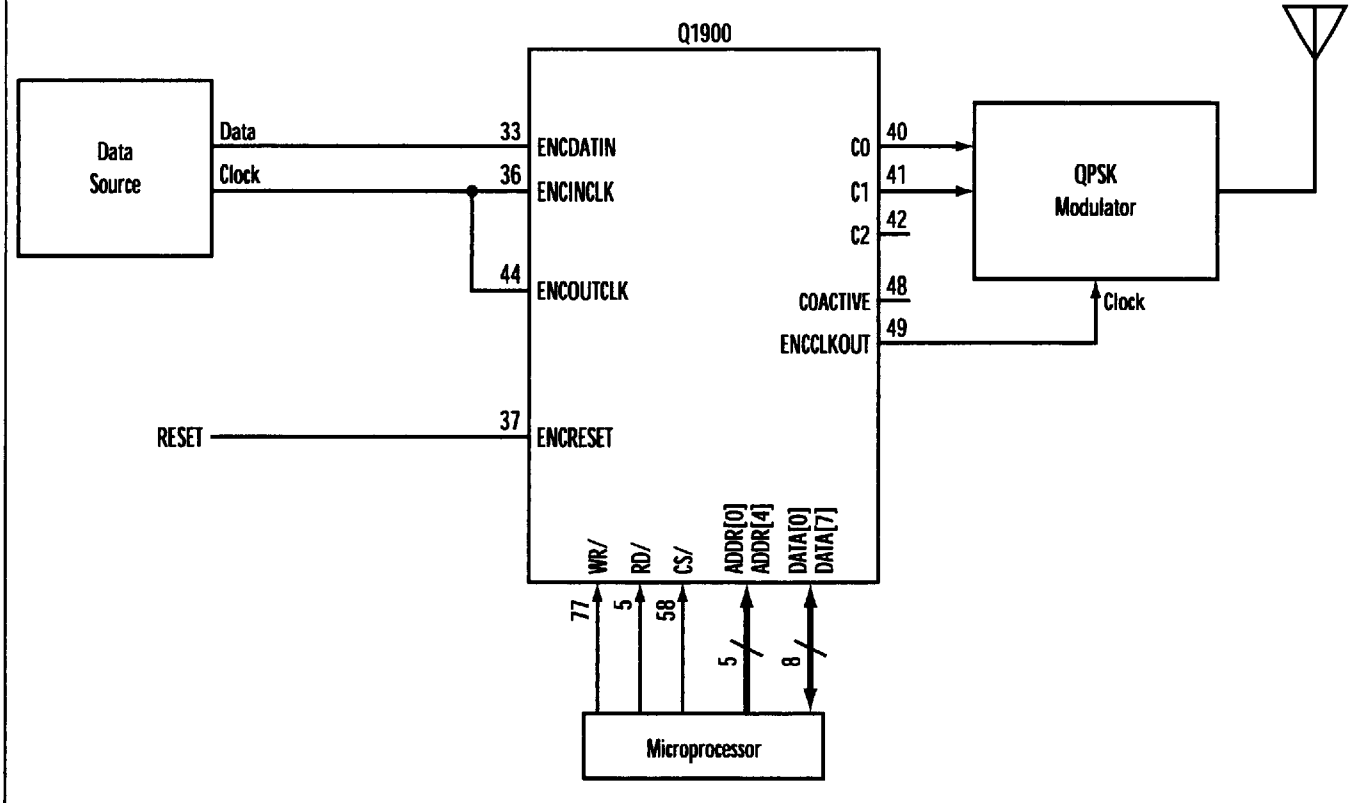
OQPSK modulation systems, an additional step is required when in the alternate synchronization state. In this case, the R1 input data is delayed by a single period of the DECINCLK signal prior to the "swap and invert" of the alternate synchronization state described for QPSK demodulators. This delay is useful for correcting the time offset of the in-phase (I) and quadrature (Q) channels of the OQPSK system.

A typical configuration of the Q1900 encoder operating in rate ½ Parallel Mode is shown in Figure 27. Data is clocked into the encoder on the rising edge of ENCINCLK. ENCOUTCLK should be the same frequency of ENCINCLK. Data is clocked out of the encoder on the rising edge of ENCCLKOUT, which is the same frequency as ENCOUTCLK. An example of the decoder operating in rate ½ Parallel Mode is shown in Figure 28. The demodulator output is quantized by a 3-bit ADC to generate the R0 and R1 soft decision inputs which are clocked into the decoder on the rising edge of DECINCLK. In this configuration, DECOUTCLK is the same frequency as DECINCLK. Decoded data is clocked out of the decoder on the rising edge of DECCLKOUT, which is the same frequency as DECOUTCLK. In most cases, the DECCLKOUT signal should be used to clock the decoded data into subsequent processing stages.

The Q1900 is programmed for rate ½ Parallel Mode operation by writing to the processor interface. An example initialization is shown in Table 9.

Figure 27. Rate ½ Parallel Viterbi Mode Encoder Example for 84-pin PLCC* Package



*Configuration for 100-pin VTQFP Package is the Same Except for Pin Numbers

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Figure 28. Rate 1/2 Parallel Viterbi Mode Decoder Example for 84-pin PLCC* Package

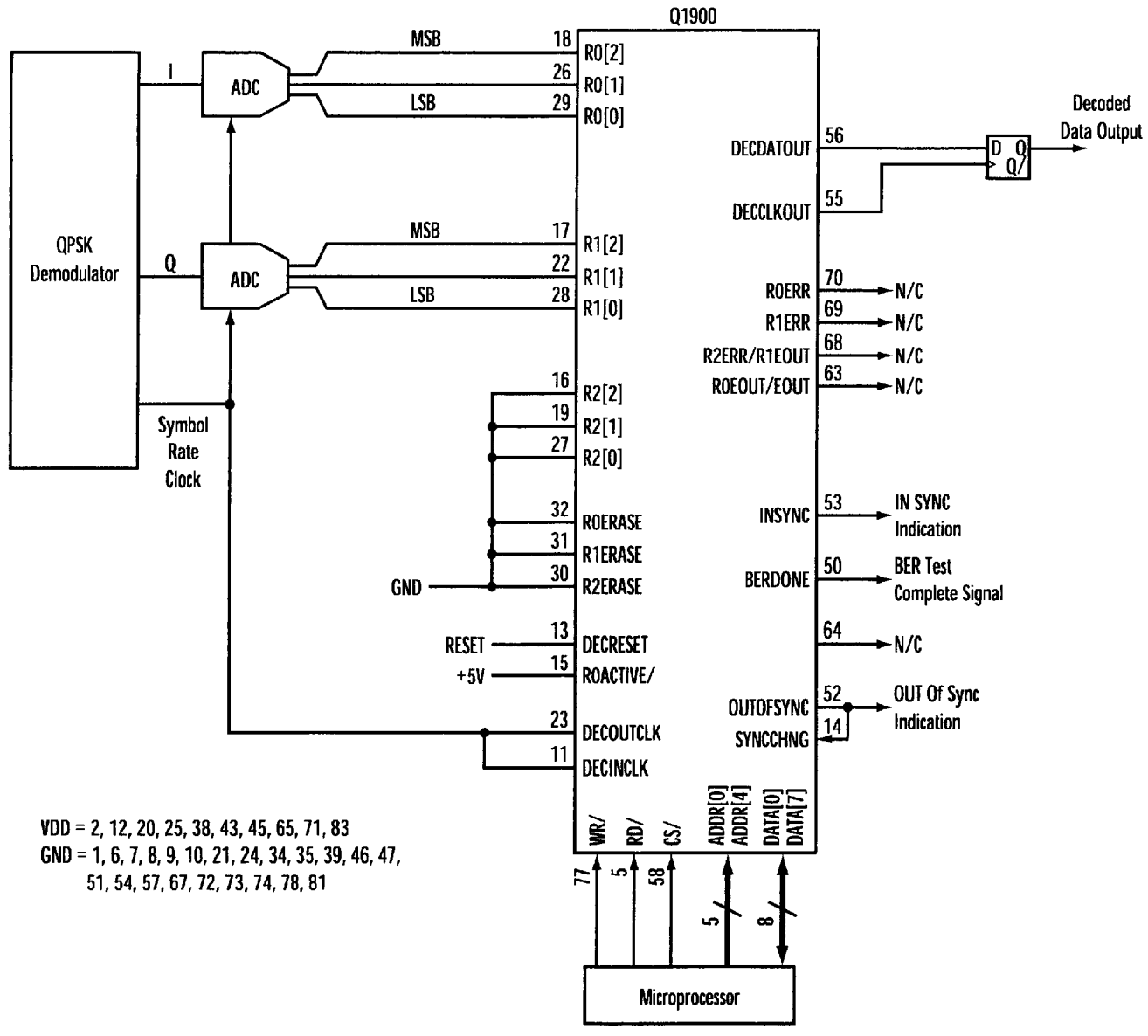

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Table 9. Rate 1/2 Parallel Viterbi Mode Initialization Example

STEP	REGISTER NAME	ADDRESS	VALUE	COMMENTS
1	Reserved Register	15H	00H	Reserved Registers Must be Set to 0 for Correct Operation
2	Reserved Register	16H	00H	
3	Decoder Data Input Register 1	00H	00H	Sets Decoder Input to Zero*
4	Decoder Data Input Register 2	01H	00H	Sets Decoder Input to Zero*
5	Encoder Data Input Register	05H	00H	Set Encoder Input to Zero*
6	Decoder Control Register 1	02H	04H	Parallell Mode, QPSK Demodulator, Rate 1/2 Selected
7	Decoder Control Register 2	03H	01H	Sign-magnitude, No Differential Encoder, No Descrambler, Direct Data Mode**
			09H	Sign-magnitude, No Differential Encoder, No Descrambler, Peripheral Data Mode**
8	Decoder Control Register 3	04H	01H	Long Memory Mode, No Decoder Reset (Yet)
9	Normalization Test Bit Count Input Register	08H	FEH	T Count*** - Threshold Set for 10%
10	Normalization Test Normalize Count Input Register	09H	F9H	N Count*** - Threshold Set for 10%
11	BER Period Input Register LS Byte	0AH	FCH	LS Byte of 24-bit Value of Period of On-chip BER Monitor (Example Period is 4000 Symbols)
12	BER Period Input Register CS Byte	0BH	FFH	CS Byte of 24-bit Value of Period of On-chip BER Monitor
13	BER Period Input Register MS Byte	0CH	FFH	MS Byte of 24-bit Value of Period of On-chip BER Monitor
14	Normalization Test Value Enable Register	17H	00H	A Write of Any Value to This Register Begins the Normalization Test
15	BER Test Value Enable Register	18H	00H	A Write of Any Value to This Register Begins the BER Test
16	Encoder Control Register 1	06H	04H	Parallel Mode, Rate 1/2, No Reset (Yet)
17	Encoder Control Register 2	07H	00H	No Differential Encoder, No Scrambler, Direct Data Mode**
			08H	No Differential Encoder, No Scrambler, Peripheral Data Mode**
18	Decoder Control Register 3	04H	05H	Long Memory Mode, Reset Decoder
19	Encoder Control Register 1	06H	06H	Parallel Mode, Rate 1/2, Reset Encoder
20	Decoder Control Register 3	04H	01H	Long Memory Mode, Clear Decoder Reset****
21	Encoder Control Register 1	06H	04H	Parallel Mode, Rate 1/2, Clear Encoder Reset*****

* This Step is Only Required for Peripheral Data Mode

** Select Direct Data Mode or Peripheral Data Mode

*** For Peripheral Data Mode, Rate 3/4 and Rate 7/8 Use T-count and N-Count From Rate 3/4 and Rate 7/8 Initialization Examples

**** After a Minimum of 2 DECINCLK and 2 DECOUTCLK Clock Periods

***** After a Minimum of 2 ENCINCLK and 2 ENCOUTCLK Clock Periods

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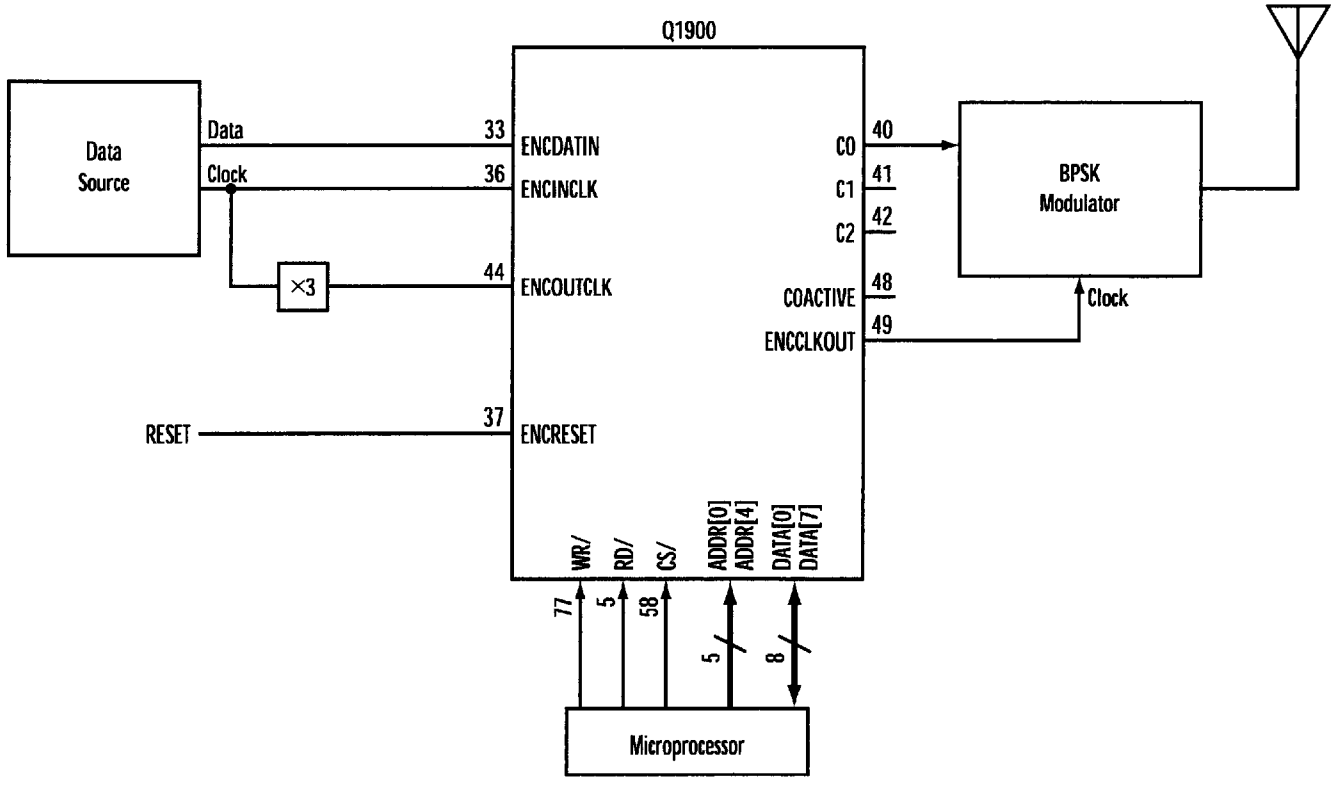
RATE 1/3 SERIAL VITERBI OPERATION

Operation with code rate 1/3 in Serial Data Mode is similar in function to the rate 1/2 serial operation previously described, except that three bits are generated by the encoder for each input information bit. When operating with rate 1/3 coding in Serial Data Mode, the decoder will group the input code words in a triplet grouping. If the SYNCCHNG signal is used to correct this code word grouping, the decoder will adjust the grouping by stopping the serial-to-parallel conversion process internally for a single period of DECINCLK. In this mode, there are three possible synchronization states. It is required that the input sequence to the decoder be the R0, R1, and finally the R2 input code word for each given symbol. This is the order in which the serialized code words C0, C1, and C2 are output from the encoder when operating in Serial Data Mode.

A typical configuration of the Q1900 encoder operating in rate 1/3 Serial Mode is shown in Figure 29. Data is clocked into the encoder on the rising edge of ENCINCLK. ENCOUTCLK should be three times the frequency of ENCINCLK. Data is clocked out of the encoder on the rising edge of ENCCLKOUT, which is the same frequency as ENCOUTCLK. An example of the decoder operating in rate 1/3 Serial Mode is shown in Figure 30. The demodulator output is quantized by a 3-bit ADC to generate the R0 soft decision input which is clocked into the decoder on the rising edge of DECINCLK. In this configuration, DECOUTCLK is one-third the frequency of DECINCLK. Decoded data is clocked out of the decoder on the rising edge of DECCLKOUT, which is the same frequency as DECOUTCLK.

The Q1900 is programmed for rate 1/3 Serial Mode operation by writing to the processor interface. An example initialization is shown in Table 10.

Figure 29. Rate 1/3 Serial Viterbi Mode Encoder Example for 84-pin PLCC* Package



*Configuration for 100-pin VTQFP Package is the Same Except for Pin Numbers

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Figure 30. Rate 1/3 Serial Viterbi Mode Decoder Example for 84-pin PLCC* Package

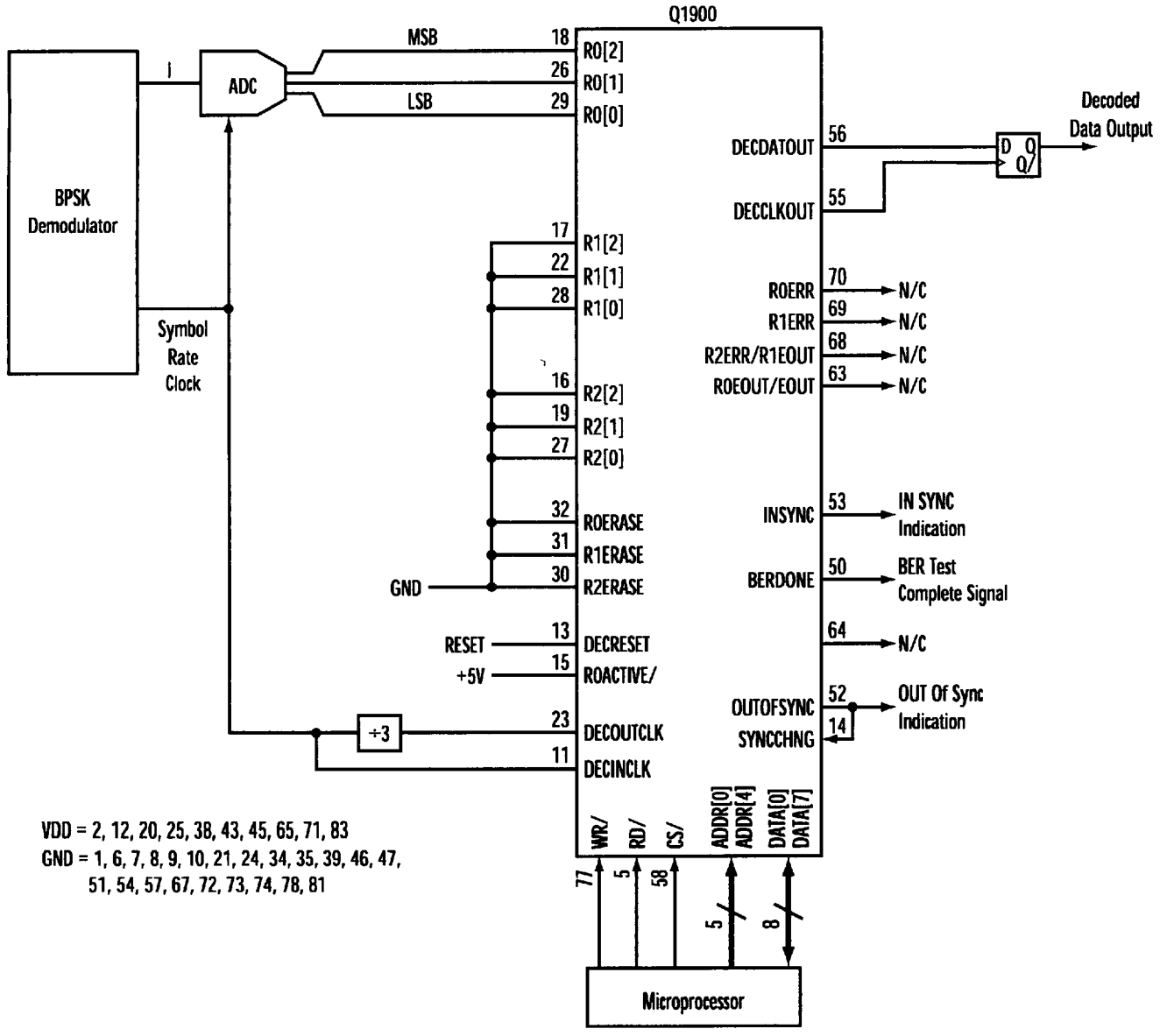

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Table 10. Rate 1/3 Serial Viterbi Mode Initialization Example

STEP	REGISTER NAME	ADDRESS	VALUE	COMMENTS
1	Reserved Register	15H	00H	Reserved Registers Must be Set to 0 for Correct Operation
2	Reserved Register	16H	00H	
3	Decoder Control Register 1	02H	11H	Serial Mode, Rate 1/3 Selected
4	Decoder Control Register 2	03H	01H	Sign-magnitude, Direct Data Mode, No Differential Encoder or Descrambler
5	Decoder Control Register 3	04H	01H	Long Memory Mode, No Decoder Reset (Yet)
6	Normalization Test Bit Count Input Register	08H	FEH	T Count - Threshold Set for 10%
7	Normalization Test Normalize Count Input Register	09H	F9H	N Count - Threshold Set for 10%
8	BER Period Input Register LS Byte	0AH	FCH	LS Byte of 24-bit Value of Period of On-chip BER Monitor (Example Period is 4000 Symbols)
9	BER Period Input Register CS Byte	0BH	FFH	CS Byte of 24-bit Value of Period of On-chip BER Monitor
10	BER Period Input Register MS Byte	0CH	FFH	MS Byte of 24-bit Value of Period of On-chip BER Monitor
11	Normalization Test Value Enable Register	17H	00H	A Write of Any Value to This Register Begins the Normalization Test
12	BER Test Value Enable Register	18H	00H	A Write of Any Value to This Register Begins the BER Test
13	Encoder Control Register 1	06H	11H	Serial Mode, Rate 1/3, No Reset (Yet)
14	Encoder Control Register 2	07H	00H	Direct Data Mode, No Differential Encoder and No Scrambler
15	Decoder Control Register 3	04H	05H	Long Memory Mode, Reset Decoder
16	Encoder Control Register 1	06H	13H	Serial Mode, Rate 1/3, Reset Encoder
17	Decoder Control Register 3	04H	01H	Long Memory Mode, Clear Decoder Reset*
18	Encoder Control Register 1	06H	11H	Serial Mode, Rate 1/3, Clear Encoder Reset**

* After a Minimum of 2 DECINCLK and 2 DECOUTCLK Clock Periods

** After a Minimum of 2 ENCINCLK and 2 ENCOUTCLK Clock Periods

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RATE 1/3 PARALLEL VITERBI OPERATION

Operation with code rate 1/3 in Parallel Data Mode is similar in function to rate 1/2 Parallel Data Mode previously described, except that three code bits are generated by the encoder for each input information bit. The Q1900 is programmed for rate 1/3 Parallel Mode operation by writing to the processor interface. An example initialization is shown in Table 11.

When operating with code rate 1/3 and Parallel Data Input Mode at the decoder, the synchronization circuit does not affect the data. Data input to the decoder in this mode must be in the correct sequence and input on the correct R0, R1, and R2 inputs. However, the on-chip differential decoder can be enabled to offset the inversion of the data which may occur in such systems as a BPSK transmission network.

Table 11. Rate 1/3 Parallel Viterbi Mode Initialization Example for 84-pin PLCC* Package

STEP	REGISTER NAME	ADDRESS	VALUE	COMMENTS
1	Reserved Register	15H	00H	Reserved Registers Must be Set to 0 for Correct Operation
2	Reserved Register	16H	00H	
3	Decoder Data Input Register 1	00H	00H	Sets Decoder Input to Zero**
4	Decoder Data Input Register 2	01H	00H	Sets Decoder Input to Zero**
5	Encoder Data Input Register	05H	00H	Set Encoder Input to Zero**
6	Decoder Control Register 1	02H	10H	Parallell Mode, QPSK Demodulator, Rate 1/3 Selected
7	Decoder Control Register 2	03H	01H	Sign-magnitude, No Differential Encoder, No Descrambler, Direct Data Mode***
			09H	Sign-magnitude, No Differential Encoder, No Descrambler, Peripheral Data Mode***
8	Decoder Control Register 3	04H	01H	Long Memory Mode, No Decoder Reset (Yet)
9	Normalization Test Bit Count Input Register	08H	FEH	T Count - Threshold Set for 10%
10	Normalization Test Normalize Count Input Register	09H	F9H	N Count - Threshold Set for 10%
11	BER Period Input Register LS Byte	0AH	F9H	LS Byte of 24-bit Value of Period of On-chip BER Monitor
12	BER Period Input Register CS Byte	0BH	FFH	CS Byte of 24-bit Value of Period of On-chip BER Monitor
13	BER Period Input Register MS Byte	0CH	FFH	MS Byte of 24-bit Value of Period of On-chip BER Monitor
14	Normalization Test Value Enable Register	17H	00H	A Write of Any Value to This Register Begins the Normalization Test
15	BER Test Value Enable Register	18H	00H	A Write of Any Value to This Register Begins the BER Test
16	Encoder Control Register 1	06H	10H	Parallel Mode, Rate 1/3, No Reset (Yet)
17	Encoder Control Register 2	07H	00H	No Differential Encoder, No Scrambler, Direct Data Mode***
			08H	No Differential Encoder, No Scrambler, Peripheral Data Mode***
18	Decoder Control Register 3	04H	05H	Long Memory Mode, Reset Decoder
19	Encoder Control Register 1	06	12H	Parallel Mode, Rate 1/3, Reset Encoder
20	Decoder Control Register 3	04H	01H	Long Memory Mode, Clear Decoder Reset****
21	Encoder Control Register	06H	10H	Parallel Mode, Rate 1/3, Clear Encoder Reset*****

* Configuration for 100-pin VTQFP package is the same Except for pin numbers

** This Step is Only Required for Peripheral Data Mode

*** Select Direct Data Mode or Peripheral Data Mode

**** After a Minimum of 2 DECINCLK and 2 DECOUTCLK Clock Periods

***** After a Minimum of 2 ENCINCLK and 2 ENCOUTCLK Clock Periods

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RATE 3/4 PARALLEL VITERBI OPERATION

When operating with code rate 3/4 in Parallel Data Mode, four encoded bits (two C0 and C1 pairs) are generated by the encoder for every three information bits. These encoded bits are output from the C0 and C1 pins at 2/3 the frequency of the input information. Likewise, four coded words (two R0 and R1 pairs) are input into the decoder for every three information bits output from the decoder. These coded words are input into the decoder through the R0 and R1 input.

Operation with the internal puncture code rates is similar to rate 1/2 parallel operation except that the possible synchronization states increase due to the ambiguity with the pattern of the puncture process. When operating with code rate 3/4 with automatic synchronization enabled, the decoder first performs the phase ambiguity resolution process. Next, the paired code words are processed by a null-symbol insertion circuit that must correctly insert the null symbols in the place where code words were erased at the encoder. When operating with code rate 3/4, this additional synchronization process adds a factor of two to the number of possible correct synchronization states for a total of four possible correct states. The Q1900 decoder synchronization circuit attempts each possible state in sequence. The synchronization state changes each time the SYNCCHNG input is asserted.

The first symbol pair output from the encoder is indicated by an active High state at the C2 (pin 42 PLCC or pin 62 VTQFP) output when operating in rate 3/4 mode. A typical configuration of the Q1900 encoder operating in rate 3/4 Parallel Mode is shown in Figure 31.

The Rate 3/4 encoder requires a hardware reset that is synchronous to the ENCINCLK and ENCOUTCLK. The Rate 3/4 encoder shall be reset by applying the rising edge of ENCRESET 20 ns prior to the rising edge of ENCOUTCLK. The relationship of ENCINCLK, ENCOUTCLK, ENCRESET and the Valid timing regions for reseting the encoder are shown in Figure 32.

Data is clocked into the encoder on the rising edge of ENCINCLK. ENCOUTCLK should be 2/3 the frequency of ENCINCLK. Data is clocked out of the encoder on the rising edge of ENCCLKOUT, which is the same frequency as ENCOUTCLK. An example of the decoder operating in rate 3/4 Parallel Mode is shown in Figure 33. The demodulator output is quantized by a 3-bit ADC to generate the R0 and R1 soft decision inputs which are clocked into the decoder on the rising edge of DECINCLK. In this configuration, DECOUTCLK is 3/2 the frequency of DECINCLK. Decoded data is clocked out of the decoder on the rising edge of DECCLKOUT which is the same frequency as DECOUTCLK. In most cases, the DECCLKOUT signal should be used to clock the decoded data into subsequent processing stages.

The Q1900 is programmed for rate 3/4 Parallel Mode operation by writing to the processor interface. An example initialization is shown in Table 12.

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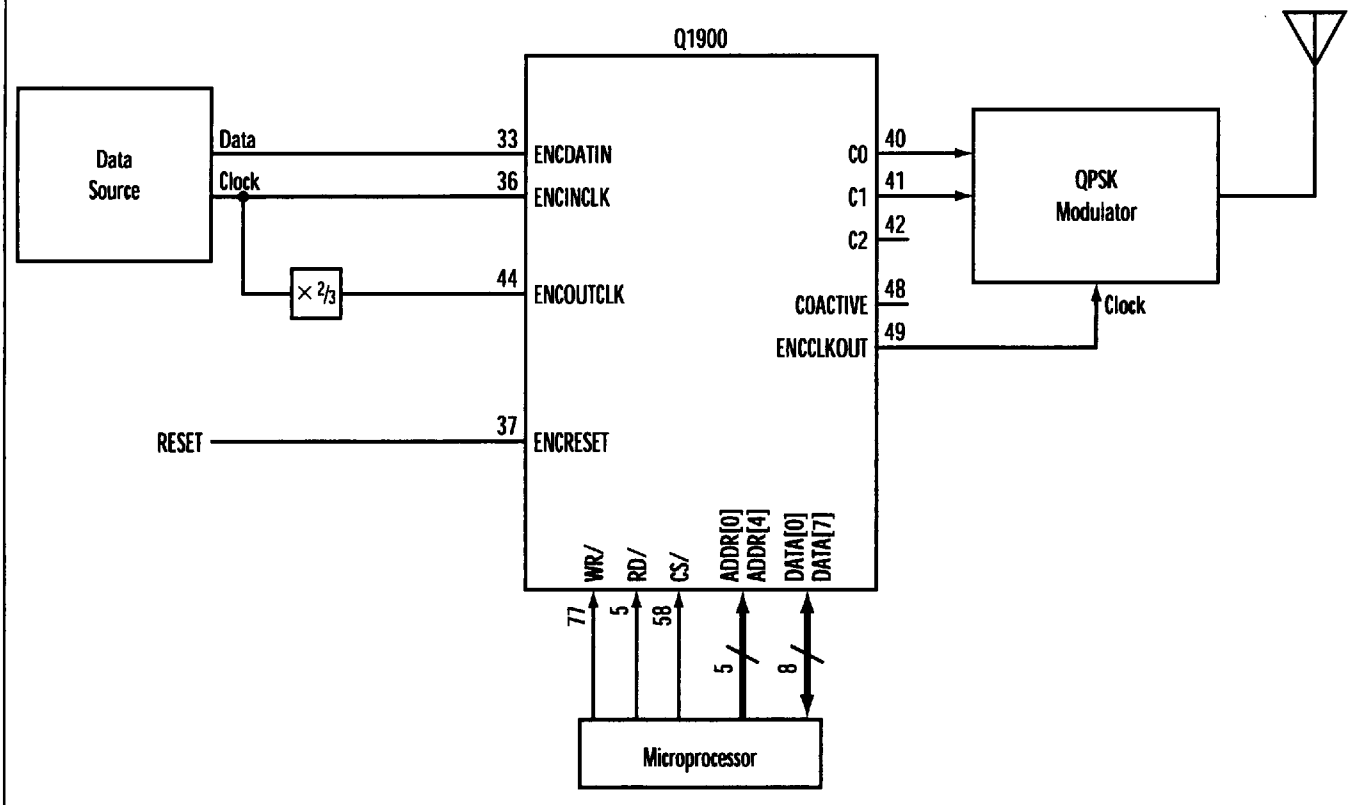
Figure 31. Rate 3/4 Parallel Viterbi Mode Encoder Example for 84-pin PLCC* Package



*Configuration for 100-pin VTQFP Package is the Same Except for Pin Numbers

Figure 32. Rate 3/4 Parallel Viterbi Mode Encoder Timing Diagram

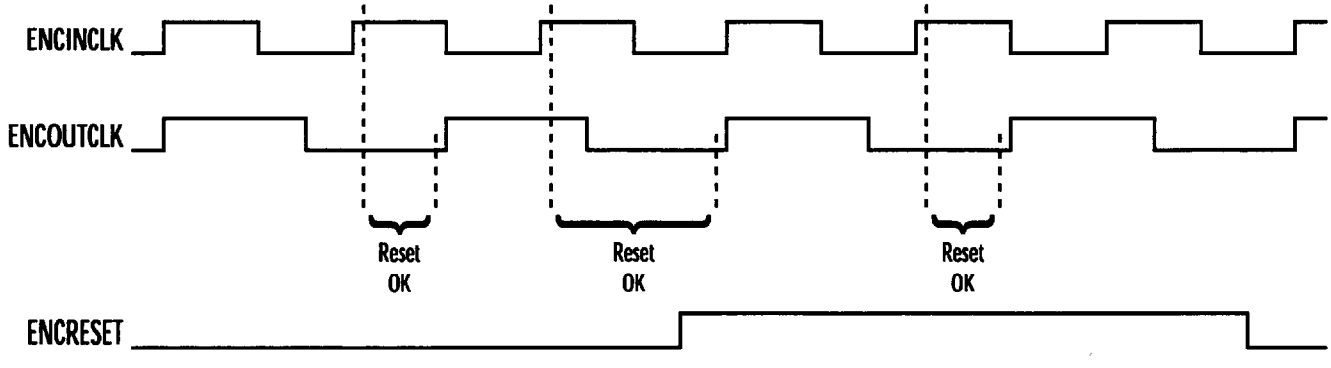


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Figure 33. Rate 3/4 Parallel Viterbi Mode Decoder Example for 84-pin PLCC* Package

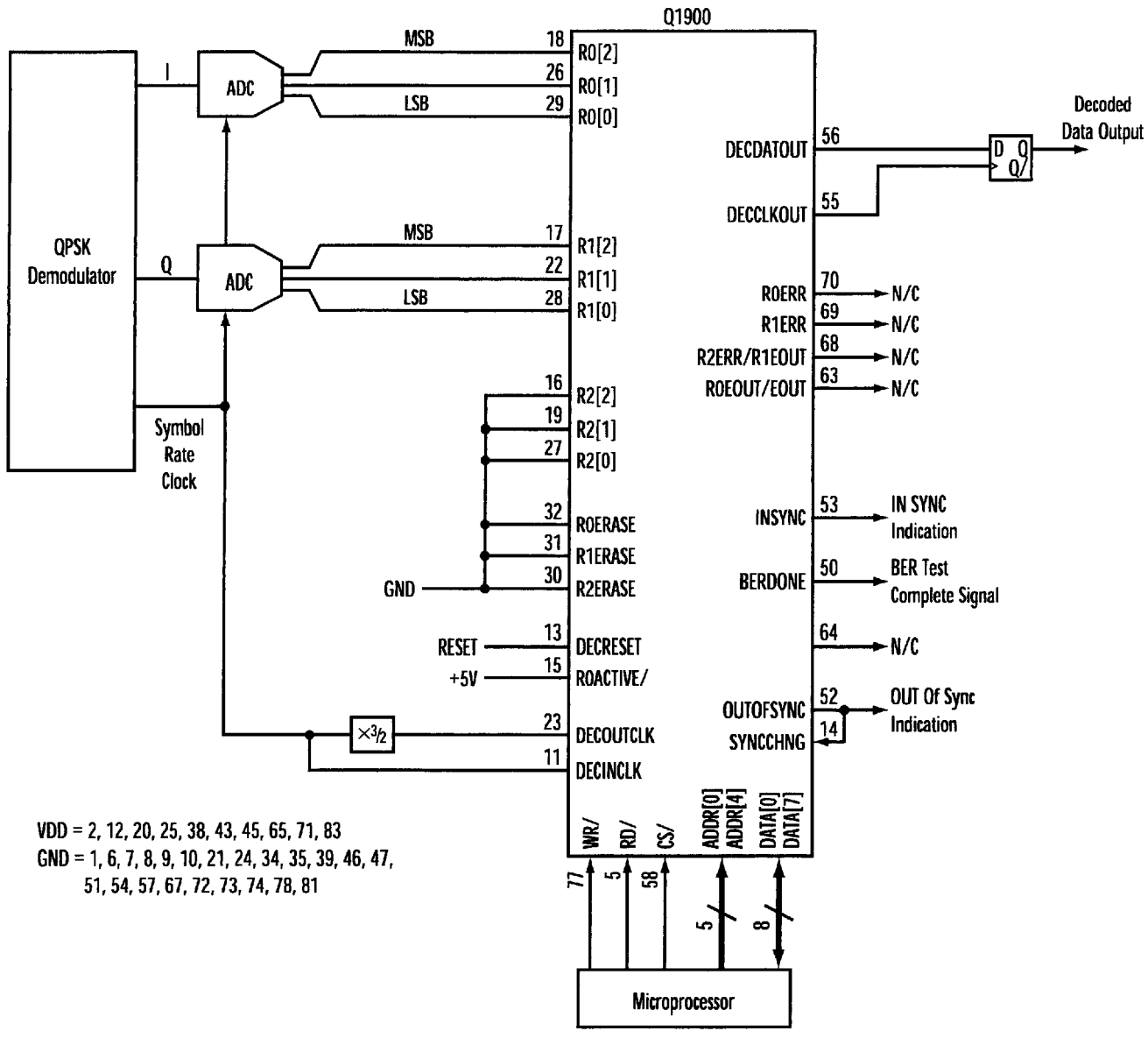

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Table 12. Rate 3/4 Parallel Viterbi Mode Initialization Example

STEP	REGISTER NAME	ADDRESS	VALUE	COMMENTS
1	Reserved Register	15H	00H	Reserved Registers Must Be Set to 0 for Correct Operation
2	Reserved Register	16H	00H	
3	Decoder Control Register 1	02H	08H	Parallel Mode, QPSK Demodulator, Rate 3/4 Selected
4	Decoder Control Register 2	03H	01H	Sign-magnitude, Direct Data Mode*, No Differential Encoder or Descrambler
5	Decoder Control Register 3	04H	01H	Long Memory Mode, No Decoder Reset (Yet)
6	Normalization Test Bit Count Input Register	08H	F4H	T Count - Threshold Set for 1.7%
7	Normalization Test Normalize Count Input Register	09H	F9H	N Count - Threshold Set for 1.7%
8	BER Period Input Register LS Byte	0AH	FCH	LS Byte of 24-bit Value of Period of On-chip BER Monitor (Example Period is 4000 Symbols)
9	BER Period Input Register CS Byte	0BH	FFH	CS Byte of 24-bit Value of Period of On-chip BER Monitor
10	BER Period Input Register MS Byte	0CH	FFH	MS Byte of 24-bit Value of Period of On-chip BER Monitor
11	Normalization Test Value Enable Register	17H	00H	A Write of Any Value to This Register Begins the Normalization Test
12	BER Test Value Enable Register	18H	00H	A Write of Any Value to This Register Begins the BER Test
13	Encoder Control Register 1	06H	08H	Parallel Mode, Rate 3/4, No Reset (Yet)
14	Encoder Control Register 2	07H	00H	Direct Data Mode, No Differential Encoder and No Scrambler
15	Decoder Control Register 3	04H	05H	Long Memory Mode, Reset Decoder
16	Issue Hardware Encoder Reset	–	–	See Description in Text**
17	Decoder Control Register 3	04H	01H	Long Memory Mode, Clear Decoder Reset***

* For Rate 3/4 Peripheral Data Mode, Use Rate 1/2 Peripheral Data Mode and Program T-count and N-count for Rate 3/4

** For a Minimum of 2 ENCINCLK and 2 ENCOUTCLK Clock Periods

*** After a Minimum of 2 DECINCLK and 2 DECOUTCLK Clock Periods

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RATE 7/8 PARALLEL VITERBI OPERATION

When operating with code rate 7/8 in Parallel Data Mode, eight encoded bits (four C0 and C1 pairs) are generated by the encoder for every seven information bits. These encoded bits are output from the C0 and C1 pins at 4/7 the frequency of the input information. Likewise, eight coded words (four R0 and R1 pairs) are input into the decoder for every seven information bits output from the decoder. These coded words are input into the decoder through the R0 and R1 input.

Operation with the internal puncture code rates is similar to rate 1/2 parallel operation, except that the possible synchronization states increase due to the ambiguity with the pattern of the puncture process. When operating with code rate 7/8 with automatic synchronization enabled, the decoder first performs the phase ambiguity resolution process. Next, the paired code words are processed by a null-symbol insertion circuit that must correctly insert the null symbols in the place where code words were erased at the encoder. When operating with code rate 7/8, this additional synchronization process adds a factor of four to the number of possibly correct synchronization states for a total of eight possibly correct states. The Q1900 decoder synchronization circuit attempts each possible state in sequence. The synchronization state changes each time the SYNCCHNG input is asserted.

The first symbol pair output from the encoder is indicated by an active High state at the C2 (pin 42 PLCC or pin 62 VTQFP) output when operating in rate 7/8 mode. A typical configuration of the Q1900 encoder operating in rate 7/8 Parallel Mode is shown in Figure 34.

The Rate 7/8 encoder requires a hardware reset that is synchronous to the ENCINCLK and ENCOUTCLK. The Rate 7/8 encoder shall be reset by applying the rising edge of ENCRESET 20 ns prior to the rising edge of ENCOUTCLK. The relationship of ENCINCLK, ENCOUTCLK, ENCRESET and the valid timing regions for reseting the encoder are shown in Figure 35. Data is clocked into the encoder on the rising edge of ENCINCLK. ENCOUTCLK should be 4/7 the frequency of ENCINCLK.

Data is clocked out of the encoder on the rising edge of ENCCLKOUT, which is the same frequency as ENCOUTCLK. An example of the decoder operating in rate 7/8 Parallel Mode is shown in Figure 36. The demodulator output is quantized by a 3-bit ADC to generate the R0 and R1 soft decision inputs which are clocked into the decoder on the rising edge of DECINCLK. In this configuration, DECOUTCLK is 7/8 the frequency of DECINCLK. Decoded data is clocked out of the decoder on the rising edge of DECCLKOUT which is the same frequency as DECOUTCLK. In most cases, the DECCLKOUT signal should be used to clock the decoded data into subsequent processing stages.

The Q1900 is programmed for rate 7/8 Parallel Mode operation by writing to the processor interface. An example initialization is shown in Table 13.

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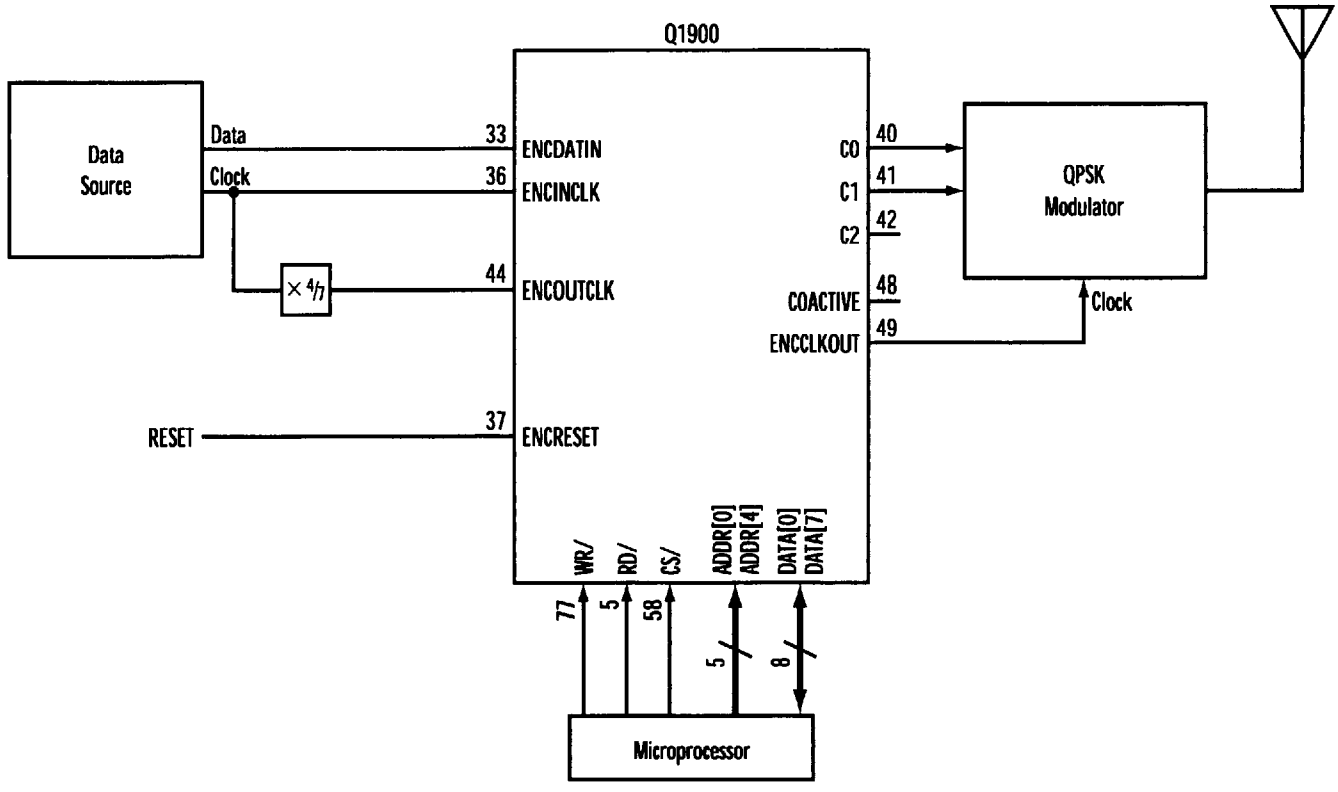
Figure 34. Rate 7/8 Parallel Viterbi Mode Encoder Example for 84-pin PLCC* Package



*Configuration for 100-pin VTQFP Package is the Same Except for Pin Numbers

Figure 35. Rate 7/8 Parallel Viterbi Mode Encoder Timing Diagram

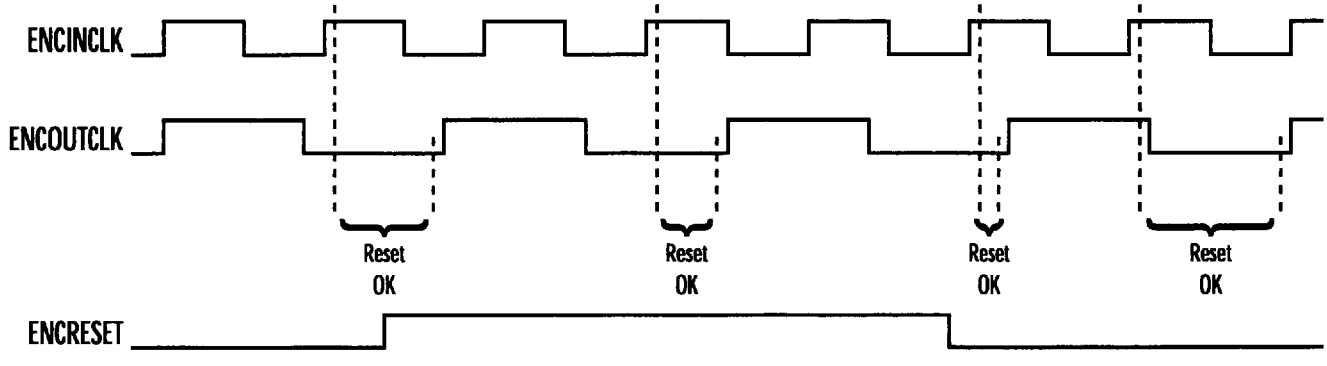


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Figure 36. Rate 7/8 Parallel Viterbi Mode Decoder Example for 84-pin PLCC* Package

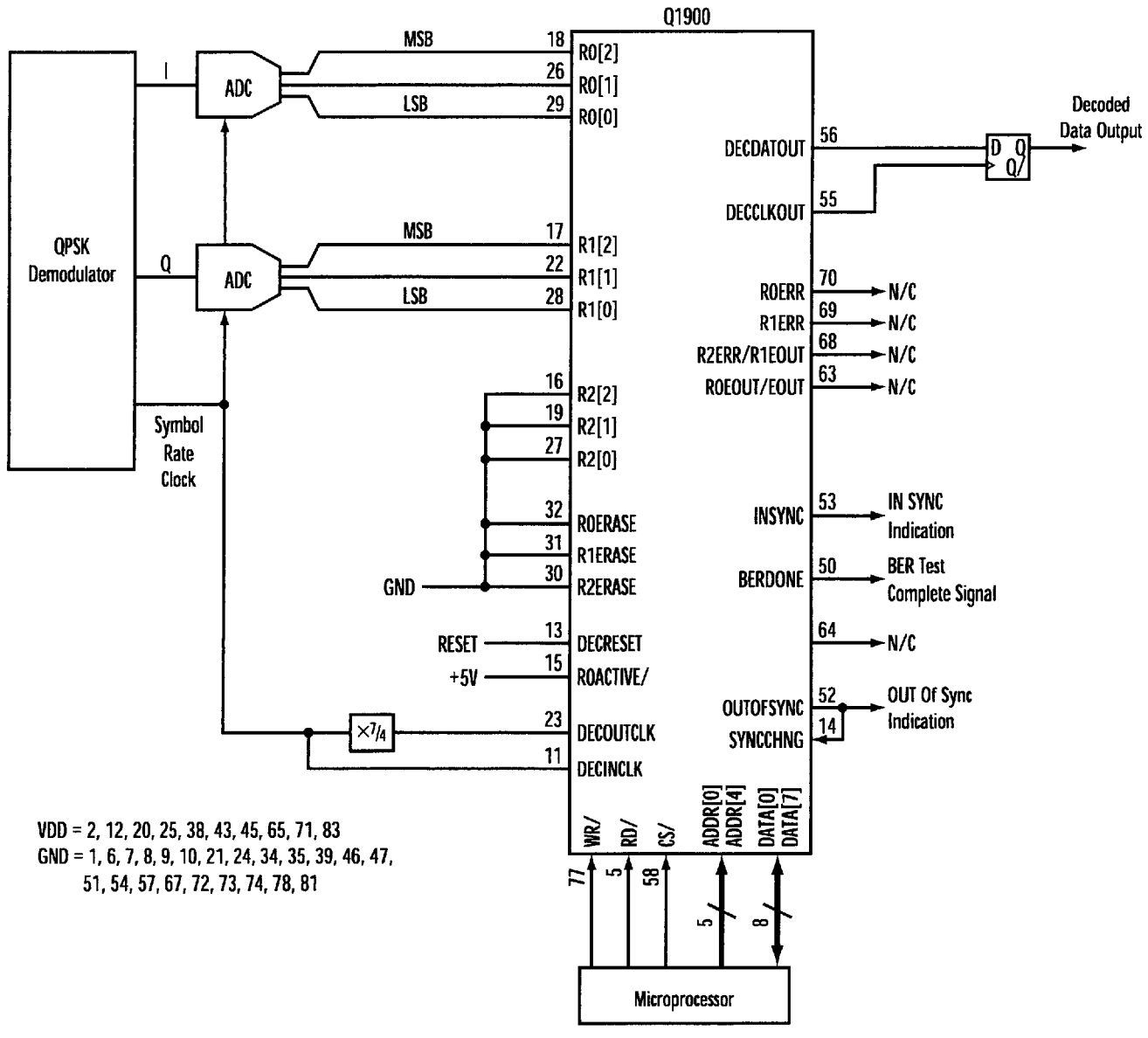

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Table 13. 7/8 Parallel Viterbi Mode Initialization Example

STEP	REGISTER NAME	ADDRESS	VALUE	COMMENTS
1	Reserved Register	15H	00H	Reserved Registers Must Be Set to 0 for Correct Operation
2	Reserved Register	16H	00H	
3	Decoder Control Register 1	02H	20H	Parallel Mode, QPSK Demodulator, Rate 7/8 Selected
4	Decoder Control Register 2	03H	01H	Sign-magnitude, Direct Data Mode*, No Differential Encoder or Descrambler
5	Decoder Control Register 3	04H	01H	Long Memory Mode, No Decoder Reset (Yet)
6	Normalization Test Bit Count Input Register	08H	E3H	T Count - Threshold Set for 0.8%
7	Normalization Test Normalize Count Input Register	09H	F8H	N Count - Threshold Set for 0.8%
8	BER Period Input Register LS Byte	0AH	FCH	LS Byte of 24-bit Value of Period of On-chip BER Monitor (Example Period is 4000 Symbols)
9	BER Period Input Register CS Byte	0BH	FFH	CS Byte of 24-bit Value of Period of On-chip BER Monitor
10	BER Period Input Register MS Byte	0CH	FFH	MS Byte of 24-bit Value of Period of On-chip BER Monitor
11	Normalization Test Value Enable Register	17H	00H	A Write of Any Value to This Register Begins the Normalization Test
12	BER Test Value Enable Register	18H	00H	A Write of Any Value to This Register Begins the BER Test
13	Encoder Control Register 1	06H	20H	Parallel Mode, Rate 7/8, No Reset (Yet)
14	Encoder Control Register 2	07H	00H	Direct Data Mode, No Differential Encoder and No Scrambler
15	Decoder Control Register 3	04H	05H	Long Memory Mode, Reset Decoder
16	Issue Hardware Encoder Reset	–	–	See Description in Text**
17	Decoder Control Register 3	04H	01H	Long Memory Mode, Clear Decoder Reset***

* For Rate 7/8 Peripheral Data Mode Use Rate 1/2 Peripheral Data Mode and Program T-count and N-count for Rate 7/8

** For a Minimum of 2 ENCINCLK and 2 ENCOUTCLK Clock Periods

*** After a Minimum of 2 DECINCLK and 2 DECOUTCLK Clock Periods

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HIGHER VITERBI CODE RATE OPERATION USING EXTERNAL PUNCTURING

The Q1900 Viterbi Mode encoder and decoder can encode and decode punctured code rates other than the rate 3/4 and 7/8 code implemented internally. Operation with these other codes requires the use of external puncture and null-symbol insertion circuits. The Q1900 decoder function includes symbol erasure inputs for the R0, R1, and R2 code words which are used to indicate a null-symbol to the decoder. When using external puncturing, external circuitry is typically used to synchronize the decoder for phase ambiguities and puncture pattern alignments.

RATE 2/3 8-PSK TRELLIS OPERATION

When operating with trellis code rate 2/3, three encoded bits (ENCC0, ENCC1, and ENCC2) are generated by the encoder for every two input information bits. Likewise, three coded words are input to the decoder for every two information bits output from the decoder.

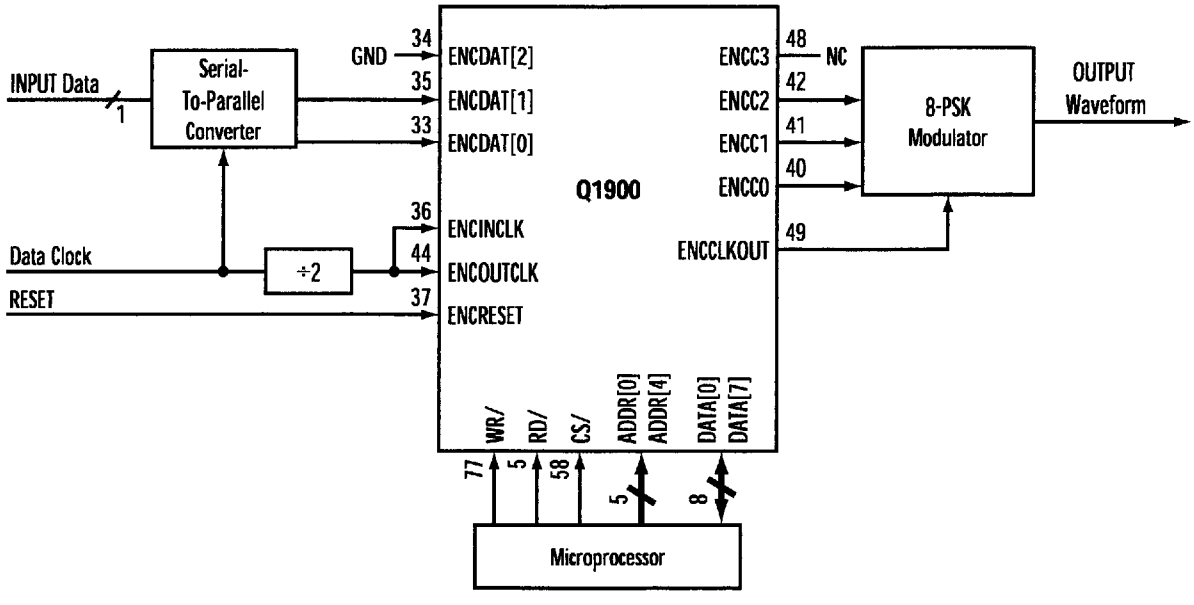
The input data stream is processed by a serial-to-parallel converter to generate the ENCDAT[0] and ENCDAT[1] input pair. This data pair is clocked into the Q1900 trellis encoder at one-half the rate of the input data (bit) clock. For every 2 input bits (ENCDAT[0] and ENCDAT[1]), the encoder generates 3 output bits (ENCC0, ENCC1, and ENCC2). See Figure 37. This 3-bit output is supplied to an external 8-PSK modulator. The mapping from the 3-bit encoder output to transmitted phase is shown in Table 14.

For rate 2/3 8-PSK operation, the ENCDAT[2] input is not used and should be grounded.

Table 14. Mapping of Rate 2/3 8-PSK Encoder Output to Transmitted Phase

Encoder Output (Binary)	Transmitted Phase
000	0°
001	45°
011	90°
010	135°
100	180°
101	225°
111	270°
110	315°

Figure 37. Rate 2/3 Trellis Mode Encoder Configuration Example for 84-pin PLCC* Package



*Configuration for 100-pin VTQFP Package is the Same Except for Pin Numbers

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At the receiver (Figure 38), the demodulated output is typically sampled and quantized. In this example, each channel is quantized by a 6-bit ADC and used to address two 4K × 8 branch metric lookup ROMs. The conversion from quantized I & Q to branch metrics and sector number is programmed in the ROMs (Table 2). Note: The conversion from I & Q to phase is:

$$\text{phase} = \tan^{-1}(Q/I).$$

For each set of branch metrics and sector number clocked into the Trellis decoder, 2 decoded outputs are generated, DECDAT[0] and DECDAT[1]. The parallel-to-serial converter that processes the output data bits requires a clock that is two times the frequency of the symbol clock.

The Q1900 trellis encoder and decoder are programmed for rate 2/3 8-PSK operation by writing to the processor interface. A register initialization for this example is shown in Table 15.

Figure 38. Rate 2/3 Trellis Mode Decoder Configuration Example for 84-pin PLCC* Package

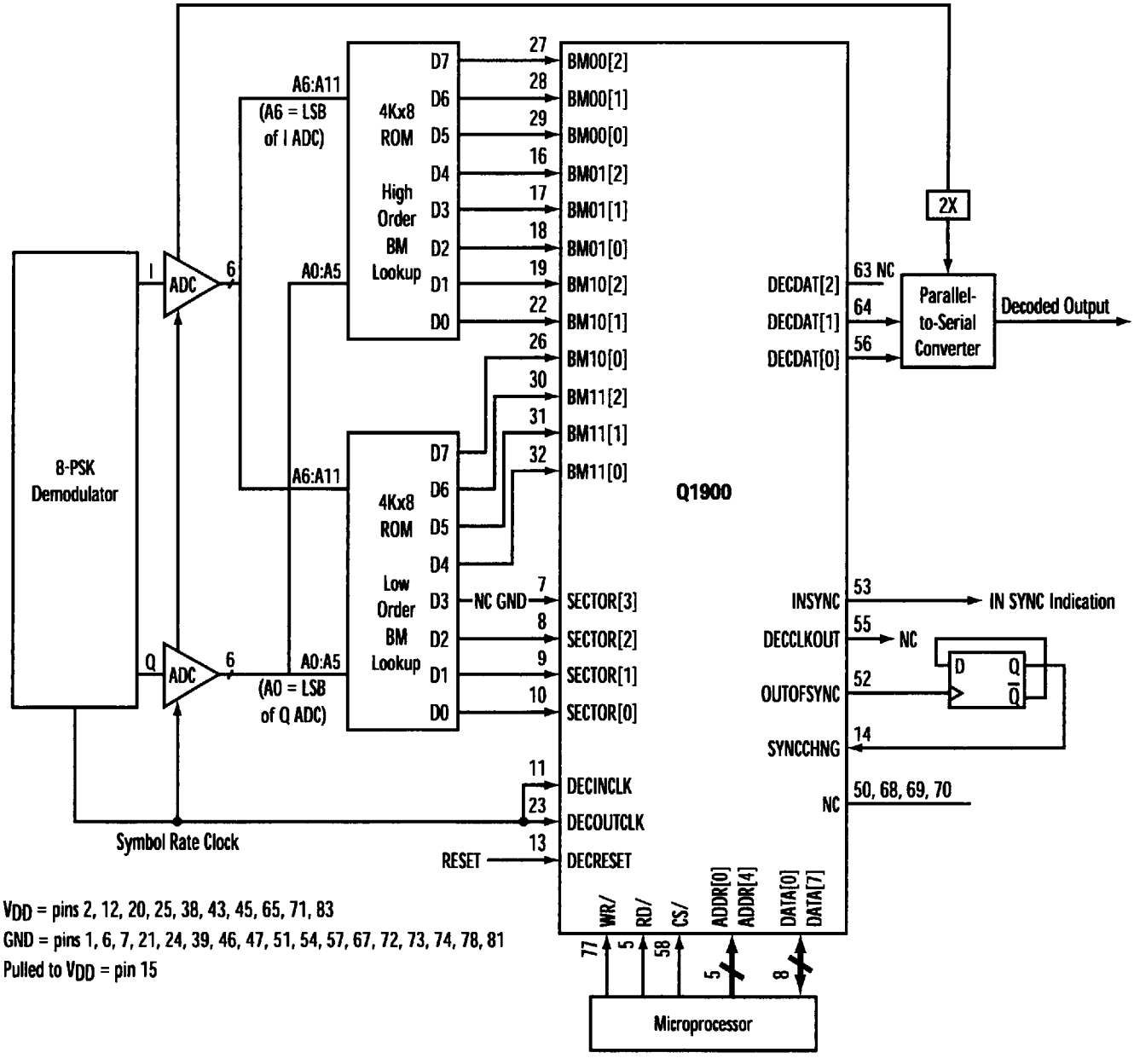

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Table 15. Rate 2/3 Trellis Mode Initialization Example

STEP	REGISTER NAME	ADDRESS	VALUE	COMMENTS
1	Reserved Register	15H	00H	Reserved Register Must Be Set to 0 for Correct Operation
2	Reserved Register	16H	00H	
3	Decoder Data Input Register 1	00H	00H	Sets Decoder Input to Zero*
4	Decoder Data Input Register 2	01H	00H	Sets Decoder Input to Zero*
5	Encoder Data Input Register	05H	00H	Sets Encoder Input to Zero*
6	Decoder Control Register 1	02H	C0H	Must Program for Correct Operation
7	Decoder Control Register 2	03H	91H	Direct Data Mode**, Ambiguity Decoder On, Rate 2/3
			99H	Peripheral Data Mode**, Ambiguity Decoder On, Rate 2/3
8	Decoder Control Register 3	04H	01H	Clear Reset Bit
9	Normalization Test Bit-Count Input Register	08H	FEH	T Count - Threshold Set for 10%
10	Normalization Test Normalize-Count Input Register	09H	F9H	N Count - Threshold Set for 10%
11	Normalization Test Value-Enable Register	17H	XXH	Write Any Value to This Register to Begin the Normalization Test
12	Encoder Control Register 1	06H	84H	Clear Reset Bit
13	Encoder Control Register 2	07H	90H	Direct Data Mode, Ambiguity Resolver On, Rate 2/3
			98H	Peripheral Data Mode, Ambiguity Resolver On, Rate 2/3
14	Decoder Control Register 3	04H	051H	Set Reset Bit (Resets Decoder)
15	Encoder Control Register 1	06H	86H	Set Reset Bit (Resets Encoder)
16	Decoder Control Register 3	04H	01H	Clear Decoder Reset ***
17	Encoder Control Register 1	06H	84H	Clear Encoder Reset Bit****

* This Step is Only Required for Peripheral Data Mode

** Select Direct Data Mode or Peripheral Data Mode

*** After a Minimum of 2 DECINCLK and 2 DECOUTCLK Clock Periods

**** After a Minimum of 2 ENCINCLK and 2 ENCOUTCLK Clock Periods

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RATE 3/4 16-PSK TRELLIS OPERATION

When operating with trellis code rate 3/4, four encoded bits (ENCC0, ENCC1, ENCC2 and ENCC3) are generated by the encoder for every three input information bits. Likewise, four coded words are input to the decoder for every three information bits output from the decoder

The input data stream is processed by a serial-to-parallel converter to generate the ENCDAT[0], ENCDAT[1], and ENCDAT[2] input group. This data group is clocked into the Q1900 at one-third the rate of the input data clock. For every 3 input bits (ENCDAT[0], ENCDAT[1], and ENCDAT[2]), the encoder generates 4 output bits (ENCC0, ENCC1, ENCC2, and ENCC3). See Figure 39. This 4-bit output is supplied to an external 16-PSK modulator. The mapping from the 4-bit encoder output to transmitted phase is shown in Table 16.

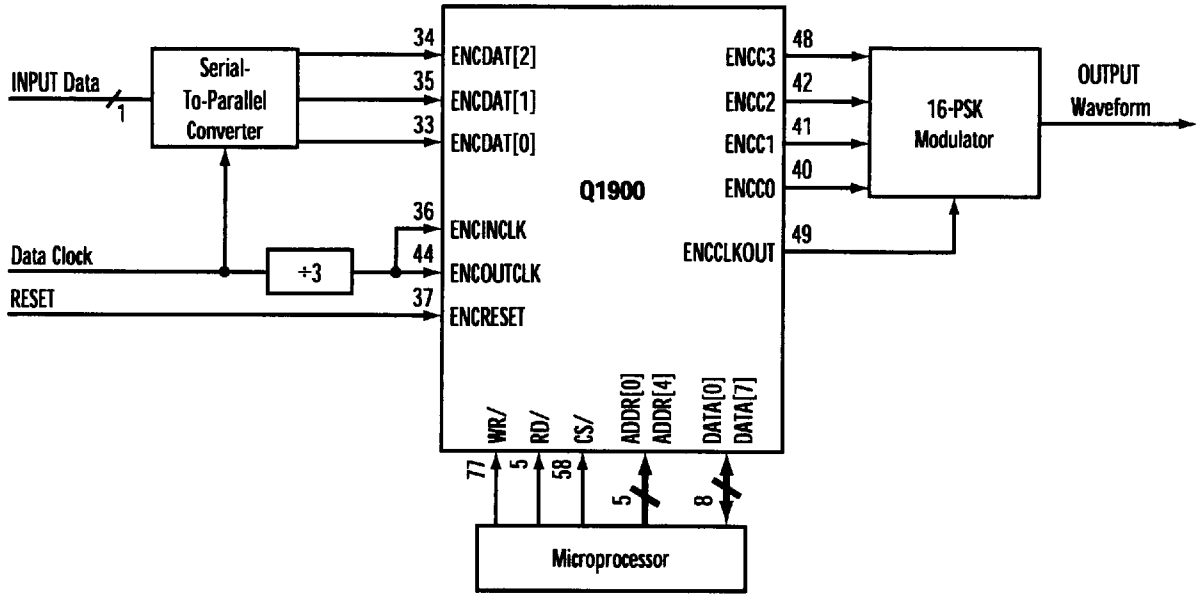
At the receiver, shown in Figure 40, the demodulated output is typically sampled and quantized. In this example, each channel is quantized by a 6-bit ADC and used to address two 4K x 8 branch metric lookup ROMs. The conversion from quantized I & Q to branch metrics and sector number is programmed in ROMs. See Table 3. Note: the conversion from I & Q to phase is:

$$\text{phase} = \tan^{-1}(Q/I)$$

For each set of branch metrics and sector numbers clocked into the trellis decoder, 3 decoded outputs are generated (DECDAT[0], DECDAT[1], and DECDAT[2]). The parallel-to-serial converter that processes the output data bits requires a clock that is three times the frequency of the symbol clock.

The Q1900 TCM encoder and PTCM decoder are programmed for rate 3/4 16-PSK operation by writing to the processor interface. An example register initialization for this example is shown in Table 17.

Figure 39. Rate 3/4 Trellis Mode Encoder Configuration Example for 84-pin PLCC* Package



*Configuration for 100-pin VTQFP Package is the Same Except for Pin Numbers

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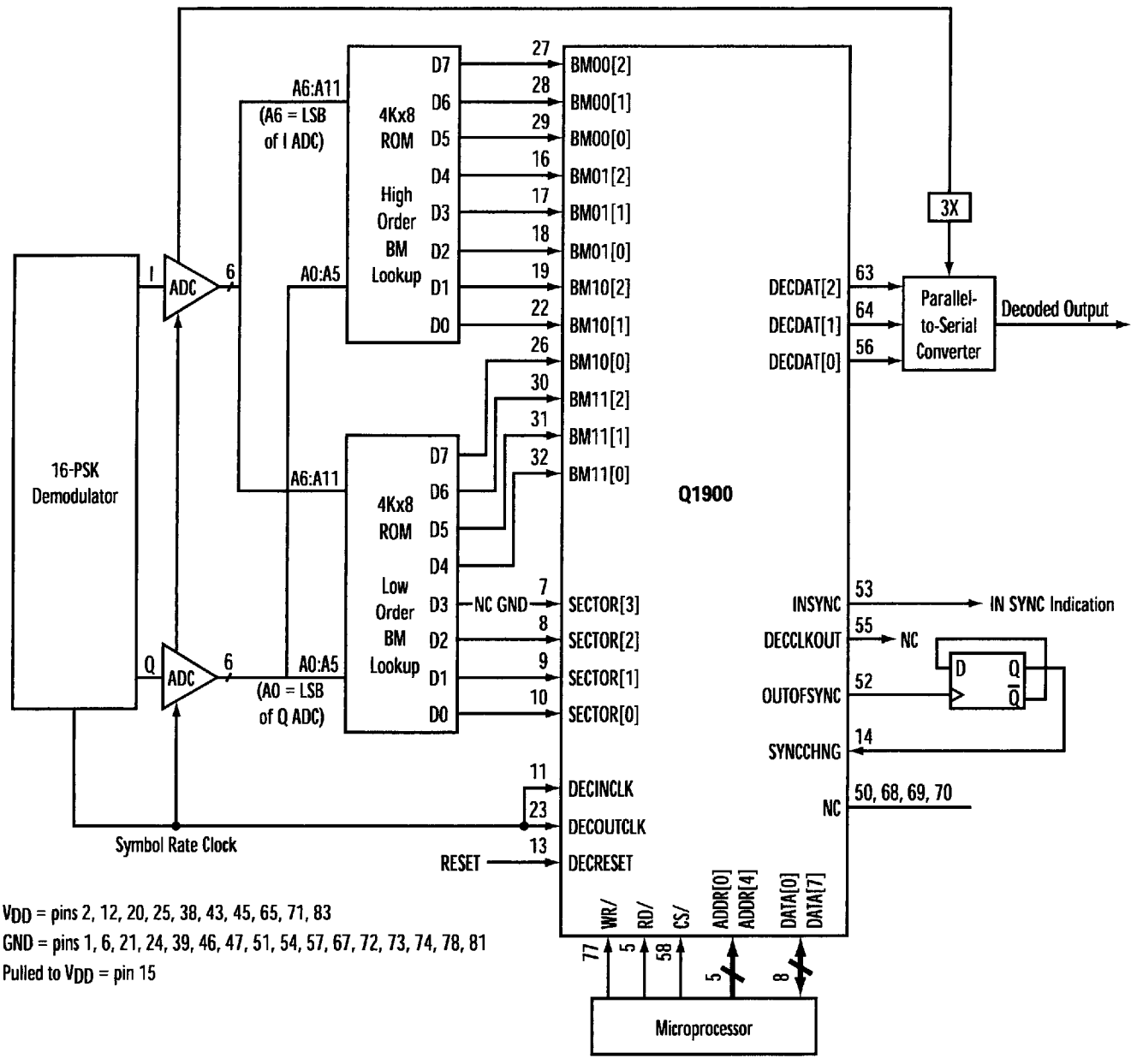
Figure 40. Rate 3/4 Trellis Mode Decoder Configuration Example for 84-pin PLCC* Package



*Configuration for 100-pin VTQFP Package is the Same Except for Pin Numbers

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Table 16. Mapping of Rate 3/4 16-PSK Encoder Output to Transmitted Phase

Encoder Output (Binary)	Transmitted Phase	Encoder Output (Binary)	Transmitted Phase
0000	0°	1100	180°
0001	22.5°	1101	202.5°
0011	45°	1111	225°
0010	67.5°	1110	247.5°
0100	90°	1000	270°
0101	112.5°	1001	292.5°
0111	135°	1011	315°
0110	157.5°	1010	337.5°

Table 17. Rate 3/4 Trellis Mode Initialization Example

STEP	REGISTER NAME	ADDRESS	VALUE	COMMENTS
1	Reserved Register	15H	00H	Reserved Register Must Be Set to 0 for Correct Operation
2	Reserved Register	16H	00H	
3	Decoder Data Input Register 1	00H	00H	Sets Decoder Input to Zero*
4	Decoder Data Input Register 2	01H	00H	Sets Decoder Input to Zero*
5	Encoder Data Input Register	05H	00H	Sets Encoder Input to Zero*
6	Decoder Control Register 1	02H	C0H	Must Program for Correct Operation
7	Decoder Control Register 2	03H	11H	Direct Data Mode**, Ambiguity Decoder On, Rate 3/4
			19H	Peripheral Data Mode**, Ambiguity Decoder On, Rate 3/4
8	Decoder Control Register 3	04H	01H	Clear Reset Bit
9	Normalization Test Bit-Count Input Register	08H	FEH	T Count - Threshold Set for 10%
10	Normalization Test Normalize-Count Input Register	09H	F9H	N Count - Threshold Set for 10%
11	Normalization Test Value-Enable Register	17H	XXH	Write Any Value to This Register to Begin the Normalization Test
12	Encoder Control Register 1	06H	84H	Clear Reset Bit
13	Encoder Control Register 2	07H	10H	Direct Data Mode, Ambiguity Resolver On, Rate 3/4
			18H	Peripheral Data Mode, Ambiguity Resolver On, Rate 3/4
14	Decoder Control Register 3	04H	051H	Set Reset Bit (Resets Decoder)
15	Encoder Control Register 1	06H	86H	Set Reset Bit (Resets Encoder)
16	Decoder Control Register 3	04H	01H	Clear Decoder Reset ***
17	Encoder Control Register 1	06H	84H	Clear Encoder Reset Bit****

* This Step is Only Required for Peripheral Data Mode

** Select Direct Data Mode or Peripheral Data Mode

*** After a Minimum of 2 DECINCLK and 2 DECOUTCLK Clock Periods

**** After a Minimum of 2 ENCINCLK and 2 ENCOUTCLK Clock Periods

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TECHNICAL SPECIFICATION

PROCESSOR INTERFACE

The on-chip processor interface of the Q1900 allows a processor to set the operational mode and monitor the device's internal status. The interface includes an 8-bit data bus, a 5-bit address bus, and read enable, write enable, and chip select lines. This interface will operate with most major microprocessor and signal processor families without wait state logic. It can also write and read data to and from the encoder and decoder functions. In this mode, the Q1900 operates as a single-chip FEC peripheral to the processor system.

The Q1900 processor interface has 4 read registers and 21 write registers for the Viterbi Mode and 2 read registers and 21 write registers for the Trellis Mode.

READ REGISTERS

Tables 18 and 19 show the memory maps for the Viterbi and Trellis Modes read registers, respectively. Tables 20 and 21 describe the functions of each read register and bit in detail for the Viterbi and Trellis Modes, respectively.

WRITE REGISTERS

Table 22 and 23 show the memory maps for the Viterbi and Trellis Modes write registers, respectively. Tables 24 and 25 describe the functions of each write register and bit in detail for the Viterbi and Trellis Modes, respectively.

Table 18. Viterbi Read Registers Memory Map

ADDRESS		DATA BITS							
DEC	HEX	D7	D6	D5	D4	D3	D2	D1	D0
00	00	Decoder Data Output Register							
		Reserved	Reserved	R0EOUT/EOUT	Reserved	R2ERR/R1EOUT	R1ERR	R0ERR	DECDATOUT
02	02	Encoder Data Output Register							
		Reserved	Reserved	Reserved	Reserved	COACTIVE	C2	C1	C0
03	03	BER Measurement LS Byte Output Register							
		Bit 7 (MS)	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0 (LS)
04	04	BER Measurement MS Byte Output Register							
		Bit 7 (MS)	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0 (LS)

Table 19. Trellis Read Registers Memory Maps

ADDRESS		DATA BITS							
DEC	HEX	D7	D6	D5	D4	D3	D2	D1	D0
00	00	Decoder Data Output Register							
		Reserved	Reserved	DECDAT[2]	DECDAT[1]	Reserved	Reserved	Reserved	DECDAT[0]
02	02	Encoder Data Output Register							
		Reserved	Reserved	Reserved	Reserved	ENCC3	ENCC2	ENCC1	ENCC0

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Table 20a. Viterbi Read Register Address 00H: Decoder Data Output Register

BIT	NAME	FUNCTION	Same Function as Input Pin PLCC/VTQFP
0	DECDATOUT	Decoder Data Output	56/39
1	ROERR	Bit-by-bit Indication of Detected Channel Bit Errors for R0	70/93
2	R1ERR	Bit-by-bit Indication of Detected Channel Bit Errors for R1	69/92
3	R2ERR/R1EOUT	If: Code Rate Set to 1/3 Then: Provides Bit-by-bit Indication of Detected Channel Bit Errors for R2 If: Code Rate Not Set to 1/3 Then: Provides R1ERASE Delayed to Align With R1ERR	68/91
4	–	Reserved	–
5	ROEOUT/EOUT	If: Code Rate Set to 1/3 Then: Provides Logic OR of ROERASE, R1ERASE, and R2ERASE Delayed to Align with ROERR, R1ERR, and R2ERR Outputs If: Code Rate Not Set to 1/3 Then: Provides ROERASE Delayed to Align with ROERR	63/85
6-7	–	Reserved	–

Table 20b. Viterbi Read Register Address 02H: Encoder Data Output Register

BIT	NAME	FUNCTION	Same Function as Input Pin PLCC/VTQFP
0	C0	Encoder Symbol C0	40/60
1	C1	Encoder Symbol C1	41/61
2	C2	Encoder Symbol C2 for Code Rate 1/3 – OR – "1" Indicates Output of First Symbol of Puncture Pattern for Code Rates 3/4 and 7/8	42/62
3	COACTIVE	In Serial Data Mode, Indicates C0 Code Bit is Active	48/70
4-7	–	Reserved	–

Table 20c. Viterbi Read Register Address 03H: BER Measurement LS Byte Output Register

BIT	NAME	FUNCTION
0-7	BER LS BYTE	Least Significant Eight Bits of the 16-bit Result of the Internal BER Measurement. Bit 0 is LSB.

Table 20d. Viterbi Read Register Address 04H: BER Measurement MS Byte Output Register

BIT	NAME	FUNCTION
0-7	BER MS BYTE	Most Significant Eight Bits of the 16-bit Result of the Internal Bit Error Rate Measurement. Bit 0 is LSB.

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Table 21a. Trellis Read Register Address 00H: Decoder Data Output Register

BIT	NAME	FUNCTION	Same Function as Input Pin PLCC/VTQFP
0	DECDAT[0]	Decoder Data Output (LSB)	56/39
1	-	Reserved	-
2	-	Reserved	-
3	-	Reserved	-
4	DECDAT[1]	Decoder Data Output (CSB)	64/86
5	DECDAT[2]	Decoder Data Output (MSB)	63/85
6-7	-	Reserved	-

Table 21b. Trellis Read Register Address 02H: Encoder Data Output Register

BIT	NAME	FUNCTION	Same Function as Input Pin PLCC/VTQFP
0	ENCC0	Encoder Output (LSB)	40/60
1	ENCC1	Encoder Output	41/61
2	ENCC2	Encoder Output	42/62
3	ENCC3	Encoder Output (MSB)	48/70
4-7	-	Reserved	-

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Table 22. Viterbi Write Register Memory Map

ADDRESS		DATA BITS							
DEC	HEX	D7	D6	D5	D4	D3	D2	D1	D0
00	00	Decoder Data Input Register 1							
		R0ERASE	R0[2]	R0[1]	R0[0]	R1ERASE	R1[2]	R1[1]	R1[0]
01	01	Decoder Data Input Register 2							
		R2ERASE	R2[2]	R2[1]	R2[0]	Set to 0	Set to 0	Set to 0	Set to 0
02	02	Decoder Control Register 1							
		Set to 0	Set to 0	RATE 7/8	RATE 1/3	RATE 3/4	RATE 1/2	OQPSK	MODE SELECT
03	03	Decoder Control Register 2							
		Set to 0	Set to 0	DESCR ENABLE	DIFF DEC ENA	PERIPR/DIRECT	SWAP ERASE	PHASE SYNC	SMG/OBN
04	04	Decoder Control Register 3							
		Set to 0	Set to 0	Set to 0	Set to 0	Set to 0	S/W DEC RESET	Set to 0	FUL/SHT MEM
05	05	Encoder Data Intput Register							
		Set to 0	Set to 0	Set to 0	Set to 0	Set to 0	Set to 0	Set to 0	ENCDATIN
06	06	Encoder Control Register 1							
		Set to 0	Set to 0	RATE 7/8	RATE 1/3	RATE 3/4	RATE 1/2	S/W ENC RESET	SER/PAR MODE
07	07	Encoder Control Register 2							
		Set to 0	Set to 0	SCRAMB ENABLE	DIFF ENC ENA	BUS/PIN MODE	Set to 0	Set to 0	Set to 0
08	08	Normalization Test Bit Count Input Register (TCOUNT)							
		Bit 7 (MS)	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0 (LS)
09	09	Normalization Test Normalize Count Input Register (NCOUNT)							
		Bit 7 (MS)	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0 (LS)
10	0A	BER Period Input Register LS Byte (BERPER)							
		Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0 (LS)
11	0B	BER Period Input Register CS Byte (BERPER)							
		Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
12	0C	BER Period Input Register MS Byte (BERPER)							
		Bit 23 (MS)	Bit 22	Bit 21	Bit 20	Bit 19	Bit 18	Bit 17	Bit 16
14	0E	Processor Decoder Input Clock Register (DECINCLK)							
		Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
15	0F	Processor Decoder Output Clock Register (DECOUTCLK)							
		Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
17	11	Processor Encoder Input Clock Register (ENCINCLK)							
		Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
18	12	Processor Encoder Output Clock Register (ENCOUTCLK)							
		Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
		Reserved Registers							
21	15	Set to 0	Set to 0	Set to 0	Set to 0	Set to 0	Set to 0	Set to 0	Set to 0
22	16	Set to 0	Set to 0	Set to 0	Set to 0	Set to 0	Set to 0	Set to 0	Set to 0
23	17	Normalization Test Value Enable Register (NTVE)							
		Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
24	18	BER Test Value Enable Register (BERTVE)							
		Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0

Notes: 1. Write registers 0DH, 10H, 13H, and 14H are not used.

2. All bits that are specified as "Set to 0" or "Set to 1" must be set to 0 or 1 for proper operation.

3. Reserved write registers 15H and 16H must be set to 0 for correct operation.

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Table 23. Trellis Write Register Memory Map

ADDRESS		DATA BITS							
DEC	HEX	D7	D6	D5	D4	D3	D2	D1	D0
00	00	**Decoder Data Input Register 1**							
		BM11[0]	BM01[0]	BM10[0]	BM00[0]	BM11[1]	BM01[1]	BM10[1]	BM00[1]
01	01	**Decoder Data Input Register 2**							
		BM11[2]	BM01[2]	BM10[2]	BM00[2]	SECTOR3	SECTOR2	SECTOR1	SECTOR0
02	02	**Decoder Control Register 1**							
		Set to 1	Set to 1	Set to 0	Set to 0	Set to 0	Set to 0	Set to 0	Set to 0
03	03	**Decoder Control Register 2**							
		TRL 8/16	Set to 0	Set to 0	DIFF DEC ENA	PERIPR/DIRECT	Set to 0	Set to 0	Set to 1
04	04	**Decoder Control Register 3**							
		Set to 0	Set to 0	Set to 0	Set to 0	Set to 0	S/W DEC RESET	Set to 0	Set to 1
05	05	**Encoder Data Intput Register**							
		Set to 0	Set to 0	Set to 0	Set to 0	Set to 0	ENCDAT[2]	ENCDAT[1]	ENCDAT[0]
06	06	**Encoder Control Register 1**							
		Set to 1	Set to 0	Set to 0	Set to 0	Set to 0	Set to 1	S/W ENC RESET	Set to 0
07	07	**Encoder Control Register 2**							
		TRL 8/16	Set to 0	Set to 0	DIFF ENC ENA	PERIPR/DIRECT	Set to 0	Set to 0	Set to 0
08	08	**Normalization Test Bit-Count Input Register (TCOUNT)**							
		Bit 7 (MS)	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0 (LS)
09	09	**Normalization Test Normalize-Count Input Register (NCOUNT)**							
		Bit 7 (MS)	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0 (LS)
14	0E	**Processor Decoder Input Clock Register (DECINCLK)**							
		Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
15	0F	**Processor Decoder Output Clock Register (DECOUTCLK)**							
		Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
17	11	**Processor Encoder Input Clock Register (ENCINCLK)**							
		Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
18	12	**Processor Encoder Output Clock Register (ENCOUTCLK)**							
		Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
21	15	**Reserved Register**							
		Set to 0	Set to 0	Set to 0	Set to 0	Set to 0	Set to 0	Set to 0	Set to 0
22	16	**Reserved Register**							
		Set to 0	Set to 0	Set to 0	Set to 0	Set to 0	Set to 0	Set to 0	Set to 0
23	17	**Normalization Test Value Enable Register (NTVE)**							
		Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0

Notes: 1. Write registers 0AH, 0BH, 0CH, 0DH, 10H, 13H, and 14H are not used.
2. All bits that are specified as "Set to 0" or "Set to 1" must be set to 0 or 1 for proper operation.
3. Reserved write registers 15H and 16H must be set to 0 for correct operation.

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Table 24a. Viterbi Write Register Address 00H: Decoder Data Input Register 1

BIT	NAME	CONTROL/INPUT	Same Function as Input Pin PLCC/VTQFP
0	R1[0]	LSB of Decoder R1 Input Symbol	28/46
1	R1[1]	CSB of Decoder R1 Input Symbol	22/38
2	R1[2]	MSB of Decoder R1 Input Symbol	17/31
3	R1ERASE	1 Erases the R1 Symbol	31/49
4	R0[0]	LSB of Decoder R0 Input Symbol	29/47
5	R0[1]	CSB of Decoder R0 Input Symbol	26/44
6	R0[2]	MSB of Decoder R0 Input Symbol	18/32
7	R0ERASE	1 Erases the R0 Symbol	32/50

Table 24b. Viterbi Write Register Address 01H: Decoder Data Input Register 2

BIT	NAME	ACCEPTS	Same Function as Input Pin PLCC/VTQFP
0-3	–	Set to 0	–
4	R2[0]	LSB of Decoder R2 Input Symbol	27/45
5	R2[1]	CSB of Decoder R2 Input Symbol	19/33
6	R2[2]	MSB of Decoder R2 Input Symbol	16/30
7	R2ERASE	If: Code Rate Set to 1/3 Then: 1 Erases the R2 Symbol	30/48

Table 24c. Viterbi Write Register Address 02H: Decoder Control Register 1

BIT	NAME	FUNCTION
0	Decoder Input Mode Selection	1 Puts Decoder in Serial Data Input Mode 0 Puts Decoder in Parallel Data Input Mode See *Parallel vs. Serial Data Modes* for more information.
1	OQPSK	If: Decoder Set to Parallel Data Mode Code Rate Set to 1/2, 3/4, or 7/8 Phase Sync Enabled Then: 1 Makes Sync Circuit Adjust for Phase Ambiguities of OQPSK Demodulators 0 Makes Sync Circuit Adjust for Phase Ambiguities of QPSK Demodulators
2	Decoder Rate 3/4 Enable	1 Makes Decoder Operate With Code Rate 1/2
3	Decoder Rate 3/4 Enable	1 Makes Decoder Operate With Code Rate 3/4 For Rate 3/4 Mode, Connect the Unused R0ERASE and R1ERASE Input Pins to Logic 0
4	Decoder Rate 1/3 Enable	1 Makes Decoder Operate With Code Rate 1/3
5	Decoder Rate 7/8 Enable	1 Makes Decoder Operate With Code Rate 7/8 For Rate 7/8 Mode, Connect the Unused R0ERASE and R1ERASE Input Pins to Logic 0
6-7	–	Set to 0

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Table 24d. Viterbi Write Register Address 03H: Decoder Control Register 2

BIT	NAME	FUNCTION
0	SMG/OBN	0 Makes Decoder Accept Offset-binary Notation Soft Decision Inputs at R0, R1, R2 1 Makes Decoder Accept Sign-magnitude Notation Soft Decision Inputs at R0, R1, R2 The following table describes the offset-binary and sign-magnitude data input encoding formats for the soft decision decoder:
1	PHASE SYNC ENA	If: The Decoder is Set to Parallel Mode, Code Rate 1/2, 3/4, or 7/8 Then: A "0" Causes the Decoder Sync State to Toggle on Every Rising Edge of SYNCCHNG A "1" causes the sync state to toggle depending on the input to SYNCCHING (level triggered). If SYNCCHNG is "1", the decoder will be in the "Normal" state. When SYNCCHNG is "0", the decoder will be in the "Swap & Invert" state. (Phase ambiguity automatic synchronization makes the decoder's automatic synchronization circuits perform symbol "Swap-and-Invert" operations to synchronize to the PSK phase ambiguities.)
2	SWAP ERASE ENA	If: PHASE SYNC ENA Enabled, Parallel Data Input, Code Rate 1/2, and External Symbol Erasure Then: 1 Internally "Swaps" R0ERASE and R1ERASE with the R0 and R1 Data 0 Disables "Swapping" Input Signals R0ERASE and R1ERASE with the Data
3	DECODER PERIPHERAL/ DIRECT DATA MODE	1 Makes Decoder Use Processor Bus Interface for Data Input/Output (Peripheral Mode) See *Processor Bus Interface* section of *Q1900 Pin Functions* table. 0 Makes Decoder Use Dedicated I/O Pins for Data Input/Output (Direct Mode) See *Decoder I/O Pins* in *Q1900 Pin Functions* table. Signals Affected: R0[0-2], R1[0-2], R2[0-2], R[0-2]ERASE, DECDATOUT
4	DIFF DEC ENA	1 Enables the Differential Decoder; 0 Disables the Differential Decoder (The Setting of This Bit Does Not Affect the Operation of the Differential Encoder)
5	DESCRAMB ENA	1 Enables the Descrambler; 0 Disables the Data Descrambler. Data descrambler uses a slightly modified CCITT algorithm preferred by most systems, including INTELSAT.
6	–	Set to 0
7	–	Set to 0

Encoding Format	Offset Binary			Sign-Magnitude		
R0[x], R1[x], R2[x] Bit:	[2]	[1]	[0]	[2]	[1]	[0]
Strongest 1:	1	1	1	1	1	1
	1	1	0	1	1	0
	1	0	1	1	0	1
Weakest 1:	1	0	0	1	0	0
Weakest 0:	0	1	1	0	0	0
	0	1	0	0	0	1
	0	0	1	0	1	0
Strongest 0:	0	0	0	0	1	1

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Table 24e. Viterbi Write Register Address 04H: Decoder Control Register 3

BIT	NAME	FUNCTION
0	FULL/SHORT MEMORY	1 Makes the Viterbi Decoder Algorithm Use a Minimum Chainback Path Depth of 96 States 0 Makes the Viterbi Decoder Algorithm Use a Minimum Chainback Path Depth of 48 States
1	–	Set to 0
2	S/W DECODER RESET	A transition from "0" to "1" resets decoder functions. Connect pin 13 PLCC or pin 27 VTQFP to logic "0" when using this software-controlled reset. Bit 2 should be set to "0" when using the DECRESET pin.
3-7	–	Set to 0

Table 24f. Viterbi Write Register Address 05H: Encoder Data Input Register

BIT	NAME	FUNCTION
0	ENCDATIN	If: Encoder Peripheral Mode Enabled Then: Accepts Encoder Data (Same Function as pin 33 PLCC or pin 51 VTQFP)
1-7	–	Set to 0

Table 24g. Viterbi Write Register Address 06H: Encoder Control Register 1

BIT	NAME	FUNCTION
0	Encoder Output Mode Selection	1 Puts Encoder in Serial Data Output Mode; 0 Puts Encoder in Parallel Data Output Mode See *Parallel vs. Serial Data Modes* for more information.
1	S/W ENCODER RESET	A transition from "0" to "1" resets decoder functions (similar to pin 37 PLCC or pin 55 VTQFP). Connect pin 37 to logic "0" when using this software-controlled reset. Bit 1 should be set to "0" when using the ENCRESET pin.
2	Encoder Rate $^1/_2$ Enable	1 Makes Encoder Operate with Code Rate $^1/_2$
3	Encoder Rate $^3/_4$ Enable	1 Makes Encoder Operate with Code Rate $^3/_4$
4	Encoder Rate $^1/_3$ Enable	1 Makes Encoder Operate with Code Rate $^1/_3$
5	Encoder Rate $^7/_8$ Enable	1 Makes Encoder Operate with Code Rate $^7/_8$
6-7	–	Set to 0

Table 24h. Viterbi Write Register Address 07H: Encoder Control Register 2

BIT	NAME	FUNCTION
0-2	–	Set to 0
3	ENCODER PERIPHERAL/ DIRECT DATA MODE	1 Makes Encoder Use Processor Bus Interface for Data Input/Output (Peripheral Mode) See *Processor Bus Interface* section of *Q1900 Pin Functions* table. 0 Makes Encoder Use I/O Pins for Data Input/Output (Direct Data Mode) See *Encoder I/O Pins* in *Q1900 Pin Functions* table. Signals Affected: ENCDATIN, C0, C1, C2
4	DIFF ENC ENA	1 Enables Differential Encoder; 0 Disables Differential Encoder The Setting of This Bit Does Not Affect the Operation of the Differential Decoder
5	SCRAMB ENA	1 Enables the Data Scrambler; 0 Disables the Data Scrambler. Data scrambler uses a slightly modified CCITT algorithm preferred by most systems, including INTELSAT.
6	–	Set to 0
7	–	Set to 0

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Table 24i. Viterbi Write Register Address 08H: Normalization Test Bit-Count Input Register

BIT	NAME	FUNCTION
0-7	TCOUNT (Bit 0 is LSB)	Determines the Length of the Synchronization Monitor Test; Requires an Eight-bit Value See *Normalization Rate Monitor Operation* for more information.

Table 24j. Viterbi Write Register Address 09H: Normalization Test Normalize-Count Input Register

BIT	NAME	FUNCTION
0-7	NCOUNT (Bit 0 is LSB)	Determines the Normalization Threshold Level for the Synchronization Monitor Test; Requires an Eight-bit Value See *Normalization Rate Monitor Operation* for more information.

Table 24k. Viterbi Write Register Address 0AH: BER Period Input Register LS Byte

BIT	NAME	FUNCTION: Determines BER Period
0-7	BER PERIOD LS Byte (Bit 0 is LSB)	LS Byte of 24-bit (Three Byte) Value of Period of On-chip BER Monitor See *Monitoring Channel Bit Error Rate* for more information.

Table 24l. Viterbi Write Register Address 0BH: BER Period Input Register CS Byte

BIT	NAME	FUNCTION: Determines BER Period
0-7	BER PERIOD CS Byte (Bit 0 is LSB)	CS Byte of 24-bit (Three Byte) Value of Period of On-chip BER Monitor See *Monitoring Channel Bit Error Rate* for more information.

Table 24m. Viterbi Write Register Address 0CH: BER Period Input Register MS Byte

BIT	NAME	FUNCTION: Determines BER Period
0-7	BER PERIOD MS Byte (Bit 0 is LSB)	MS Byte of 24-bit (Three Byte) Value of Period of On-chip BER Monitor See *Monitoring Channel Bit Error Rate* for more information.

Table 24n. Viterbi Write Register Address 0EH: Processor Decoder Input Clock Register

BIT	NAME	FUNCTION
0-7	DECINCLK (Software-controlled)	Generates (When Given Any Value) a Single DECINCLK Clock Cycle Connect Pin 11 (DECINCLK) to Logic 0 When Using This Software-controlled Clock

Table 24o. Viterbi Write Register Address 0FH: Processor Decoder Output Clock Register

BIT	NAME	FUNCTION
0-7	DECOUTCLK (Software-controlled)	Generates (When Given Any Value) a Single DECOUTCLK Clock Cycle Connect Pin 23 (DECOUTCLK) to Logic 0 When Using This Software-controlled Clock

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Table 24p. Viterbi Write Register Address 11H: Processor Encoder Input Clock Register

BIT	NAME	FUNCTION
0-7	ENCINCLK (Software-controlled)	Generates (When Given Any Value) a Single ENCINCLK Clock Cycle Connect Pin 36 PLCC or pin 66 VTQFP (ENCINCLK) to Logic 0 When Using This Software-controlled Clock

Table 24q. Viterbi Write Register Address 12H: Processor Encoder Output Clock Register

BIT	NAME	FUNCTION
0-7	ENCOUTCLK (Software-controlled)	Generates (When Given Any Value) a Single ENCOUTCLK Clock Cycle Connect pin 44 PLCC or pin 66 VTQFP (ENCOUTCLK) to Logic 0 When Using This Software-controlled Clock

Table 24r. Viterbi Write Register Address 17H: Normalization Test Value Enable Register

BIT	NAME	FUNCTION
0-7	Normalization Test Values Enable (Software-controlled)	Performs Two Functions (When Given Any Value): 1. Enables the Values Previously Loaded into These Registers: Normalization Test Bit Count Register (Write Address 08H) Normalization Test Normalize Count Register (Write Address 09H) 2. Restarts the Normalization Rate Test

Table 24s. Viterbi Write Register Address 18H: BER Test Value Enable Register

BIT	NAME	FUNCTION
0-7	BER Test Values Enable (Software-controlled)	Performs Two Functions (When Given Any Value): 1. Enables the Value Previously Loaded into the BER Period Register (Three Bytes–Write Addresses 0AH, 0BH, and 0CH) 2. Restarts the BER Test

Notes:

1. Write registers 0DH, 10H, and 14H are not used.
2. All bits that are specified as "Set to 0" or "Set to 1" must be set to 0 or 1 for proper operation.
3. Reserved write registers 15H and 16H must be set to 0 for correct operation.

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Table 25a. Trellis Write Register Address 00H: Decoder Data Input Register 1

BIT	NAME	FUNCTION	Same Function as Input Pin PLCC/VTQFP
0	BM00[1]	Branch Metric 00 (CSB)	28/46
1	BM10[1]	Branch Metric 10 (CSB)	22/38
2	BM01[1]	Branch Metric 01 (CSB)	17/32
3	BM11[1]	Branch Metric 11 (CSB)	31/49
4	BM00[0]	Branch Metric 00 (LSB)	29/47
5	BM10[0]	Branch Metric 10 (LSB)	26/44
6	BM01[0]	Branch Metric 01(LSB)	18/32
7	BM11[0]	Branch Metric 11 (LSB)	32/50

Table 25b. Trellis Write Register Address 01H: Decoder Data Input Register 2

BIT	NAME	FUNCTION	Same Function as Input Pin PLCC/VTQFP
0	SECTOR0	Sector Number (LSB)	10/24
1	SECTOR1	Sector Number	9/23
2	SECTOR2	Sector Number	8/22
3	SECTOR3	Sector Number (MSB)	7/21
4	BM00[2]	Branch Metric 00 (MSB)	27/45
5	BM10[2]	Branch Metric 10 (MSB)	19/33
6	BM01[2]	Branch Metric 01(MSB)	16/30
7	BM11[2]	Branch Metric 11 (MSB)	30/48

Table 25c. Trellis Write Register Address 02H: Decoder Control Register 1

BIT	NAME	FUNCTION
0-5	-	Set to 0
6-7	-	Set to 1

Table 25d. Trellis Write Register Address 03H: Decoder Control Register 2

BIT	NAME	FUNCTION
0	-	Set to 1
1-2	-	Set to 0
3	Decoder Peripheral/ Direct Data Mode	1 Makes Decoder Use Processor Bus Interface for Data Input/Output (Peripheral Mode) See *Processor Bus Interface* section in the *Q1900 Pin Functions* tables. 0 Makes Decoder Use Dedicated I/O Pins for Data Input/Output (Direct Data Mode) See *Decoder I/O Pins* in *Q1900 Pin Functions* tables.
4	DIF DEC ENA	1 Enables the Differential Decoder and Ambiguity Resolver Decoder; 0 Disables the Differential Decoder and Ambiguity Resolver decoder (The setting of this bit does not affect the operation of the differential encoder and ambiguity resolver encoder.)
5	-	Set to 0
6	-	Set to 0
7	8-PSK/16-PSK	1 Selects Rate $^2/_3$ 8-PSK Operation; 0 Selects Rate $^3/_4$ 16-PSK Operation

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Table 25e. Trellis Write Register Address 04H: Decoder Control Register 3

BIT	NAME	FUNCTION
0	-	Set to 1
1	-	Set to 0
2	Software Decoder RESET	A transition from 0 to 1 resets decoder functions. Connect pin 13 PLCC or pin 27 VTQFP to logic 0 when using this software-controlled reset. Bit 2 should be set to 0 when using the DECRESET pin.
3	-	Set to 0

Table 25f. Trellis Write Register Address 05H: Encoder Data Input Register

BIT	NAME	FUNCTION
0	ENCDAT[0]	If: Encoder Peripheral Mode Enabled Then: Accepts Encoder Data (Same Function as Pin 33 PLCC or Pin 51 VTQFP)
1	ENCDAT[1]	If: Encoder Peripheral Mode Enabled Then: Accepts Encoder Data (Same Function as Pin 35 PLCC or Pin 53 VTQFP)
2	ENCDAT[2]	If: Encoder Peripheral Mode Enabled Then: Accepts Encoder Data (Same Function as Pin 34 PLCC or Pin 52 VTQFP)
3-6	-	Set to 0
7	-	Set to 0

Table 25g. Trellis Write Register Address 06H: Encoder Control Register 1

BIT	NAME	FUNCTION
0	-	Set to 0
1	Software Decoder RESET	A transition from 0 to 1 resets decoder functions. Connect Pin 37 PLCC or Pin 55 VTQFP to logic 0 when using this software-controlled reset. Bit 1 should be set to 0 when using the ENCRESET pin.
2	-	Set to 1
3-6	-	Set to 0
7	-	Set to 1

Table 25h. Trellis Write Register Address 07H: Encoder Control Register 2

BIT	NAME	FUNCTION
0-2	-	Set to 0
3	Encoder Peripheral/ Direct Data Mode	1 Makes Encoder Use Processor Bus Interface for Data Input/Output (Peripheral Mode) See *Processor Bus Interface* section in the *Q1900 Pin Functions* tables. 0 Makes Encoder Use Dedicated I/O Pins for Data Input/Output (Direct Data Mode) See *Encoder I/O Pins* in *Q1900 Pin Functions* tables.
4	DIF ENC ENA	1 Enables the Differential Encoder and Ambiguity Resolver Encoder; 0 Disables the Differential Encoder and Ambiguity Resolver Encoder. (The setting of this bit does not affect the operation of the differential decoder and ambiguity resolver decoder.)
5	-	Set to 0
6	-	Set to 0
7	8-PSK/16-PSK	0 Selects Rate $^2/_3$ 8-PSK Operation; 1 Selects Rate $^3/_4$ 16-PSK Operation

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Table 25i. Trellis Write Register Address 08H: Normalization Test Bit-Count Input Register

BIT	NAME	FUNCTION
0-7	T COUNT (Bit 0 is LSB)	Determines the Length of the Synchronization Monitor Test; Requires an 8-bit Value See *Normalization Rate Monitor Operation* for more information.

Table 25j. Trellis Write Register Address 09H: Normalization Test Normalize-Count Input Register

BIT	NAME	FUNCTION
0-7	N COUNT (Bit 0 is LSB)	Determines the Normalization Threshold for the Synchronization Monitor Test; Requires an 8-bit Value See *Normalization Rate Monitor Operation* for more information.

Table 25k. Trellis Write Register Address 0EH: Processor Decoder Input Clock Register

BIT	NAME	FUNCTION
0-7	DECINCLK (Software-controlled)	Generates (When Given Any Value) a Single DECINCLK Clock Cycle Connect Pin 11 PLCC or Pin 25 VTQFP (DECINCLK) to Logic 0 When Using This Software-controlled Clock

Table 25l. Trellis Write Register Address 0FH: Processor Decoder Output Clock Register

BIT	NAME	FUNCTION
0-7	DECOUTCLK (Software-controlled)	Generates (When Given Any Value) a Single DECOUTCLK Clock Cycle Connect Pin 23 PLCC or Pin 39 VTQFP (DECOUTCLK) to Logic 0 When Using This Software-controlled Clock

Table 25m. Trellis Write Register Address 11H: Processor Encoder Input Clock Register

BIT	NAME	FUNCTION
0-7	ENCINCLK (Software-controlled)	Generates (When Given Any Value) a Single ENCINCLK Clock Cycle Connect Pin 36 PLCC or Pin 54 VTQFP (ENCINCLK) to Logic 0 When Using This Software-controlled Clock

Table 25n. Trellis Write Register Address 12H: Processor Encoder Output Clock Register

BIT	NAME	FUNCTION
0-7	ENCOUTCLK (Software-controlled)	Generates (When Given Any Value) a Single ENCOUTCLK Clock Cycle Connect Pin 44 PLCC or Pin 66 VTQFP (ENCOUTCLK) to Logic 0 When Using This Software-controlled Clock

Table 25o. Trellis Write Register Address 15H: Reserve Registers

BIT	NAME	FUNCTION
0-7	-	Set to 0

Table 25p. Trellis Write Register Address 16H: Reserve Registers

BIT	NAME	FUNCTION
0-7	-	Set to 0

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Table 25q. Trellis Write Register Address 17H: Normalization Test Value-Enable Register

BIT	NAME	FUNCTION
0-7	Norm Test Values Enable (Software-controlled)	Performs Two Functions (When Given Any Value): 1) Enables the Values Previously Loaded into These Registers: Normalization Test Bit-Count Register (Write Address 08H) Normalization Test Normalize-Count Register (Write Address 09H) 2) Restarts the Normalization Rate Test

Notes:

1. Write registers 0AH, 0BH, 0CH, 0DH, 10H, 13H, and 14H are not used.
2. All bits that are specified as "Set to 0" or "Set to 1" must be set to zero or one for proper operation.
3. Reserved write registers 15H and 16H must be set to zero for correct operation.

PIN DESCRIPTIONS

Figures 41 and 42 show the location of the input and output pins for Viterbi Mode and Trellis Mode for the 84-pin PLCC package. Tables 26 and 27 describe the function of each pin for the Viterbi Mode and the Trellis Mode for the PLCC package.

Figures 43 and 44 show the location of the input and output pins for Viterbi Mode and Trellis Mode for the 100-pin VTQFP package. Tables 28 and 29 describe the function of each pin for the Viterbi Mode and Trellis Mode for the 100-pin VTQFP package.

Figure 41. 84-PIN Pinout for PLCC Packaging for Viterbi Mode

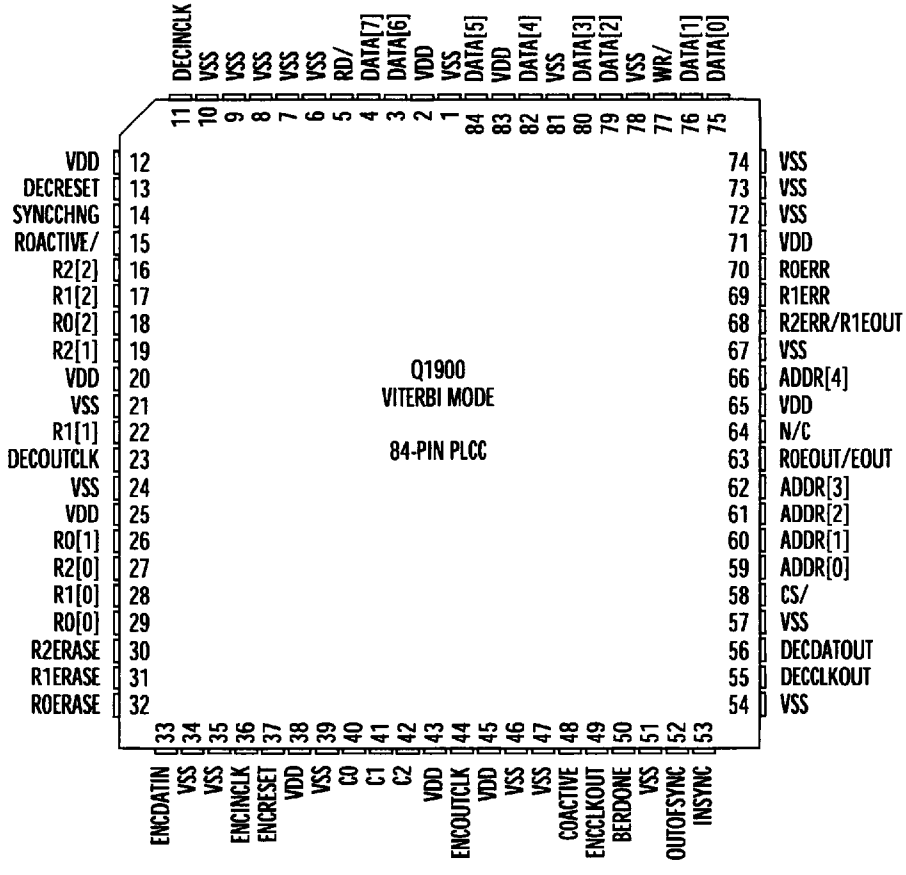

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Table 26. Q1900 PLCC Pin Functions for Viterbi Mode

SECTION	NAME	PIN #	TYPE	FUNCTION	NOTES
Encoder I/O Pins	ENCDATIN	33	INPUT	Encoder Data Input	
	ENCINCLK	36	INPUT	Encoder Data Input Clock	
	ENCOUTCLK	44	INPUT	Encoder Symbol Output Clock	
	ENCCLKOUT	49	OUTPUT	Encoder Symbol Clock Output	
	COACTIVE	48	OUTPUT	Indicates Output of C0 Bit	1
	C0	40	OUTPUT	Encoder Symbol C0	2
	C1	41	OUTPUT	Encoder Symbol C1	
	C2	42	OUTPUT	Encoder Symbol C2	3
	ENCRESET	37	INPUT	Master Encoder Reset (Active High)	
Decoder I/O Pins	R0[0], R0[1], R0[2]	29 (LSB), 26, 18	INPUT	Decoder R0 Input Symbol	4
	R1[0], R1[1], R1[2]	28 (LSB), 22, 17	INPUT	Decoder R1 Input Symbol	
	R2[0], R2[1], R2[2]	27 (LSB), 19, 16	INPUT	Decoder R2 Input Symbol	5
	R0ACTIVE/	15	INPUT	Low Selects R0 as Input	6
	R0ERASE	32	INPUT	High Erases R0 Symbol	13
	R1ERASE	31	INPUT	High Erases R1 Symbol	13
	R2ERASE	30	INPUT	High Erases R2 Symbol	13
	DECINCLK	11	INPUT	Decoder Symbol Input Clock	
	DECOUTCLK	23	INPUT	Decoder Data Output Clock	
	DECCLKOUT	55	OUTPUT	Decoder Data Clock Output	
	DECRESET	13	INPUT	High Master Resets Decoder Circuitry	
	SYNCCHNG	14	INPUT	Decoder Sync Change Control (Active High)	
	OUTOFSYNC	52	OUTPUT	Sync Monitor Test Failure	7
	INSYNC	53	OUTPUT	Sync Monitor Test Pass	8
	DECDATOUT	56	OUTPUT	Decoder Data Output	
	R0ERR	70	OUTPUT	Indicates Channel Bit Errors of R0	9
	R1ERR	69	OUTPUT	Indicates Channel Bit Errors of R1	9
	R2ERR/R1EOUT	68	OUTPUT	Indicates Channel Bit Errors	9, 10
	R0EOUT/EOUT	63	OUTPUT	Indicates Error Signal Timing	11
Processor Bus Interface Pins	DATA[0] – DATA[7]	75, 76, 79, 80, 82, 84, 3, 4	I/O	Processor Interface Data Bus (DATA[0] is LSB)	
	ADDR[0] – ADDR[4]	59 (LSB), 60, 61, 62, 66	INPUT	Processor Interface Address Bus	
	WR/	77	INPUT	Processor Interface Write Strobe (Active Low)	
	RD/	5	INPUT	Processor Interface Read Strobe (Active Low)	
	CS/	58	INPUT	Processor Interface Chip Select (Active Low)	
	BERDONE	50	OUTPUT	BER Test Indicator	12
Voltage Supply Pins	VDD (+5V)	2, 12, 20, 25, 38, 43, 45, 65, 71, 83	POWER		
	VSS	1, 6, 7, 8, 9, 10, 21, 24, 34, 35, 39, 46 47, 51, 54, 57, 67, 72, 73, 74, 78, 81	GROUND		
	N/C	64	UNUSED	Make No Connection to This Pin	

Notes:
1. In Serial Mode, pin 48 is active High during the period of ENCCLKOUT when C0 encoded bit is output.
2. In Serial Mode, pin 40 serves as the encoder output for all output symbols.
3. In rate 3/4 or 7/8, pin 42 is active High during output of first symbol of puncture pattern.
4. In Serial Mode, pins 29, 26, and 18 serve as the decoder input for all input symbols.
5. Decoder R2 (input pins 27, 19, 16) is used only for rate 1/3 parallel operation.
6. In Serial Mode, a Low on pin 15 indicates the symbol at R0 is the current decoder input symbol.
7. Pin 52 pulses High for two periods of DECCLKOUT when the internal synchronization monitor test fails.
8. Pin 53 pulses High for two periods of DECCLKOUT when the internal synchronization monitor test passes.
9. Pins 70, 69, and 68 indicate channel bit errors bit-by-bit for R0, R1, and R2, respectively (active High for one period of DECCLKOUT).
10. Rate 1/3: Pin 68 indicates channel bit errors. Rate 1/2: Pin 68 indicates R1ERASE delayed to align to R1ERR output.
11. Rate 1/3: Pin 63 indicates logic OR of R0ERASE/R1ERASE/R2ERASE delayed to align with R0ERR/R1ERR/R2ERR. Rate 1/2: Pin 63 indicates R0ERASE delayed to align to R0ERR output.
12. Pin 50 indicates completion of internal BER measurement test (active High.)
13. The R0ERASE (pin 32), R1ERASE (pin 31), and R2ERASE (pin 30) erase inputs must be connected to logic "0" when symbol erasures are not being used. Symbol erasure inputs are used to implement punctured code rates other than the rate 3/4 and 7/8 patterns implimented internally on the device.

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Figure 42. 84-pin Pinout for PLCC Packaging for Trellis Mode

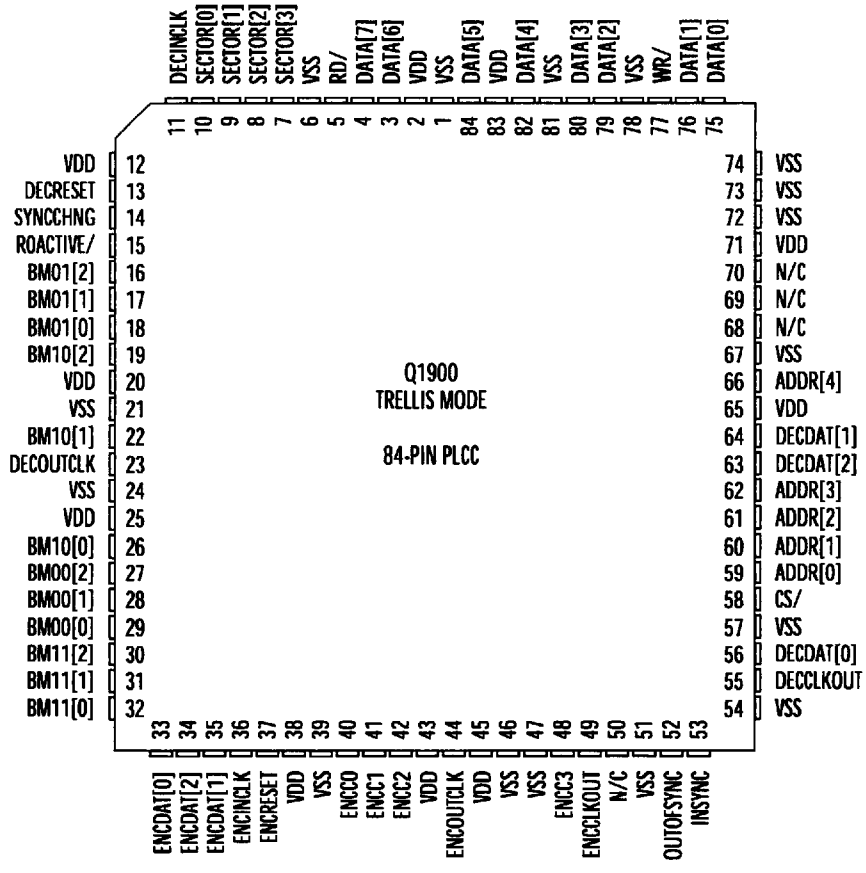

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Table 27. Q1900 PLCC Pin Functions for Trellis Mode

SECTION	NAME	PIN #	TYPE	FUNCTION	NOTES
Encoder I/O Pins	ENCDAT[0]	33	INPUT	Encoder data input (LSB)	
	ENCDAT[1]	35	INPUT	Encoder data input (CSB)	
	ENCDAT[2]	34	INPUT	Encoder data input (MSB)	1
	ENCINCLK	36	INPUT	Encoder data input clock	
	ENCOUTCLK	44	INPUT	Encoder symbol output clock	
	ENCLKOUT	49	OUTPUT	Encoder symbol clock output	
	ENCC0	40	OUTPUT	Encoder output (LSB)	
	ENCC1	41	OUTPUT	Encoder output	
	ENCC2	42	OUTPUT	Encoder output	
	ENCC3	48	OUTPUT	Encoder output (MSB)	2
	ENCRESET	37	INPUT	Master encoder reset (active high)	
Decoder I/O Pins	ROACTIVE/	15	INPUT	Set to logic high	
	BM00[0,1,2]	29 (LSB), 28, 27	INPUT	Branch metric input 00	
	BM01[0,1,2]	18 (LSB), 17, 16	INPUT	Branch metric input 01	
	BM10[0,1,2]	26 (LSB), 22, 19	INPUT	Branch metric input 10	
	BM11[0,1,2]	32 (LSB), 31, 30	INPUT	Branch metric input 11	
	SECTOR[0]	10	INPUT	Sector number (LSB)	
	SECTOR[1]	9	INPUT	Sector number	
	SECTOR[2]	8	INPUT	Sector number	
	SECTOR[3]	7	INPUT	Sector number (MSB)	1
	DECINCLK	11	INPUT	Decoder symbol input clock	
	DECOUTCLK	23	INPUT	Decoder data output clock	
	DECCLKOUT	55	OUTPUT	Decoder data clock output	
	DECRESET	13	INPUT	High master resets decoder circuitry	
	SYNCCHNG	14	INPUT	Decoder sync change control (active high)	
	OUTOFSYNC	52	OUTPUT	Sync monitor test failure	3
	INSYNC	53	OUTPUT	Sync monitor test pass	4
	DECDAT[0]	56	OUTPUT	Decoder data output (LSB)	
	DECDAT[1]	64	OUTPUT	Decoder data output (CSB)	
	DECDAT[2]	63	OUTPUT	Decoder data output (MSB)	2
Processor Bus Interface Pins	DATA[0] – DATA[7]	75, 76, 79, 80, 82, 84, 3, 4	I/O	Processor interface data bus (DATA[0] is LSB)	
	ADDR[0] – ADDR[4]	59 (LSB), 60, 61, 62, 66	INPUT	Processor interface address bus	
	WR/	77	INPUT	Processor interface write strobe (active low)	
	RD/	5	INPUT	Processor interface read strobe (active low)	
	CS/	58	INPUT	Processor interface chip select (active low)	
Voltage Supply Pins	VDD (+5V)	2, 12, 20, 25, 38, 43, 45, 65, 71, 83	POWER		
	VSS	1, 6, 21, 24, 39, 46, 47, 51, 54, 57, 67, 72, 73, 74, 78, 81	GROUND		
	N/C	50, 68, 69, 70	UNUSED	Make no connection to these pins.	

Notes: 1. This input is used only for rate ¾ 16-PSK mode. This input should be set to a logic low when not used.
2. This is valid for rate ¾ 16-PSK mode only.
3. Pin 52 pulses high for two periods of DECCLKOUT when the internal synchronization monitor test fails.
4. Pin 53 pulses high for two periods of DECCLKOUT when the internal synchronization monitor test passes.

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Figure 43. 100-PIN Pinout for VTQFP Packaging for Viterbi Mode

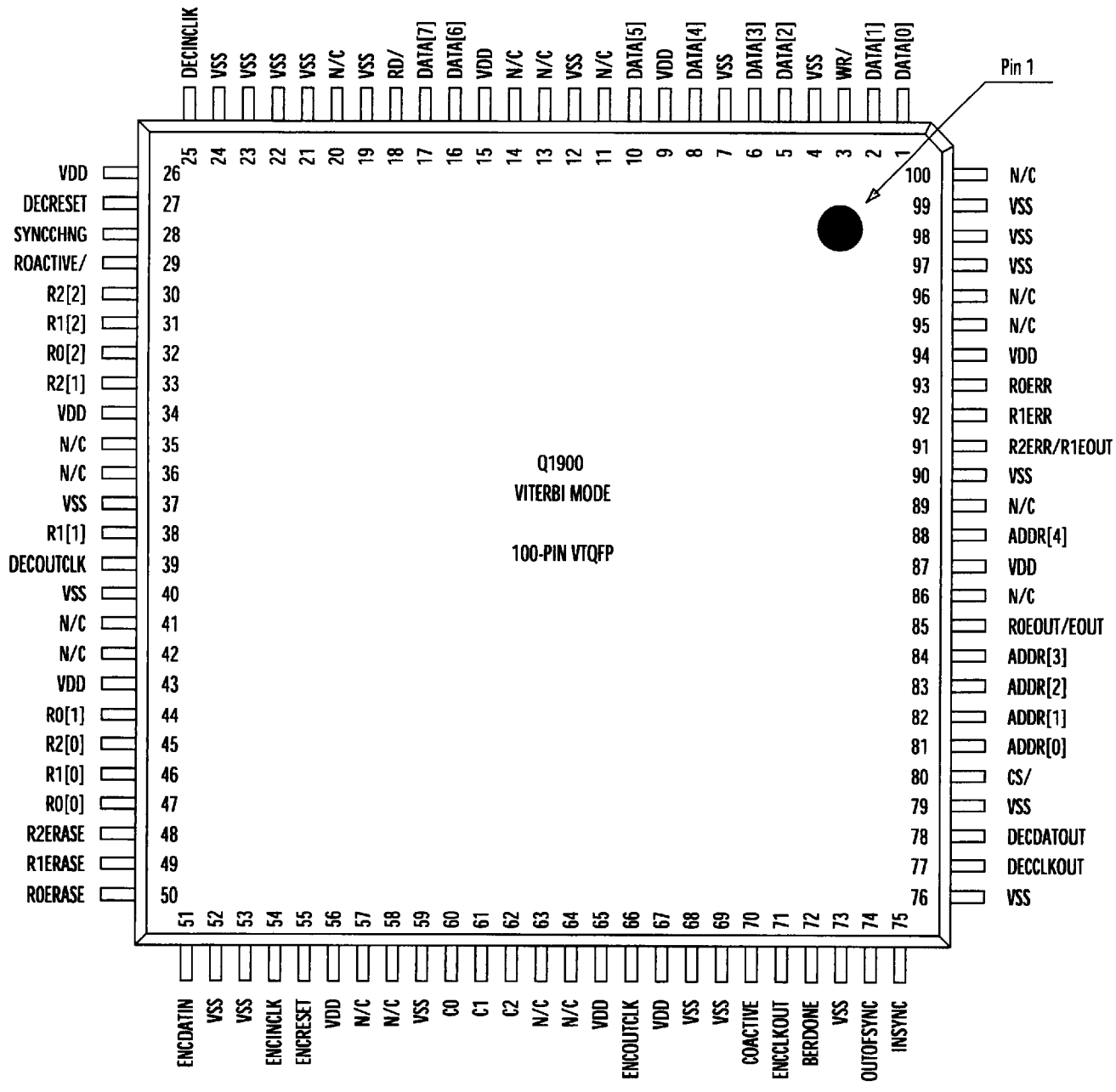

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Table 28. Q1900 VTQFP Pin Functions for Viterbi Mode

SECTION	NAME	PIN #	TYPE	FUNCTION	NOTES
Encoder I/O Pins	ENCDATIN	51	INPUT	Encoder Data Input	
	ENCINCLK	54	INPUT	Encoder Data Input Clock	
	ENCOUTCLK	66	INPUT	Encoder Symbol Output Clock	
	ENCCLKOUT	71	OUTPUT	Encoder Symbol Clock Output	
	COACTIVE	70	OUTPUT	Indicates Output of C0 Bit	1
	C0	60	OUTPUT	Encoder Symbol C0	2
	C1	61	OUTPUT	Encoder Symbol C1	
	C2	62	OUTPUT	Encoder Symbol C2	3
	ENCRESET	55	INPUT	Master Encoder Reset (Active High)	
Decoder I/O Pins	R0[0], R0[1], R0[2]	47 (LSB), 44, 32	INPUT	Decoder R0 Input Symbol	4
	R1[0], R1[1], R1[2]	46 (LSB), 38, 31	INPUT	Decoder R1 Input Symbol	
	R2[0], R2[1], R2[2]	45 (LSB), 33, 30	INPUT	Decoder R2 Input Symbol	5
	R0ACTIVE/	29	INPUT	Low Selects R0 as Input	6
	R0ERASE	50	INPUT	High Erases R0 Symbol	13
	R1ERASE	49	INPUT	High Erases R1 Symbol	13
	R2ERASE	48	INPUT	High Erases R2 Symbol	13
	DECINCLK	25	INPUT	Decoder Symbol Input Clock	
	DECOUTCLK	39	INPUT	Decoder Data Output Clock	
	DECCLKOUT	77	OUTPUT	Decoder Data Clock Output	
	DECRESET	27	INPUT	High Master Resets Decoder Circuitry	
	SYNCCHNG	28	INPUT	Decoder Sync Change Control (Active High)	
	OUTOFSYNC	74	OUTPUT	Sync Monitor Test Failure	7
	INSYNC	75	OUTPUT	Sync Monitor Test Pass	8
	DECDATOUT	78	OUTPUT	Decoder Data Output	
	R0ERR	93	OUTPUT	Indicates Channel Bit Errors of R0	9
	R1ERR	92	OUTPUT	Indicates Channel Bit Errors of R1	9
	R2ERR/R1EOUT	91	OUTPUT	Indicates Channel Bit Errors	9, 10
	R0EOUT/EOUT	85	OUTPUT	Indicates Error Signal Timing	11
Processor Bus Interface Pins	DATA[0] – DATA[7]	1, 2, 5, 6, 8, 10, 16, 17	I/O	Processor Interface Data Bus (DATA[0] is LSB)	
	ADDR[0] – ADDR[4]	81 (LSB), 82, 83, 84, 88	INPUT	Processor Interface Address Bus	
	WR/	3	INPUT	Processor Interface Write Strobe (Active Low)	
	RD/	18	INPUT	Processor Interface Read Strobe (Active Low)	
	CS/	80	INPUT	Processor Interface Chip Select (Active Low)	
	BERDONE	72	OUTPUT	BER Test Indicator	12
Voltage Supply Pins	VDD	9, 15, 26, 34, 43, 56, 65, 67, 87, 94	POWER		
	VSS	4, 7, 12, 19, 21, 22, 23, 24, 37, 40, 52, 53, 59,68, 69, 73, 76, 79, 90, 97, 98, 99	GROUND		
	N/C	11, 13, 14, 20, 35, 36,41, 42, 57, 58, 63, 64, 86, 89, 95, 96, 100	UNUSED	Make No Connection to This Pin	

Notes: 1. In Serial Mode, pin 70 is active High during the period of ENCCLKOUT when C0 encoded bit is output.
2. In Serial Mode, pin 60 serves as the encoder output for all output symbols.
3. In rate 3/4 or 7/8, pin 62 is active High during output of first symbol of puncture pattern.
4. In Serial Mode, pins 47, 44, and 32 serve as the decoder input for all input symbols.
5. Decoder R2 (input pins 45, 33, 30) is used only for rate 1/3 parallel operation.
6. In Serial Mode, a Low on pin 29 indicates the symbol at R0 is the current decoder input symbol.
7. Pin 74 pulses High for two periods of DECCLKOUT when the internal synchronization monitor test fails.
8. Pin 75 pulses High for two periods of DECCLKOUT when the internal synchronization monitor test passes.
9. Pins 93, 92, and 91 indicate channel bit errors bit-by-bit for R0, R1, and R2, respectively (active High for one period of DECCLKOUT).
10. Rate 1/3: Pin 91 indicates channel bit errors. Rate 1/2: Pin 91 indicates R1ERASE delayed to align to R1ERR output.
11. Rate 1/3: Pin 85 indicates logic OR of R0ERASE/R1ERASE/R2ERASE delayed to align with R0ERR/R1ERR/R2ERR. Rate 1/2: Pin 85 indicates R0ERASE delayed to align to R0ERR output.
12. Pin 72 indicates completion of internal BER measurement test (active High.)
13. The R0ERASE (pin 50), R1ERASE (pin 49), and R2ERASE (pin 48) erase inputs must be connected to logic "0" when symbol erasures are not being used. Symbol erasure inputs are used to implement punctured code rates other than the rate 3/4 and 7/8 patterns implimented internally on the device.

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Figure 44. 100-pin Pinout for VTQFP Package for Trellis Mode

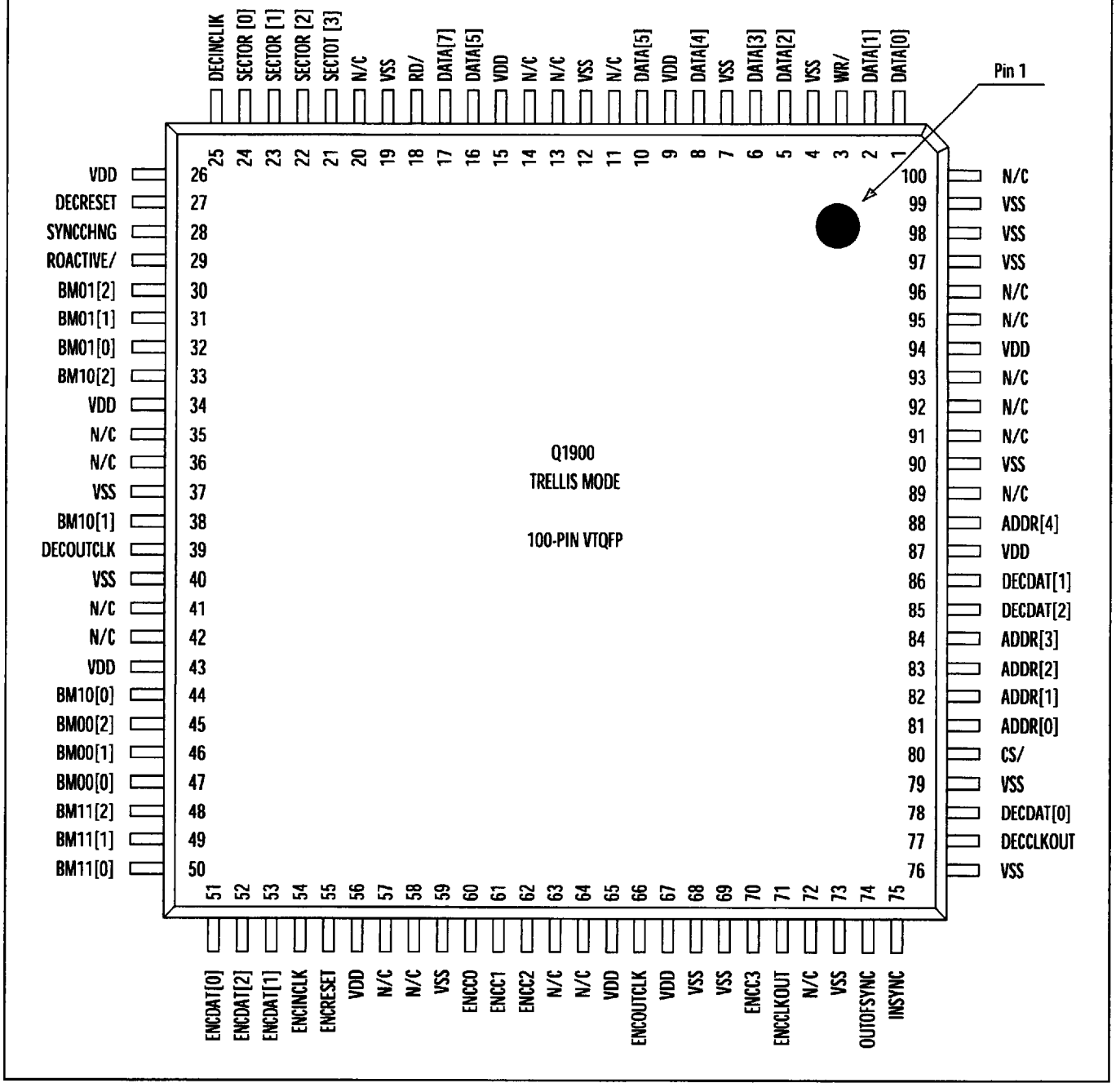

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Table 29. Q1900 VTQFP Pin Functions for Trellis Mode

SECTION	NAME	PIN #	TYPE	FUNCTION	NOTES
Encoder I/O Pins	ENCDAT[0]	51	INPUT	Encoder data input (LSB)	
	ENCDAT[1]	53	INPUT	Encoder data input (CSB)	
	ENCDAT[2]	52	INPUT	Encoder data input (MSB)	1
	ENCINCLK	54	INPUT	Encoder data input clock	
	ENCOUTCLK	66	INPUT	Encoder symbol output clock	
	ENCLKOUT	71	OUTPUT	Encoder symbol clock output	
	ENCC0	60	OUTPUT	Encoder output (LSB)	
	ENCC1	61	OUTPUT	Encoder output	
	ENCC2	62	OUTPUT	Encoder output	
	ENCC3	70	OUTPUT	Encoder output (MSB)	2
	ENCRESET	55	INPUT	Master encoder reset (active high)	
Decoder I/O Pins	ROACTIVE/	29	INPUT	Set to logic high	
	BM00[0,1,2]	47 (LSB), 46, 45	INPUT	Branch metric input 00	
	BM01[0,1,2]	32 (LSB), 31, 30	INPUT	Branch metric input 01	
	BM10[0,1,2]	44 (LSB), 38, 33	INPUT	Branch metric input 10	
	BM11[0,1,2]	50 (LSB), 49, 48	INPUT	Branch metric input 11	
	SECTOR[0]	24	INPUT	Sector number (LSB)	
	SECTOR[1]	23	INPUT	Sector number	
	SECTOR[2]	22	INPUT	Sector number	
	SECTOR[3]	21	INPUT	Sector number (MSB)	1
	DECINCLK	25	INPUT	Decoder symbol input clock	
	DECOUTCLK	39	INPUT	Decoder data output clock	
	DECCLKOUT	77	OUTPUT	Decoder data clock output	
	DECRESET	27	INPUT	High master resets decoder circuitry	
	SYNCCHNG	28	INPUT	Decoder sync change control (active high)	
	OUTOFSYNC	74	OUTPUT	Sync monitor test failure	3
	INSYNC	75	OUTPUT	Sync monitor test pass	4
	DECDAT[0]	78	OUTPUT	Decoder data output (LSB)	
	DECDAT[1]	86	OUTPUT	Decoder data output (CSB)	
	DECDAT[2]	85	OUTPUT	Decoder data output (MSB)	2
Processor Bus Interface Pins	DATA[0] – DATA[7]	1, 2, 5, 6, 8, 10, 16, 17	I/O	Processor interface data bus (DATA[0] is LSB)	
	ADDR[0] – ADDR[4]	81, 82, 83, 84, 88	INPUT	Processor interface address bus	
	WR/	3	INPUT	Processor interface write strobe (active low)	
	RD/	18	INPUT	Processor interface read strobe (active low)	
	CS/	80	INPUT	Processor interface chip select (active low)	
Voltage Supply Pins	VDD (+5V)	9, 15, 26, 34, 43, 56, 65, 67, 87, 94	POWER		
	VSS	4, 7, 12, 19, 37, 40, 59, 68, 69, 73, 76, 79, 90, 97, 98, 99	GROUND		
	N/C	11, 13, 14, 20, 35, 36, 41, 42, 57, 58, 63, 64, 72, 89, 91, 92, 93, 95, 96, 100	UNUSED	Make no connection to these pins.	

Notes:

1. This input is used only for rate 3/4 16-PSK mode. This input should be set to a logic low when not used.
2. This is valid for rate 3/4 16-PSK mode only.
3. Pin 74 pulses high for two periods of DECCLKOUT when the internal synchronization monitor test fails.
4. Pin 75 pulses high for two periods of DECCLKOUT when the internal synchronization monitor test passes.

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ELECTRICAL SPECIFICATIONS

ABSOLUTE MAXIMUM RATING

Tables 30 and 31 provide the absolute maximum ratings and device thermal ratings for the Q1900. Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. The absolute Maximum Ratings are stress ratings only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Table 30. Absolute Maximum Ratings

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS
Storage Temperature	T_S	-65	–	+150	°C
Junction Temperature	T_J	–	–	+150	°C
Voltage on Any Input Pin		-0.3	–	V_{DD} + 0.3	V
Voltage on V_{DD} and on Any Output Pin		-0.3	–	+7	V

Table 31. Device Thermal Ratings

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS
Junction to Ambient Resistance (Still Air)					
84 Pin PLCC Package	θ_{ja}	–	+27	–	°C/W
100 Pin VTQFP Package	θ_{ja}	–	+51	–	°C/W
Junction to Case Resistance					
84 Pin PLCC Package	θ_{jc}	–	+12	–	°C/W
100 Pin VTQFP Package	θ_{jc}	–	+19	–	°C/W

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DC ELECTRICAL CHARACTERISTICS

Table 32 shows the DC electrical characteristics for the Q1900.

Table 32. DC Electrical Characteristics

PARAMETER	SYMBOL	MIN	MAX	UNITS	COMMENTS	NOTES
Supply Voltage	V_{DD}	4.5	5.5	V		
Operating Temperature, Case	T_C	-55	+ 125	°C		
High-Level Input Voltage	V_{IH}	2.0	VDD + 0.3	V		
Low-Level Input Voltage	V_{IL}	-0.3	0.8	V		
Input Low Leakage Current	I_{IL}	-1.0	–	µA	$V_{IN} = V_{SS}$; $V_{DD} = V_{DD(MAX)}$	
Input High Leakage Current	I_{IH}	–	1.0	µA	$V_{IN} = V_{DD} = V_{DD(MAX)}$	
Input High Leakage Current with Pull-down	I_{IHPD}	20	120	µA	$V_{IN} = V_{DD} = V_{DD(MAX)}$	1, 6
Tri-state Leakage Current High	I_{OZH}	–	1.0	µA	$V_{IN} = V_{DD} = V_{DD(MAX)}$	2, 7
Tri-state Leakage Current Low	I_{OZL}	-1.0	–	µA	$V_{IN} = V_{SS}$; $V_{DD} = V_{DD(MAX)}$	2, 7
High-Level Output Voltage	V_{OH}	VDD - 0.8	–	V		3, 8
Low-Level Output Voltage	V_{OL}	–	0.4	V		4, 9
Output Short Circuit Current	I_{OS}	–	300	mA		5, 10
Input Capacitance	C_{IN}	5	15	pF		
Power Dissipation (Quiescent)	P_D	–	0.2	W		
Power Dissipation (@ 30 MHz)	P_D	–	0.8	W	Parallel Operating Modes	

Notes:

For Q1900 84-Pin PLCC Package:

1. Pins 11, 23, 36, and 44 have pull-down devices. All other inputs do not.
2. For DATA[0] – DATA[7].
3. Pins 50, 52, and 53 have I_{OH} = - 8mA. All other output pins have I_{OH} = -16mA.
4. Pins 50, 52, and 53 have I_{OL} = + 8mA. All other output pins have I_{OL} = + 16mA.
5. Not more than one output shorted at a time for less than one second.

For Q1900 100-Pin VTQFP Package:

6. Pins 25, 39, 54, and 66 have pull-down devices. All other inputs do not.
7. For Data [0] - DATA [7]:
8. Pins 72, 74, and 75 have I_{OH} = -8mA. All other output pins have I_{OH} = -16mA.
9. Pins 72, 74, and 75 have I_{OL} = +8mA. All other output pins have I_{OL} = +16 mA.
10. Not more than one output shorted at a time for less than one second.

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TIMING CHARACTERISTICS

Figures 45 - 47 and Tables 33 - 35 provide the timing specifications for the Q1900. These specifications are valid only for the recommended operating conditions.

Figure 45. Processor Interface Timing Diagram

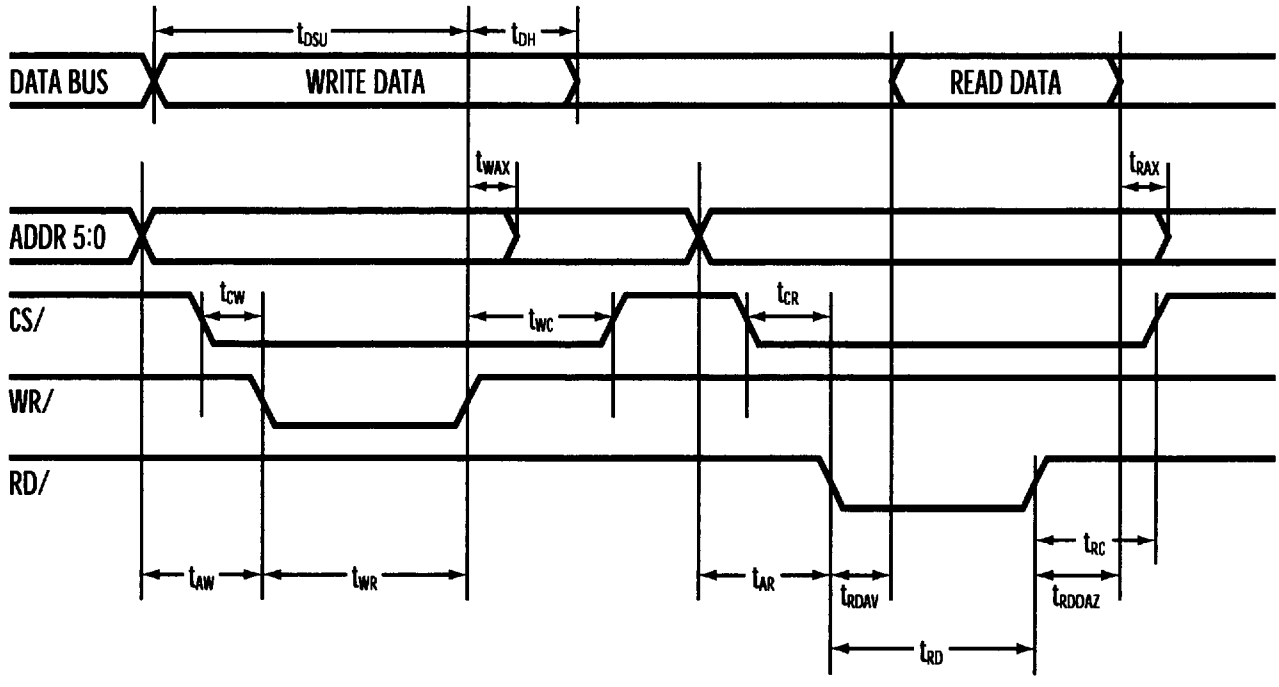

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Table 33a. Processor Interface Timing Parameters (Write Signal)

PARAMETER (Write Signal)	SYMBOL	MIN*	MAX*	UNITS
Data Setup to WR/ Rising	t_{DSU}	20	–	ns
Data Hold After WR/ Rising	t_{DH}	5	–	ns
CS/ Falling to WR/ Falling	t_{CW}	15	–	ns
Address Hold After WR/ Rising	t_{WAX}	5	–	ns
CS/ Hold After WR/ Rising	t_{WC}	5	–	ns
Address Valid to WR/ Falling	t_{AW}	20	–	ns
WR/ Period	t_{WR}	80	–	ns

Table 33b. Processor Interface Timing Parameters (Read Signal)

PARAMETER (Read Signal)	SYMBOL	MIN*	MAX*	UNITS
Address Valid to RD/ Falling	t_{AR}	20	–	ns
RD/ Period	t_{RD}	80	–	ns
CS/ Falling to RD/ Falling	t_{CR}	15	–	ns
Address Hold After WR/ rising	t_{RAX}	5	–	ns
CS/ Hold After RD/ Rising	t_{RC}	5	–	ns
RD/ Falling to DATA Valid	t_{RDAV}	–	60	ns
Data Hold After RD/ Rising	t_{RDDAZ}	0	15	ns

* T_C = -55 to 125°C, V_{DD} = 4.5 to 5.5 V

Values assume a 75 pF load on the data bus pins. All timings are measured from the switching level of 1.4 V.

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Figure 46. Encoder Clock Timing Diagram

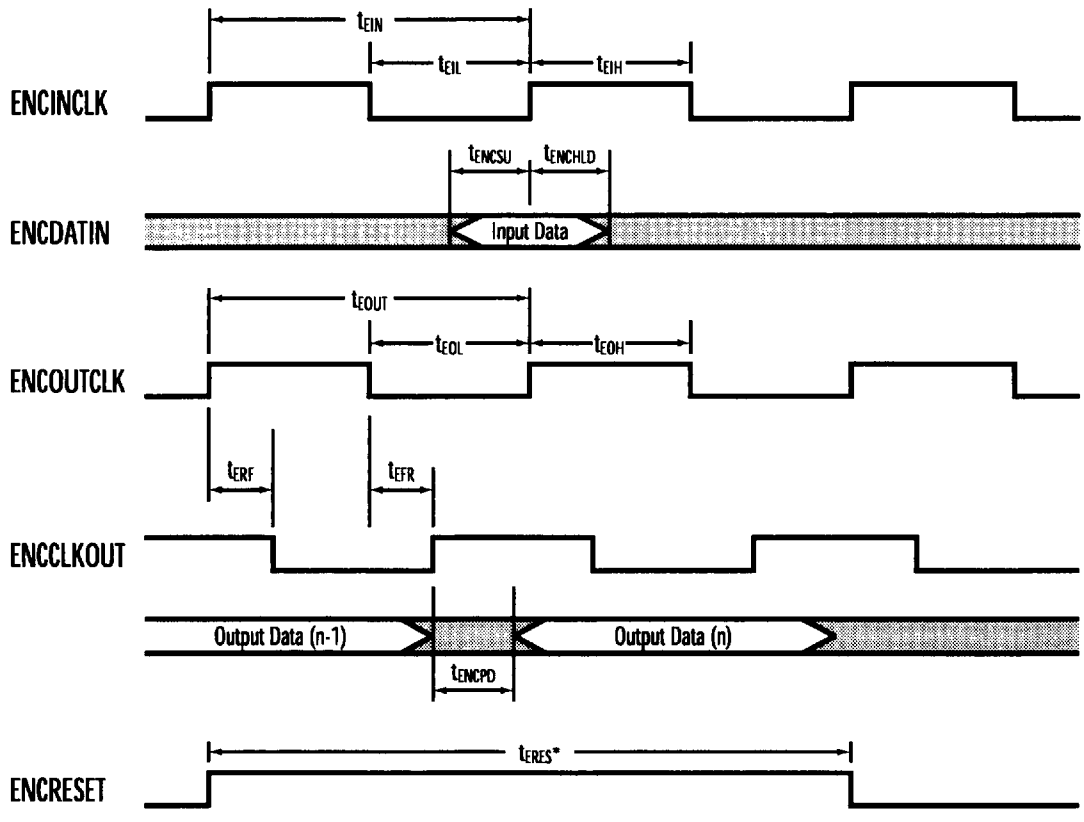

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Table 34a. Encoder Clock Timing Parameters for Viterbi Mode (all Parallel Rates)

PARAMETER	SYMBOL	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	UNITS
Supply Voltage	V_{DD}	4.5	5.5	4.5	5.5	4.75	5.5	5.0	5.5	V
Operating Temperature, Case	T_C	-55	125	-40	85	-40	85	-40	85	°C
Max Frequency (=1/t_{EIN})	ENCINCLK	–	20	–	25	–	28	–	30	MHz
Encoder IN Clock Period	t_{EIN}	50	–	40	–	35.7	–	33.3	–	ns
ENCDATIN Setup to ENCINCLK Rise	t_{ENCSU}	5	–	5	–	5	–	5	–	ns
ENCDATIN Hold After ENCINCLK Rise	t_{ENCHLD}	5	–	5	–	5	–	5	–	ns
ENCINCLK Clock Low & High Period	t_{EIL} & t_{EIH}	20	–	16	–	14.3	–	13.3	–	ns
Max Frequency (=1/t_{EOUT})	ENCOUTCLK		20	–	25	–	28	–	30	MHz
Encoder OUT Clock Period	t_{EOUT}	50		40	–	35.7	–	33.3	–	ns
ENCOUTCLK Rise to ENCCLKOUT Fall	t_{ERF}	–	15	–	12	–	10.7	–	10	ns
ENCOUTCLK Fall to ENCCLKOUT Rise	t_{EFR}	–	15	–	12	–	10.7	–	10	ns
ENCOUTCLK Low & High Period	t_{EOL} & t_{EOH}	20	–	16	–	14.3	–	13.3	–	ns
Data Valid After Clock Output Rising	t_{ENCPD}	0	5	0	5	0	5	0	5	ns
Minimum Reset Period	t_{ERES}	100*	–	80*	–	72*	–	67*	–	ns

* Minimum Value is 2 $ECLK_{MAX}$ where $ECLK_{MAX}$ = the Period of ENCINCLK or ENCOUTCLK, whichever is greater.

Values assume a 30 pF load on Output Pins. All timings are measured from the switching level of 1.4 V.

Table 34b. Encoder Clock Timing Parameters for Viterbi Mode (Rate 1/2 and 1/3 Serial)

PARAMETER	SYMBOL	MIN	MAX	MIN	MAX	UNITS
Supply Voltage	V_{DD}	4.5	5.5	4.5	5.5	V
Operating Temperature, Case	T_C	-55	125	-40	85	°C
Max Frequency (=1/t_{EIN}) Rate 1/2 Serial	ENCINCLK	–	20	–	25	MHz
Max Frequency (=1/t_{EIN}) Rate 1/3 Serial	ENCINCLK	–	13.3	–	16.7	MHz
Encoder IN Clock Period Rate 1/2 Serial	t_{EIN}	50	–	40	–	ns
Encoder IN Clock Period Rate 1/3 Serial	t_{EIN}	75	–	60	–	ns
ENCDATIN Setup to ENCINCLK Rise	t_{ENCSU}	5	–	5	–	ns
ENCDATIN Hold After ENCINCLK Rise	t_{ENCHLD}	5	–	5	–	ns
ENCINCLK Clock Low & High Period	t_{EIL} & t_{EIH}	20	–	16	–	ns
Max Frequency (=1/t_{EOUT}) Rate 1/2 and 1/3 Serial	ENCOUTCLK	–	40	–	50	MHz
Encoder OUT Clock Period Rate 1/2 and 1/3 Serial	t_{EOUT}	25	–	20	–	ns
ENCOUTCLK Rise to ENCCLKOUT Fall	t_{ERF}	–	15	–	12	ns
ENCOUTCLK Fall to ENCCLKOUT Rise	t_{EFR}	–	15	–	12	ns
ENCOUTCLK Low & High Period	t_{EOL} & t_{EOH}	20	–	16	–	ns
Data Valid After Clock Output Rising	t_{ENCPD}	0	5	0	5	ns
Minimum Reset Period	t_{ERES}	100*	–	80*	–	ns

* Minimum Value is 2 $ECLK_{MAX}$ where $ECLK_{MAX}$ = the Period of ENCINCLK.

Values assume a 30 pF load on Output Pins. All timings are measured from the switching level of 1.4 V.

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Figure 47. Decoder Clock Timing Diagram

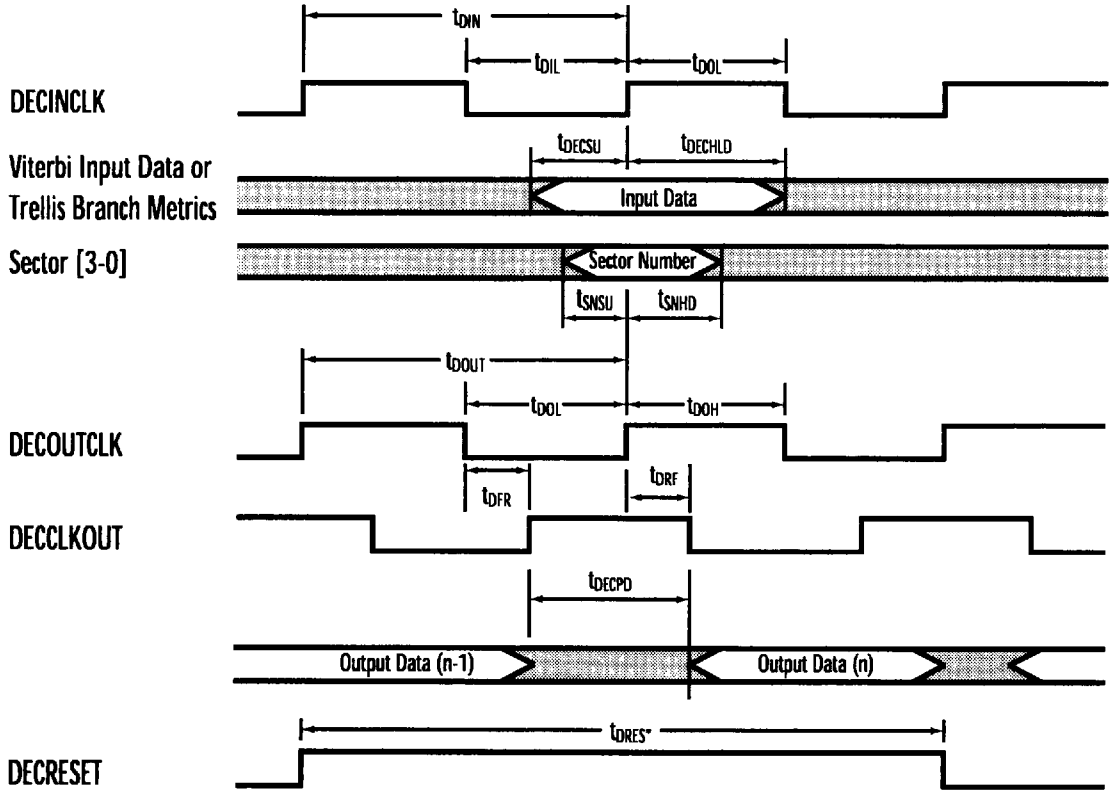

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Table 35a. Decoder Clock Timing Parameters for Viterbi Mode (all Parallel Rates) and Trellis Mode (all Rates)

PARAMETER	SYMBOL	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	UNITS
Supply Voltage	V_{DD}	4.5	5.5	4.5	5.5	4.75	5.5	5.0	5.5	V
Operating Temperature, Case	T_C	- 55	125	- 40	85	- 40	85	- 40	85	°C
Max Frequency (=1/t_{DIN})	DECINCLK	–	20	–	25	–	28	–	30	MHz
Decoder IN Clock Period	t_{DIN}	50		40	–	35.7	–	33.3	–	ns
Data Setup to DECINCLK Rise	t_{DECSU}	5	–	5	–	5	–	5	–	ns
Data Hold After DECINCLK Rise	t_{DECHLD}	5	–	5	–	5	–	5	–	ns
DECINCLK Low & High Period	t_{DIL} & t_{DOH}	20	–	16	–	14.3	–	13.3	–	ns
Max Frequency (=1/t_{DOUT})	DECOUTCLK	–	20	–	25	–	28	–	30	MHz
Decoder OUT Clock Period	t_{DOUT}	50	–	40	–	35.7	–	33.3	–	ns
DECOUTCLK Rise to DECCLKOUT Fall	t_{DRF}	–	18	–	15	–	13	–	12	ns
DECOUTCLK Fall to DECCLKOUT Rise	t_{DFR}	–	18	–	15	–	13	–	12	ns
DECOUTCLK Low & High Period	t_{DOL} & t_{DOIH}	20	–	16	–	14.3	–	13.3	–	ns
Sector Number Setup to DECOUTCLK Rise	t_{SNSU}	5	–	5	–	5	–	5	–	ns
Sector Number Hold to DECOUTCLK Rise	t_{SNHD}	5	–	5	–	5	–	5	–	ns
Data Valid After Clock Output Rising	t_{DECPD}	0	12	0	12	0	12	0	12	ns
Minimum Reset Period	t_{DRES}	100*	–	80*	–	72*	–	67*	–	ns

* Minimum Value is 2 * $DCLK_{MAX}$, where $DCLK_{MAX}$ = the Period of DECINCLK or DECOUTCLK, whichever is greater.

Values assume a 30 pF load on Output Pins. All timings are measured from the switching level of 1.4 V.

Table 35b. Decoder Clock Timing Parameters for Viterbi Mode (Rate 1/2 and 1/3 Serial)

PARAMETER	SYMBOL	MIN	MAX	MIN	MAX	UNITS
Supply Voltage	V_{DD}	4.5	5.5	4.5	5.5	V
Operating Temperature, Case	T_C	- 55	125	- 40	85	°C
Max Frequency (=1/t_{DIN}) Rate 1/2 and 1/3 Serial	DECINCLK	–	40	–	50	MHz
Decoder IN Clock Period Rate 1/2 and 1/3 Serial	t_{DIN}	25	–	20	–	ns
Data Setup to DECINCLK Rise	t_{DECSU}	5	–	5	–	ns
Data Hold After DECINCLK Rise	t_{DECHLD}	5	–	5	–	ns
DECINCLK Low & High Period	t_{DIL} & t_{DOH}	20	–	16	–	ns
Max Frequency (=1/t_{DOUT}) Rate 1/2 Serial	DECOUTCLK	0	20	0	25	MHz
Max Frequency (=1/t_{DOUT}) Rate 1/3 Serial	DECOUTCLK	0	13.3	0	16.7	MHz
Decoder OUT Clock Period Rate 1/2 Serial	t_{DOUT}	50	–	40	–	ns
Decoder OUT Clock Period Rate 1/3 Serial	t_{DOUT}	75	–	60	–	ns
DECOUTCLK Rise to DECCLKOUT Fall	t_{DRF}	–	18	–	15	ns
DECOUTCLK Fall to DECCLKOUT Rise	t_{DFR}	–	18	–	15	ns
DECOUTCLK Low & High Period	t_{DOL} & t_{DOIH}	20	–	16	–	ns
Sector Number Setup to DECOUTCLK Rise	t_{SNSU}	5	–	5	–	ns
Sector Number Hold to DECOUTCLK Rise	t_{SNHD}	5	–	5	–	ns
Data Valid After Clock Output Rising	t_{DECPD}	0	12	0	12	ns
Minimum Reset Period	t_{DRES}	100*	–	80*	–	ns

* Minimum Value is 2 * $DCLK_{MAX}$, where $DCLK_{MAX}$ = the Period of DECOUTCLK.

Values assume a 30 pF load on Output Pins. All timings are measured from the switching level of 1.4 V.

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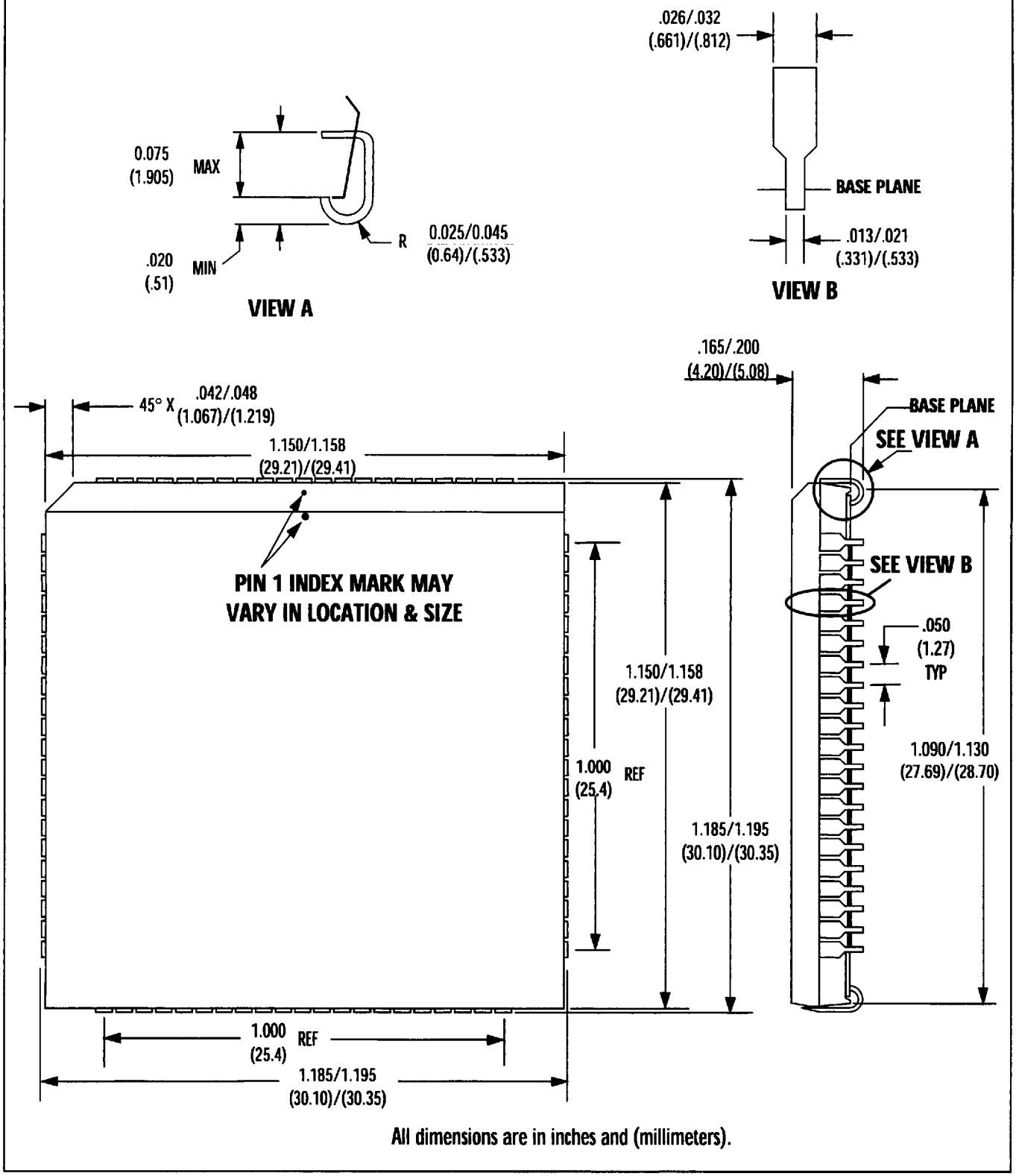
PACKAGES

The Q1900 is available in two packages, an 84-pin PLCC or a 100-pin VTQFP. The package drawings are given in Figure 48 for the PLCC package and Figure 49 for the VTQFP package. Dimensions are given in inches (mm). A suggested socket for the 84-pin PLCC is AMP P/N 821573-1 (through-hole board mounted) or P/N 822282-1.

Figure 48. Q1900 PLCC Package Diagram



All dimensions are in inches and (millimeters).

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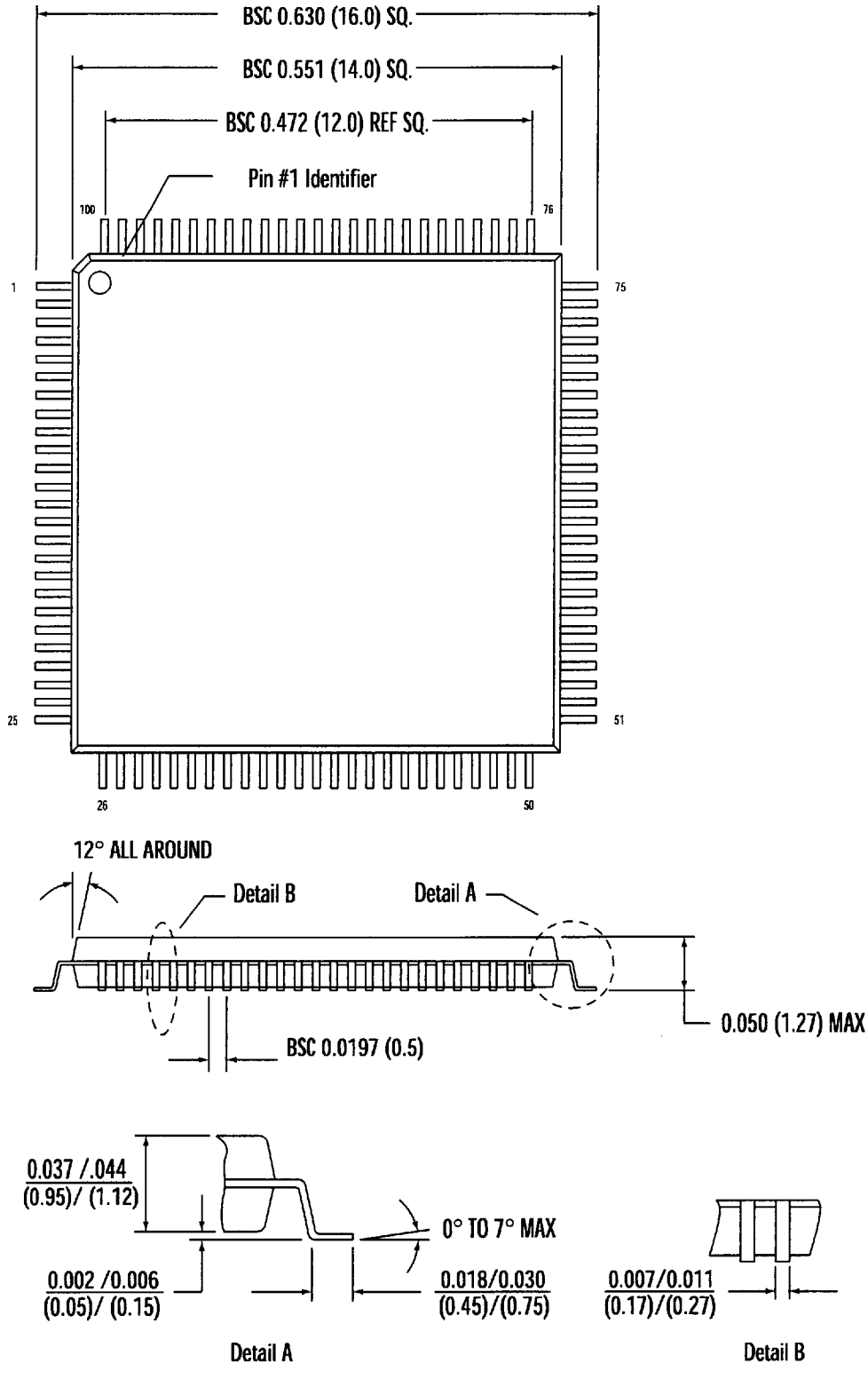
Figure 49. Q1900 VTQFP Package Diagram



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