Q20000 FEATURES

- Up to 18,777 gates, channelless architecture
- 100 ps equivalent gate delays
- Low power (0.5-1.0 mW/gate)
- 10K, 10KH, 100K ECL and mixed ECL/TTL capability
- Structured arrays with 1.25 GHz PLLs[1]
- High precision programmable delay line macros
- Speed/power programmability
- Single cell 25 and 50 ohm parallel termination drive
- Symmetrical rise and fall times
- Operation over commercial, industrial and military environmental conditions
- Up to 100% utilization

DESCRIPTION

The AMCC Q20000 Series of logic arrays is comprised of nine products ranging in density from 450 to 18,777 equivalent gates including structured arrays with 1.25 GHz PLLs.[1] The Q20000 "TURBO" ECL/TTL series is optimized to provide high performance and proven reliability to today's advanced hi-rel commercial, industrial and military semicustom applications.

Q20000 arrays are designed to operate at frequencies as high as 1.25 GHz. These Turbo arrays achieve this very high performance by combining an advanced process with innovative AC-coupled active drive circuitry. The combination of this advanced process and patented circuit design technique has achieved operating performance efficiencies as much as eight times greater than previous bipolar families.

An extensive library of SSI, MSI and LSI logic macros, including phase-locked loops and high resolution programmable delay lines, is currently available in conjunction with AMCC's MacroMatrix® design kit. The library features speed/power options that allow the designer to maximize critical path speed and density while minimizing overall chip power. MacroMatrix is available for Mentor 8.x for both HP7XX and SUN platforms.

Figure 6. Q20080 Die

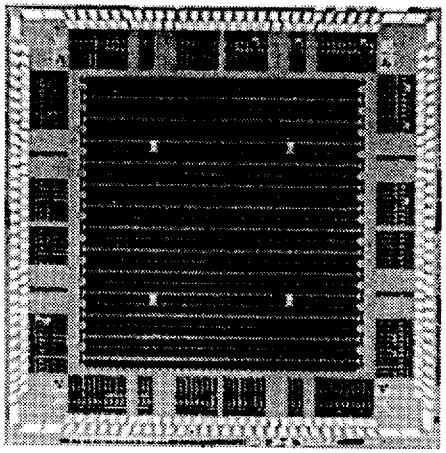

Table 9. Performance Summary

PARAMETER	VALUE
Typical gate delay [2]	100–250 ps
Maximum toggle frequency	1.25 GHz
Maximum TTL input frequency	100 MHz
Maximum TTL output frequency	60 MHz
Maximum ECL input frequency (DIFF)	1.25 GHz
Maximum ECL output frequency	
single ended	350 MHz
Darlington (single ended, mixed mode only)	600 MHz
differential	1.0 GHz
CML [3]	1.25 GHz
ECL I/O pair delay (min/max)	330/560 ps

Table 10. Q20000 "TURBO" ECL/TTL Product Summary

Parameter	Q20004	Q20010	Q20025	Q20045	Q20080	Q20120	Q20P010[1]	Q20P025[1]	Q20M100
Equivalent Gates -Flip Flop [4]	450	979	2687	4520	7494	12518	649	2178	8980
-Full Adder [5]	671	1469	4032	6782	11242	18777	973	3272	13475
Core Cells	123	267	733	1233	2044	3414	177	595	2450
I/O Cell Count [6]	30	68	102	130	164	200	34	51	195
Structured Array Blocks	–	–	–	–	–	–	PLL	PLL	Memory
Power (W)[7]	<1W	1–2	2–3	3–5	5–9	8–14	1.5–2.5	2–4	10–17

[1] Refer to the Q20000 "TURBO" + PLL section of this data sheet for further information.
[2] Based opon the use of complex macros and availability of speed/power options.
[3] 1.25 GHz CML output available in Q20P010 and Q20P025 only.
[4] Computed using 11 gate equivalent, 3 cell 3:1 MUXed D Flip-Flop – FF48 Macro.
[5] Computed using 11 gate equivalent, 2 cell, One bit Full Adder, AD05 Macro.
[6] Available I/O signals depends upon package and macro selection. Some I/O macros utilize more than one I/O cell.
[7] Assumes 50% Inputs, 50% Outputs, Mixed mode supply. Utilization determines actual array power dissipation.

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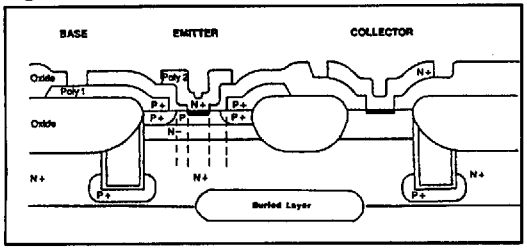
TECHNOLOGY

The Q20000 Series of ultra high performance ECL/TTL logic arrays is fabricated using a one micron bipolar process incorporating polysilicon emitter contacts, trench oxide isolation and an advanced base emitter structure (Figure 7). The 1μm wide trench reduces the collector substrate capacitance to less than half and doubles packing density when compared to conventional oxide isolated devices.

The minimum emitter feature size of 1μm × 2μm (.6 × 1.6 effective) combined with the low capacitance of the double poly, trench isolated process, achieves a cut-off frequency (F_t) of 14 GHz. The three level metal interconnect system employs fine pitch geometries of 4μm first, 5μm second and 7μm for the third level of metal.

Figure 7. Process Cross Section

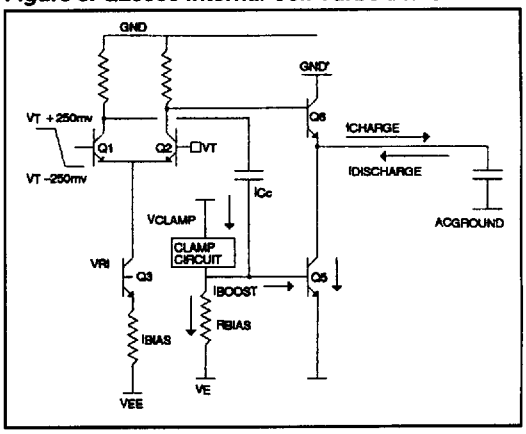


DESIGN INNOVATIONS

Conventional ECL structures use an output emitter follower biased with a static current source. When replicated and used hundreds or thousands of times per array these static current sources consume large amounts of current. As gate densities increase, this static current becomes a large power burden.

To overcome this power burden, AMCC developed a patented dynamic discharge circuit (Figure 8) in place of the static current source for the emitter follower. This dynamic discharge circuit is comprised of a capacitively coupled active pull down arrangement. The static power requirements when using this innovative technique are reduced substantially. Output skews between rising and falling edge delays are virtually eliminated and are significantly less affected by interconnect loading. This circuit technique in effect "**Turbo** Charges" the output.

Figure 8. Q20000 Internal Cell Turbo Driver



The Turbo circuit is beneficial for circuits operating at frequencies as high as 600 MHz and is used in implementing the majority of macro functions in Q20000 series designs. For circuit paths operating between 600 MHz and 1.25 GHz, the Q20000 Series Macro Library includes functions with the traditional ECL output emitter follower structure.

The I/O cell also benefits from the innovative **Turbo** design. Off chip skews for ECL outputs (10KH or 100K) as well as loading effects versus conventional emitter follower structures are greatly improved. If a dual supply is available, the I/O cell can be configured with a Darlington output stage plus **Turbo**. This option gives a single I/O cell the ability to drive a 25 ohm parallel terminated line at reduced switch current, thereby reducing power requirements.

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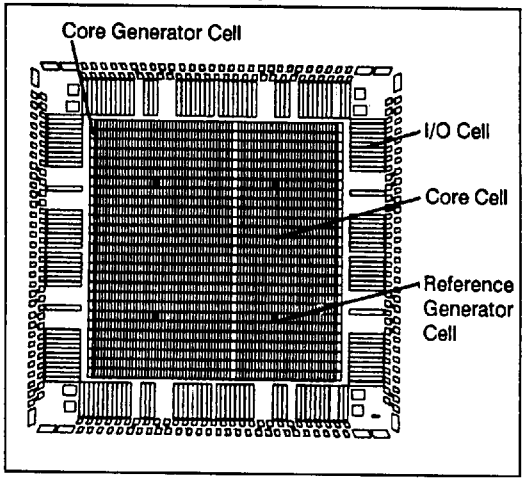
ARCHITECTURE

ARRAY ARCHITECTURE

The Q20000 Series utilizes a channelless architecture called **Sea-of-Cells®.** The Sea-of-Cells organization eliminates the dedicated routing channels between cells used in channeled array architectures, thereby effectively doubling the core density. Utilization is maintained at above 95% because of three levels of metal interconnect and AMCC's state-of-the-art place and route software. First level metal is used primarily for macro definition while second and third metal levels handle inter-macro routing. The reduced static power of the **Turbo** cell allows power and ground distribution to be interspersed on the second and third metal levels, eliminating the need for a dedicated power plane.

Figure 9. Q20080 Die Organization



Like previous ECL logic array families from AMCC, the internal core cell of the Q20000 Series uses logic efficient three level series gated structures. The three level structure can operate over the full military temperature (–55°C ambient to +125°C case) and voltage range of ECL 10KH or 100K logic because of AMCC's unique design. Table 10 lists representative macro functions and the number of cells required for implementation of each. A latch can be implemented in only one cell.

The I/O cells are designed to interface with either 10KH, 100K or TTL thresholds. For over 600 MHz operation, a differential CML output structure is also available for use with selected I/O cells and package pins.

Each I/O cell in the array family can be either an input or an output. Bi-directional operation is achieved by paralleling any two adjacent I/O cells. The flexible I/O structure of the Q20000 family allows operation in either 100% ECL, 100% TTL and mixed ECL/TTL I/O in either dual supply or single supply configurations.

Table 10. Functional Density

MACRO FUNCTION	CELL USAGE	MACRO NAME
Flip-Flop with AR; A/AN outputs	2	FF12
Flip-Flop with EXORed Data; Q output	2	FF22
Flip-Flop with 3:1 MUXed Data, Q output	3	FF48
D Latch	1	LA11
4:1 Mux	2	MX21
2 Input Exclusive-OR, Y output	1	EX30
4-Bit Carry Look Ahead Adder	24	ADD00
4-Bit Counter with AR, AS	26	CTR02
8-Bit Comparator	40	CMP00

STRUCTURED ARRAYS

Three members of the Q20000 "TURBO" ECL/TTL family feature embedded functions. The Q20P025 and Q20P010 arrays include a 1.25GHz PLL with 2500 and 1000 usable logic gates, respectively. The Q20M100 array includes eight 32 x 18 bit RAM blocks (total 4K) and 10,000 usable gates. For detailed information on the arrays featuring on-chip PLLs, refer to the *Q20000 "TURBO" + PLL* pages later in this section. For detailed information on the arrays featuring RAM blocks, see the Q20M100 data sheet on the AMCC website (www.amcc.com).

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LOGIC CELL FUNCTIONS

HIGH SPEED/LOW POWER MACROS

The Q20000 Series macro library offers maximum flexibility in the optimization of circuit performance and power consumption. A full complement of macros is offered with low power, standard and high speed options. The high speed options require somewhat more power than standard options, but provide a significant improvement in propagation delay and/or maximum operating frequency. The low power versions of macros can be used to reduce power consumption in non-critical paths. Table 11 illustrates the speed, power and frequency tradeoffs for the three options of one sample macro.

Table 11. Macro Speed Power Options: Example

GT65 — 8-INPUT OR	High Speed	Standard	Low Power
T_{PD} min/max (ps)[1]	87/160	103/189	167/298
I_{EE} (mA)	1.12	0.776	0.455
Max Operating Freq. (MHz)	1200	800	600

[1]Tpd = $[T_{PD(+)} + T_{PD(-)}]/2$. Path shown is any input to Y output.

DIFFERENTIAL MACROS

The Q20000 family offers a wide range of differential macros to facilitate high speed designs. Both core and I/O macros are available to allow fully differential paths and maximize the noise immunity and speed of your design. These differential macros are included as a standard part of the AMCC Design Kit. Ask your AMCC rep for more details.

INTERNAL LOGIC CELL CAPABILITIES

The Q20000 Series internal logic cells are all identical in structure and are uniformly positioned in a Sea-Of-Cells matrix across the internal core area of the array. Each cell contains 13 uncommitted transistors and 13 resistors. The cells are individually configurable to provide a variety of logic functions by placing macros from the Q20000 Series macro library. The macro library provides SSI, MSI and some basic LSI functions. Higher functionality macros provide the advantages of higher speed, lower power and increased circuit density over a logically equivalent SSI macro implementation.

FLEXIBLE I/O STRUCTURE

The Q20000 Series I/O cells are configurable to provide a universal range of interface options for both single and dual supply modes. The mixed ECL/TTL capabilities allow interface to both technologies on a single chip without the use of external translators. Refer to Table 12 to see the wide variety of available interface options, which can be mixed as required by each design.

Table 12. Signal Interface Options

INPUT	BIDIRECTIONAL	OUTPUT
TTL	TTL Transceivers	TTL Totem Pole TTL Tri-State TTL Open Collector
ECL 10K and 10KH	ECL 10K and 10KH Transceivers	ECL 10K and 10KH
ECL 100K	ECL 100K Transceiver	ECL 100K
CML		CML Open Collector

ECL INTERFACE

The Q20000 Series arrays can interface to standard and positive reference (+5V) ECL 10K, 10KH and 100K levels. ECL inputs can enter the array from any I/O cell and, in some cases, may be connected directly to core cells without additional buffering. Additionally, signals can be input differentially to remove common mode noise.

ECL outputs can leave the arrays from any I/O cell. Different configurations of the I/O cells provide for a 50 ohm or 25 ohm output drive. Differential CML outputs are available for high frequency paths.

The Q20000 Series allows for a special type of ECL output macro which incorporates a Darlington output configuration. These macros maintain standard ECL 10K, 10KH and 100K output levels, while netting an improvement in drive capability and toggle frequency over standard ECL outputs. While requiring dual power supplies, the Darlington output macros will accommodate 25 or 50 ohm loads in a single I/O location while maintaining ECL standard levels.

Bidirectional ECL operation is available using two adjacent I/O cells.

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TTL INTERFACE

TTL inputs can be placed in any I/O cell. Once on-chip, TTL signals are automatically converted to internal voltage levels for internal logic operations.

Signals leaving the array are translated from an internal voltage level to TTL level in the I/O cell. Following this translation, TTL outputs are available in totem pole, 3-state or open collector configurations. TTL outputs, like inputs, can be located in any I/O cell.

Bidirectional TTL operation is available in single cell and dual I/O cell implementations.

CUSTOM MACROS

AMCC has developed a macro development system to simplify the design and implementation of custom macros. This tool suite uses a correct-by-construction approach to insure that macros meet all the pertinent design rules and parametrics. As individual circuit applications warrant, macros with unique characteristics can be developed to optimize a customer's design.

POWER SUPPLY CONFIGURATIONS

On the Q20000 Series arrays there are four basic interface configurations: single-supply ECL, single supply PECL, dual-supply mixed TTL/ECL and single-supply mixed TTL/ECL. Power supply requirements for each mode of operation are shown in Table 13.

Table 13. I/O Power Supply Configuration

I/O MODE	V_{EE}	V_{CC}
ECL 100K	-4.2 to -4.8 V[1]	-
ECL 10K, 10KH	-4.7 to -5.7V	-
ECL 100K/TTL	-4.2 to -4.8V[1]	4.5 to 5.5V
ECL 10K, 10KH/TTL	-4.7 to -5.7V	4.5 to 5.5V
PECL 100K	-	4.5 to 5.5V
PECL 10K, 10KH	-	4.5 to 5.5V
PECL 100K/TTL	-	4.5 to 5.5V
PECL 10K, 10KH/TTL	-	4.5 to 5.5V

[1]May be configured with a -5.7 supply. Consult AMCC for DC parametrics.

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PACKAGING

THE Q20000 "TURBO" ECL/TTL logic array family is available in a range of standard packages including thermally enhanced plastic, surface-mountable ceramic chip carriers and ceramic pin grid arrays (see Table 14). Other package types, including ball grid arrays will be supported as required by new ASIC opportunities. For additional details, consult the AMCC website (www.amcc.com) and check out the AMCC Packaging Guide.

Table 14. Q20000 "TURBO" ECL/TTL Family Packaging Matrix

PKG DESCRIPTION/ DIE NAME	Q20004	Q20010	Q20025	Q20045	Q20080	Q20120
Plastic 28 PLCC	X					
Plastic 44 PLCC	X	X				
Plastic 68 PLCC	X	X				
Plastic 68 PLCC/EDQUAD	X	X				
Plastic 52 PQFP	X	X				
Plastic 80 PQFP/EDQUAD		X	X			
Plastic 100 PQFP/EDQUAD		X	X			
Plastic 120 PQFP/EDQUAD			X	X		
Plastic 160 PQFP/EDQUAD				X	X	
Plastic 208 PQFP/EDQUAD				X	X	
Ceramic 100 LDCC		X				
Ceramic 132 LDCC			X	X		
Ceramic 196 LDCC				X	X	
Ceramic 224 LDCC					X	X
Ceramic 100 PGA		X				
Ceramic 149 PGA			X			
Ceramic 209 PGA				X		
Ceramic 251 PGA					X	
Ceramic 300 PGA						X

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FEATURES

- On-chip high frequency phase-locked loop
- Up to 1.25 GHz capability
- Edge jitter as low as 10ps (rms) and 50 ps (pk-pk)
- 900 to 3000 gates of customizable digital logic
- Utilizes proven Q20000 Series macro library
- 100 ps equivalent gate delays
- Low power (0.5–1.0 mW/gate)
- 10K, 10KH, 100K ECL, PECL and mixed ECL/TTL capability
- Speed/power programmable logic and I/O
- Operation over commercial and military ranges
- Up to 95% utilization of digital logic
- Full logic simulation modeling support of PLL functions

Table 15. Performance Summary

Parameter	Value
Phase-Locked Loop	
Operating Frequency	125 MHz–1.25 GHz
Edge Jitter (pk–pk)	50–100 ps
Residual BER	10E–12
Acquisition Time (typical)	1.0 µs
Digital	
Typical Gate Delay	100–250 ps
Maximum Toggle Frequency	1.25 GHz
Maximum TTL Input Frequency	100 MHz
Maximum TTL Output Frequency	80 MHz
Maximum ECL Input Frequency	1.25 GHz
Maximum ECL Output Frequency	1.25 GHz

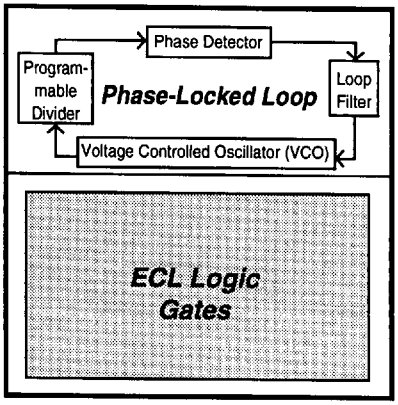
Table 16. Product Summary

	Q20P010	Q20P025
Equivalent Gates		
Full Adder Method	928	3120
Flip-flop Method	637	2142
Internal Logic Cells	177	595
I/O Pins [1]		
PLL Related		
Loop Filter	0	0
Signals	12	12
Powers & Grounds	8	8
Digital		
Signals	up to 34[2]	up to 51[2]
Powers & Grounds	20	22
AC Monitor & Thermal Diode	4	4
Maximum Total Power (W)	1.5–3	2–3

[1] See Table 17 for packaging options.

[2] Actual number of signal pins available depends on package choice.

Figure 10. Q20000 "TURBO" + PLL Architecture



APPLICATIONS

- High speed datacom
- High performance telecom
- Timing generation circuits
- Video shift registers
- Frequency synthesis
- Self-timed systems

DESCRIPTION

The AMCC Q20P010 and Q20P025 PLL logic arrays offer gate densities of 900 and 3000 equivalent gates with an on-chip high frequency phase-locked loop. Combining a PLL with user-definable Q20000 series arrays, the Q20P010 and Q20P025 are tailored for high speed serial communication, video, and clock generation applications.

Clock synthesis and clock recovery macros are available for the on-chip phase-locked loop. Speed options ranging from 125 MHz to 1.25 GHz are available. Complete simulation models, implementing all CSU/CRU functions, are available for digital logic simulation on Mentor workstations as well as the LASAR simulator. Lock detect, local and link loopback features are also supported.

For the digital logic portion of the array, an extensive library of SSI and MSI macros is available as part of AMCC's MacroMatrix™ design kit. Latches, parallel-to-serial converters, encode/decode functions, high speed shift registers, bit error rate computation and divide-down counters can easily be assembled to operate in conjunction with the phase-locked loop to meet specific application needs.

DIGITAL LOGIC

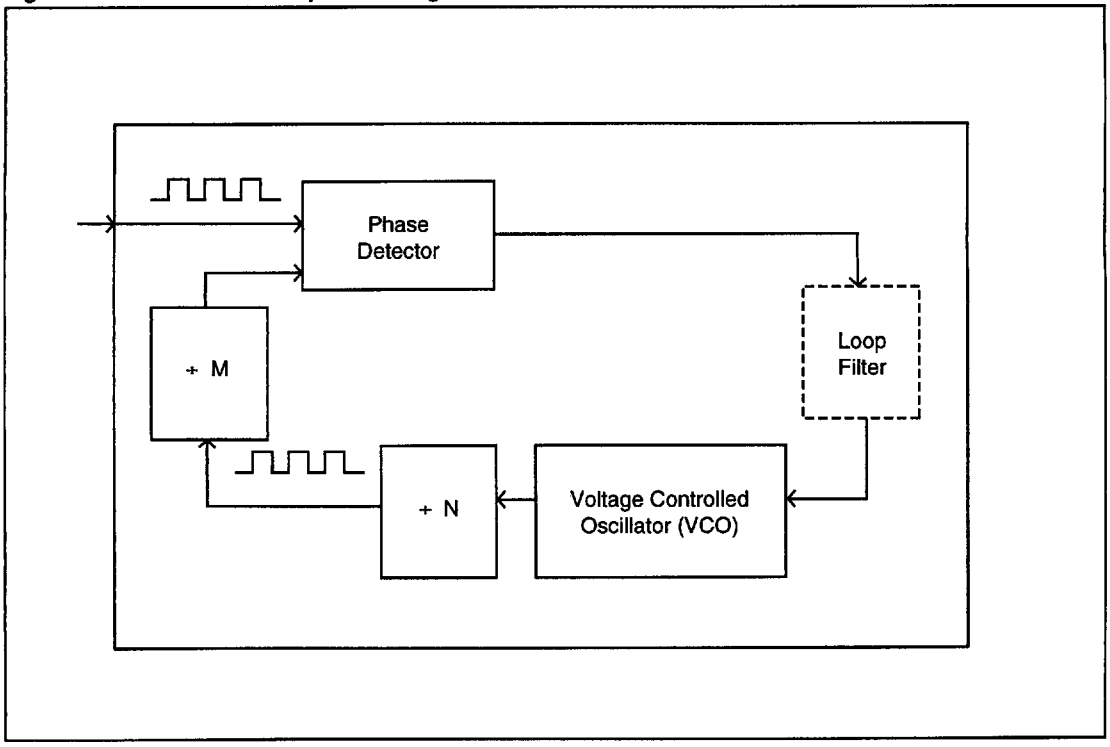
The Q20000 Series is the industry's first ECL logic array family to utilize a channelless architecture called **Sea-of-Cells™**. The Sea-of-Cells organization eliminates the dedicated routing channels between cells thereby doubling the core density. Utilization is maintained at greater than 95% due to three layer metal interconnect and AMCC's state-of-the-art place and route system. A full complement of SSI and MSI macros is offered with low power, standard and high speed options. For more information on the Q20000 "TURBO" + PLL digital logic, see the **ARCHITECTURE** and **LOGIC CELL FUNCTIONS** paragraphs in this section of the data book (pages 11-15 and 11-16).

To minimize noise injection from the core logic into the PLL section of the device, all core logic must be operated synchronously with the PLL.

PHASE-LOCKED LOOP MACROS

A selection of clock synthesis and clock recovery macros are available for the on-chip phase-locked loop. PLL center frequencies of 1000, 1062, 1244 and 1250 MHz are available with user selectable divide ratios of 1, 2, 4, and 8. This results in speed options of 125, 133, 155, 250, 266, 311, 500, 531, 622, 625, 1000, 1062, 1244 and 1250 MHz that are available to operate synchronously with the logic in the digital portion of the array. Additional frequency options can be created to meet specific design requirements. AMCC defined loop filter components for each frequency option have been established for applications with divide ratios up to 500, transition densities from 30% to 70%, and run lengths up to 64-bit times. Lock detect, local and link loopback features are also supported in any of these configurations.

Figure 11. Phase-Locked Loop Block Diagram



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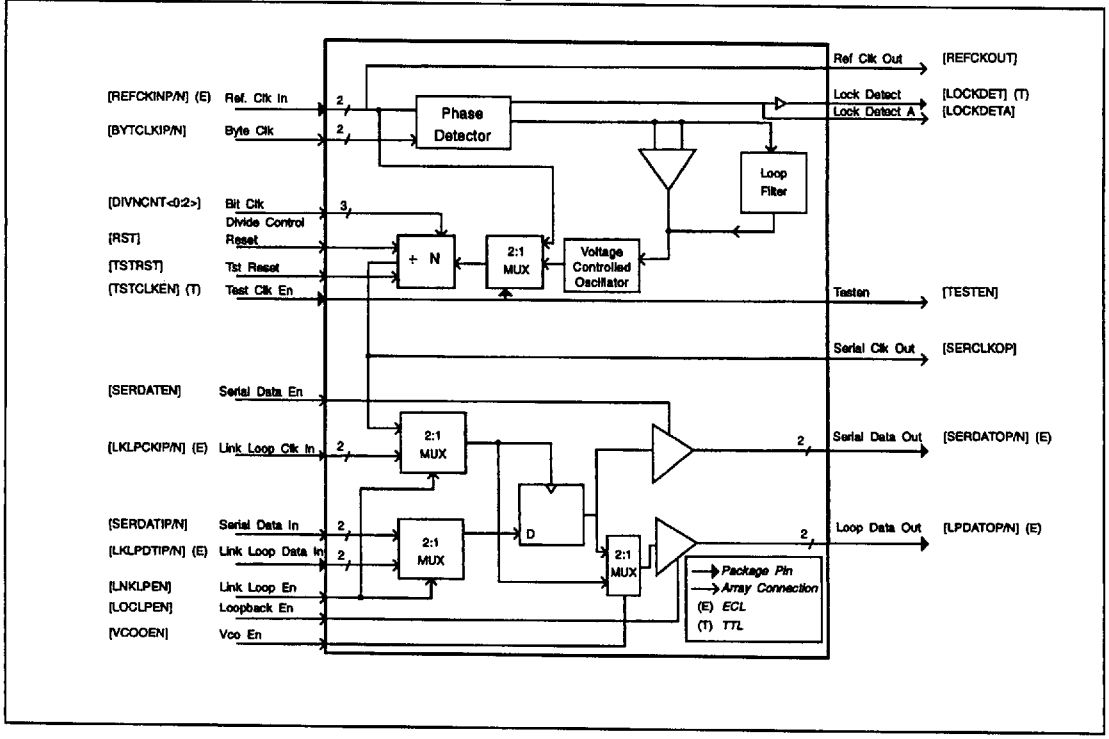
ENCODING/DECODING

High speed datacom and telecom applications frequently require a standard encoding scheme to ensure favorable bit stream characteristics and inter-operability. AMCC offers an encoder/decoder scheme implemented using standard macro library components. Popular in datacom applications, IBM's 8B/10B encoding scheme offers DC-balance and short run lengths in an efficiently architected implementation. The 8B/10B macros are available under a licensing and nondisclosure agreement. CMI encoding and decoding blocks, especially popular in telecom applications where copper is the transmission medium, are available as well. Other encoding and decoding schemes can easily be designed as needed using the digital portion of the Q20P010 and Q20P025 arrays.

FLEXIBLE I/O STRUCTURE

The Q20P010 and Q20P025 array I/O cells are configurable to provide a flexible range of interface options. The I/O cells are designed to interface with standard (-5.2V or 4.5V) and positive reference (+5V) ECL 10KH and ECL 100K or TTL thresholds. The mixed ECL/TTL capabilities allow interface to both technologies on a single chip without the use of external translators. For dual power supply devices, the I/O is also capable of a Darlington-type ECL output which provides significant improvement in drive capability, toggle frequency, and power dissipation over standard ECL outputs.

Figure 12. Representative Transmitter Block Diagram



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PHASE-LOCKED LOOP

The basic phase-locked loop components are shown in the PLL block diagram (Figure 11). The loop consists of a phase detector, which compares the phase difference between the VCO and the reference input, a loop filter, which converts the phase detector output into a smooth DC voltage, and the VCO, which generates a frequency based on its input voltage.

PLL building blocks differ for clock synthesis and clock recovery. This is due in large part to the differences in reference inputs to the phase detector. In the case of the clock synthesis PLL (see Figure 12), the reference input is a very stable crystal-based source. For clock recovery from a serial data stream (see Figure 13), the reference input has varying transition density; i.e., different run lengths of 1's and 0's with short term frequency variations. Since the loop filter generates a control voltage for the VCO input based on the output of the phase detector, different sets of loop filter components must be specified for clock synthesis versus clock recovery applications.

In addition, appropriate filter components will be required for different encoding schemes, acquisition time requirements and system noise environments. AMCC provides selectable sets of on-chip resistors and capacitors appropriate for specific system conditions.

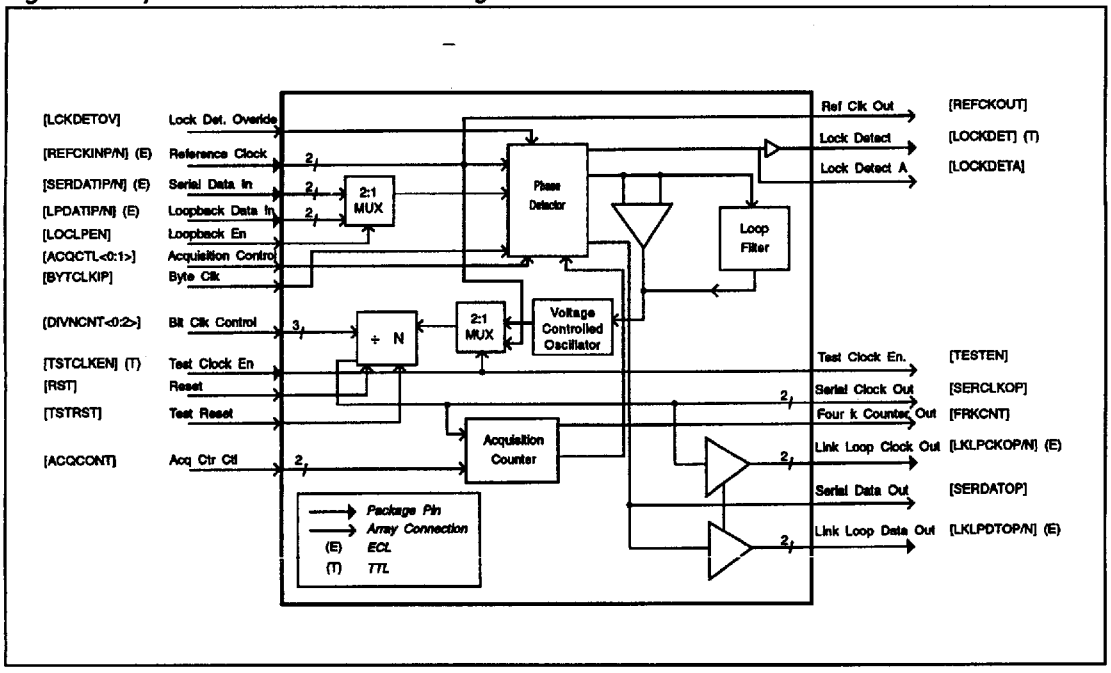
SPECIAL FEATURES

Lock Detect

For clock recovery macros, lock detect indicates the phase state of the PLL relative to the incoming data stream. Control pins from the core logic area permit lock detect to be indicated after 512, 1024, 2048, or 4096 bit times depending upon loop filter parameters. On CRU macros, if the serial data inputs have an instantaneous phase jump, the CRU will not indicate out-of-lock state, but will recover correct phase alignment within the pre-loaded bit times.

For the CSU macro, lock detect indicates the phase state of the PLL relative to the incoming reference clock.

Figure 13. Representative Receiver Block Diagram



LOOPBACK MODE

Local Loopback

Local and link loopback are supported for both datacom or telecom applications. Local loopback requires both a transmit chip and a receive chip. When enabled, serial encoded data from the transmit chip is sent to the receive chip where the clock is extracted and the data decoded. The parallel data output by the receiver is then sent to the subsystem for verification. This loopback mode provides the capability to perform offline testing of the interface to guarantee the integrity of the serial channel before enabling the transmission medium, and allows system diagnostics.

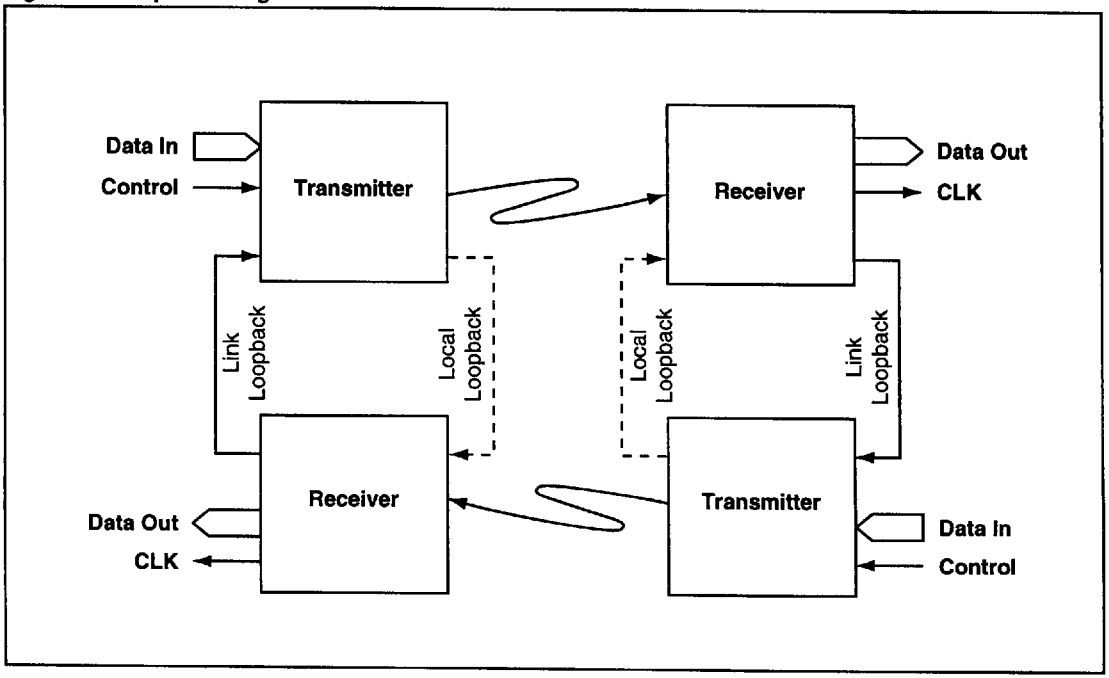
Link Loopback

Link loopback provides a means for link testing. When link loopback mode is enabled, the transmitter accepts serial clock and data from the receiver chip. The serial data is reclocked using the link loopback clock to minimize the data distortion and then transmitted via the serial data output pins. Link loopback can also be used to implement a repeater function. In this case, clock jitter and data distortion will determine the allowable number of repeaters in the path.

TEST/BYPASS MODE

Clock recovery and clock synthesis macros have testability input pins to aid in functional testing or PLL clock bypass tests. "Test Clock Enable" places the macros into test mode. An externally generated clock can then be input via the reference clock inputs. The PLL clock bypass path is typically capable of operating at up to 1.25 GHz to allow at speed testing of the chip functions, or for applications in which a user selectable external clock signal needs to be supported.

Figure 14. Loopback Diagram



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Clock Synthesis Macros

The clock synthesis PLL will generate a high frequency clock in phase with the input reference. A typical frequency multiplication factor is 20, and multipliers as high as 500 have been implemented. Critical parameters for the clock synthesis PLL are jitter and accuracy. AMCC loop filter components are set to optimize the loop for minimum phase jitter and maximum accuracy, with less emphasis on acquisition time. Loop filter parameters can be varied by AMCC on a custom basis.

Specifications

Input Reference Frequency — The input reference frequency can be a selected divide ratio of the synthesized clock frequency.

Reference Clock Jitter — The reference clock needs to be generated from a stable source such as a crystal oscillator. The allowable rms jitter cannot exceed .04% of the reference clock pulse width.

Input Reference Stability — The reference clock stability should be better than 100 ppm.

Acquisition Time — The loop acquisition time will depend on the loop filter parameters. (1.0 µs to 10 µs values are typical).

Edge jitter — The output edge jitter will depend on the loop filter parameters. (50 to 100 ps (pk-pk) values are typical).

Supply Voltage Sensitivity — Power supply noise rejection will be between 40 and 60 dB depending on the noise spectrum.

Clock Recovery Macros

The clock recovery PLL will generate a clock which is at the same frequency and 180 degrees out of phase with the serial data input. This generates clock and data outputs from the incoming serial bit stream which feeds the subsequent parallel conversion. An external clock reference is used to reduce initial acquisition time and to provide stability in the absence of serial data. The filter parameters are set to optimize the loop for the anticipated serial data input characteristics. These include: maximum run length and transition density of 1's or 0's, and the jitter associated with the fiber optic link. Loop filter parameters can be varied on a custom basis by AMCC.

Specifications

Input Reference Frequency — The input reference frequency can be a selected divide ratio of the VCO clock frequency. The maximum divide ratio is 500.

Reference Clock Jitter — The reference clock needs to be generated from a stable clock source such as a crystal oscillator. For maximum performance rms jitter should not exceed .04% of the reference clock pulse width.

Input Reference Stability — The reference clock stability should be less than 100 ppm.

Acquisition Time — The loop acquisition time will depend on the loop filter parameters. (1.0 µs to 10 µs values are typical)

Edge Jitter — The edge jitter will depend on the loop filter parameters and the serial data input specifications. (50 ps to 100 ps (pk-pk) values are typical)

Supply Voltage Sensitivity — Power supply noise rejection will be between 40 and 60 dB depending on the noise spectrum.

Data Rate — The possible serial data rates from which a clock can be recovered will be grouped around the VCO center frequency, with integer divide ratios of 1, 2, 4, 8, etc.

Allowed Data Jitter — The allowed input data jitter will be a function of the required acquisition time, along with the loop filter parameters, data rate, and bit error rate. The jitter specification includes duty cycle distortion, random jitter and data dependent jitter.

Pull In Range — The pull in range of the VCO is ±6%.

Bit Error Rate — Bit error rates of 10^{-12} or lower are achievable.

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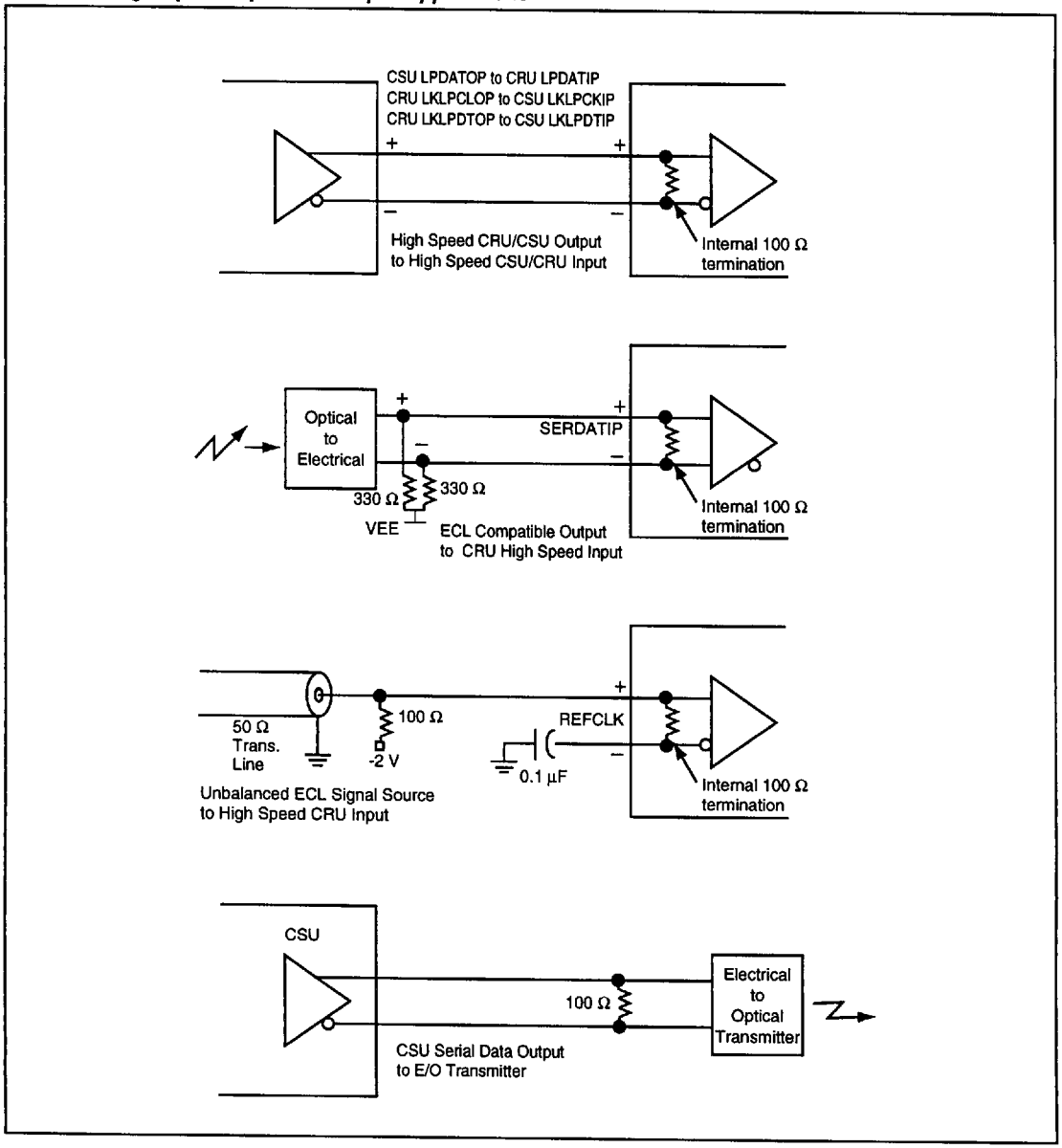
HIGH SPEED I/O CONNECTIONS

The high speed ECL compatible differential inputs in both the CRU and CSU macros have a built in 100Ω termination resistor across the differential pair, eliminating terminating components in loopback and data paths and ensuring low jitter interfaces. Figure 15 shows some examples of high speed CSU/CRU input and output connections.

Figure 15. High Speed Input and Output Applications



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PACKAGING

The Q20000 "TURBO" + PLL arrays are available in a range of standard packages including plastic, thermally enhanced plastic (EDQUAD), and surface-mountable ceramic chip carriers. Packages have been custom designed as necessary to offer controlled impedance on high speed signal lines and minimum digital noise injection to the PLL area. Table 17 provides a matrix illustrating many of the packages available for these products. Other packaging options are available on an as needed basis.

Table 17. Q20000 "TURBO" + PLL Family Packaging Matrix

PKG DESCRIPTION/ DIE NAME	Q20P010	Q20P025
Plastic 44 PLCC	X	
Plastic 44 PLCC/EDQUAD	X	
Plastic 68 PLCC	X	
Plastic 68 PLCC/EDQUAD	X	
Plastic 52 TQFP/EDQUAD	X	
Plastic 80 PQFP/EDQUAD	X	
Plastic 100 PQFP/EDQUAD	X	X
Plastic 120 PQFP/EDQUAD		X
Ceramic 68 LDCC	X	
Ceramic 100 LDCC	X	X
Ceramic 132 LDCC		X

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TIMING VERNIER PD01S

The PD01S is a programmable delay macro in the Q20000 "TURBO" family that provides a timing generation or deskew function for precision timing applications such as ATE, instrumentation, clock distribution, and high speed busses.

Key features of the PD01S include:

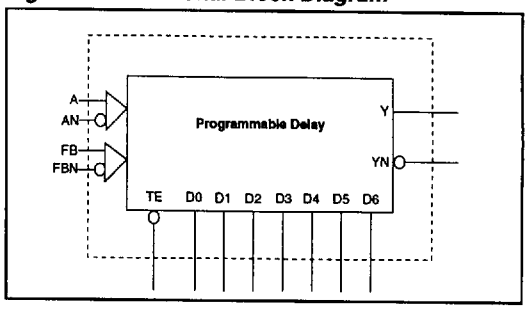
- Up to 30 delay lines per array possible
- Local macro voltage regulation for superior crosstalk performance
- Cascadable for greater delay range
- 64 core cells in size
- Ring oscillator mode for testability
- 7 decode bits for 127 selectable delay steps

A differential signal is applied to input pins A/AN, is modified with the addition of a delay specified by the binary input address pins D[6:0], and emerges at output pins Y/YN. The test enable input (TE) is held high for normal operation. When the TE input is set low to put the vernier into the test mode, the Y/YN output is internally inverted and fed back to the A/AN input. This allows the PD01S to function as a ring oscillator and enables operation verification. Changing the binary code of address pins D[6:0], changes the frequency of oscillations of the PD01S macro, allowing for convenient testing of accuracy through delta frequency measurements.

Table 18. Performance Summary

	PD01S	PD02S
Delay Step Resolution (typ)	40 ps	320 ps
Delay Step Resolution (max)	60 ps	340 ps
Minimum delay range	2.1 ns	1.8 ns
IEE (typ)	40 mA	21 mA
Max frequency	400 MHz	400 MHz
Minimum pulse width	1.25 ns	1.25 ns
Minimum propagation delay	2.0 ns	1.0 ns
Linearity to D1 ?	YES	-
Monotonic?	YES	YES

Figure 16. Functional Block Diagram



VERNIER CHARACTERISTICS

- (Y,YN) = (A,AN)
- NOMINAL DELAY = (20*D0 + 40*D1 + 80*D2 + 160*D3 + 320*D4 + 640*D5 + 1280*D6 +2000)ps
- TE = Low, Puts PD01S into Ring Oscillator Mode
- TE = High, Normal Mode

TIMING VERNIER PD02S

The PD02S is a programmable delay macro with identical characteristics to the PD01S, but it does not include the three least significant bits. It is designed to be cascaded to the PD01S, thereby adding steps and increasing the delay range of the vernier while keeping the functionality identical.

Key features of the PD02S include:

- Up to fifteen 4 ns verniers (PD01S + PD02S) per array possible
- Local macro voltage regulation for superior crosstalk performance
- Can be cascaded with additional PD02 macros to add delay in 2ns (typ) increments

A differential signal is applied to input pins A/AN, and outputs Y/YN drive the A/AN inputs of a PD01S or another PD02S macro. An incremental delay is added by the PD02S which is specified by the binary input address pins D[6:3], and the signal emerges at outputs Y/YN.

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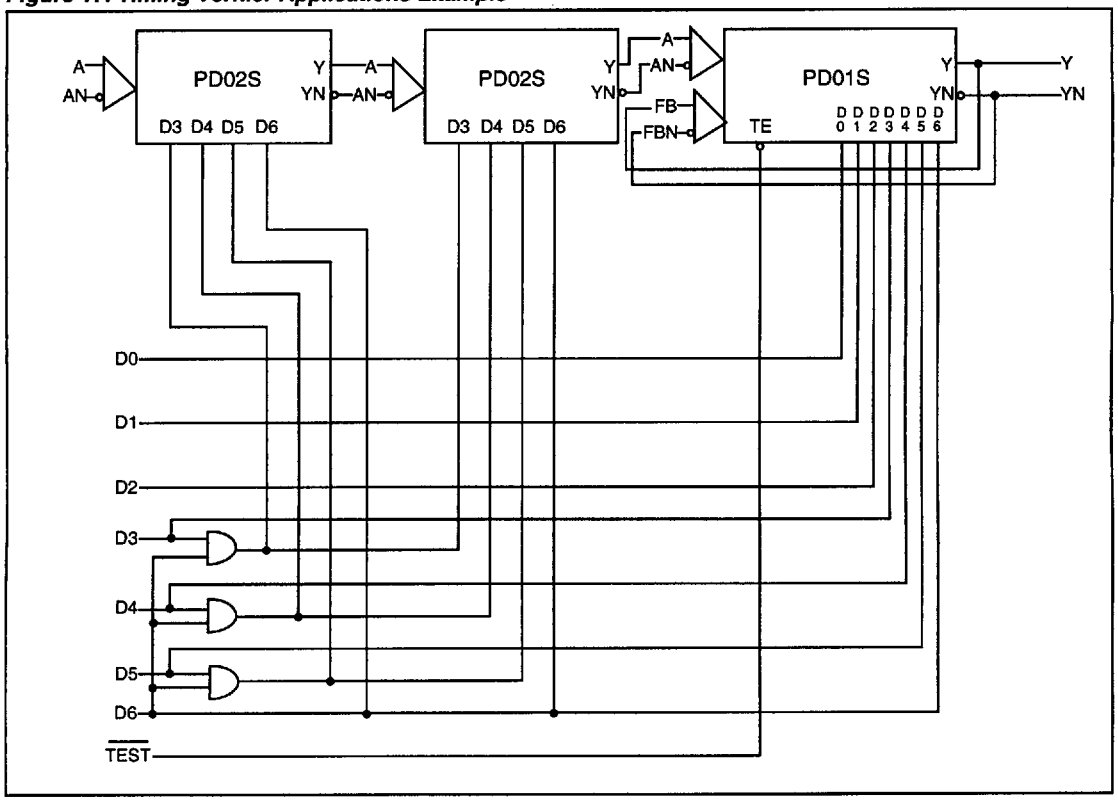
APPLICATION EXAMPLE

Requirements: 5ns span, 20ps typical delay resolution, 60ps worst case delay resolution.

Solution: 1 PD01S cascaded with 2 PD02S macros. See Figure 17.

Figure 17. Timing Vernier Applications Example



DESIGN INTERFACE

AMCC has structured its circuit design interface to provide maximum flexibility while ensuring design correctness. For implementations using a Mentor workstation, AMCC provides MacroMatrix software. MacroMatrix works in conjunction with Mentor 8.X to provide the following capabilities:

- Schematic Capture
- Logic Simulation
- Pre-Layout Delay Estimation (Front Annotation)
- Array and Technology-Specific Rules Checks (ERCs)
- Estimated Power Computation
- Layout Netlist Generation
- Post-Layout Timing Verification (Back Annotation)
- Graphical Floor Planning (IPL)
- Dynamic Timing and Test Vector Analysis (RaceCheck™)

Upon submission of the design database to AMCC, a comprehensive review of the circuit is performed making use of the very same EWS and MacroMatrix tools used by the designer. No "golden simulator" is employed to verify the timing of the design. No translation of the logic data is required so the chance of non design-related errors is virtually eliminated.

AMCC DESIGN SERVICES

AMCC also provides a number of additional support services including:

- A continually updated Website located at www.amcc.com
- Local and factory applications engineering support
- Thorough design documentation
- Full design implementation - Turnkey

Table 19. Recommended Operating Conditions-Commercial

Parameter	Min	Nom	Max	Units
ECL Supply Voltage[1,2] (V_{EE}) V_{CC} = 0 10K, 10KH Mode 100K Mode	 -4.94 -4.2	 -5.2 -4.5	 -5.46 -4.8[3]	 V V
ECL Input Signal Rise/Fall Time	-	1.0	3.0	ns
ECL Input Voltage	-2.0			V
TTL Supply Voltage (V_{CC})[1]	4.75	5.0	5.25	V
PECL Supply Voltage	4.75	5.0	5.25	V
TTL Output Current Low (I_{OL})			20	mA
Operating Temperature	0 (ambient)		70 (ambient)	°C
Junction Temperature			130	°C

Table 20. Recommended Operating Conditions-Military

Parameter	Min	Nom	Max	Units
ECL Supply Voltage[1,2] (V_{EE}) V_{CC} = 0 10K, 10KH Mode 100K Mode	 -4.7 -4.5	 -5.2 -4.5	 -5.7 -4.8[3]	 V V
ECL Input Signal Rise/Fall Time	-	1.0	3.0	ns
TTL Supply Voltage (V_{CC})[1]	4.5	5.0	5.5	V
PECL Supply Voltage	4.75	5.0	5.25	V
TTL Output Current Low (I_{OL})			20	mA
Operating Temperature	-55 (ambient)		125 (case)	°C
Junction Temperature			150	°C

Table 21. Absolute Maximum Ratings[4]

ECL Supply Voltage V_{EE} (V_{CC} = 0)	-8.0 VDC
ECL Input Voltage (V_{CC} = 0)	GND to -2.0 V
ECL Output Source Current (continuous)	-50mA DC
TTL Supply Voltage (V_{EE} = 0)	7.0 V
TTL Input Voltage V_{CC} (V_{EE} = 0)	5.5 V
Operating Temperature	-55°C (ambient) to +125°C (case)
Operating Junction Temperature T_J	+150°C
Storage Temperature	-65°C to +150°C

[1] Power sequencing is required on all dual supply ECL/TTL circuits. The positive supply must be turned on at least 30 ms before the negative supply.

[2] For ECL circuits using a V_{TT} = V_{CC} - 2V termination supply externally, this supply should be turned on at least 30 ms after the V_{CC} supply.

[3] -5.7V is possible. Consult AMCC for ECL 100K DC parametric operating at this voltage.

[4] Long term exposure at these limits may result in permanent change or damage to the circuits. Actual circuit operation at these conditions is not recommended nor implied.

Table 22. AC Electrical Characteristics

Symbol	Parameter		Test Conditions	COM 0°C/+70°C		MIL -55°C/+125°C		Unit
				Min	Max	Min	Max	
t_{IPD}-ECL	ECL Input Propagation Delay Including Buffer IE94S			59	263	57	281	ps
t_{IPD}-TTL	TTL Input Propagation Dealy Including Buffer IT50H			93	535	65	602	ps
t_{OPD}-ECL	ECL Output Propagation Delay - Darlington OK40S		No Load	185	340	157	356	ps
t_{OPD}-TTL	TTL Output Propagation Delay	Standard OT67S	No Load	2213	4292	2056	4375	ps
t_{FPD}	Internal Equivalent Gate Delay	Low Power		120	250	120	250	ps
		Standard		105	175	105	175	ps
F_{maxt}	Internal Flip/Flop Toggle Freq.	High Speed			1.25		1.25	GHz
F_{IN}-ECL	ECL Input Frequency at Package Pin[1]	Single-Ended			600		600	MHz
		Differencial High Speed			800		800	MHz
		Driver			1.25		1.25	GHz
F_{out}-ECL	ECL Output Frequency at Package Pin[1]	Single-Ended			350		350	MHz
		Differencial			1.25		1.25	GHz
		Darlington			600		600	MHz
		CML			1.25		1.25	GHz
F_{in}-TTL	TTL Input Frequency at Package Pin[1]	Standard			60		60	MHz
		High Speed			100		100	MHz
F_{out}-TTL	TTL Output Frequency at Package Pin	Low Power			20		20	MHz
		Standard			80		45	MHz

Table 23. ECL 10K Input/Output DC Characteristics V_{EE} = -5.2V[1]

					T_{case}	Unit
	-55°C	0°C	25°C	70°C	125°C	
V_{OHmax}[3]	V_{CC}-850	V_{CC}-770	V_{CC}-730	V_{CC}-650	V_{CC}-575	mV
V_{IHmax}[5]	V_{CC}-800	V_{CC}-720	V_{CC}-680	V_{CC}-600	V_{CC}-525	mV
V_{OHmin}[3]	V_{CC}-1080	V_{CC}-1000	V_{CC}-980	V_{CC}-920	V_{CC}-850	mV
V_{IHmin}[5]	V_{CC}-1255	V_{CC}-1145	V_{CC}-1105	V_{CC}-1045	V_{CC}-1000	mV
V_{ILmax}[5]	V_{CC}-1510	V_{CC}-1490	V_{CC}-1475	V_{CC}-1450	V_{CC}-1400	mV
V_{OLmax}	V_{CC}-1655	V_{CC}-1625	V_{CC}-1620	V_{CC}-1585	V_{CC}-1545	mV
V_{OLmin}	V_{CC}-1980	V_{CC}-1980	V_{CC}-1980	V_{CC}-1980	V_{CC}-1980	mV
V_{ILmin}[5]	V_{CC}-2000	V_{CC}-2000	V_{CC}-2000	V_{CC}-2000	V_{CC}-2000	mV
I_{IH}[2] (max)	30	30	30	30	30	µA
I_{IL}[2] (max)	-.5	-.5	-.5	-.5	-.5	µA

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Table 24. ECL 100K Input/Output DC Characteristics V_{EE} = -4.5 V[3]

Symbol	Parameter	Test DC Conditions	Comm 0°/+70°C			MIL -55°/+125°C			Unit
			Min	Typ	Max	Min	Typ	Max	
V_{OH}	Output Voltage HIGH	Loading is 50 Ohms to -2V	V_{CC}-1053		V_{CC}-850	V_{CC}-1080		V_{CC}-835	mV
V_{OL}	Output Voltage LOW	Loading is 50 Ohms to -2V	V_{CC}-1830		V_{CC}-1605	V_{CC}-1880		V_{CC}-1595	mV
V_{IHmin}[5]	Input Voltage HIGH	Maximum input voltage HIGH	V_{CC}-1145		V_{CC}-800	V_{CC}-1145		V_{CC}-800	mV
V_{ILmax}[5]	Input Voltage LOW	Maximum input voltage LOW	V_{CC}-1950		V_{CC}-1475	V_{CC}-1950		V_{CC}-1475	mV
I_L[2]	Input LOW Current	$V_{IN} = V_{ILmax}$			-0.5			-0.5	µA
I_H[2]	Input HIGH Current	$V_{IN} = V_{IHmax}$			30			30	µA

Table 25. TTL Input/Output DC Characteristics

Symbol	Parameter	Test DC Conditions		Comm 0°/+70°C			Mil -55°/+125°C			Unit
				Min	Typ[4]	Max	Min	Typ[4]	Max	
V_{IH}[5]	Input HIGH Voltage	Guaranteed input HIGH voltage for all inputs		2.0			2.0			V
V_{IL}[5]	Input LOW Voltage	Guaranteed input LOW voltage for all inputs				0.8			0.8	V
V_{IK}	Input clamp diode voltage	V_{CC} = Min, I_{IN} = -18 mA			-.8	-1.2		-.8	-1.2	V
V_{OH}	Output HIGH Voltage	V_{CC} = Min, I_{OH} = -1 mA		2.7	3.4		2.4	3.4		V
V_{OL}	Output LOW Voltage	V_{CC} = Min	I_{OL} = 4 mA			0.4			0.4	V
			I_{OL} = 20 mA			0.5			0.5	V
I_{OZH}	Output "off current HIGH (3-state)	V_{CC} = Max, V_{OUT} = 2.4V		-50		50	-50		50	µA
I_{ZOL}	Output "off" current LOW (3-state)	V_{CC} + Max, V_{OUT} = 0.4V		-50		50	-50		50	µA
I_{IH}	Input HIGH current	V_{CC} = Max, V_{IN} = 2.7V				50			50	µA
I_I	Input HIGH current at MAX	V_{CC} = Max, V_{IN} = 5.5V				1.0			1.0	mA
I_{IL}[6]	Input LOW current	V_{CC} = Max, V_{IN} = 0.5V				-0.4			-0.4	mA
I_{OS}	Output short circuit current	V_{CC} = Max, V_{OUT} = 0.5V		-25		-100	-25		-100	mA

1 Data measured with V_{EE} = -5.2 ± .1V (or V_{CC} = 5.0 ± .1V for +5V ref. ECL 10K) assuming a +50°C rise between ambient (T_a) and junction temperature (T_J) for -55°C, 0°C, +25°C and +70°C, and a +25°C rise for +125°C. Specifications will vary based upon T_J. See AMCC Packaging and Design Guides concerning V_{OH} and V_{OL} adjustments associated with T_J for packages and operating conditions.

2 Per fan-in.

3 Data measured at thermal equilibrium, with maximum T_J not to exceed recommended limits. See AMCC Packaging Guide to compute T_J for specific package and operating conditions. For +5V ref. ECL 100K, V_{OH} and V_{OL} specifications will vary based upon power supply. See AMCC Design Guide for adjustment factors.

4 Typical limits are at 25°C, V_{CC} = 5.0V.

5 These input levels provide zero noise immunity and should only be tested in a static, noise-free environment. Use extreme care in defining input levels for dynamic testing. Many outputs may be changed at once, so there will be significant noise at the device pins and they may not actually reach V_{IL} or V_{IH} until the noise has settled. AMCC recommends using $V_{IL} \leq 0.4V$ and $V_{IH} \geq 2.4V$ for dynamic TTL testing and V_{ILMIN} and V_{IHMAX} for ECL testing.

6 For standard speed options only.

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