

# Q2334

## DUAL DIRECT DIGITAL SYNTHESIZER



### FEATURES

- Two Complete Direct Digital Synthesizer Functions On-chip
- Processor Interface for Control of Phase and Frequency
- Patented Algorithmic Sine Lookup Function
- Patented Noise Reduction Circuit
- Synchronous PSK and FSK Modulation Inputs
- Phase Resolution: 0.00000008° Using Processor-controlled Phase Adjustment
- Double Buffered Registers Allow Synchronous, Phase Coherent Frequency Change
- Simple External Multiplex Control for Binary Frequency Shift Keying (BFSK) Modulation
- Low Power: 667 mW Maximum at 50 MHz Clock Frequency per DDS
- Evaluation Board Available: Q0310

### APPLICATIONS

- Spread Spectrum Modulators
- Quadrature Oscillators
- Programmable Frequency Synthesizers
- Satellite Receivers
- Cellular Base Stations
- Magnetic Resonance Imaging (MRI)
- VXI-based ATE
- SONAR/RADAR
- Paging Systems
- High Performance Test Equipment
- Digital Radios and Modems
- HF Transceivers
- Local Oscillator Generation for VSAT, DBS, and GPS Applications

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## INTRODUCTION

QUALCOMM's Q2334 Dual Direct Digital Synthesizer (DDS) generates high resolution digitized sine wave signals using phase accumulation techniques combined with a patented on-chip sine lookup and Noise Reduction Circuit (NRC). The Q2334 contains two independent DDS functions controlled from a single microprocessor interface. This interface controls both the phase and the frequency of the generated sine waves as well as the device's operating mode. Synchronous inputs are also provided to allow for phase and frequency modulation.

The Q2334 provides greater than 76 dB rejection of phase truncation spurs and 72 dB amplitude quantization signal-to-noise ratio. This synthesizer is ideally suited for applications requiring high resolution sine wave generation, fast phase and frequency switching, and excellent phase and frequency stability.

The two independent on-chip DDS functions

provide an efficient technique for implementation of full-duplex systems, quadrature oscillators, and spread spectrum systems.

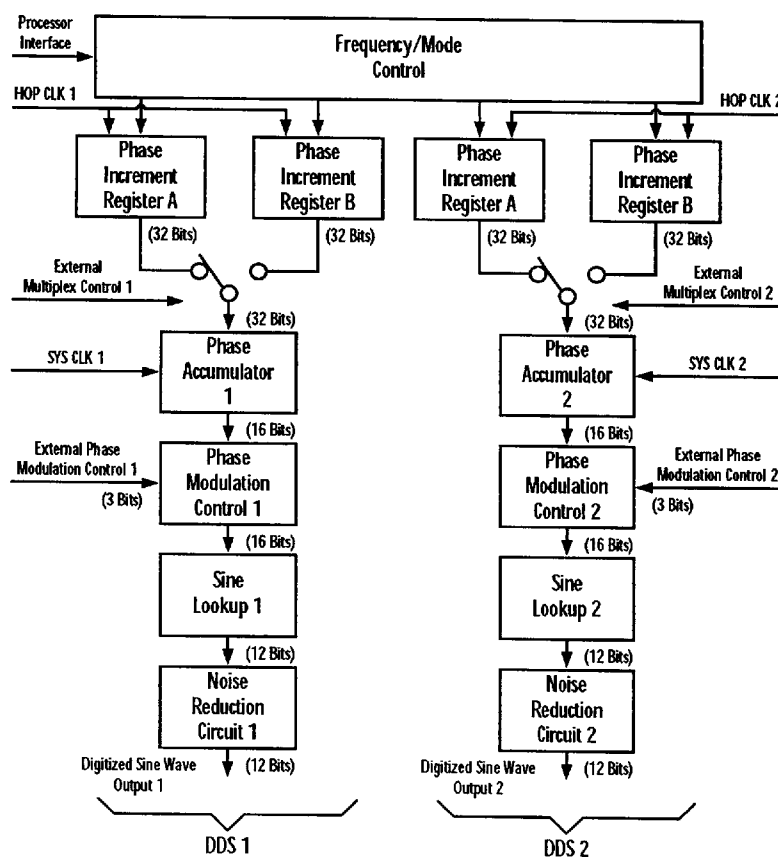
## GENERAL DESCRIPTION

The Q2334 consists of two independent DDS functions, each controlled by a common microprocessor interface, as illustrated in Figure 1.

Each DDS contains the following:

- Two Phase Increment Registers (PIR), A and B
- External Multiplex (Phase Increment Register) Control
- 32-Bit Wide Phase Accumulator
- 3-Bit External Phase Modulation Control
- Patented Sine Lookup Algorithm (see *Patent Reference 1*)
- Patented Noise Reduction Circuit (NRC) (see *Patent Reference 2*)

Figure 1. Q2334 Dual DDS Block Diagram



## INTERNAL ARCHITECTURE

### PROCESSOR INTERFACE

The processor interface controls the phase and frequency of the Q2334 DDS and is compatible with commonly used 8-bit microprocessors. This interface includes address decoding, chip selection, and write controls to load all on-chip control and phase increment registers. Table 1 provides the register address map for the device. Each register is write-only and is decoded from the five-bit input address bus.

**Table 1. Q2334 Microprocessor Interface Register Address Map**

DDS1 REGISTER ADDRESS (HEX)	DDS2 REGISTER ADDRESS (HEX)	FUNCTION
00	10	PIRA Bits 0-7 (LSB)
01	11	PIRA Bits 8-15
02	12	PIRA Bits 16-23
03	13	PIRA Bits 24-31 (MSB)
04	14	PIRB Bits 0-7 (LSB)
05	15	PIRB Bits 8-15
06	16	PIRB Bits 16-23
07	17	PIRB Bits 24-31 (MSB)
08	18	SMC
09	19	Reserved (not used)
0A	1A	AMC
0B	1B	Reserved (not used)
0C	1C	ARR
0D	1D	Reserved (not used)
0E	1E	AHC
0F	1F	Reserved (not used)

### PHASE INCREMENT REGISTERS (PIRs)

Two independent 32-bit phase increment registers (A and B) are provided for each DDS function in the Q2334. Each phase increment register is 32-bits wide. Phase Increment Register A (PIRA) of each DDS provides the phase increment for the most basic single-frequency operation. Phase Increment Register B (PIRB) provides the phase increment for a range of functions useful in various modes of operation of the DDS. The 32-bit value for each register is loaded using four 8-bit write operations. Each PIR is double-buffered and the phase increment used by the phase accumulator is unaffected by this new stored value until a hop clock signal is asserted.

### MODE CONTROL REGISTERS

The specific mode of the DDS operation is controlled by the Synchronous Mode Control (SMC) register and the Asynchronous Mode Control (AMC) register. The SMC is used for operations that may change throughout the operation of the DDS. The AMC should be setup once during initialization.

### SYNCHRONOUS MODE CONTROL (SMC) REGISTER

The SMC register and the two PIRs are double buffered. That is, these registers can be loaded at any time using the processor interface, but the values become active only when the signal HOP CLK is asserted. This makes possible the advanced synchronous phase and frequency change features of the Q2334 which are especially important when using the device in modulation or phase-locked loop applications.

The Asynchronous Hop Clock (AHC) can also be used to activate the double-buffered settings. Refer to the *Asynchronous Hop Clock* section for more information.

Figure 2 provides the bit definition for this SMC register. Bit 0 (LSB), 4, 5, 6, and 7 are reserved and should be set to logic "0". The remaining bits of the SMC register are the Hop Clock Phase Modulation Enable (HPME), External Multiplexer Enable (EME), and the External Phase Modulation Enable (EPME). Each of these bits is described below.

### HOP CLOCK PHASE MODULATION ENABLE (HPME)

The HPME bit is used when operating in the Internal Phase Modulation Mode. When the HPME bit is set to logic "1", the phase increment value stored in PIRB is added to the phase accumulator once each time the HOP CLK signal is asserted. If the Phase Modulation Add Enable (PMAE) bit is set to logic "0", all 32 bits of PIRB are used for the one time. However, if the PMAE bit is set to "1", the 8 MSB of PIRB are added to the 8 MSB of PIRA to form the 8 MSB to be accumulated with the 24 LSB of PIRA.

When the HPME bit is set to a logic "1", the HOP CLK signal is internally extended to two SYS CLK

Figure 2. Q2334 Synchronous Mode Control (SMC) Register

D7	D6	D5	D4	D3	D2	D1	D0
0*	0*	0*	0*	HOP CLK PHASE MOD ENABLE (HPME)	EXT MUX ENABLE (EME)	EXT PHASE MOD ENABLE (EPME)	0*

ADDRESS  $\times$  08 or 18 [hex]

\* These bits must be set to 0.

cycles. The two SYS CLK cycles make it possible for the phase accumulator to add the contents from PIRB once, and then switch the process immediately back to PIRA. To disable the Internal Phase Modulation Mode, as is the case when you want to reconfigure operation to the Basic Oscillator Mode for example, the HPME bit is reset to "0". The HOP CLK is required to initiate this change and during the HPME's transition from "1" to "0", the HOP CLK is no longer internally extended to two SYS CLK cycles and therefore the accumulation process will still accumulate the contents from PIRB. In order to switch the accumulation process back to PIRA, re-load PIRA with the intended frequency value, then assert another HOP CLK. Asserting a successive HOP CLK without re-loading PIRA will not switch the accumulation process from PIRB to PIRA. If desired, the contents of PIRB can be loaded with the same contents intended for PIRA concurrently with the HPME bit being disabled to "0". If this is done, then when the HPME transitions, the output will look as though only PIRA is being accumulated, although the user will want to make sure to re-load PIRA with the desired value and assert another HOP CLK so the accumulation process ends up on PIRA.

#### EXTERNAL MULTIPLEXER ENABLE (EME)

The EME bit enables the External Multiplex Control. When this bit is set to logic "1", the EXT MUX signal determines whether the value stored in PIRA or PIRB will be used for the phase accumulation process. The selection on the EXT MUX signal is synchronously

activated on the rising edge of the MUX CLK signal when the EME is set to logic "1". If the EME bit is set to logic "0", then the External Multiplex Control is disabled and the signal on EXT MUX is ignored. In this case, the contents of PIRA will be used for the accumulation process.

#### EXTERNAL PHASE MODULATION ENABLE (EPME)

The EPME enables the External Phase Modulation function. When this bit is set to "1", the PM EXT BITS are read and the corresponding phase offset is latched into the Q2334 each time the PM CLK is asserted. If External Phase Modulation is not used, set the EPME bit to "0". (Refer to the *External Phase Modulation* section.)

#### ASYNCHRONOUS MODE CONTROL (AMC) REGISTER

The AMC register has an active value once the information has been written to it. This register does not require a HOP CLK signal to become active. The AMC register of each DDS function includes control bits which should only be configured during initialization of the Q2334. The AMC commands should be activated before any other commands are asserted to the DDS in order for all commands to be received and processed properly. These control bits, as shown in Figure 3, include the DAC strobe or DAC strobe invert (DAC STB, DAC STB/), Phase Modulation Add Enable (PMAE), Output Format, and NRC Enable. Each of these is described below. Bits 4 and 6 of the AMC register are reserved and should be set to "0".

#### DAC STROBE, DAC STROBE INVERT (DACSTB, DACSTB/)

The DAC Strobe is a delayed version of the system clock which is provided along with the DAC BIT outputs in order to facilitate strobing this digitized sine value into a sample-and-hold DAC or other register. A non-inverted or inverted DAC Strobe is provided so that DAC devices with different triggering requirements can be easily accommodated. The DAC Output Timing specifications must be synchronized with respect to the falling edge of SYS CLK and are therefore only guaranteed in relation to the falling edge of SYS CLK. Trying to use the DACSTB timing associated with the rising edge of SYS CLK could potentially violate DAC setup time and result in strobing erroneous DAC BIT data.

When the AMC's D7 register is set to a "0", the DAC Strobe is non-inverted in relation to the system clock. This allows the falling edge of DACSTB to be used in compliance with SYS CLK. When the D7 register is set to a "1", the sense of the DAC Strobe is inverted in relation to the system clock. This allows the rising edge of DACSTB to be used in compliance with SYS CLK.

#### PHASE MODULATION ADD ENABLE (PMAE)

The PMAE bit is not used unless the HPME bit is set to "1". The PMAE bit controls the way in which the value stored in PIRB is used for the one-time accumulation by the phase accumulator. When the PMAE bit is set to logic "1" and PIRB is active for accumulation, the 8 MSB of PIRB are added to the 8 MSB of PIRA to form the 8 MSB to be accumulated. The 24 LSB of PIRA are used as the 24 LSB of the phase accumulator input value. This technique is useful for systems utilizing the Internal Phase Modulation Mode of operation. By storing the synthesizer frequency in the PIRA and modifying only the most significant byte of the PIRB, a 256-state phase modulator is implemented. This feature saves computation time in the processor controlling the DDS operation when a phase modulation system with 256-state (i.e.,  $360^\circ/256 = 1.41$  degrees) phase resolution is adequate. Using only the 8 MSB of PIRB to control the phase modulation allows the user to establish a byte-wide Direct Memory Access (DMA) control from the processor to the DDS function phase modulation register (i.e., PIRB), thus simplifying the processor

Figure 3. Q2334 Asynchronous Mode Control (AMC) Register

D7	D6	D5	D4	D3	D2	D1	D0
DAC STB	0*	PHASE MOD ADD ENABLE (PMAE)	0*	OUTPUT FORMAT**	NRC ENABLE BITS***		

\* These bits must be set to 0.

ADDRESS  $\times$  0A or 1A [hex]

**Output Format	D3
Two's Complement	0
Offset Binary	1

***DAC SIZE (# OF BITS)	D2	D1	D0
6	0	0	0
7	0	0	1
8	0	1	0
9	0	1	1
10	1	0	0
11	1	0	1
12	1	1	0
DISABLE NRC	1	1	1

overhead required to control the DDS function in rapidly switching phase modulation systems. When the PMAE bit is set to logic "0", all 32-bits of PIRB will be accumulated in the phase accumulator when PIRB is active allowing a phase resolution of  $360^\circ/2^{32}$ , i.e., 84 nano-degrees.

#### OUTPUT FORMAT

The Output Format bit determines the binary coding of the DAC output bits of each DDS function. When this bit is set to logic "1", the DAC output is encoded in offset binary format. When this bit is set to logic "0", the DAC output bits are encoded in two's complement format. Table 2 shows the effect of the setting of the Output Format bit.

**Table 2. Q2334 DAC Output Formats**

VALUE	OUTPUT FORMAT = 1 (OFFSET BINARY)		OUTPUT FORMAT = 0 (TWO's COMPLEMENT)	
	MSB	LSB	MSB	LSB
MAX Value	1	1	0	1
...	1	1	0	1
...	...	...	...	...
...	...	...	...	...
Half MAX + 1	1	0	0	0
Half MAX - 1	0	1	1	1
...	...	...	...	...
...	...	...	...	...
...	0	0	1	0
MIN Value	0	0	1	0

#### NRC ENABLE

When using the on-chip Noise Reduction Circuit (NRC) function, the number of significant bits to be used from the DAC outputs must be programmed into NRC Enable bits. The DAC bit-width is encoded in three bits as shown in Figure 3. When using a DAC with fewer than 12-bits resolution, the most significant DAC output bits are valid. The NRC function is disabled when the NRC Enable bits are set to 111 (binary). The function of the NRC circuit is described in the *Noise Reduction Circuit* section.

#### ACCUMULATOR RESET REGISTER (ARR)

Each DDS function on the Q2334 includes an Accumulator Reset Register (ARR). By writing any

value to the ARR, the accumulator reset function is armed. The next time the HOP CLK is asserted, the phase accumulator is reset to zero.

#### ASYNCHRONOUS HOP CLOCK (AHC)

Each DDS function includes an Asynchronous Hop Clock (AHC) register. When any value is written to this register, the previously stored values in the double-buffered PIRA, PIRB, and SMC registers are activated. This allows processor control of activation of these settings in an identical fashion as with the assertion of the HOP CLK signal. Note that the HOP CLK signal must be "Low" when the AHC register is accessed in order to activate the new register values. Also note that the timing for the AHC is exactly the same as the HOP CLK signal. Activation of the stored settings occurs within four SYS CLK periods after writing to the AHC register.

The AMC register has an active value once the information has been written to it. This register does not require a HOP CLK signal to become active.

#### PHASE INCREMENT MULTIPLEXER CONTROL

The phase increment multiplexer function selects which PIR (A or B) is used for the accumulation process. This multiplexing function provides a simple Binary Frequency Shift Keying (BFSK) interface to the DDS.

The signal EXT MUX controls the selection of the value stored in either PIRA or PIRB. For EXT MUX = 0, PIRA is selected; for EXT MUX = 1, PIRB is selected. The signal MUX CLK enables the selection made by the EXT MUX signal. The selection made by the EXT MUX signal is activated synchronously once during the low-to-high transition on the MUX CLK signal.

The MUX CLK signal is internally synchronized to the SYS CLK signal of the DDS. (Refer to the *Asynchronous Input* information contained in Figure 11 and Table 10.) The selection of the EXT MUX control may occur as frequently as once every four periods of SYS CLK. (Refer to the *External Control Timing* information contained in Figure 10 and Table 9.)

## PHASE ACCUMULATOR

Two 32-bit wide phase accumulators are included in the Q2334, one for each DDS function. These accumulators compute and store the sum of the previously computed phase value and the phase increment value from either PIRA or PIRB once during each period of SYS CLK.

## PHASE MODULATION CONTROL

Using the external phase modulation inputs, PM EXT BIT0-2, the output of the phase accumulator can be offset by phase increments of 45 degrees (from 0 degrees to 315 degrees) without affecting the operation of the phase accumulator. Table 3 shows the phase offset for the possible settings of the 3-bit external phase modulation inputs. These inputs are latched into the DDS function when the signal PM CLK is asserted. Changes in the external phase modulation are synchronized internally to the DDS function. This provides a simple 8-Phase Shift Keying (8PSK) interface to the DDS.

Refer to the *Modes of Operation* section for more detailed information on phase modulation.

## SINE LOOKUP FUNCTION

The Q2334 DDS implements a patented technique to generate a sine wave lookup (see *Patent Reference 1*). This algorithm takes the 16 MSB from the phase accumulator to generate a 12-bit sine wave value. Using this high precision lookup function, the phase truncation noise of the sine wave output is kept below 76 dB. This technique differs considerably from the traditional method of using a ROM lookup function.

Table 3. Q2334 External Phase Modulation Offset Settings

PM EXT BIT			ABSOLUTE PHASE OFFSET (degrees)
2	1	0	
0	0	0	0
0	0	1	45
0	1	0	90
0	1	1	135
1	0	0	180
1	0	1	225
1	1	0	270
1	1	1	315

This advanced look-up technique provides highly accurate and precise sine wave generation.

## NOISE REDUCTION CIRCUIT (NRC)

Noise due to amplitude quantization is often assumed to be random and uniformly distributed. However, because a sine wave function is periodic, this is not always the case. At certain output frequencies, amplitude quantization errors become highly correlated, thereby causing spurs.

Spurs associated with round-off errors of the quantized sine wave outputs can be significantly reduced by enabling the on-chip Noise Reduction Circuit (NRC). This patented circuit distributes the noise energy evenly across the frequency band, thus reducing the amplitudes of peak spurious components (see *Patent Reference 2*).

It is important to properly set the NRC Enable bits, because the operation of the NRC is scaled to the LSB. If an incorrectly sized DAC is specified, performance will be reduced.

If the Q2334 is used to generate narrowband outputs and a low noise floor is required, the signal should be bandpass filtered and the NRC disabled. As stated above, when the NRC is enabled it distributes the noise evenly across the frequency band and raises the noise floor. When the NRC is disabled, the noise floor is slightly lower and the quantization errors show up as discrete spurious. However, since the signal is bandpass filtered, the broadband spurious will be negligible.

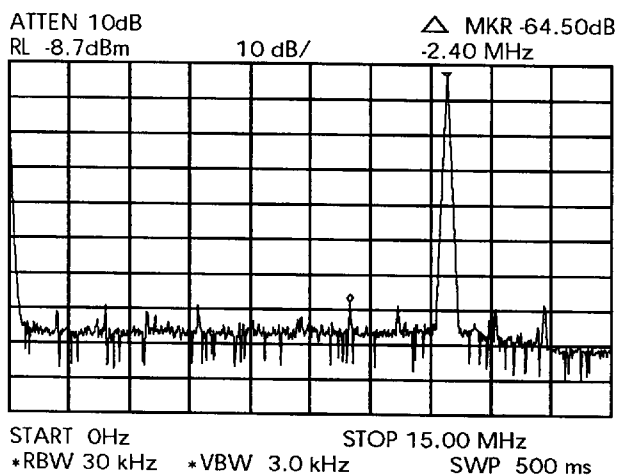
The output of the NRC (a 12-bit wide digitized sine wave) is normally connected to an external DAC function. This output value can be encoded in offset binary or two's complement format (see Figure 3).

Figures 4 and 5 show typical spectra of the analog converted outputs from the Q2334 with the NRC enabled and disabled. These spectra were measured with the DDS operating with a 10-bit DAC. The synthesized frequency in each of these figures is 10.8 MHz from a 30 MHz system clock frequency. The measurement frequency spans from 0 to 15 MHz, the resolution bandwidth is 30 kHz, the video bandwidth is 3 kHz, and the scale is 10 dB per vertical division.

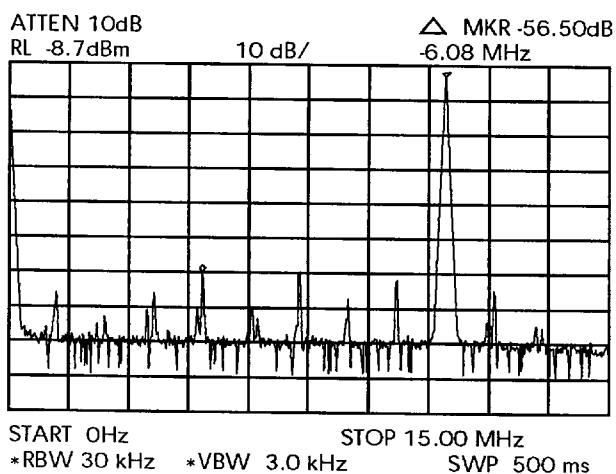


Figure 6 shows the typical performance of the Q2334 DDS when operating with a 10-bit DAC with NRC disabled and no LPF. This figure shows a 5 MHz output generated from a 20 MHz system clock frequency and the image at 15 MHz. This 15 MHz spur results from the negative image folded around the 30 MHz clock frequency. This image would normally be filtered by a LPF at the output of the DAC.

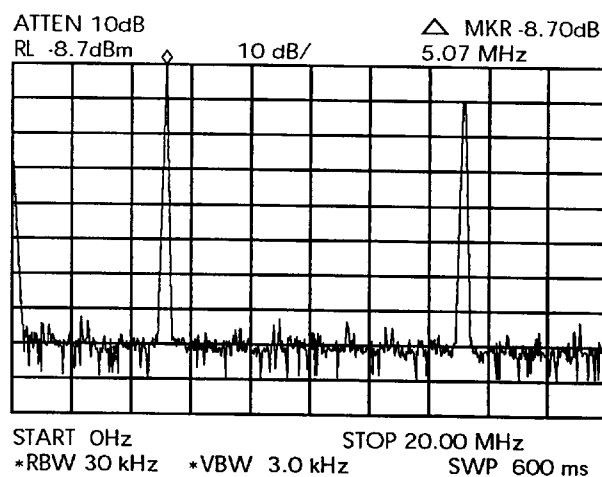
**Figure 4. Q2334 Typical Spectrum with NRC Enabled (10-bit DAC)**



**Figure 5. Q2334 Typical Spectrum with NRC Disabled (10-bit DAC)**



**Figure 6. Q2334 Typical Spectrum with LPF Disabled (10-bit DAC)**



## INPUT/OUTPUT SIGNALS

Figure 7 provides the pin configuration of the Q2334 DDS package and Table 4 provides a summary of the input/output signal pin assignments.

## SIGNALS COMMON FOR BOTH DDSs

The following signals are used in common for both DDS functions on the Q2334.

### DATA0...DATA7

INPUTS (6, 7, 8, 9, 43, 42, 41, 40)

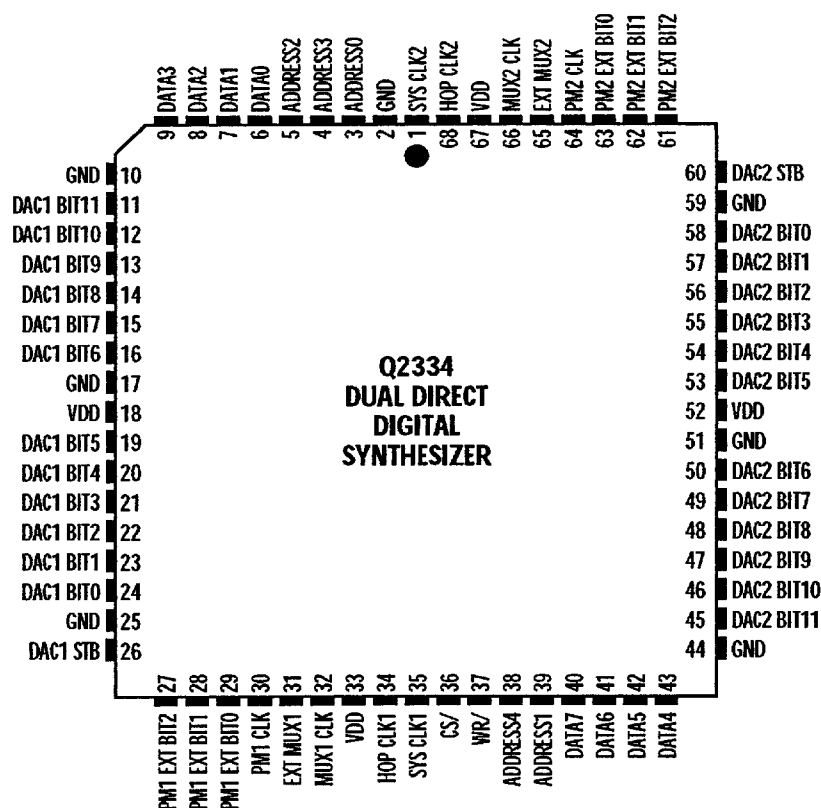
8-bit data bus for writing values to the on-chip processor interface registers. This bus is used for write operations only. DATA0 is the LSB.

### ADDRESS0...ADDRESS4

INPUTS (3, 39, 5, 4, 38)

5-bit address bus to select the internal processor interface registers. Addresses must be held fixed during the active period of the WR/ signal. ADDRESS0 is the LSB.

Figure 7. Q2334 Package Pin Configuration



#### CS/

INPUT (36)

Chip Select. Must be held "Low" during processor write accesses to the Q2334. Can be held "Low" all the time.

#### WR/

INPUT (37)

When "Low" while CS/ is "Low", writes the value of the data bus to the register determined by the address bus.

#### V<sub>DD</sub>

INPUT (18, 33, 52, 67)

Provides power to all Q2334 circuitry.

#### GND

INPUT (2, 10, 17, 25, 44, 51, 59)

Provides electrical ground reference for signal and power inputs.

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#### SIGNALS INDEPENDENT FOR EACH DDS

The following signals pertain to a specific DDS function (1 or 2) on the Q2334.

#### SYS CLK1, SYS CLK2

INPUT (35, 1)

Provides the fundamental clock frequency of the synthesized sine waveform. Internal operations of the phase accumulator, external phase modulation, and phase increment registers are synchronized to this clock signal.

#### HOP CLK1, HOP CLK2

INPUT (34, 68)

The HOP CLK signal controls the activation of the selection of the double buffered registers. HOP CLK must be active "High" for at least one SYS CLK period and can be asserted once every ten SYS CLK periods.

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Table 4. Q2334 Input/Output Signals

PIN #	NAME	I/O TYPE	DESCRIPTION	PIN #	NAME	I/O TYPE	DESCRIPTION
1	SYS CLK2	INPUT	System Clock to DDS #2	35	SYS CLK1	INPUT	System Clock to DDS#1
2	GND	INPUT	Ground Connection	36	CS/	INPUT	Chip Select - Low during Processor Writes
3	ADDRESS0	INPUT	Processor Interface Address Bus-bit 0 (LSB)	37	WR/	INPUT	Writes the Value of Data Bus into Register - Active Low
4	ADDRESS3	INPUT	Processor Interface Address Bus-bit 3	38	ADDRESS4	INPUT	Processor Interface Address Bus-bit 4 (MSB)
5	ADDRESS2	INPUT	Processor Interface Address Bus-bit 2	39	ADDRESS1	INPUT	Processor Interface Address Bus-bit 1
6	DATA0	INPUT	Processor Interface Data Bus-bit 0 (LSB)	40	DATA7	INPUT	Processor Interface Data Bus-bit 7 (MSB)
7	DATA1	INPUT	Processor Interface Data Bus-bit 1	41	DATA6	INPUT	Processor Interface Data Bus-bit 6
8	DATA2	INPUT	Processor Interface Data Bus-bit 2	42	DATA5	INPUT	Processor Interface Data Bus-bit 5
9	DATA3	INPUT	Processor Interface Data Bus-bit 3	43	DATA4	INPUT	Processor Interface Data Bus-bit 4
10	GND	INPUT	Ground Connection	44	GND	INPUT	Ground Connection
11	DAC1 BIT11	OUTPUT	DDS#1 Digitized Sine Wave Output-bit 11 (MSB)	45	DAC2 BIT11	OUTPUT	DDS#2 Digitized Sine Wave Output-bit 11 (MSB)
12	DAC1 BIT10	OUTPUT	DDS#1 Digitized Sine Wave Output-bit 10	46	DAC2 BIT10	OUTPUT	DDS#2 Digitized Sine Wave Output-bit 10
13	DAC1 BIT9	OUTPUT	DDS#1 Digitized Sine Wave Output-bit 9	47	DAC2 BIT9	OUTPUT	DDS#2 Digitized Sine Wave Output-bit 9
14	DAC1 BIT8	OUTPUT	DDS#1 Digitized Sine Wave Output-bit 8	48	DAC2 BIT8	OUTPUT	DDS#2 Digitized Sine Wave Output-bit 8
15	DAC1 BIT7	OUTPUT	DDS#1 Digitized Sine Wave Output-bit 7	49	DAC2 BIT7	OUTPUT	DDS#2 Digitized Sine Wave Output-bit 7
16	DAC1 BIT6	OUTPUT	DDS#1 Digitized Sine Wave Output-bit 6	50	DAC2 BIT6	OUTPUT	DDS#2 Digitized Sine Wave Output-bit 6
17	GND	INPUT	Ground Connection	51	GND	INPUT	Ground Connection
18	V <sub>DD</sub>	INPUT	+5V Power Supply Connection	52	V <sub>DD</sub>	INPUT	+5V Power Supply Connection
19	DAC1 BIT5	OUTPUT	DDS#1 Digitized Sine Wave Output-bit 5	53	DAC2 BIT5	OUTPUT	DDS#2 Digitized Sine Wave Output-bit 5
20	DAC1 BIT4	OUTPUT	DDS#1 Digitized Sine Wave Output-bit 4	54	DAC2 BIT4	OUTPUT	DDS#2 Digitized Sine Wave Output-bit 4
21	DAC1 BIT3	OUTPUT	DDS#1 Digitized Sine Wave Output-bit 3	55	DAC2 BIT3	OUTPUT	DDS#2 Digitized Sine Wave Output-bit 3
22	DAC1 BIT2	OUTPUT	DDS#1 Digitized Sine Wave Output-bit 2	56	DAC2 BIT2	OUTPUT	DDS#2 Digitized Sine Wave Output-bit 2
23	DAC1 BIT1	OUTPUT	DDS#1 Digitized Sine Wave Output-bit 1	57	DAC2 BIT1	OUTPUT	DDS#2 Digitized Sine Wave Output-bit 1
24	DAC1 BIT0	OUTPUT	DDS#1 Digitized Sine Wave Output-bit 0 (LSB)	58	DAC2 BIT0	OUTPUT	DDS#2 Digitized Sine Wave Output-bit 0 (LSB)
25	GND	INPUT	Ground Connection	59	GND	INPUT	Ground Connection
26	DAC1 STB	OUTPUT	DDS#1 Synchronous Strobe to Facilitate Clocking the DAC BITs into a DAC	60	DAC2 STB	OUTPUT	DDS#2 Synchronous Strobe to Facilitate Clocking the DAC BITs into a DAC
27	PM1 EXT BIT2	INPUT	DDS#1 Controls the External PM Value-bit 2	61	PM2 EXT BIT2	INPUT	DDS#2 Controls the External PM Value-bit 2
28	PM1 EXT BIT1	INPUT	DDS#1 Controls the External PM Value-bit 1	62	PM2 EXT BIT1	INPUT	DDS#2 Controls the External PM Value-bit 1
29	PM1 EXT BIT0	INPUT	DDS#1 Controls the External PM Value-bit 0	63	PM2 EXT BIT0	INPUT	DDS#2 Controls the External PM Value-bit 0
30	PM1 CLK	INPUT	DDS#1 Enables the Values in PM EXT BITs	64	PM2 CLK	INPUT	DDS#2 Enables the Values in PM EXT BITs
31	EXT MUX1	INPUT	DDS#1 Controls which PIR is Being Accumulated	65	EXT MUX2	INPUT	DDS#2 Controls which PIR is Being Accumulated
32	MUX1 CLK	INPUT	DDS#1 Enables the Value on EXT MUX1	66	MUX2 CLK	INPUT	DDS#2 Enables the Value on EXT MUX2
33	V <sub>DD</sub>	INPUT	+5V Power Supply Connection	67	V <sub>DD</sub>	INPUT	+5V Power Supply Connection
34	HOP CLK1	INPUT	Hop Clock to DDS#1	68	HOP CLK2	INPUT	Hop Clock to DDS#2

**EXT MUX1, EXT MUX2**

INPUT (31, 65)

When latched into the DDS with the signal MUX1 CLK (or MUX2 CLK) this signal determines which PIR (A or B) will be used for the incremental phase accumulator input value. When the EXT MUX signal is set to "1", the value stored in PIRB will be used by the phase accumulator. When the EXT MUX signal is set to "0", the value stored in PIRA will be used.

**MUX1 CLK, MUX2 CLK**

INPUT (32, 66)

The rising edge of this signal latches and enables the value on the EXT MUX inputs. This signal must be held "High" for a minimum of three SYS CLK periods. Activation of the EXT MUX inputs is synchronized internally to SYS CLK.

**PM1 EXT BIT0...PM1 EXT BIT2,****PM2 EXT BIT0...PM2 EXT BIT2****INPUTS** (29, 28, 27, 63, 62, 61)

External phase modulation inputs which control 45 degree phase offsets in the phase accumulated values in accordance with the settings provided in Table 3. PM EXT BITs are active when the signal PM CLK is asserted and are synchronized internally to the DDS function to SYS CLK.

**PM1 CLK, PM2 CLK****INPUT** (30, 64)

The rising edge of this signal latches and enables the value on the PM EXT BIT inputs. This signal must be held "High" for a minimum of three SYS CLK periods. The PM EXT BIT inputs are synchronized internally to SYS CLK.

**DAC1 BIT0...DAC1 BIT11, DAC2 BIT0...DAC2 BIT11****OUTPUTS** (24, 23, 22, 21, 20, 19, 16, 15, 14, 13, 12, 11, 58, 57, 56, 55, 54, 53, 50, 49, 48, 47, 46, 45)

Digitized sine wave outputs encoded in offset binary or two's complement format, depending on settings in the AMC Registers. One sample is generated during each period of SYS CLK. DAC BIT 0 is the LSB.

**DAC1 STB, DAC2 STB****OUTPUT** (26, 60)

Provides a synchronous strobe to facilitate clocking of the DAC BIT outputs into an external register or sampled DAC. One DAC STB is generated during each period of SYS CLK. Essentially, the DAC STB (or DAC STB/) is a delayed version of SYS CLK.

**MODES OF OPERATION**

Each DDS can be independently set to perform a wide range of expanded functions of the basic operation, as described in the following paragraphs.

**BASIC SYNTHESIZER MODE**

In its most Basic Operational Mode, each DDS on the Q2334 can provide a fixed frequency digitized sine wave output. The frequency of this sine output is determined by the frequency of the clock input and the

value stored in the PIRs. (See formula (1) in the *Phase Increment Value* section of the *General DDS* section.)

To set the Q2334 up in a Single Frequency Output Mode, the SMC should be set to "00" (hex). The AMC should be set according to the size of the DAC selected and the desired output format. The PMAE bit should also be set to "0". (Refer to the *Simple Oscillator Mode Example* section.)

**PHASE MODULATION MODE**

The Q2334 provides two means to implement phase modulation of a basic frequency output, referred to as Internal Phase Modulation and External Phase Modulation.

Internal Phase Modulation provides extremely fine resolution up to 0.00000008° of the phase adjustment ( $2^{32}$  - state phase resolution), while External Phase Modulation is designed for 45° increment phase shifts.

**INTERNAL PHASE MODULATION**

Internal Phase Modulation operates as a differential phase adjustment technique and requires use of the processor interface. The Internal Phase Modulation Mode is activated by loading PIRA with the correct phase increment for the basic frequency without phase modulation. PIRB is then loaded with the phase increment value equal to the phase increment value stored in PIRA plus the value of the desired phase offset. The phase accumulator uses PIRA for most phase accumulations.

Setting the HPME bit in the SMC register to logic "1" arms the DDS to use the 32-bit value in PIRB for one phase accumulation cycle when the signal HOP CLK is asserted. Since the phase increment value in PIRB is only used once for each HOP CLK assertion, the net effect is to cause a phase change to the generated sine wave.

When the PMAE bit is set to logic "1", the 8 MSB of PIRB are added to the 8 MSB of PIRA to form the 8 MSB to be accumulated with the 24 LSB of PIRA. This 32-bit value is used for one-time accumulation. If PMAE is "0", all 32 units of PIRB will be used for the accumulation.

The one-time phase shift occurs every time the HOP CLK signal is asserted. The phase shift can occur as often as the HOP CLK signal can be asserted. (Refer to *Processor Interface Timing* shown in Figure 8 and Table 7).

If it is desired to change the phase offset value, PIRB must be reloaded before the HOP CLK cycle with the new phase offset for the next HOP CLK period. The HPME bit will remain set to "1" until reset by the processor. (Refer to the *Hop Clock Phase Modulation Enable* section.)

## EXTERNAL PHASE MODULATION

External Phase Modulation operates as an absolute phase adjustment technique and utilizes special synchronous inputs separate from the processor interface. When using the External Phase Modulation Mode, the phase increment value for the unmodulated input is written into PIRA. PIRB is not used in the External Phase Modulation Mode.

The External Phase Modulation Enable (EPME) bit in the SMC register is set to logic "1" to enable the External Phase Modulation Mode. When the EPME bit is set to "1", the phase offset determined by the PM EXT BITs are latched into the DDS function each time the signal PM CLK is asserted. This PM EXT BIT setting causes a phase offset in 45° increments as indicated in Table 3. This mode of operation allows very simple control of the DDS as a binary, quaternary, or 8-ary phase shift keyed (8PSK) modulator.

## BINARY FREQUENCY SHIFT KEYING (BFSK) MODULATION MODE

Two PIRs are provided for each DDS function allowing for Binary Frequency Shift Keyed (BFSK) modulation without any additional hardware. The Q2334 provides signals allowing this switch to occur synchronously.

BFSK Modulation is achieved by setting the phase increment value in PIRA to generate the first frequency and the value in the PIRB to generate the second frequency. The EME bit is then set to logic "1" to enable the external multiplexer controls.

If the EXT MUX signal is set to logic "1" when the MUX CLK signal is asserted, the phase accumulator

will choose the phase increment value from PIRB. If the EXT MUX signal is set to logic "0" when the MUX CLK is asserted, the phase accumulator will choose the phase increment value from PIRA. Changing the value of the EXT MUX input causes the alternation between the frequency controlled by PIRA and the frequency controlled by PIRB.

After the BFSK Mode is set up and the PIRA and PIRB contents are active, the EXT MUX signal can be changed as fast as the MUX CLK can be asserted. (See *External Control Timings* shown in Figure 10 and Table 9). The MUX CLK timing is the only restriction on how fast the accumulation can be switched from PIRA to PIRB.

## MINIMUM SHIFT KEYING (MSK) MODULATION MODE

The Minimum Shift Keying (MSK) Modulation Mode is a subset of the BFSK Mode described above. The operation is the same, but the two frequencies are selected at a known mathematically determined rate. The MSK Modulation Mode is linear MSK and can be generated by setting the frequency shift rate equal to the separation between the two frequencies. This is where MSK got its name, since it is the minimum spacing between the two frequencies that can be accomplished while still recovering the signal with a given shift rate. If the frequency spacing is closer than the frequency shift rate, the information cannot be recovered. If the spacing is too far apart, the information can be retrieved using FSK demodulation techniques, although MSK will not be generated from the resultant spectra. To produce the two MSK frequencies, the values in PIRA and PIRB correspond to incrementing and decrementing phase values (respectively) that must change through  $\pm 90$  degrees for each symbol time of the frequency shift rate. This is obtained by loading PIRA and PIRB with frequency values such that the mid-point value between them is separated by  $\pm$  FSK rate/2. This must occur without any phase discontinuities but since the DDS changes frequencies in a phase continuous fashion, this is not a problem. The overall result due to the slow phase transitions between the frequencies is a reduction in the high-frequency spectral content, thus attenuating

the sidelobes. The spectrum is said to be more efficient since more power is contained in the main lobe and less in the sidelobes. The EME bit of the SMC register is set to logic "1", as in the BFSK Mode, and the EXT MUX and MUX CLK signals control the shift between the values of PIRA and PIRB.

### FREQUENCY HOPPING MODE

Simple frequency hopping can be enabled by writing a new phase increment value of the desired frequency in PIRA. Since PIRA is a double buffered register, this value will be activated at the next assertion of the HOP CLK signal.

Assuming each frequency to be generated requires all 32 bits to be changed, then four 8-bit writes to PIRA would be needed. (See *Processor Interface Timing* shown in Figure 8 and Table 7.) After PIRA has been loaded, the assertion of the HOP CLK will activate these settings and the resulting frequency will be output from the Q2334 within 31 clock cycles. The frequency value can be changed as fast as the new phase increment value can be written to PIRA and a HOP CLK signal asserted. (Also see Figure 8 and

Table 7.) Once all 32 bits have been activated, the contents will remain until the register is written again. Subsets within the register may also be written. This allows for the changing of an existing register value using a single 8-bit write as opposed to four 8-bit writes.

### PIPELINE DELAY

The output of the Q2334 DDS will reflect the change in status activated by the HOP CLK within 30 to 31 SYS CLK periods. When the EXT MUX signal is enabled, the associated PIR will affect the output in 29 to 30 SYS CLK periods after the MUX CLK has been asserted. If External Phase Modulation is implemented, the phase shift will occur 28 to 29 SYS CLK periods after the rising of the PM CLK.

The one SYS CLK ambiguity occurs because the MUX CLK, PM CLK, and HOP CLK signals are allowed to be asynchronous in relation to the SYS CLK. To keep the internal operation of the Q2334 synchronous, the signals are input to synchronizing circuitry which resolves the signal to within one clock period.

## TECHNICAL SPECIFICATIONS

### ABSOLUTE MAXIMUM RATINGS

Table 5 shows the absolute maximum ratings of the Q2334. Stresses above those listed may cause permanent damage to the device. This is a stress rating only and functional operation of the device at

these or any other conditions above those indicated in the operational sections of this data book is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

**Table 5. Q2334 Absolute Maximum Ratings**

PARAMETER	SYMBOL	MIN	MAX	UNITS	NOTE
Storage Temperature	$T_S$	-55	+85	°C	—
Operating Temperature	$T_A$	0	+70	°C	—
Junction Temperature	$T_J$	—	+150	°C	1
Voltage on any Input Pin	—	-0.3	$V_{DD} + 0.3$	V	—
Voltage on VDD & any Output Pin	—	-0.3	+7.0	V	—
DC Input Current	$I_{IN}$	-10	+10	μA	—

Note:

1. For thermal management consideration, the Junction to Case Thermal Resistance,  $\theta_{JC}$  is 10.7°C/W typical, and the Junction to Ambient Thermal Resistance,  $\theta_{JA}$  is 33°C/W typical.

### DC ELECTRICAL CHARACTERISTICS

Table 6 shows the DC electrical characteristics for the Q2334.

**Table 6. Q2334 DC Electrical Characteristics**

PARAMETER	SYMBOL	MIN	MAX	UNITS	NOTES
Supply Voltage	$V_{DD}$	4.75	5.25	V	—
High-level Input Voltage	$V_{IH}$	2.0	$V_{DD} + 0.3$	V	—
Low-level Input Voltage	$V_{IL}$	-0.3	0.8	V	—
Input Leakage Current	$I_L$	—	1.0	μA	—
High-level Output Voltage	$V_{OH}$	2.4	—	V	1
Low-level Output Voltage	$V_{OL}$	—	0.4	V	2
Power Dissipation @ Maximum SYS CLK	$P_D$	—	0.67 @50 MHz	W	3,4

Notes:

1.  $I_{OH} = -1.6$  mA.
2.  $I_{OL} = 1.6$  mA.
3. Power rating is per DDS. If both DDS1 and DDS2 are operating at same conditions, the power will be doubled.
4. For other clock frequencies,  
Power  $\leq (13.33 \text{ mW/MHz}) * (\text{Clock Frequency})$ ;  
Current  $\leq (2.66 \text{ mA/MHz}) * (\text{Clock Frequency})$ .

## TIMING SPECIFICATIONS

Figures 8 through 11 and Tables 7 through 10 show the timing specifications of the Q2334.

Figure 8. Q2334 Processor Interface Timing Diagram

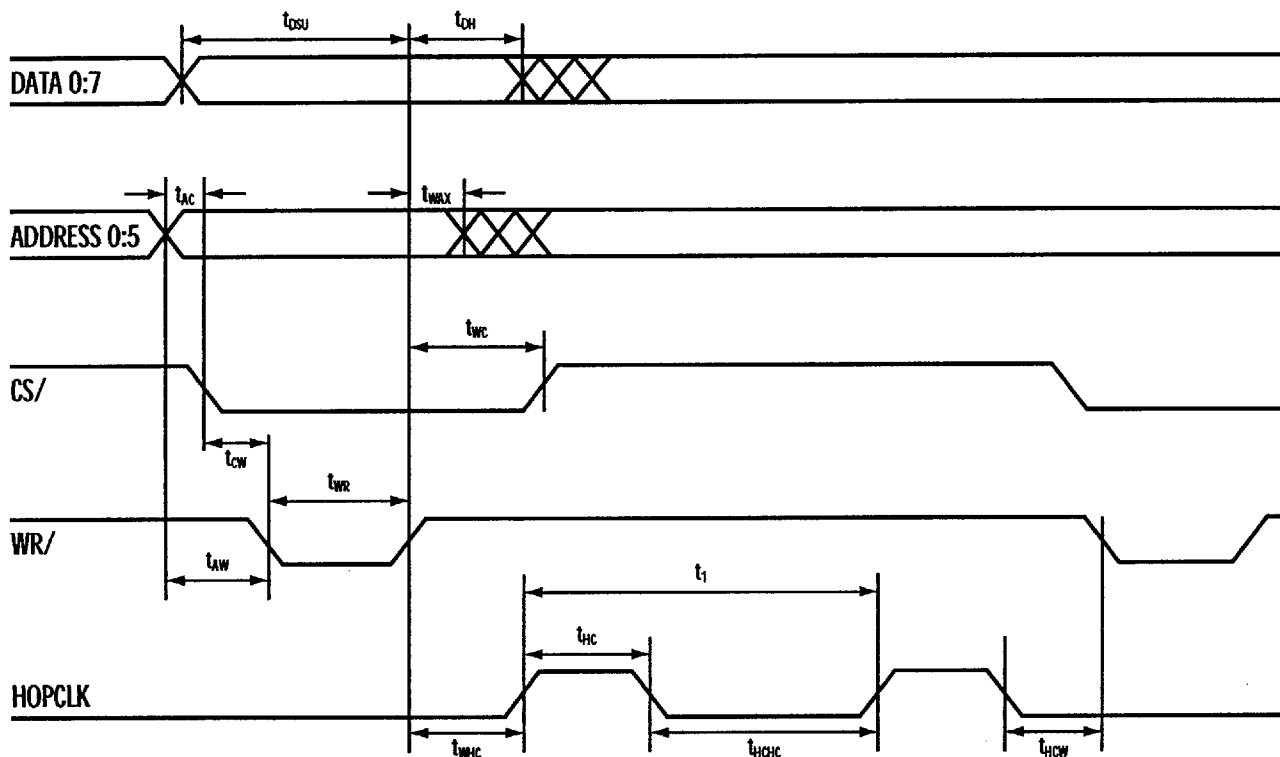


Table 7. Q2334 Processor Interface Timing Parameters

PARAMETER	SYMBOL	MIN	MAX	UNITS	NOTES
Data Setup to WR/ Rising	$t_{DSU}$	10	—	ns	—
Data Hold After WR/ Rising	$t_{DH}$	5	—	ns	—
Address Valid to CS/ Falling	$t_{AC}$	0	—	ns	—
Address Hold After WR/ Rising	$t_{HAX}$	5	—	ns	—
CS/ Setup to WR/ Falling	$t_{WC}$	0	—	ns	—
CS/ Hold After WR/ Rising	$t_{CW}$	0	—	ns	—
WR/ Rising to HOP CLK Rising	$t_{WR}$	10	—	ns	1
HOP CLK Pulse Width	$t_{HC}$	$t_{CYC}$	—	ns	2
HOP CLK Falling Edge to HOP CLK Rising Edge	$t_{HCHC}$	$4 \cdot t_{CYC}$	—	ns	2
HOP CLK Falling Edge to WR/	$t_{HCW}$	$10 \cdot t_{CYC}$	—	ns	1,2
Address Valid to WR/ Falling	$t_{AW}$	15	—	ns	—
WR/ Period	$t_{WR}$	40	—	ns	—
Time Between HOP CLK	$t_1$	$10 \cdot t_{CYC}$	—	ns	2

### Notes:

1. When CS/ is active "Low".
2.  $t_{CYC}$  is the system clock period.



Figure 9. Q2334 DAC Output Timing Diagram

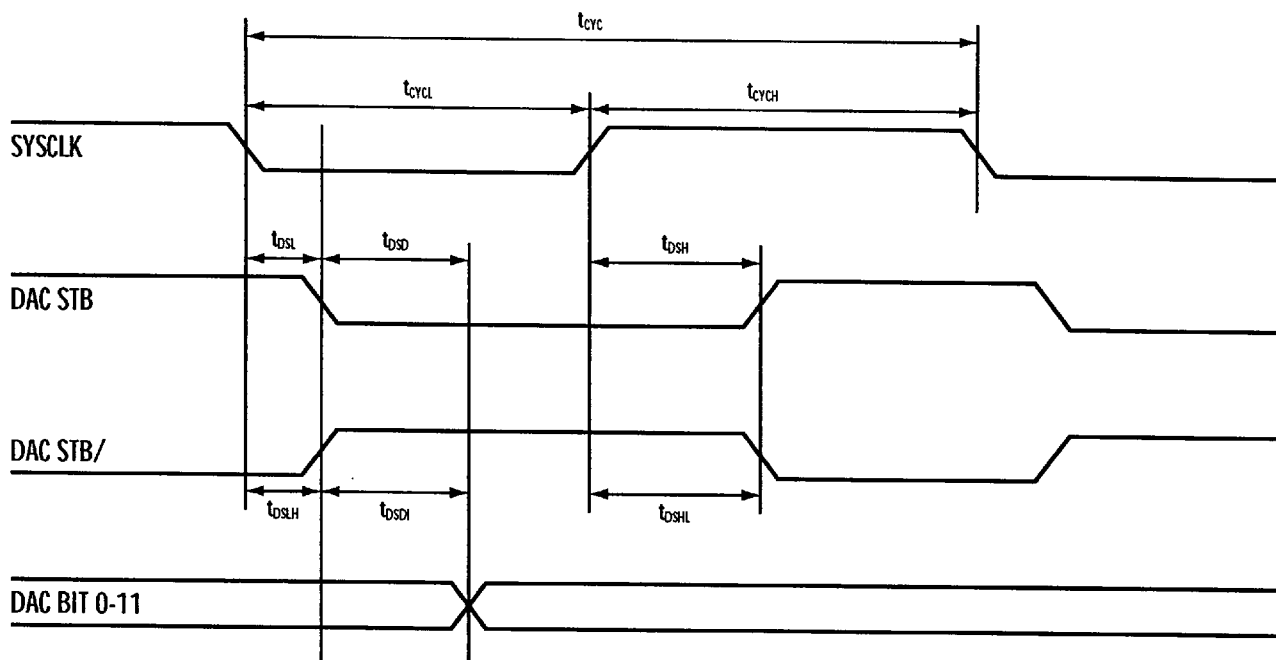


Table 8. Q2334 DAC Output Timing Parameters

PARAMETER	SYMBOL	20 MHz Max Clock		30 MHz Max Clock		40 MHz Max Clock		50 MHz Max Clock		UNITS	NOTES
		MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX		
SYS CLK Cycle Period	$t_{CYC}$	50	1000	33	1000	25	1000	20	1000	ns	1, 2, 3
SYS CLK Low Period	$t_{CYL}$	22	478	15	485	11.25	488.75	8.5	491.5	ns	—
SYS CLK High Period	$t_{CYH}$	22	478	15	485	11.25	488.75	8.5	491.5	ns	—
SYS CLK Low to DAC STB Low	$t_{DSL}$	—	10	—	10	—	10	—	10	ns	4
SYS CLK Low to DAC STB/ High	$t_{DSLH}$	—	10	—	10	—	10	—	10	ns	4
SYS CLK High to DAC STB High	$t_{DSH}$	—	10	—	10	—	10	—	10	ns	4
SYS CLK High to DAC STB/ Low	$t_{DSHL}$	—	10	—	10	—	10	—	10	ns	4
DAC STB Low to DAC BIT Output	$t_{DSD}$	4	20	4	17	4	17.5	4	14	ns	4
DAC STB/ High to DAC BIT Output	$t_{DSDI}$	4	20	4	17	4	17.5	4	14	ns	4

Notes:

1. The Q2334C-50N will operate up to 30 MHz maximum clock with  $-55 \leq T \leq 125^{\circ}\text{C}$  and  $4.5 \leq V_{DD} \leq 5.5 \text{ V}$ .
2. The Q2334C-50N will operate up to 40 MHz maximum clock with  $-40 \leq T \leq 85^{\circ}\text{C}$  and  $4.5 \leq V_{DD} \leq 5.5 \text{ V}$ .
3. The Q2334 contains dynamic logic. Minimum SYS CLK frequency is 1.0 MHz.
4. Assumes a 25pF capacitive loading.

Figure 10. Q2334 External Control Timing Diagram

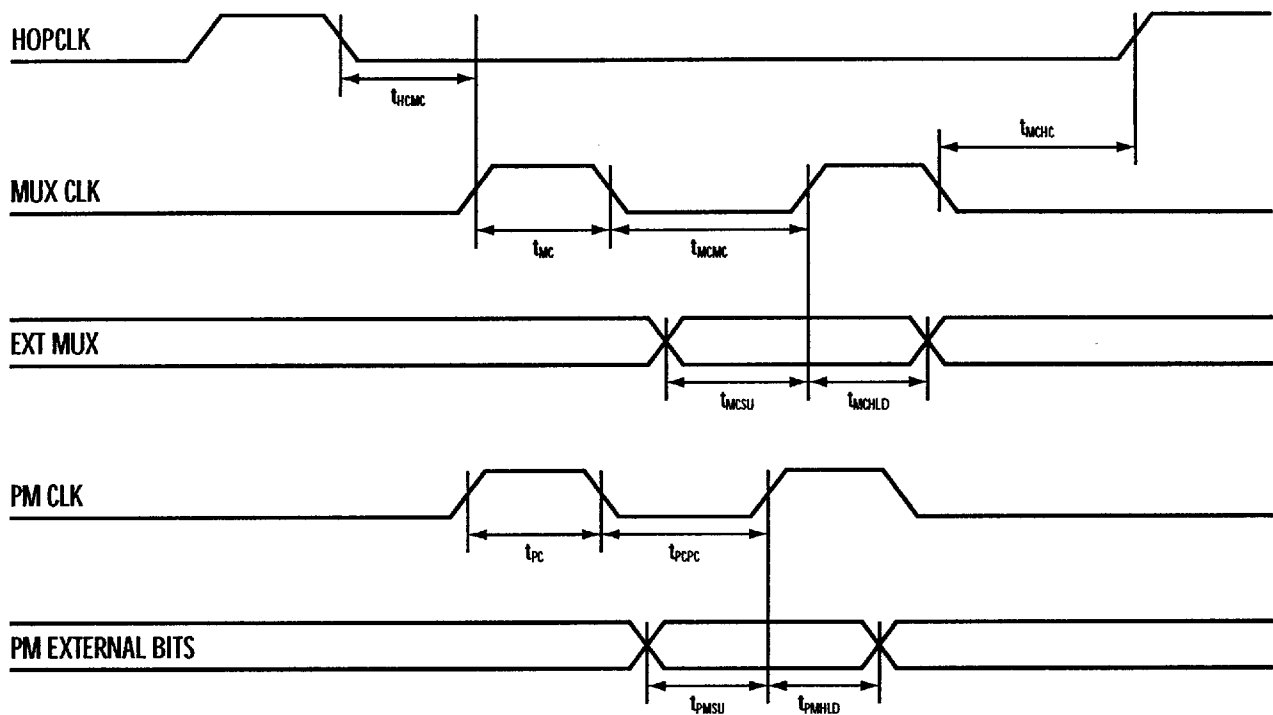


Table 9. Q2334 External Control Timing Parameters

PARAMETER	SYMBOL	MIN	MAX	UNITS	NOTES
HOP CLK Falling to MUX CLK Rising	$t_{H2MC}$	$t_{CYC}$	—	ns	1
MUX CLK High Period	$t_{MC}$	$3 \cdot t_{CYC}$	—	ns	1
MUX CLK Low Period	$t_{MCNC}$	$t_{CYC}$	—	ns	1
MUX CLK Falling to HOP CLK Rising	$t_{MCHC}$	$10 \cdot t_{CYC}$	—	ns	1
EXT MUX Setup to MUX CLK	$t_{MCSU}$	10	15	ns	—
EXT MUX Hold After MUX CLK	$t_{MCHLD}$	10	15	ns	—
PM CLK High Period	$t_{PC}$	$3 \cdot t_{CYC}$	—	ns	1
PM CLK Low Period	$t_{PCPC}$	$t_{CYC}$	—	ns	1
PM Data Setup to PM CLK	$t_{PMSU}$	10	15	ns	—
PM Data Hold After PM CLK	$t_{PMHLD}$	10	15	ns	—

Notes:

1.  $t_{CYC}$  is the system clock period.

## PLCC PACKAGING

The Q2334C-50N is packaged in the 68-pin plastic leaded chip carrier (PLCC) shown in Figure 11. The dimensions are given in inches and (mm).

Figure 11. Q2334 68-pin PLCC Package Diagram

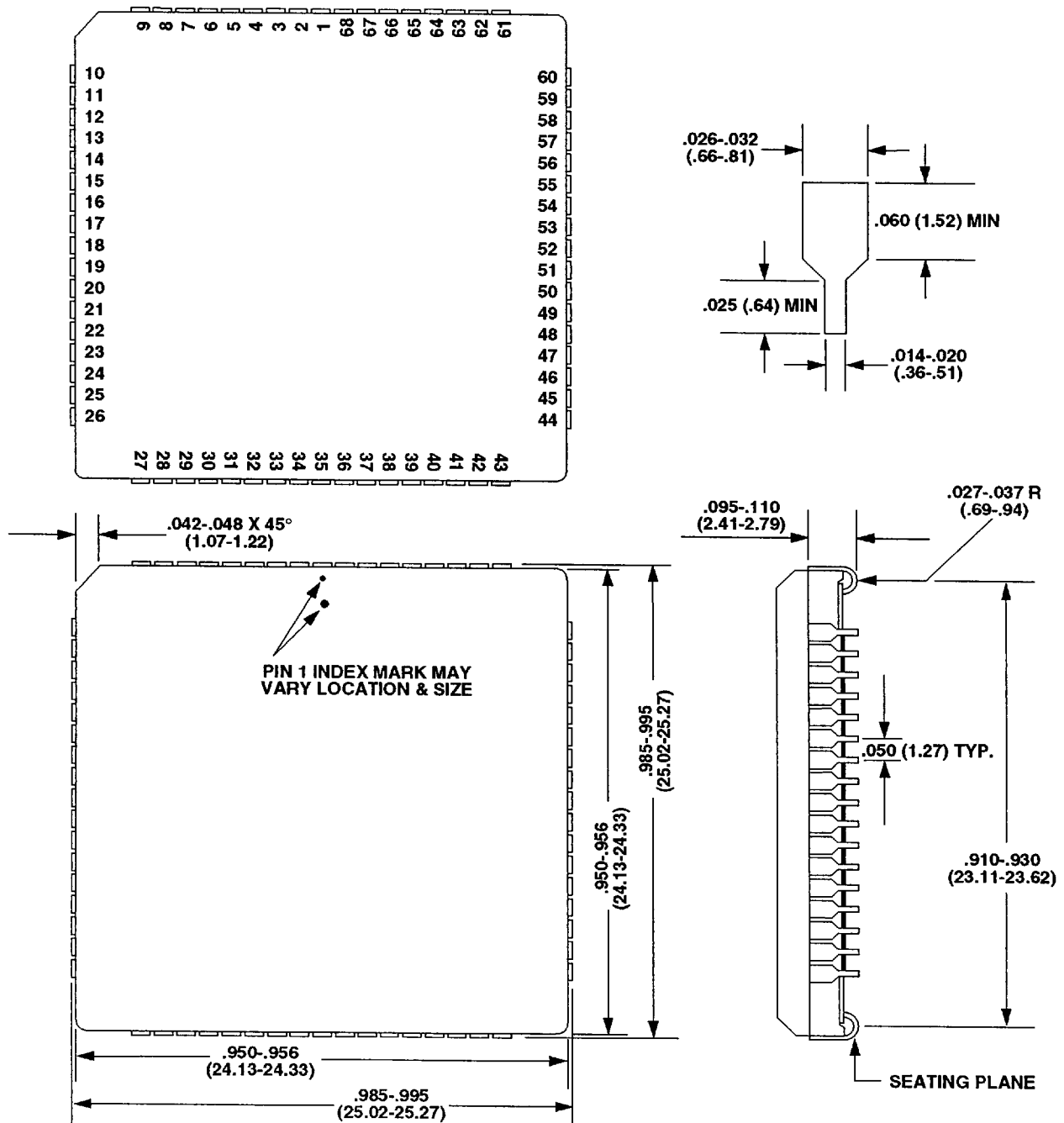
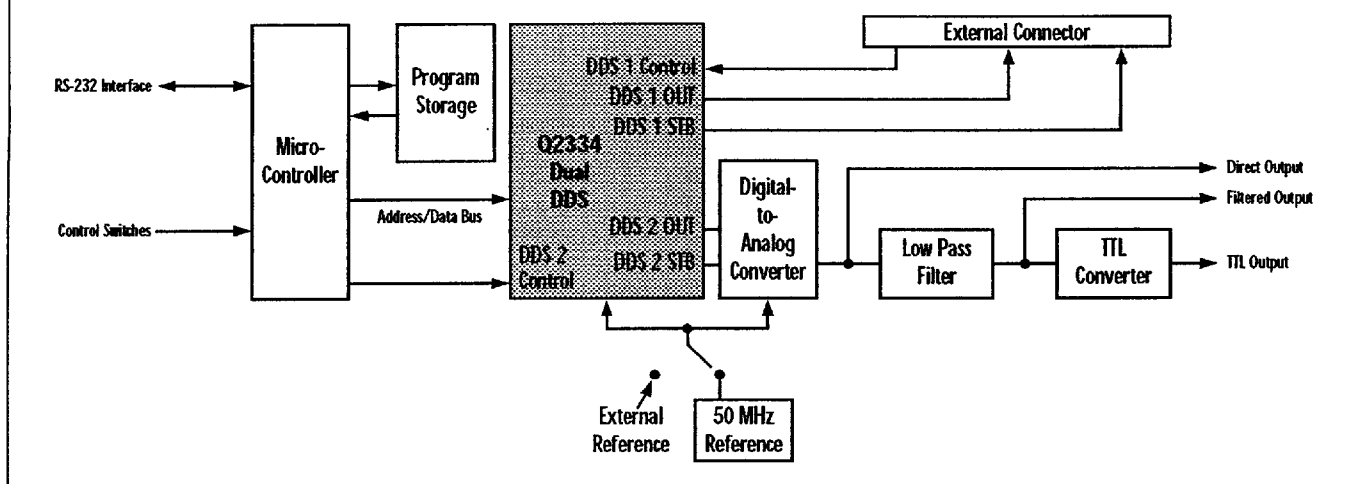


Figure 12. Q0310 Block Diagram



## Q0310 DDS EVALUATION BOARD

The Q0310 is an evaluation board for the Q2334 DDS. The Q0310 is a complete DDS System that includes a Q2334C-50N, pre-programmed microcontroller, 10-bit DAC, and low pass filter all designed onto an 8" x 4" x 1.5" printed circuit card that is fully assembled and tested. An 8031 microcontroller controls the DDS using a monitor program contained in the on-board EPROM. This program interacts through the switches on the board for stand-alone operation or through the RS-232 port for remote operation. A block diagram of this particular configuration is shown in Figure 12. The menu-driven monitor program can exercise all of the following modes of operation:

- Basic Oscillator
- Frequency Sweep (Fast or Slow)
- Frequency Hop
- 8-PSK Modulator
- 256-PSK Modulator
- MSK Modulator

A Q0310 User's Guide with complete documentation including schematics, parts list, and microcontroller code (available in floppy disk) is included.

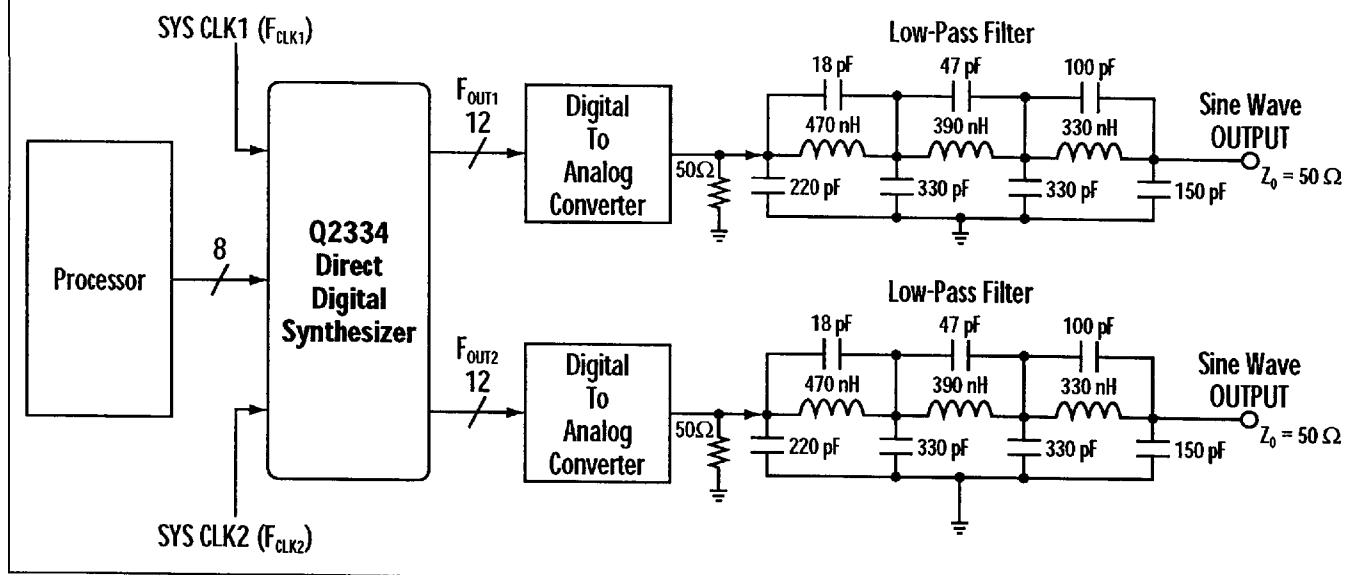
## DDS SYSTEM DIAGRAM

Figure 13 provides a basic diagram of a Q2334 DDS system. Note the LPF used is a seven pole elliptical filter designed for operation with a 50 MHz clocked DDS, which rolls off at approximately 20 MHz. This is the filter topology used in the Q0310 DDS Evaluation Board. Each system has different specifications, and the design of the LPF should take the system requirements into account.

## RECOMMENDED SOCKETS

Methode Electronics 213-052-602 Low Profile Surface Mount 68-pin carrier socket; AMP 821574-1 thru-hole 68-pin carrier socket.

Figure 13. Q2334 DDS System



## PATENT REFERENCES

- 1.) U.S. Patent No. 4,905,177 - "High Resolution Phase to Sine Amplitude Conversion," QUALCOMM, Feb. 27, 1990.
- 2.) U.S. Patent No. 4,901,265 - "Pseudorandom Dither for Frequency Synthesis Noise," QUALCOMM, Feb. 13, 1990.