5-126 Qmp

000975

DEVICE SPECIFIC † 975 Amc

APPLIED MICRO CIRCUITS CORPORATION

Q6000A SERIES CMOS LOGIC ARRAYS

FEATURES

TECHNOLOGY
Q6000A Series arrays feature 1.8-micron silicon-gate CMOS with two-level metalization, offering high performance and up to 85% chip utilization.

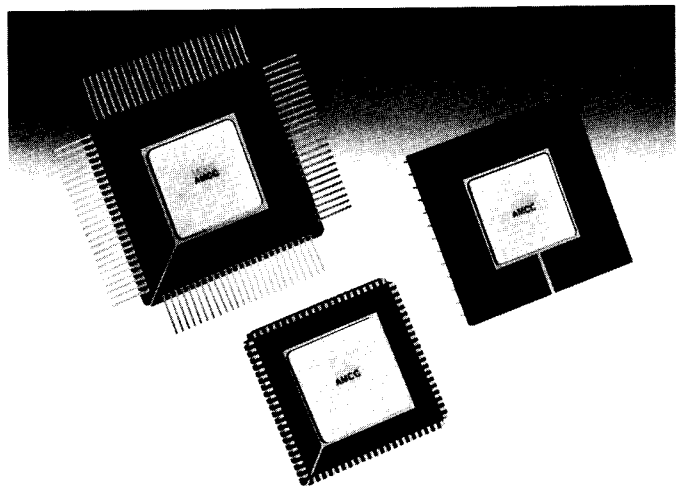
SIX ARRAY SIZES
1400 to 6200 equivalent gate densities are available in the Q6000A Series.

UP TO 154 I/0 CAPABILITY
The Q6000A Series arrays have from 74 I/Os on the Q1400D to 154 I/Os on the Q6200D.

EXTENSIVE MSI MACROS
Q6000A Series arrays provide extensive MSI macros for ease in system design. There are over 180 hard-wired macros consisting of powerful MSI, I/O, logic and storage macros characterized for immediate use in system design.

HIGH SPEED WITH LOW POWER
Q6000A Series arrays feature a 1.3ns typical internal gate delay (2-input NAND gate) dissipating less than 20μW per gate per MHz.

STTL & CMOS COMPATIBLE
Q6000A Series logic arrays offer a wide selection of I/O macros which are compatible with CMOS and TTL systems using a single +5V power supply.



DESCRIPTION
The AMCC Q6000A Series consists of the Q1400D, Q1750D, Q2700D, Q3300D, Q4300D and Q6200D arrays. These arrays offer densities ranging from 1400 to 6200 equivalent 2-input NAND gates. The Series is optimized to provide a systems approach to high performance, low-power semicustom military and commercial applications.

The AMCC Q6000A Series arrays are fabricated using a state-of-the-art 1.8-micron, double-level-metal process to provide high density and speed with low power. When combined with an advanced, interactive CAD system they provide a quick and cost-effective solution to discrete IC replacement.

An extensive library of predefined single- and multiple-cell logic macros is provided for the Q6000A Series. In addition to a broad variety of basic logic functions, such as gates and flip/flops, the library offers one of the most extensive selections of hard-wired MSI macros. The extended MSI library provides commonly used logic functions such as 4-bit counters, full adders and shift registers which are optimized to provide improved speed and circuit density over logically equivalent SSI macros. The hard-wired approach to MSI design leads to accurate repeatable performance of these functions over the full temperature range, as well as, greater silicon efficiency over gate-level logic designs.

PERFORMANCE SUMMARY

PARAMETER	VALUE
Typical internal gate delay (2-input NAND, fanout = 2, including 2mm metal)	1.3ns
Maximum flip/flop toggle frequency	60MHz
Typical TTL input delay (includes a fanout of 2)	T_{PLH} = 2.3ns T_{PHL} = 2.5ns
Typical CMOS input delay (includes a fanout of 2)	T_{PLH} = 1.6ns T_{PHL} = 1.4ns
Typical TTL output delay (15 pf load)	T_{PLH} = 4.1ns T_{PHL} = 5.2ns
Typical CMOS output delay (10 pf load)	T_{PLH} = 3.8ns T_{PHL} = 5.1ns
TTL compatible output drive (V_{OL} = 0.4 VDC)	8mA
Power dissipation per basic gate	Less than 20 μWatt/Gate-MHz
Average cell utilization	85%

TABLE 1

RESOURCE SUMMARY

DESCRIPTION	Q1400D	Q1750D	Q2700D	Q3300D	Q4300D	Q6200D
Basic 2-input NAND gates	1394	1746	2667	3312	4342	6206
Dedicated input cells	6	6	6	6	6	8
Bidirectional I/O cells	68	76	94	104	120	146
Recommended power connections (each power connection requires 1 I/O cell)	4	6	8	8	12	16

TABLE 2

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ARCHITECTURE

Q6200D – Die Size 382 x 382 Mils

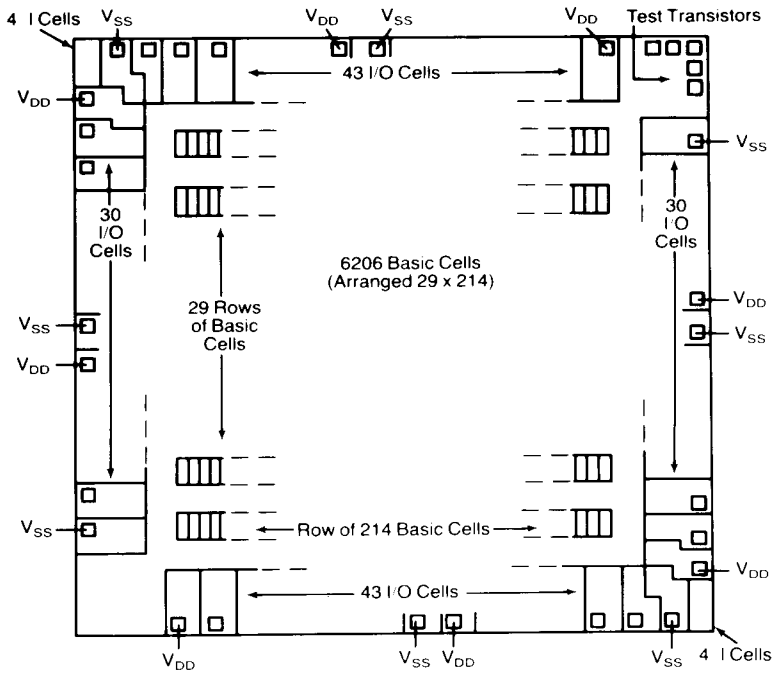


FIGURE 1

Q3300D – Die Size 273 x 273 Mils

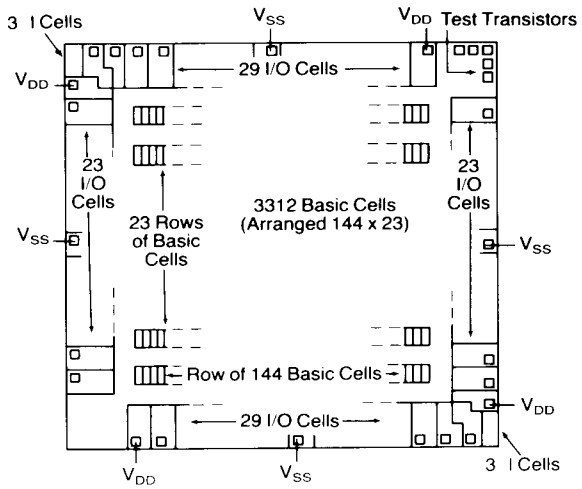


FIGURE 2

Q1750D – Die Size 202 x 202 Mils

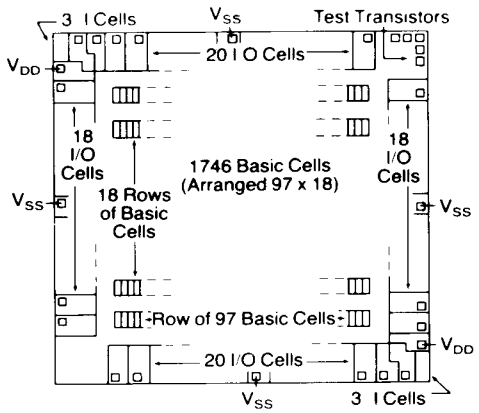


FIGURE 3

ARRAY ARCHITECTURE

The Q6000A Series logic array structure is comprised of two basic configurable internal and I/O cell types. The macro libraries provide the available logic and I/O functions with customization performed by adding a two-layer metal interconnect to the base array according to the customer specified design. Interconnections between macros use both first and second layers of metal and are performed automatically by AMCC CAD software. Liberal allocation of interconnect routing channels permits a high 85% cell utilization.

The core of each logic array is comprised of a matrix of internal cells organized in a row-column configuration. I/O cells and multiple power and ground connections are distributed around the perimeter of the device. Representative Q6000A Series die layouts are illustrated in Figures 1 - 3.

INTERNAL CELL

The Q6000A Series arrays' internal cell resources are presented in Table 2 on page 1. All internal cells have identical structure, consisting of two P-channel and two N-channel transistors, and are positioned in uniform rows across the arrays. Single cells support simple SSI macros while multiple internal cells are utilized for more complex SSI and MSI functions.

I/O CELL

Located around the periphery of the chip, two types of Q6000A Series interface cells are provided. I/O cells, positioned along the sides of the device, may be individually configured as TTL or CMOS inputs, outputs or bi-directional interfaces. Large dimension transistors are used in the I/O cells for external interface to both TTL and CMOS logic. Positioned in the corners of each array, "I" cells permit inputs meeting either TTL or CMOS logic levels. Mixed TTL/CMOS operation is permitted.

MACRO CAPABILITIES

AMCC offers an extensive selection of macros, ranging from fundamental Boolean logic to complex MSI functions. Created from ten or fewer internal cells, more than 50 basic logic macros are available, including simple and complex gates, inverters, buffers, latches and flip/flops. Representative standard macros with their associated performance are presented in Figure 4.

TYPICAL STANDARD MACROS

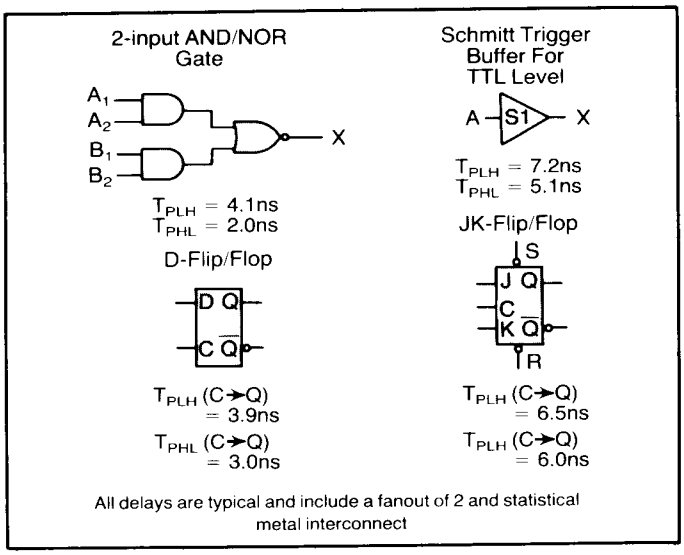
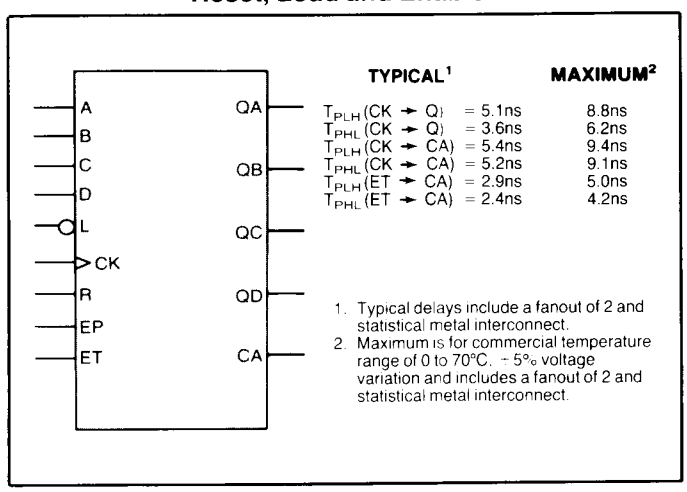


FIGURE 4

With more than 60 functions, AMCC's Q6000A Series offers the broadest library of hard-wired MSI macros. Including functions such as adders, counters, decoders, data and shift registers and multiplexers, MSI macros simplify and speed the design process. Compared to other software-based MSI macro functions, AMCC's hard-wired MSI macros offer higher speed and predictable repeatable performance. Typical MSI macro function and performance are provided in Figure 5.

TYPICAL MSI MACRO

Fully Synchronous 4-bit Binary Counter With Reset, Load and Enable



	TYPICAL[1]	MAXIMUM[2]
T_{PLH} (CK → Q)	= 5.1ns	8.8ns
T_{PHL} (CK → Q)	= 3.6ns	6.2ns
T_{PLH} (CK → CA)	= 5.4ns	9.4ns
T_{PHL} (CK → CA)	= 5.2ns	9.1ns
T_{PLH} (ET → CA)	= 2.9ns	5.0ns
T_{PHL} (ET → CA)	= 2.4ns	4.2ns

1. Typical delays include a fanout of 2 and statistical metal interconnect.
2. Maximum is for commercial temperature range of 0 to 70°C, ± 5% voltage variation and includes a fanout of 2 and statistical metal interconnect.

FIGURE 5

PROPAGATION DELAYS

Q6000A Series circuit propagation delays result from a combination of factors, including:

- Macro-intrinsic propagation delay
- Input signal polarity
- Fanout loading
- Metal loading
- Junction temperature
- Supply voltage
- Process variation

The impact of all these factors for an individual macro is captured in the equation for computing maximum propagation delay:

$$Tmax = (To + K * FO) * MF$$

where Tmax is the maximum macro delay for either positive or negative edge transitions, To is the intrinsic macro delay, FO is fanout and metal load seen by the macro, K is a coefficient which translates the loading effect from capacitance to ns and MF is the multiplication factor reflecting the impact of temperature, process and voltage. Curves indicating the effects of temperature and voltage are provided in Figures 6 and 7. The process variation factor is approximately 1.5 . For the total delay, individual macro propagation times along the signal path must be summed.

CMOS PROPAGATION DELAYS AS A FUNCTION OF TEMPERATURE

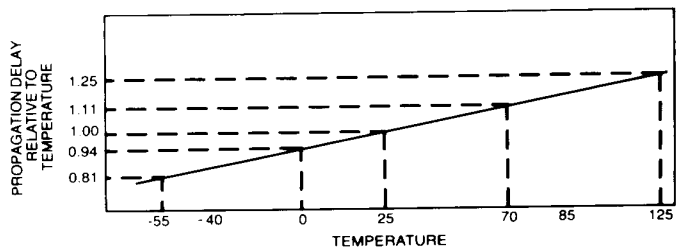


FIGURE 6

CMOS PROPAGATION DELAYS AS A FUNCTION OF SUPPLY VOLTAGE

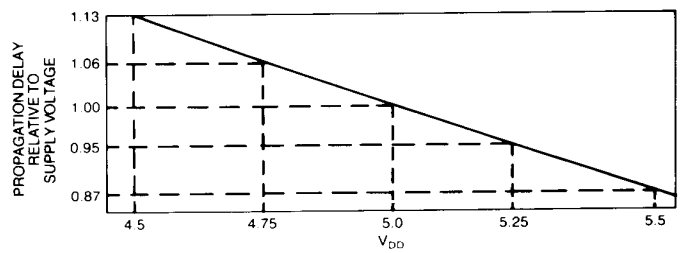


FIGURE 7

Prior to layout, the metal loading element of the multiplication factor is estimated using the front annotation software provided as part of AMCC's MacroMatrix™ design kit. The front annotation software provides statistical estimates of metal length based upon macro fanout. After layout, precise metal length data is available from the MacroMatrix back annotation software for use in final timing analysis.

I/O CAPABILITY

LOW POWER

I/O CAPABILITY

The Q6000A Series I/O cells are configurable to provide a full range of interface options. Input, bi-directional and output functions are provided to meet both TTL and CMOS logic levels. A Schmitt Trigger macro option is available to enhance input signal definition. Direct access to and from internal logic is also available via selected interface macros.

Fully TTL threshold-compatible input macros contain buffers which translate signals to internal voltage operating levels. With an ability to sink 6 mA and source 2 mA, the Q6000A output macros offer LSTTL compatibility. Output drive of up to 24 mA is achievable by combining adjacent output buffers. Bi-directional TTL interface can be achieved within a single I/O cell.

The Q6000A Series arrays also support standard CMOS logic threshold levels. CMOS input macros recognize signals below 1.0 volts as logic level LOW and above 3.5 volts as logic level HIGH. CMOS output and bi-directional I/Os use macros identical to TTL. CMOS and TTL interface macros may be combined as desired on the array.

The Q6000A Series I/O cells are configurable to provide a full range of interface options.

FLEXIBLE I/O STRUCTURE

INPUT	BI-DIRECTIONAL	OUTPUT
TTL Inverting TTL True TTL Schmitt Trigger CMOS Inverting CMOS True CMOS Scmitt Trigger Inverting Clock True Clock	TTL 3-state with Buffered Input and Output TTL 3-state with Direct Input and Buffered Output	True Buffer 3-state Buffer Open Drain Totem Pole

TABLE 3

POWER PIN REQUIREMENTS

AMCC offers considerable flexibility in power and ground specification. To maintain high noise margins, the quantity of power connections indicated in Table 2 on page 1 are recommended. Each V_{DD} and V_{SS} occupies one I/O cell. For circuits with a high number of simultaneously switching outputs extra power and ground pads may be added to ensure noise immunity.

POWER DISSIPATION

AMCC's Q6000A Series arrays have been designed for high performance while maintaining low power dissipation. The CMOS array's power consumption has both passive and active constituents. Passive power consists of two components — leakage current which flows from the supply to ground and DC current which passes through both internal and I/O devices when in the ON state. Quiescent power due to leakage is on the order of a few microwatts, and generally considered negligible, while DC current through ON devices is usually less than 10% of total power consumption.

Physically, a CMOS device acts as a capacitor (C) storing a charge at a voltage (V), thereby holding an energy $\frac{1}{2} CV^2$. When the device switches, the stored energy is released and power is dissipated. Power consumption, therefore, is a linear function of operating frequency (f) but is also directly dependent upon the number of gates switching during a particular clock cycle. Total device power is represented by the equation:

$$\text{Power} = C * V^2 * f * (\text{number of gates switching})$$

Active dissipation for Q6000A CMOS arrays is the sum of internal logic and I/O macro power. Internal power consumption is approximately 20 μW/gate-MHz for utilized gates which switch during the clock cycle. Dominated by output macros, I/O power dissipation is a strong function of external capacitive loading (C_L). Output macro power dissipation is about 25 μW/I/O-MHz-pf(C_L). Typical power dissipation for Q6000A Series arrays are plotted in Figure 8.

TYPICAL POWER DISSIPATION AT 30 MHz

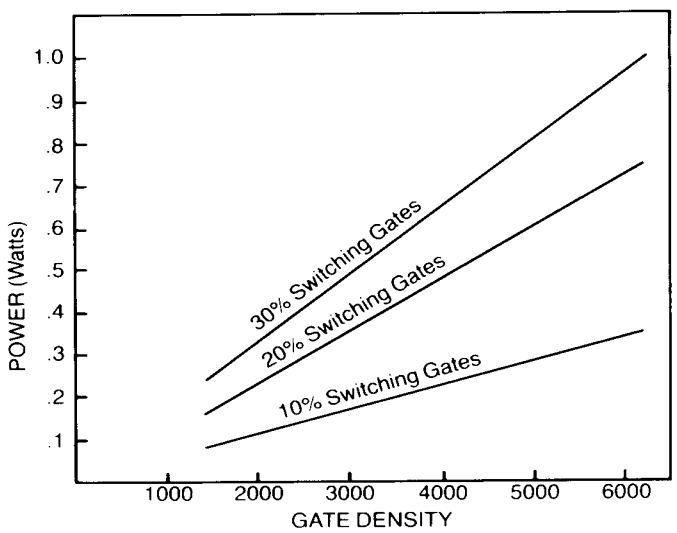


FIGURE 8

Q6000A DESIGN SUPPORT

PACKAGING

DESIGN INTERFACE

The AMCC circuit development interface has been structured to provide maximum flexibility with respect to customer involvement. AMCC provides fully supported macro libraries on several popular engineering workstations for on-site array development. The following workstation CAD tools are available as part of AMCC MacroMatrix design kit.

WORKSTATION SUPPORT

- Schematic capture
- Logic simulation
- Engineering rule checks (ERC)
- Pre- and post-route timing verification

In addition, AMCC has developed a comprehensive set of CAD tools to assure "correct by construction", quick turnaround logic array designs.

AMCC CAD TOOLS

- Auto placement and routing
- Interactive pre-place, pre-route
- Test fault coverage grading
- Design rule & interconnect verification
- Post-route timing verification

These CAD tools are used by AMCC to complete a circuit design from an engineering workstation-generated schematic and simulation output.

MSI MACROS

AMCC had developed over 50 MSI-level logic macros for design with the Q6000A arrays. A representative group of these macros is listed below.

- Quad D Latch with Reset
- 3:8 Decoder with Strobe
- Octal 2:1 Mux with Strobe
- Synchronous 4-Bit Counter with Reset, Load and Enable
- 8-Bit Shift Register with Parallel Out and Reset
- Quad Set Scan D Flip/Flops with Reset
- Octal D Flip/Flop with Reset
- Synchronous 4-Bit Up/Down Counter with Load and Enable
- Synchronous 4-Bit Dual Clock Up/Down Counter with Reset and Load
- 4-Bit Adder with Look Ahead Carry.

AMCC-PROVIDED SERVICES

In addition to providing the required CAD capability to allow customer design of arrays, AMCC provides a number of services to support customer design.

- Logic conversion and simulation
- Custom macro development
- High-level engineering support
- Comprehensive training courses and documentation

PACKAGING

The Q6000A Series devices are available in any of the following package configurations. Requirements for special packaging will be evaluated on an individual basis. Plastic packages are available for high production volumes — consult AMCC.

PACKAGING							
PACKAGE PIN COUNT	PACKAGE TYPE	Q1400D 74 PADS	Q1750D 82 PADS	Q2700D 100 PADS	Q3300D 110 PADS	Q4300D 126 PADS	Q6200D 154 PADS
24	DIP	•	•	•	•	•	
28	DIP	•	•	•	•	•	
40	DIP	•	•	•	•	•	
44	LCC	•	•	•	•		
48	DIP	•	•	•	•	•	
64	LDFP LDCC	• •	• •	• •	• •	•	
68	PGA LCC	• •	• •	• •	• •	• •	•
84	PGA LDFP LCC	• • •	• • •	• • •	• • •	• • •	• • •
100	PGA LDCC			• •	• •	• •	• •
120	PGA				•	•	•
132	LDCC				•	•	•
144	PGA					•	•
180	PGA						•

LDCC – Leaded Chip Carrier, LCC – Leadless Chip Carrier, DIP – Dual In-line Package, PGA – Pin Grid Array, LDFP – Leaded Flat Pack.

TABLE 4

OPERATING CONDITIONS

ABSOLUTE MAXIMUM RATING (V_{SS} = OV)

SYMBOL	PARAMETER	VALUE	UNIT
V_{DD}	Supply Voltage	- 0.3 to 7.0	V
V_{IN}	Input Voltage	- 0.3 to V_{DD} + 0.3	V
V_{OUT}	Output Voltage	- 0.3 to V_{DD} + 0.3	V
T_{STG}	Storage Temperature	- 65 to + 150	°C

TABLE 5

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	VALUE	UNIT
V_{DD}	Supply Voltage	+ 5 ± 10%	V
T_{OPR}	Operating Temperature	- 55 to + 125	°C

TABLE 6

TTL DC CHARACTERISTICS[1]

SYMBOL	PARAMETER	CONDITION	MIN	TYP	MAX	UNIT
V_{IL}	Input Low Voltage	V_{DD} = 4.5 V			0.8	V
V_{IH}	Input High Voltage	V_{DD} = 5.5 V	2.0			V
V_T+	Schmitt Trigger[2] Positive Going Threshold	V_{DD} = 5.5 V			2.4	V
V_T-	Schmitt Trigger[2] Negative Going Threshold	V_{DD} = 4.5 V	0.6			V
I_{IH}	Input High Current	V_{DD} = 5.5 V, V_{IN} = V_{DD}		1	10	µA
I_{IL}	Input Low Current	V_{DD} = 5.5 V, V_{IN} = V_{SS}	-10	-1		µA
	Input Low Current (Inputs with Pull-up Resistors)		-100			µA
V_{OL}	Output Low Voltage	V_{DD} = 4.5V, I_{OL} = 8.0mA			0.4	V
V_{OH}	Output High Voltage	V_{DD} = 4.5 V, I_{OH} = -8.0mA	2.4			V
I_{DD}	Stand-By Current	V_{IN} = V_{DD} or V_{SS}			10	µA
I_{OZ}	Tri-State Leakage Current	V_{OH} = V_{SS} or V_{DD}	-10		10	µA
I_{OS}	Output Short[4] Circuit Current	V_{DD} = 5.5V, V_O = V_{DD}	32		115	mA
		V_{DD} = 5.5V, V_O = V_{SS}	-13		-40	mA
C_{IN}	Input Capacitance				5[3]	pf

Notes:
1. Specified at V_{DD} = +5V ±10% over military temperature range of - 55°C to + 125°C
2. Schmitt Trigger is non-inverting. For inverting Schmitt Trigger, V_T+ is negative going threshold, while V_T- is positive going threshold.
3. Not including package lead capacitance.
4. For one output shorted with a maximum duration of one second. Only one output can be shorted at a time.

TABLE 7

CMOS DC CHARACTERISTICS[1]

SYMBOL	PARAMETER	CONDITION	MIN	TYP	MAX	UNIT
V_{IL}	Input Low Voltage	V_{DD} = 4.5V			1	V
V_{IH}	Input High Voltage	V_{DD} = 5.5V	3.5			V
V_T+	Schmitt Trigger[2] Positive Going Threshold	V_{DD} = 5.5V			4	V
V_T- V	Schmitt Trigger[2] Negative Going Threshold	V_{DD} = 4.5V	0.8			
I_{IH}	Input High Current	V_{DD} = 5.5V, V_{IN} = V_{DD}		1	10	µA
I_{IL}	Input Low Current	V_{DD} = 5.5V, V_{IN} = V_{SS}	-10	-1		µA
	Input Low Current (Inputs with Pull-up Resistors)		-100			µA
V_{OL}	Output Low Voltage	V_{DD} = 4.5V, I_{OL} = 3.0mA			0.2	V
V_{OH}	Output High Voltage	V_{DD} = 4.5V, I_{OH} = -3.0mA	4.0			V
I_{DD}	Stand-By Current	V_{IN} = V_{SS} or V_{DD}			10	µA
I_{OZ}	Tri-State Leakage Current	V_{OH} = V_{SS} or V_{DD}	-10		10	µA
I_{OS}	Output Short[4] Circuit Current	V_{DD} = 5.5V, V_O = V_{DD}	32		115	mA
		V_{DD} = 5.5V, V_O = V_{SS}	-13		-40	mA
C_{IN}	Input Capacitance				5[3]	pf

Notes:
1. Specified at V_{DD} = +5V ±10% over military temperature range of - 55°C to + 125°C
2. Schmitt Trigger is non-inverting. For inverting Schmitt Trigger, V_T+ is negative going threshold, while V_T- is positive going threshold.
3. Not including package lead capacitance.
4. For one output shorted with a maximum duration of one second. Only one output can be shorted at a time.

TABLE 8

OPERATING CONDITIONS

AC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETERS		CONDITION	COMMERCIAL 0°C TO 70°C			MILITARY -55°C TO 125°C			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	
t_{IPD}	Input Buffer Propagation Delay	Low to High	Fan Out = 2		2.3			2.3		ns
		High to Low			2.5			2.5		ns
t_{OPD}[1]	Output Buffer Propagation Delay	Low to High	C_L = 15pf		4.1			4.1		ns
		High to Low			5.2			5.2		ns
		Low to High	C_L = 50pf		6.8			6.8		ns
		High to Low			6.4			6.4		ns
t_{FPD}	Internal Equivalent Gate Delay	Low to High	2-Input NAND Fanout = 2, 2mm Metal		1.7			1.7		ns
		High to Low			1.3			1.3		ns
F_{MAXT}	Max. Internal Flip/Flop Toggle Frequency				85			85		MHz
F_{IN}[2]	Max. Input Frequency at Package Pin				60			60		MHz
t_{PZH}	Enable Time to High Level (Bidirectional Output Buffer, Fig. 9)		C_L = 15 pf		5.1			5.1		ns
			C_L = 50 pf		7.6			7.6		ns
t_{PZL}	Enable Time to Low Level (Bidirectional Output Buffer, Fig. 9)		C_L = 15 pf		6.4			6.4		ns
			C_L = 50 pf		7.5			7.5		ns
t_{PHZ}	Disable Time from High Level (Bidirectional Output Buffer, Fig. 9)		C_L = 15 pf		6.4			6.4		ns
			C_L = 50 pf		7.5			7.5		ns
t_{PLZ}	Disable Time from Low Level (Bidirectional Output Buffer, Fig. 9)		C_L = 15 pf		5.1			5.1		ns
			C_L = 50 pf		7.6			7.6		ns

TABLE 9

3-STATE ENABLE/DISABLE TIMING

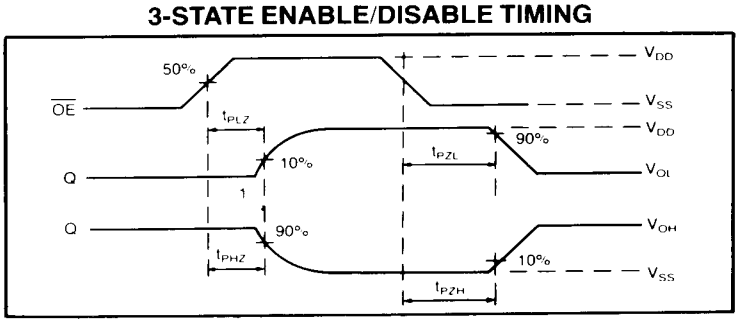


FIGURE 9

LOAD CIRCUIT FOR THREE-STATE OUTPUTS

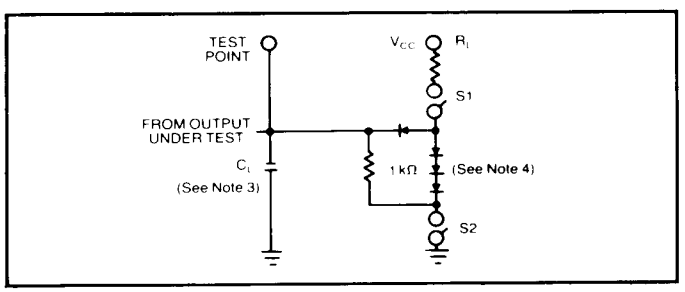


FIGURE 10

TEST CIRCUIT SWITCH TABLE

TEST FUNCTIONS	S1	S2
tp_{ZH}	Open	Closed
tp_{ZL}	Closed	Open
tp_{HZ}	Closed	Closed
tp_{LZ}	Closed	Closed

TABLE 10

Notes:
1. Standard TTL load circuit used, see Figure 10 (S1 & S2 closed)
2. Package selection will determine the maximum input frequency. Consult AMCC
3. CL includes probe and jig capacitance
4. All diodes are 1N916 or 1N3064

NOTES

REPRESENTED BY:

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