PRELIMINARY
T-52-33-05

82261
CMOS MULTI-FUNCTION LSI PERIPHERAL

- **CMOS Multi-function Peripheral Combining Four Components into Single Chip:**
  - **82C84A**
  - **82C59A**
  - **82C53**
  - **82C55A**
- **Same Functions and Complete Compatibility with Discrete NMOS Components***
- **Offers Optimal Board-Space Savings**
- **80C86/C88 and 8086/88 Compatible**
- **8 MHz Operation**
- **100-Pin Gull-Wing Flat-package**
- **Low-Power CMOS Technology**
- **TTL Compatible Inputs/Outputs**

The Intel 82261 is a high-performance CMOS multi-function peripheral designed to service the requirements of the 80C86/C88 and 8086/88 processors. The chip integrates four peripherals—82C84A, 82C59A, 82C53 and 82C55A, and is functionally identical to the discrete components. Its advanced, space-saving 100-pin gull-wing flat-package requires less than ⅓ board space of the separate components.

The clock oscillator (82C84A) generates up to 8 MHz system clock for the processor. The programmable interrupt controller (82C59A) can handle up to 8 vectored interrupts. Eight additional external interrupt controllers may be cascaded to support a maximum of 64 interrupts. The programmable interval timer (82C53) provides 3 independent 16-bit counters, each capable of handling clock inputs up to 5 MHz. The programmable I/O (82C55A) provides three 8-bit ports.

*Except 8284A. Identical to 82C84A.

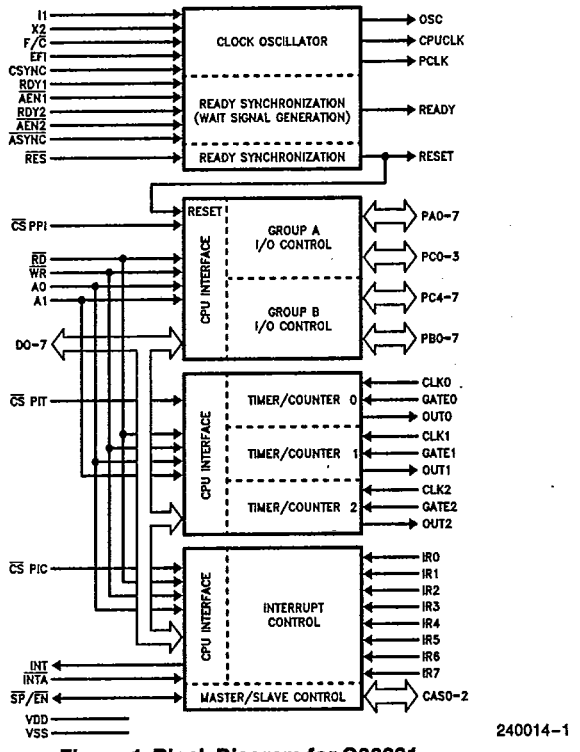

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Figure 1. Block Diagram for G82261

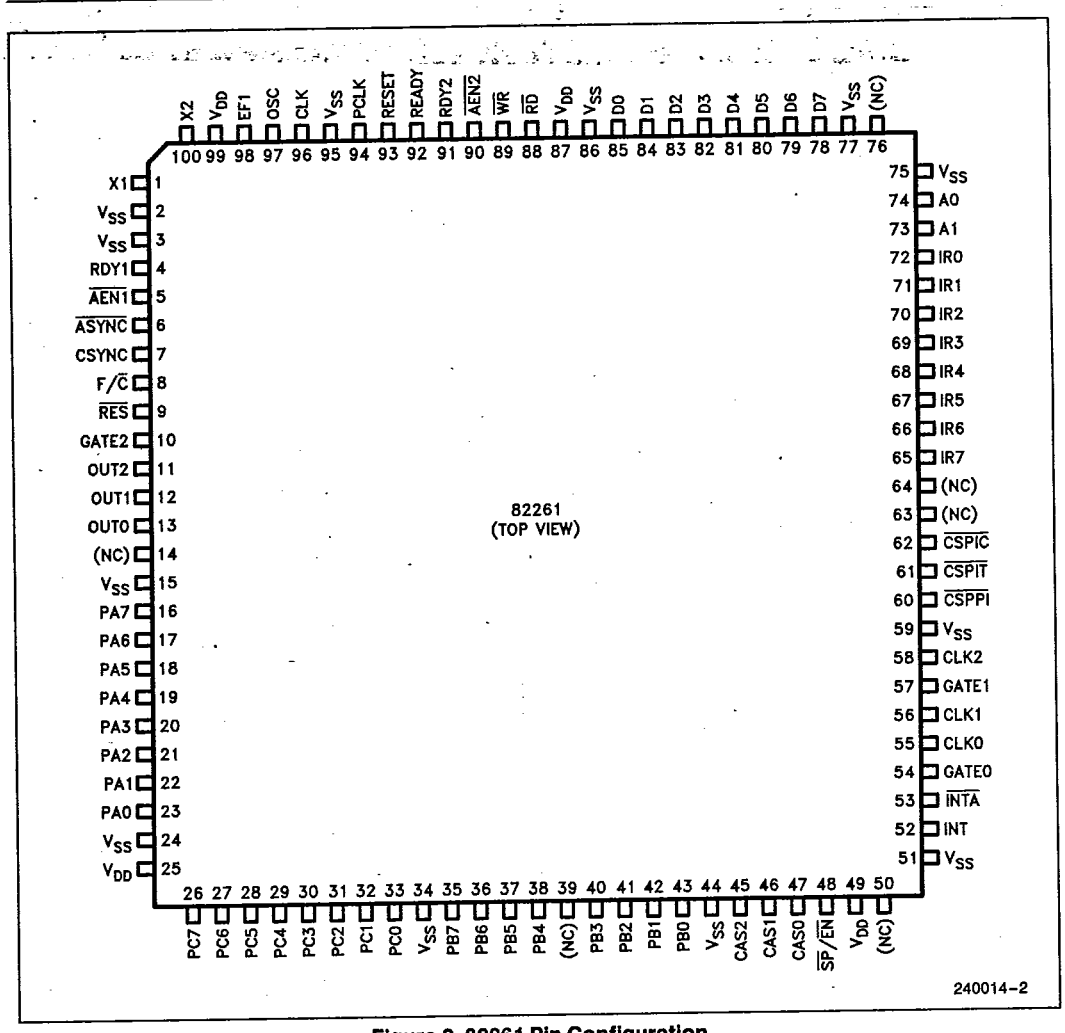


Figure 2. 82261 Pin Configuration

FUNCTIONAL DESCRIPTION

Figure 1 shows the functional block diagram of the 82261 LSI. A summary of features of individual functional units is listed below:

A. Programmable Timer/Counter (Equivalent to 82C53)

- 3 16-bit counters—count binary/BCD
- Programmable rate generator
- Programmable one-shot
- Square wave rate generator
- Software triggered strobe
- Hardware triggered strobe

B. Programmable Interrupt Controller (Equivalent to 89C59A)

- 8-level interrupt controller with programmable priorities
- Expandable to 64 levels in master/slave configuration
- Masking capability for individual Interrupt levels

C. Programmable I/O (Equivalent to 82C55A)

- 3 8-bit ports with programmable I/O operation
- Direct bit set/reset capabilities to ease peripheral control interface

D. Clock Generator (Equivalent to 82C84A)

- Generates system and peripheral clocks for 8086/88 systems
- Supports a choice of a crystal or an external frequency source
- Provides READY synchronization
- Capable of clock synchronization with other 82C84A/82261 in multiprocessor configurations
- Generates system reset for the 8086/88 from Schmitt trigger input

For a detailed operation of these functional units, please refer to their respective data sheets in the Intel 'Microprocessor and Peripheral Handbook' (order #230843). The pin diagram and package dimensions for the 82261 are shown in Figure 2 and Figure 3 respectively.

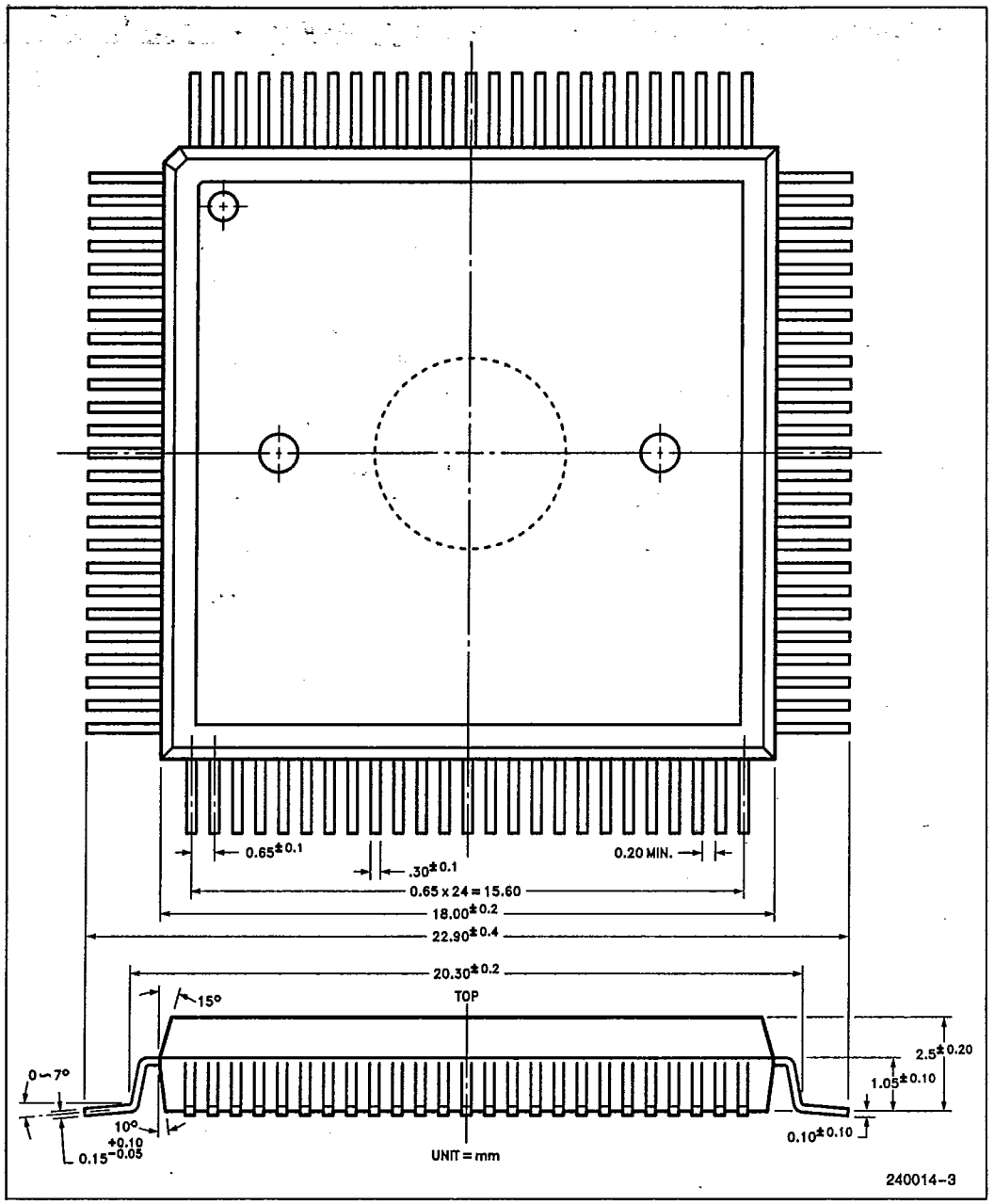


Figure 3. Package Dimensions

Table 1. 82261 Pin Definitions*

Symbol	Pin	Type	Function
D7–D0	78–85	I/O	Bidirectional, TRI-STATE data bus. The bus is floated when $\overline{RD}$, $\overline{WR}$, and $\overline{INTA}$ are all active high.
A1–A0	73–74	I	These input signals, in conjunction with $\overline{RD}$, $\overline{WR}$, and $\overline{CS}$, are used to select the internal registers of each functional block. Refer to Tables 2–5 for a complete decoding information.
$\overline{WR}$	89	I	An active low signal on this pin allows to write to the 82261. Data (D0–D7) is written to the 82261 at the rising edge of the $\overline{WR}$ pulse.
$\overline{RD}$	88	I	An active low signal on this pin allows to read from the 82261.
$\overline{CSPIC}$	62	I	Chip-Select for the Interrupt Controller block.
$\overline{CSPIT}$	61	I	Chip-Select for the Timer/Counter block.
$\overline{CSPPI}$	60	I	Chip-Select for the I/O Control Block.
RESET	93	O	This is an active high signal used to reset the CPU. Internally, it is also used to reset the I/O port (82C55A). Its timing characteristics are determined by $\overline{RES}$. All three ports, PA, PB, and PC, are set to the input mode upon reset.
$\overline{RES}$	9	I	An active low on this pin generates the RESET signal. This is a schmitt trigger input to be connected to an R-C circuit to establish the power-up reset of proper duration.
X1, X2	1, 100	I	Crystal connection terminals. Crystal frequency should be three times the desired CPU clock rate. When F/$\overline{C}$ is strapped high, X1 should be tied to V_{CC} or V_{SS}, and X2 should be left open.
F/$\overline{C}$	8	I	F/$\overline{C}$ is a strapping option. When strapped low, CPU clock (CLK) is generated from the crystal input (X1, X2). When strapped high, CLK is generated from the EFI input.
EFI	98	I	This input is used to generate the CPU clock (CLK) when the F/$\overline{C}$ input is strapped high. The input signal is a square wave with 3 times the desired CPU clock. EFI must be tied high or low when F/$\overline{C}$ is strapped low.
CLK	96	O	System clock used by the CPU and other devices which connect to the processor's local bus. It has 1/3 of the crystal or the EFI frequency, and 1/3 duty cycle.
PCLK	94	O	Peripheral clock. It has 50% duty cycle and 1/2 of the CLK frequency.
OSC	97	O	TTL level output of the internal oscillator circuitry. Its frequency is that of the crystal. The output is not affected when CSYNC is active high.
RDY1, RDY2	4 91	I	Data ready signals. When active high, it is an indication for the CPU from the currently selected device that data has been received, or is available. RDY1 is qualified by $\overline{AEN1}$ while RDY2 is qualified by $\overline{AEN2}$.
$\overline{AEN1}$ $\overline{AEN2}$	5 90	I	Address enable signals. When active low, $\overline{AEN1}$ qualifies RDY1, and $\overline{AEN2}$ qualifies RDY2. Two $\overline{AEN}$ signals are provided to access two multi-master system buses. In non multi-master configurations, the $\overline{AEN}$ inputs are tied low.
READY	92	O	This is an active high signal synchronized with the RDY input. READY is cleared after the guaranteed hold time for the CPU has been met.
$\overline{ASYNC}$	6	I	Ready synchronization mode select. When held low, READY becomes active after second synchronization. When high or open (an internal pull-up is provided), READY goes active with the first synchronizaton.

Table 1. 82261 Pin Definitions* (Continued)

Symbol	Pin	Type	Function
CSYNC	7	I	Clock synchronization signal. This is an active high signal to permit other 82C84A and/or 82261 in the system to be synchronized to provide clocks that are in phase. Internal counters are reset when CSYNC is active high. Counting resumes when CSYNC goes low. CSYNC must be externally synchronized with EFI. Must be tied to ground when using the internal oscillator.
CLK0 CLK1 CLK2	55 56 58	I	Clock input signal for corresponding timers/counters. When a count is set in a counter, count-down begins at the next falling edge of the related CLK.
OUT0 OUT1 OUT2	13 12 11	O	Timer/Counter outputs. The output waveforms are synchronized with the respective clocks.
GATE0 GATE1 GATE2	54 57 10	I	Gate Inputs. Control start/stop/reset operation in accordance with their respective timer/counter modes.
PA7–PA0	16–23	I/O	8-bit I/O latch/buffer (same as 82C55A port A).
PB7–PB0	35–43	I/O	8-bit I/O latch/buffer (same as 82C55A port B).
PC7–PC0	26–33	I/O	Same as 82C55A port C. It can be divided and used as two 4-bit ports under the mode control. Each 4-bit port contains a 4-bit latch and can be used for control signal outputs and status signal inputs in conjunction with ports A and B.
IR7–IR0	65–72	I	Interrupt request signals. These are asynchronous inputs. A device may request an interrupt by raising (low → high) one of the IR lines (edge triggered method), or simply by holding it high (level triggered method).
$\overline{INTA}$	53	I	Interrupt acknowledge from the CPU. A sequence of $\overline{INTA}$ pulses issued by the CPU allows the 82261 to place the interrupt vector on the data bus.
INT	52	O	CPU interrupt. This pin goes active high whenever a valid interrupt request (IR) is asserted.
$\overline{SP}/\overline{EN}$	48	I/O	Slave program/Buffer enable. Used in the buffer mode to control buffer transceivers. In non-buffered mode it is used to designate a master (SP = 1) or slave (SP = 0).
V_{SS}	2 3 15 24 34 44 51 59 75 77 86 95	I	Ground.
V_{CC}	25 49 87 99	I	Supply Voltage.

*Pins not listed here are all "No Connects" (NC).

Table 2. Chip Selects for Individual Functional Blocks

$\overline{WR}$	$\overline{RD}$	$\overline{CSPIT}$	$\overline{CSPIO}$	$\overline{CSPIC}$	$\overline{INTA}$	D0-7	Operation of Data Bus
1	0	0	1	1	1	OUT	Timer/Counter Part → Data
1	0	1	0	1	1	OUT	I/O Part → Data
1	0	1	1	0	1	OUT	Interrupt Control Part → Data
1	1	1	1	1	0	OUT	Interrupt Control Part → Data
0	1	0	1	1	1	IN	Data → Timer/Counter Part
0	1	1	0	1	1	IN	Data → I/O Part
0	1	1	1	0	1	IN	Data → Interrupt Control Part
1	0	X	X	X	1	Z	Data Bus High Impedance
X	X	1	1	1	1	Z	Data Bus High Impedance

NOTE:
X stands for don't care

Table 3. Chip Selects for I/O Control Block

A1	A0	$\overline{WR}$	$\overline{RD}$	$\overline{CSPIO}$	Operation	
0	0	1	0	0	PA → Data Bus*	Read
0	1	1	0	0	PB → Data Bus	
1	0	1	0	0	PC → Data Bus	
1	1	1	0	0	Inhibit	
0	0	0	1	0	Data Bus → PA	Write
0	1	0	1	0	Data Bus → PB	
1	0	0	1	0	Data Bus → PC	
1	1	0	1	0	Data Bus → Control	
X	X	X	X	1	Data Bus High Impedance	
X	X	1	1	0	Data Bus High Impedance	

Table 4. Chip Selects for Timer/Counter Block

A1	A0	$\overline{WR}$	$\overline{RD}$	$\overline{CSPIT}$	Operation of Bus
0	0	1	0	0	Read from Counter #0
0	1	1	0	0	Read from Counter #1
1	0	1	0	0	Read from Counter #2
1	1	1	0	0	No Operation (High Impedance)
0	0	0	1	0	Write to Counter #0
0	1	0	1	0	Write to Counter #1
1	0	0	1	0	Write to Counter #2
1	1	0	1	0	Write Mode Word
X	X	1	1	X	Disable (High Impedance)

Table 5. Chip Selects for Interrupt Control Block

D4	D3	A0	$\overline{WR}$	$\overline{RD}$	$\overline{CSPIC}$	$\overline{INTA}$	Operation of Bus
X	X	0	1	0	0	1	Read from IRR, ISR
X	X	1	1	0	0	1	Read from IMR
0	0	0	0	1	0	1	Write OCW2
0	1	0	0	1	0	1	Write OCW3
1	X	0	0	1	0	1	Write ICW1
X	X	1	0	1	0	1	Write ICW2, ICW3 and ICW4
X	X	X	1	1	0	1	High Impedance
X	X	X	X	X	1	1	High Impedance
X	X	X	1	1	1	0	Read the Interrupt Vector

ABSOLUTE MAXIMUM RATINGS*

Operating Temperature .....0°C to +70°C
Storage Temperature .....−65°C to +150°C
Supply Voltage V_{DD} .....−0.3V to +7.0V
Voltage on any Input.....−0.3V to V_{DD} +0.3V
Voltage on any Output .....−0.3V to V_{DD} +0.3V
Power Dissipation.....500 mW

Notice: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

NOTICE: Specifications contained within the following tables are subject to change.

D.C. CHARACTERISTICS T_A = 0°C to 70°C, V_{CC} = +5V ±10%.

Symbol	Parameter	Min	Max	Units	Test Conditions
V_{IL}	Input Low Voltage	+0.3V	0.8	V	
V_{IH}	Input High Voltage	2.0	V_{CC}	V	2.5V for $\overline{RES}$
V_{OL}	Output Low Voltage		0.45V	V	(Note 1)
V_{OH}	Output High Voltage	(Note 2)		V	(Note 2)
I_{LI}	Input Leakage Current	(Note 3)	+10	µA	V_{IN} = V_{CC} to 0V
I_{OFL}	Output Float Leakage Current	−10	+10	µA	V_{IN} = V_{CC} to 0V
I_{DAR}	Darlington Drive Current	−1		mA	For ports A, B, C of I/0 Control
I_{DD}	V_{CC} Supply Current		80	mA	(Note 4)
I_{CCSB}	V_{CC} Supply Current-Standby		10	µA	V_{CC} = 5.5V V_{IN} = V_{CC} or GND Port Conditions If I/P = Open/High O/P = Open Only With Data Bus = High/Low $\overline{CS}$ = High Reset = Low Pure Inputs = Low/High
V_{INH}−V_{IHR}	$\overline{RES}$ Input Hysteresis	0.25		V	

NOTES:
1. I_{OL} = 5 mA for CLK, PCLK, OSC, READY, RESET
   = 2.5 mA for Ports A, B, C of I/O Control Block
   = 2.2 mA for other outputs
2. V_{OH} = 4V, I_{OH} = −1 mA for CLK
   = 2.8V, I_{OH} = −1 mA for PCLK, OSL, READY, RESET
   = 3.5V, I_{OH} = −100 µA for INT
   = 2.4V, I_{OH} = −400 µA for other outputs
3. I_{LI} Min = −300 µA for IR0−IR7 and −200 µA for $\overline{ASYNC}$
4. Output: Open, $f_{CLK0\sim2}$ = 5 MHz, f_{OSC} = 24 MHz

CAPACITANCE T_A = 25°C, V_{CC} = GND = 0V

Symbol	Parameter	Min	Max	Units	Test Conditions
C_{IN}	Input Capacitance*		10	pF	Unmeasured pins returned to GND f_c = 1 MHz
$C_{I/O}$	I/O Capacitance*		20	pF	

*Except X1, X2, OSC, CLK, PCLK, READY, RESET.

A.C. CHARACTERISTICS T_A = 0°C to 70°C, V_{DD} = 5.0V ±10%

TIMINGS FOR READ/WRITE CYCLES (for timer/counter, I/O, and interrupt control blocks)

READ CYCLE

Symbol	Parameter	Min	Max	Units
t_{AR}	$\overline{CS}$*, Address Stable before $\overline{READ}$ for Timer/Counter for I/O and Interrupt Control	 30 0		 ns ns
t_{RA}	$\overline{CS}$*, Address Hold Time for $\overline{READ}$	0		ns
t_{RR}	$\overline{READ}$ Pulse Width	150		ns
t_{RD}	Data Delay from $\overline{READ}$ (Note 1)		120	ns
t_{DF}	$\overline{READ}$ to Data Floating (Note 2)	10	85	ns
t_{RV}	Command Recovery Time	200		ns

WRITE CYCLE

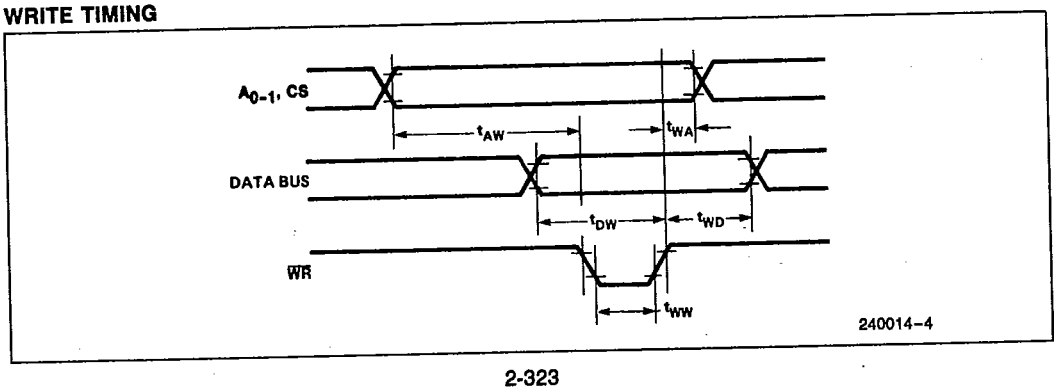
Symbol	Parameter	Min	Max	Units
t_{AW}	$\overline{CS}$, Address Stable before $\overline{WRITE}$	0		ns
t_{WA}	$\overline{CS}$, Address Hold Time for $\overline{WRITE}$	0		ns
t_{WW}	$\overline{WRITE}$ Pulse Width for Timer/Counter for I/O and Interrupt Control	 160 120		 ns ns
t_{DW}	Data Set Up Time for $\overline{WRITE}$	120		ns
t_{WD}	Data Hold Time for $\overline{WRITE}$	0		ns
t_{RV}	Command Recovery Time	200		ns

*$\overline{CS}$ means $\overline{CSPIT}$, $\overline{CSPPI}$, or $\overline{CSPIC}$.

NOTES:
1. C_L = 150 pF.
2. C_L = 20 pF, R_L = 2 KΩ.

WAVEFORMS FOR READ/WRITE CYCLES
(for Timer/Counter, I/O, and Interrupt Control Blocks)

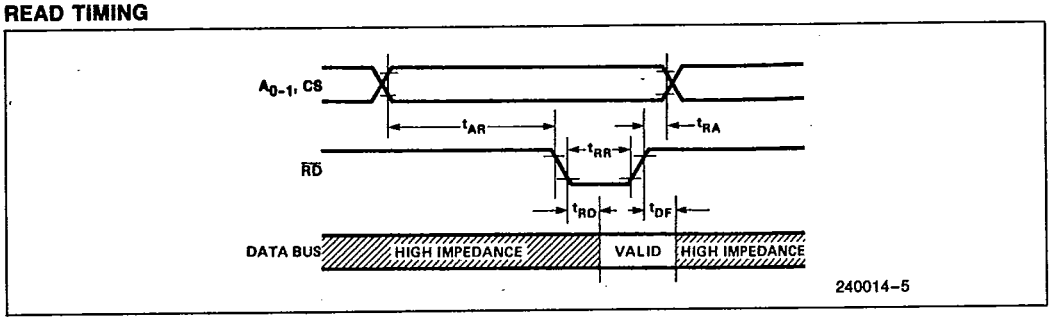
WRITE TIMING



A.C. CHARACTERISTICS (Continued)

WAVEFORMS FOR READ/WRITE CYCLES (for Timer/Counter, I/O, and Interrupt Control Blocks) (Continued)

READ TIMING

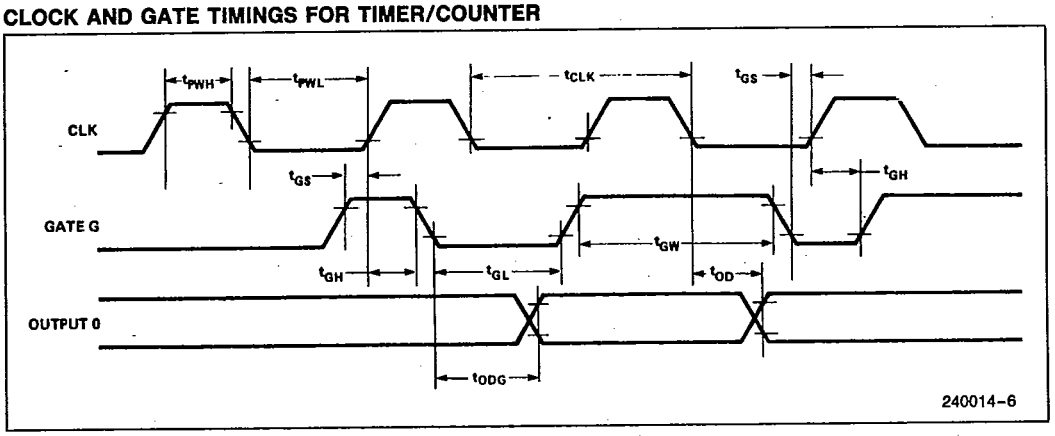


CLOCK AND GATE TIMINGS FOR TIMER/COUNTER

Symbol	Parameter	Min	Max	Units
t_{CLK}	Clock Period	200	DC	ns
t_{PWH}	High Pulse Width	80		ns
t_{PWL}	Low Pulse Width	60		ns
t_{GW}	Gate Width High	50		ns
t_{GL}	Gate Width Low	50		ns
t_{GS}	Gate Set Up Time to CLK ↑	50		ns
t_{GH}	Gate Hold Time after CLK ↑	50		ns
t_{OD}	Output Delay from CLK ↓ (Note 1)		150	ns
t_{ODG}	Output Delay from Gate ↓ (Note 1)		120	ns

NOTES:
1. C_L = 150 pF.

CLOCK AND GATE TIMINGS FOR TIMER/COUNTER



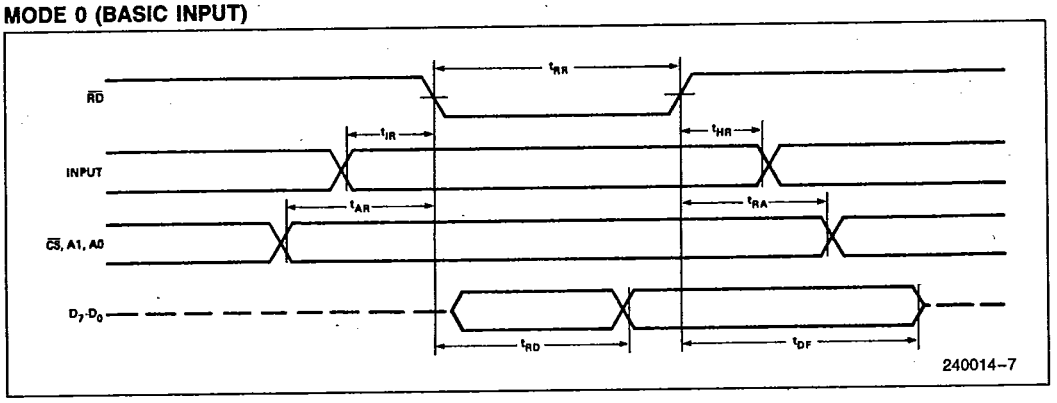
TIMING FOR I/O CONTROL BLOCK

Symbol	Parameter	Min	Max	Units	Test Conditions
t_{WB}	$\overline{WR}$ = 1 to Output		350	ns	C_L = 150 pF
t_{IR}	Peripheral Data Before $\overline{RD}$	0		ns	
t_{HR}	Peripheral Data After $\overline{RD}$	0		ns	
t_{AK}	$\overline{ACK}$ Pulse Width	300		ns	
t_{ST}	$\overline{STB}$ Pulse Width	350		ns	
t_{PS}	Per. Date Before $\overline{STB}$ High	0		ns	
t_{PH}	Per. Data After $\overline{STB}$ High	150		ns	
t_{AD}	$\overline{ACK}$ = 0 to Output		300	ns	C_L = 150 pF
t_{KD}	$\overline{ACK}$ = 1 to Output Float	20	250	ns	C_L = 150 pF
t_{WOB}	$\overline{WR}$ = 1 to $\overline{OBF}$ = 0		300	ns	C_L = 150 pF
t_{AOB}	$\overline{ACK}$ = 0 to $\overline{OBF}$ = 1		350	ns	C_L = 150 pF
t_{SIB}	$\overline{STB}$ = 0 to IBF = 1		300	ns	C_L = 150 pF
t_{RIB}	$\overline{RD}$ = 1 to IBF = 0		300	ns	C_L = 150 pF
t_{RIT}	$\overline{RD}$ = 0 to INTR = 1		400	ns	C_L = 150 pF
t_{SIT}	$\overline{STB}$ = 1 to INTR = 1		300	ns	C_L = 150 pF
t_{AIT}	$\overline{ACK}$ = 1 to INTR = 1		350	ns	C_L = 150 pF
t_{WIT}	$\overline{WR}$ = 0 to INTR = 0(1)		450	ns	C_L = 150 pF

NOTE:
1. INTR ↑ may occur as early as $\overline{WR}$ ↓.

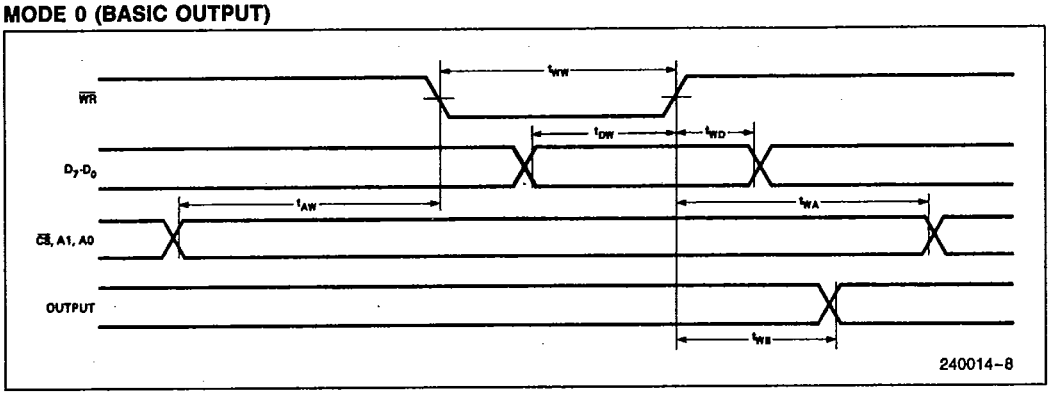
WAVEFORMS FOR I/O CONTROL BLOCK

MODE 0 (BASIC INPUT)

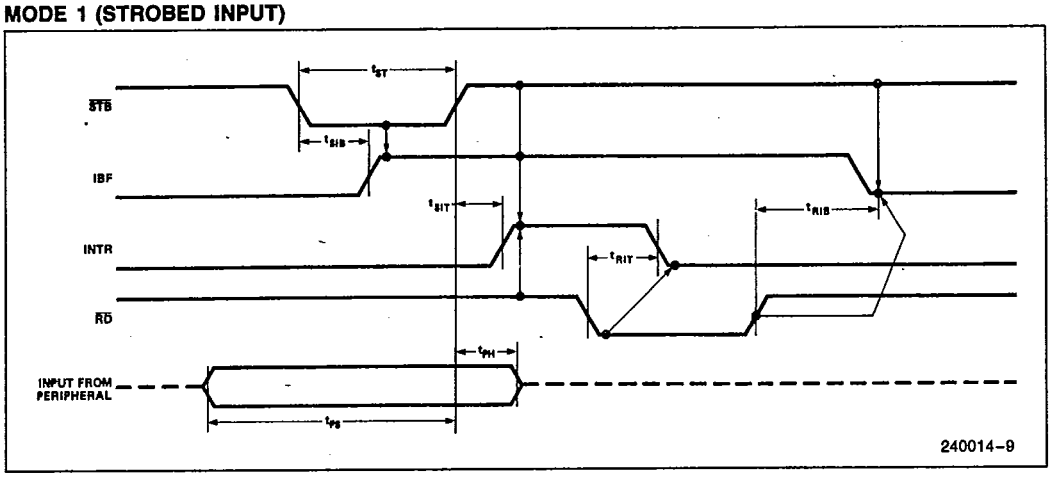


A.C. CHARACTERISTICS (Continued)

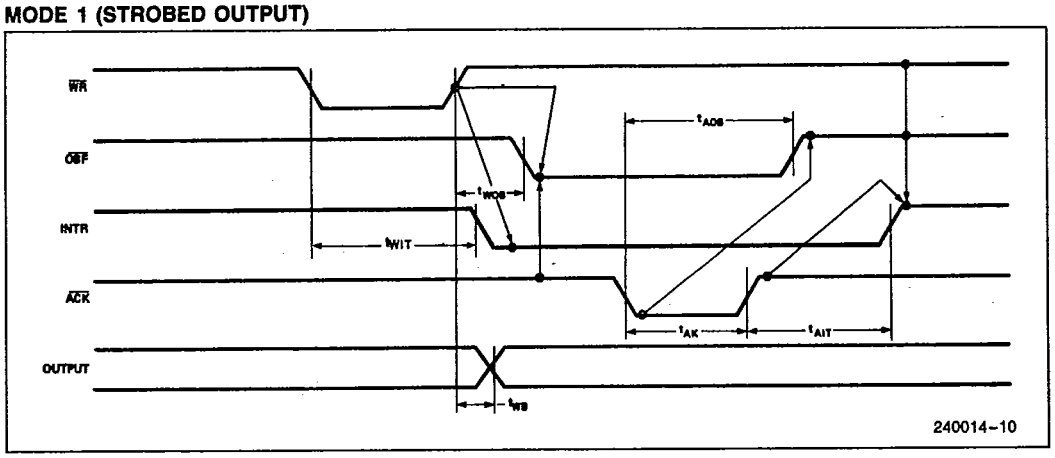
MODE 0 (BASIC OUTPUT)



MODE 1 (STROBED INPUT)

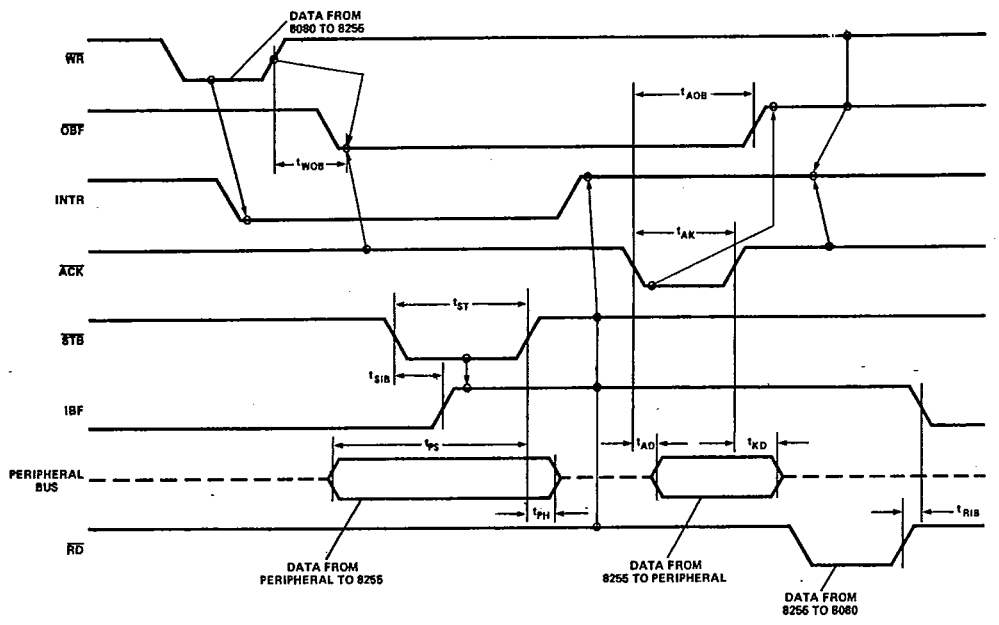


MODE 1 (STROBED OUTPUT)



WAVEFORMS FOR I/O CONTROL BLOCK (Continued)

MODE 2 (BIDIRECTIONAL)



NOTE:
Any sequence where $\overline{WR}$ occurs before $\overline{ACK}$ AND $\overline{STB}$ occurs before $\overline{RD}$ is permissible.
($INTR = IBF \bullet \overline{MASK} \bullet \overline{STB} \bullet \overline{RD} + \overline{OBF} \bullet \overline{MASK} \bullet \overline{ACK} \bullet \overline{WR}$)

TIMING FOR $\overline{\text{INTA}}$ CYCLES

TIMING REQUIREMENTS

Symbol	Parameter	Min	Max	Units	Test Conditions
TAHRL	A0/$\overline{\text{CS}}$ Setup to $\overline{\text{INTA}}$ ↓	0		ns	
TRHAX	A0/$\overline{\text{CS}}$ Hold after $\overline{\text{INTA}}$ ↑	0		ns	
TRLRH	$\overline{\text{RD}}$/$\overline{\text{INTA}}$ Pulse Width	120		ns	
TJLJH	Interrupt Request Width (Low)	100		ns	(Note 1)
TCVIAL	Cascade Setup to Second or Third $\overline{\text{INTA}}$ ↓ (Slave Only)	40		ns	
TRHRL	End of $\overline{\text{INTA}}$ to next $\overline{\text{INTA}}$ within an $\overline{\text{INTA}}$ sequence only	160		ns	
TCHCL	End of Command to next Command (Not same command type) End of $\overline{\text{INTA}}$ sequence to next $\overline{\text{INTA}}$ sequence (Note 2)	250		ns	

NOTES:
1. This is the low time required to clear the input latch in the edge triggered mode.
2. Worst case timing for TCHCL in an actual microprocessor system is typically much greater than 400 ns (i.e. 8085A = 1.6 μs, 8085-A2 = 1 μs, 80C86 = 1 μs, 80C86-2 = 625 ns).

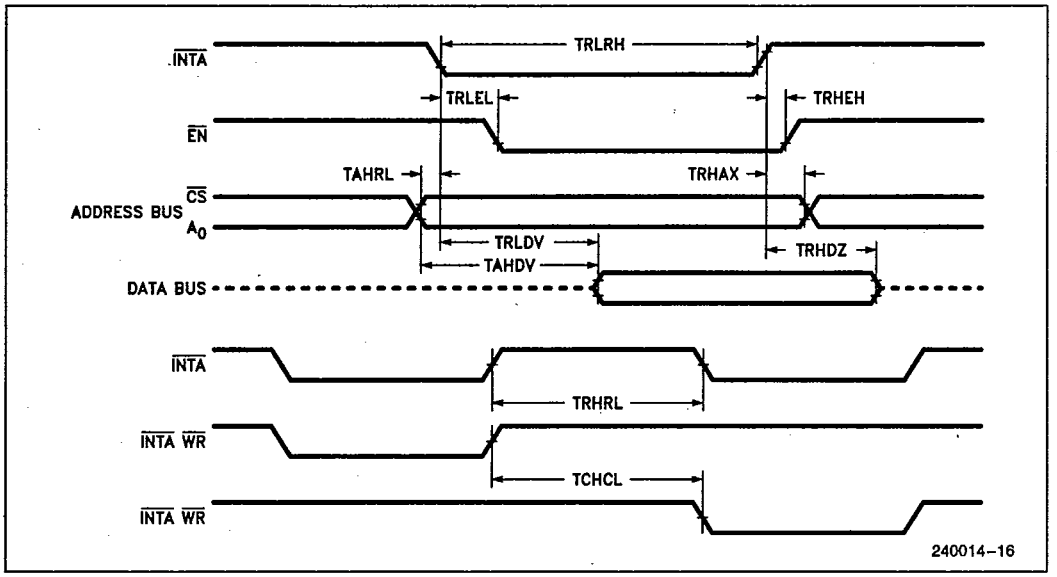
TIMING FOR $\overline{\text{INTA}}$ CYCLES (Continued)

TIMING RESPONSES

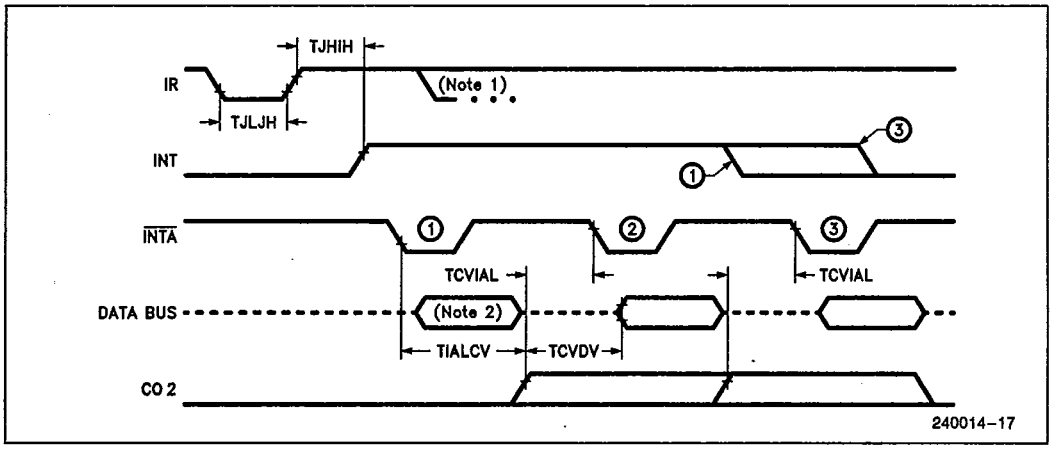
Symbol	Parameter	Min	Max	Units
TRLDV	Data Valid from $\overline{\text{INTA}}$ ↓		120	ns
TRHDZ	Data Float after $\overline{\text{INTA}}$ ↑	10	85	ns
TJHIH	Interrupt Output Delay		300	ns
TIALCV	Cascade Valid from First $\overline{\text{INTA}}$ ↓ (Master Only)		360	ns
TRLEL	Enable Active from $\overline{\text{RD}}$ ↓ or $\overline{\text{INTA}}$ ↓		100	ns
TRHEH	Enable Inactive from $\overline{\text{RD}}$ ↑ or $\overline{\text{INTA}}$ ↑		150	ns
TAHDV	Data Valid from Stable Address ($\overline{\text{CS}}$, A0, INT)		200	ns
TCVDV	Cascade Valid to Valid Data		200	ns

WAVEFORMS FOR $\overline{INTA}$ CYCLES

$\overline{INTA}$



$\overline{INTA}$ SEQUENCE



NOTES:
1. Interrupt request must remain HIGH at least until leading edge of first $\overline{INTA}$.
2. Cycle 1 in 80C86 and 80C88 systems, the Data Bus is not active.

TIMINGS FOR CLOCK GENERATOR BLOCK

TIMING REQUIREMENTS

Symbol	Parameter	Min	Max	Units	Test Conditions
t_{EHEL}	External Frequency HIGH Time	13		ns	90%–90% V_{IN}
t_{ELEH}	External Frequency LOW Time	13		ns	10%–10% V_{IN}
t_{ELEL}	EFI Period	41.6		ns	
	XTAL Frequency	8	24	MHz	
t_{R1VCL}	RDY1, RDY2 Active Setup to CLK	35		ns	$\overline{ASYNC}$ = HIGH
t_{R1VCH}	RDY1, RDY2 Active Setup to CLK	35		ns	$\overline{ASYNC}$ = LOW
t_{R1VCL}	RDY1, RDY2 Inactive Setup to CLK	35		ns	
t_{CLR1X}	RDY1, RDY2 Hold to CLK	0		ns	
t_{AYVCL}	$\overline{ASYNC}$ Setup to CLK	50		ns	
t_{CLAYX}	$\overline{ASYNC}$ Hold to CLK	0		ns	
t_{A1VR1V}	$\overline{AEN1}$, $\overline{AEN2}$ Setup to RDY1, RDY2	15		ns	
t_{CLA1X}	$\overline{AEN1}$, $\overline{AEN2}$ Hold to CLK	0		ns	
t_{YHEH}	CSYNC Setup to EFI	20		ns	
t_{EHYL}	CSYNC Hold to EFI	10		ns	
t_{YHYL}	CSYNC Width	$2 \bullet t_{ELEL}$		ns	
t_{I1HCL}	$\overline{RES}$ Setup to CLK (Note 3)	65		ns	(Note 2)
t_{CLI1H}	$\overline{RES}$ Hold to CLK	20		ns	(Note 2)
t_{ILIH}	Input Rise Time		20	ns	(Note 1)
t_{IHIL}	Input Fall Time		12	ns	(Note 1)

NOTES:
1. Transition between 0.8V and 2.0V.
2. Setup and hold necessary only to guarantee recognition at next clock.
3. For system reset, period of $\overline{RES}$ pulse must be at least 50 μs during or after power-on. Subsequent reset pulse should be 500 ns min.

TIMINGS FOR CLOCK GENERATOR BLOCK (Continued)

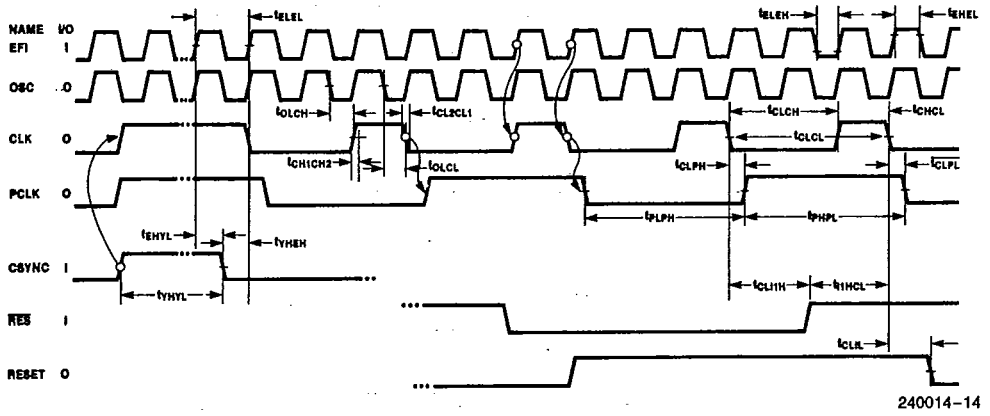
TIMING RESPONSES

Symbol	Parameter	Min	Max	Units	Test Conditions
t_{CLCL}	CLK Cycle Period	125		ns	
t_{CHCL}	CLK HIGH Time	$(1/3\ t_{CLCL}) + 2$		ns	
t_{CLCH}	CLK LOW Time	$(2/3\ t_{CLCL}) - 15$		ns	
t_{CH1CH2} t_{CL2CL1}	CLK Rise or Fall Time		10	ns	1.0V to 3.5V
t_{PHPL}	PCLK HIGH Time	$t_{CLCL} - 20$		ns	
t_{PLPH}	PCLK LOW Time	$t_{CLCL} - 20$		ns	
t_{RYLCL}	Ready Inactive to CLK (Note 2)	−8		ns	
t_{RYHCH}	Ready Active to CLK (Note 1)	$(2/3\ t_{CLCL}) - 15$		ns	
t_{CLIL}	CLK to Reset Delay		40	ns	
t_{CLPH}	CLK to PCLK HIGH DELAY		22	ns	
t_{CLPL}	CLK to PCLK LOW Delay		22	ns	
t_{OLCH}	OSC to CLK HIGH Delay	−5	22	ns	
t_{OLCL}	OSC to CLK LOW Delay	2	35	ns	
t_{OLOH}	Output Rise Time (expect CLK)		20	ns	Except CLK from 0.8V to 2.0V
t_{OHOL}	Output Fall Time (expect CLK)		12	ns	Expect CLK from 2.0V to 0.8V

NOTES:
1. Applies only to T3 and TW states.
2. Applies only to T2 states.

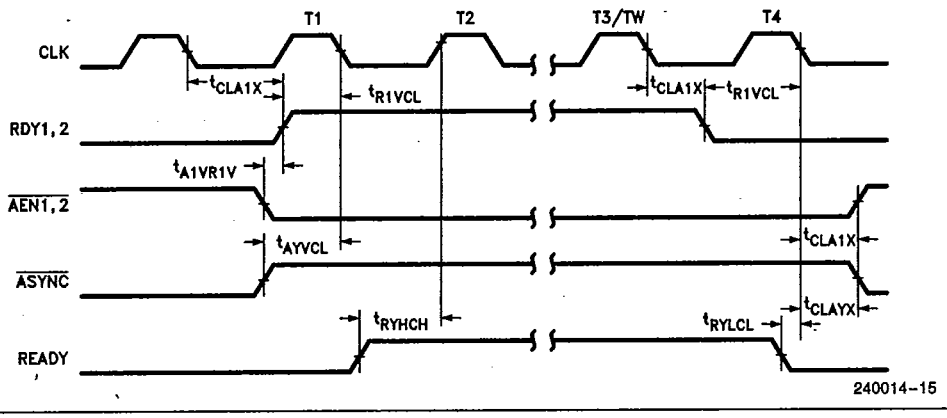
WAVEFORMS FOR CLOCK GENERATOR BLOCK

CLOCKS AND RESET SIGNALS



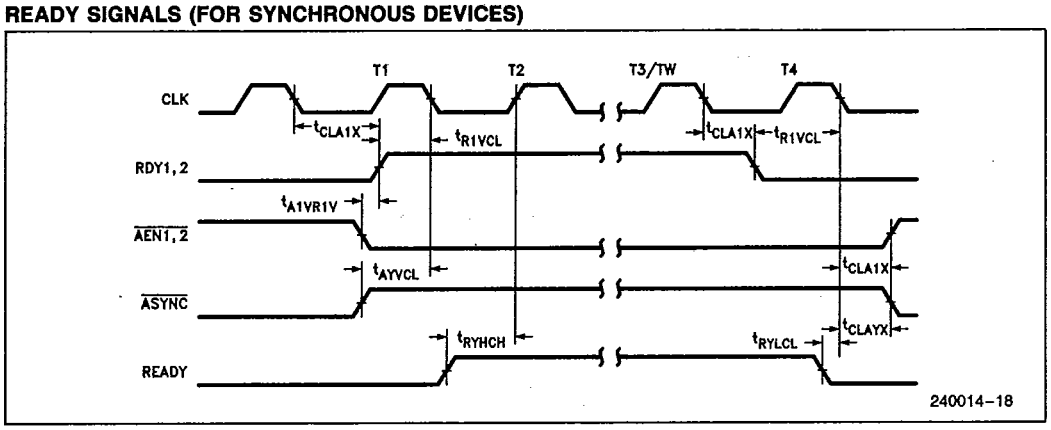
NOTE:
All timing measurements are made at 1.5V unless otherwise noted.

READY SIGNALS (FOR ASYNCHRONOUS DEVICES)

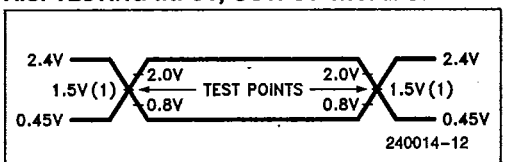


WAVEFORMS FOR CLOCK GENERATOR BLOCK (Continued)

READY SIGNALS (FOR SYNCHRONOUS DEVICES)

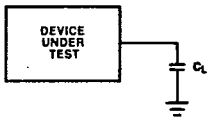


A.C. TESTING INPUT, OUTPUT WAVEFORM

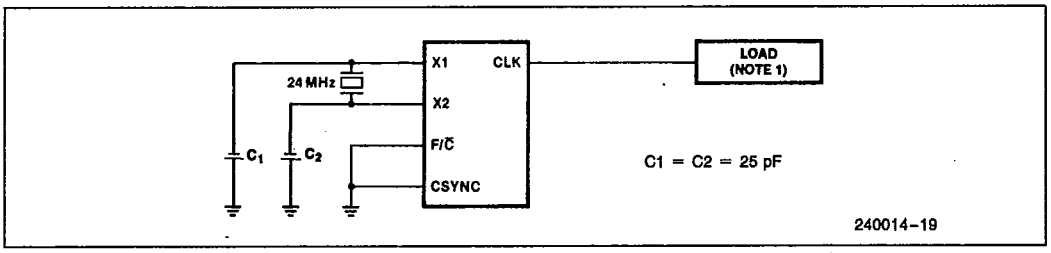


A.C. Testing: All Input signals must switch between 0.45V and 2.4V. T_{RISE} and T_{Fall} must be ≤ 15 ns. Only CLK measurements are made at 1.5V.

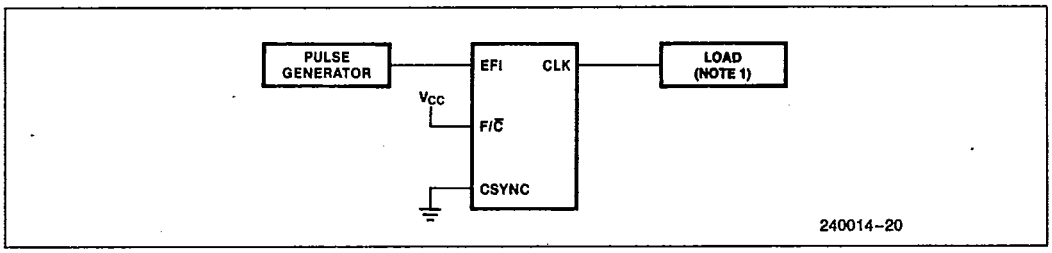
A.C. TESTING LOAD CIRCUIT



C_L = 100 pF for CLK
C_L = 30 pF for READY, PCLK, RESET, OSC
C_L = 150 pF for other outputs

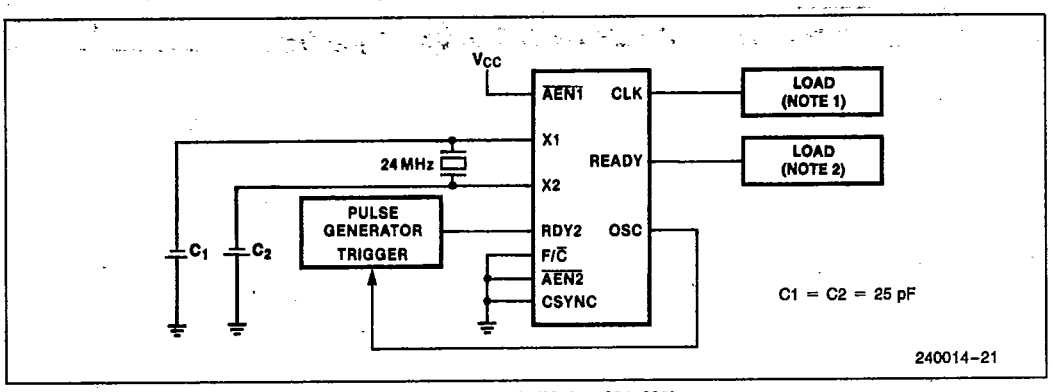


Clock High and Low Time (Using X1, X2)

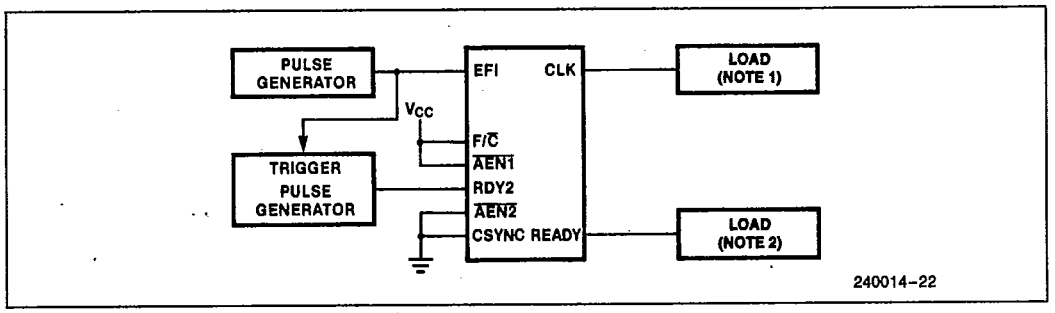


Clock High and Low Time (Using EFI)

NOTE:
1. C_L = 100 pF



Ready to Clock (Using X1, X2)



Ready To Clock (Using EFI)

NOTES:
1. C_L = 100 pF
2. C_L = 30 pF