

DEVICE SPECIFICATION

0889002 APPLIED MICRO CIRCUITS

90D 00360

DT-42-11-09

Q9000 SERIES CMOS LOGIC ARRAYS

FEATURES

TECHNOLOGY

Q9000 Series arrays feature 1.5-micron silicon-gate CMOS with two-level metalization, offering high performance and up to 90% chip utilization.

SIX ARRAY SIZES

2230 to 9250 equivalent gate densities are available in the Q9000 Series.

162 I/O CAPABILITY

The Q9000 Series arrays have from 82 I/Os on the Q2200J to 162 I/Os on the Q8000J.

EXTENSIVE MSI MACROS

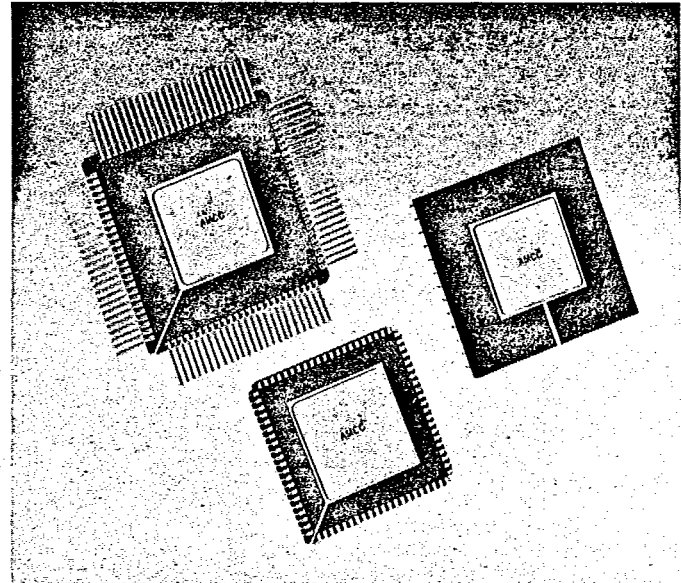
Q9000 Series arrays provide extensive MSI macros for ease in system design. There are over 180 hard-wired macros consisting of powerful MSI, I/O, logic and storage macros characterized for immediate use in system design.

HIGH SPEED WITH LOW POWER

Q9000 Series arrays feature a 1.2ns typical internal gate delay (2-input NAND gate) dissipating less than 18 μ W per gate per MHz.

STTL & CMOS COMPATIBLE

Q9000 Series logic arrays offer a wide selection of I/O macros which are compatible with CMOS and TTL systems using a single +5V power supply.



DESCRIPTION

The AMCC Q9000 Series consists of the Q2200J, Q3400J, Q4900J, Q6200J, Q8000J and Q9300J arrays. These arrays offer densities ranging from 2230 to 9250 equivalent 2-input NAND gates. The Series is optimized to provide a systems approach to high performance, low-power semicustom military and commercial applications.

The AMCC Q9000 Series arrays are fabricated using a state-of-the-art 1.5-micron, double-level-metal process to provide high density and speed with low power. When combined with an advanced, interactive CAD system they provide a quick and cost-effective solution to discrete IC replacement.

An extensive library of predefined single- and multiple-cell logic macros is provided for the Q9000 Series. In addition to a broad variety of basic logic functions, such as gates and flip/flops, the library offers one of the most extensive selections of hard-wired MSI macros. The extended MSI library provides commonly used logic functions such as 4-bit counters, full adders and shift registers which are optimized to provide improved speed and circuit density over logically equivalent SSI macros. The hard-wired approach to MSI design leads to accurate repeatable performance of these functions over the full temperature range, as well as, greater silicon efficiency over gate-level logic designs.

| PERFORMANCE SUMMARY | |
|---|--|
| PARAMETER | VALUE |
| Typical internal gate delay (2-input NAND, fanout = 2, including 2mm metal) | 1.2ns |
| Maximum flip/flop toggle frequency | 90MHz |
| Typical TTL input delay (includes a fanout of 2) | $T_{PLH} = 1.7ns$ $T_{PHL} = 3.2ns$ |
| Typical CMOS input delay (includes a fanout of 2) | $T_{PLH} = 1.5ns$ $T_{PHL} = 1.5ns$ |
| Typical TTL output delay (15 pf load) | $T_{PLH} = 4.1ns$ $T_{PHL} = 4.0ns$ |
| Typical CMOS output delay (10 pf load) | $T_{PLH} = 3.7ns$ $T_{PHL} = 3.2ns$ |
| TTL compatible output drive ($V_{OL} = 0.4VDC$) | 6mA |
| Power dissipation per basic gate | Less than 18 μ Watt/Gate-MHz |
| Average cell utilization | 87% |

TABLE 1

| RESOURCE SUMMARY | | | | | | |
|--|--------|--------|--------|--------|--------|---------|
| DESCRIPTION | Q2200J | Q3400J | Q4900J | Q6200J | Q8000J | Q9300J* |
| Basic 2-input NAND gates | 2232 | 3432 | 4900 | 6210 | 8000 | 16500 |
| Total pads available (including 8 fixed power/ground pads) | 90 | 112 | 136 | 158 | 178 | 178 |
| Recommended power/ground pads | 8 | 8 | 12 | 16 | 16 | 20 |
| Total I/O pads available | 82 | 104 | 124 | 142 | 162 | 158 |

Sea-of-Gates array. Maximum cell utilization = 50% (8250 usable gates). See "Q9300J," page 2.

TABLE 2

ARCHITECTURE

Q8000J-Die Size 344 x 403 Mils

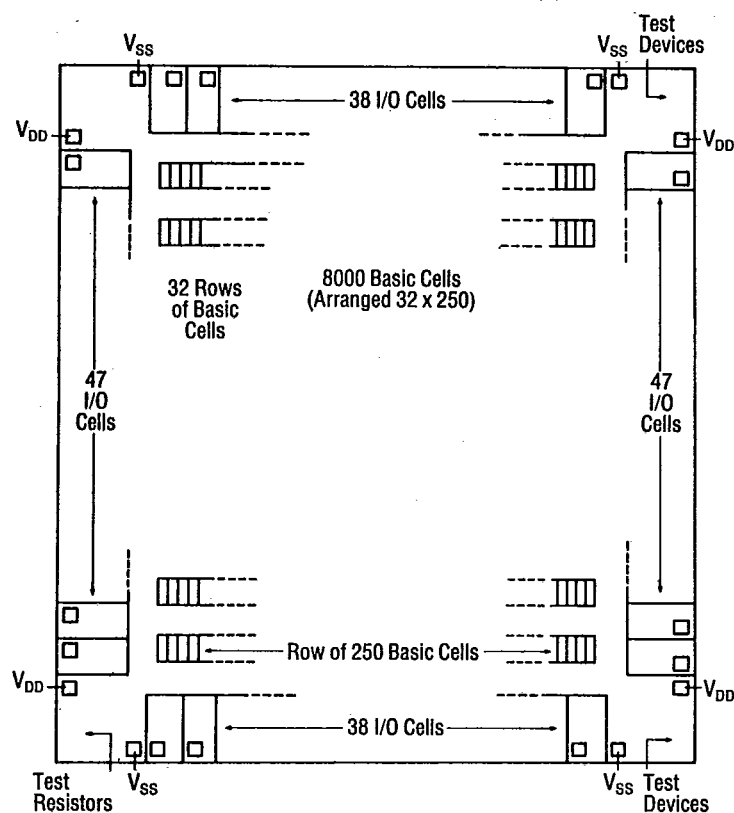


FIGURE 1

ARRAY ARCHITECTURE

The Q9000 Series logic array structure is comprised of two basic configurable internal and I/O cell types. The macro libraries provide the available logic and I/O functions with customization performed by adding a two-layer metal interconnect to the base array according to the customer specified design. Interconnections between macros use both first and second layers of metal and are performed automatically by AMCC CAD software. Liberal allocation of interconnect routing channels permits cell utilization of up to 90%.

The core of each logic array is comprised of a matrix of internal cells organized in a row-column configuration. I/O cells and multiple power and ground connections are distributed around the perimeter of the device. Representative Q9000 Series die layouts are illustrated in Figures 1 - 3.

INTERNAL CELL

The Q9000 Series arrays' internal cell resources are presented in Table 2 on page 1. All internal cells have identical structure, consisting of two P-channel and two N-channel transistors, and are positioned in uniform rows across the arrays. Single cells support simple SSI macros while multiple internal cells are utilized for more complex SSI and MSI functions.

Q9300J—"SEA-OF-GATES" ARRAY

The Q9300J array makes use of a channel-less, or "sea-of-gates" architecture to achieve maximum gate density in a minimum of chip area. The inner, or core, area of the array is completely packed with basic cells; there are no designated routing channels. When the array is personalized for an application, macros are placed using the core cells just as they would be on a channeled array. However, the interconnection of the

Q4900J-Die Size 285 x 287 Mils

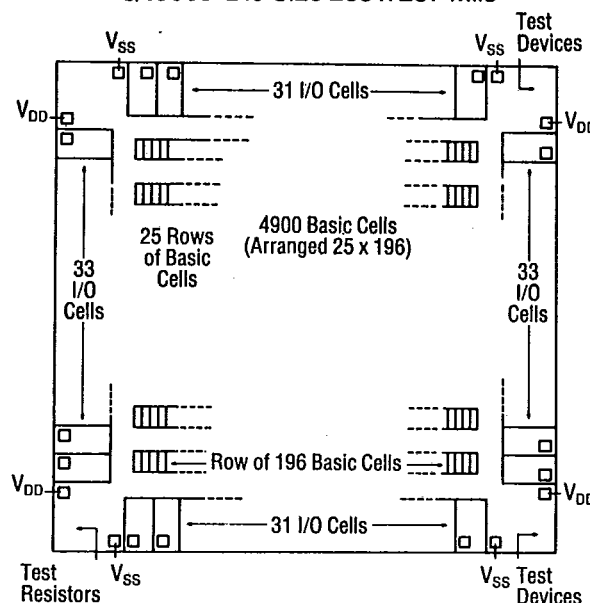


FIGURE 2

Q2200J-Die Size 204 x 205 Mils

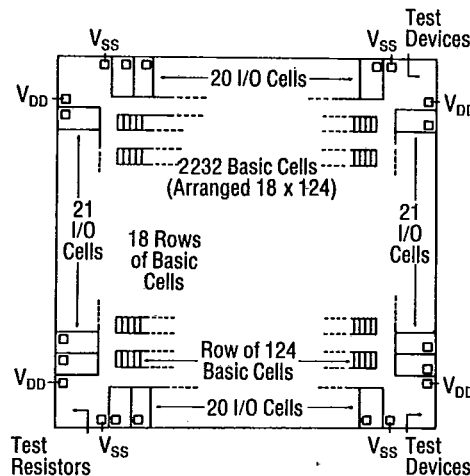


FIGURE 3

macros is accomplished by routing directly over areas of the cells not being occupied by logic. Effectively, routing channels are created during the layout process allowing greater densities than those of other arrays.

The Q9300J is designed to make use of the same basic structure as the Q8000J which has a total available gate count of 8000 (87% are usable). When the routing channels are replaced by additional core cells, the total available gate count jumps to 16,500. With a maximum 50% utilization of the available gates (blockages created by the interconnect prevent the use of macros in the routing paths), the high density Q9300J can support up to 8250 usable gates.

I/O CELL

I/O cells, positioned along the sides of the device, may be individually configured as TTL or CMOS inputs, outputs or bi-directional interfaces. Large dimension transistors are used in the I/O cells for external interface to both TTL and CMOS logic. Positioned in the corners of each array are four V_{DD} pads and four V_{SS} pads for +5V power and ground, respectively.

Q9000 SERIES

0889002 APPLIED MICRO CIRCUITS

MACRO CAPABILITIES

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PROPAGATION DELAYS

MACRO CAPABILITIES

AMCC offers an extensive selection of macros, ranging from fundamental Boolean logic to complex MSI functions. Created from ten or fewer internal cells, more than 50 basic logic macros are available, including simple and complex gates, inverters, buffers, latches and flip/flops. Representative standard macros with their associated performance are presented in Figure 4.

TYPICAL STANDARD MACROS

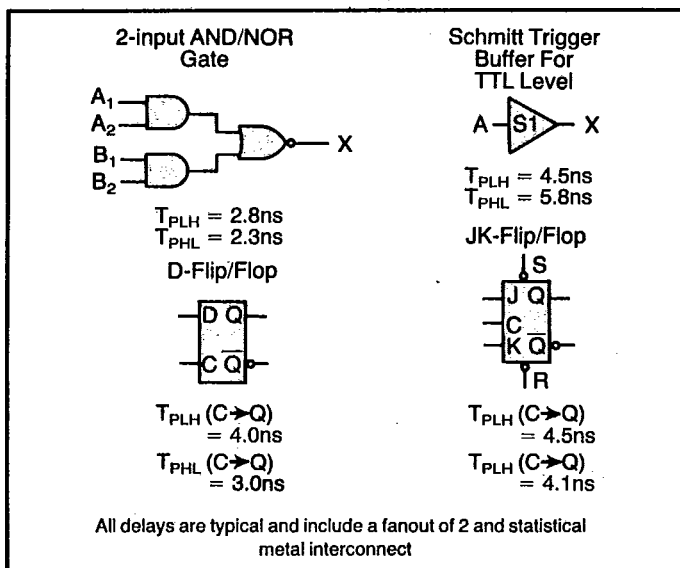


FIGURE 4

With more than 50 functions, AMCC's Q9000 Series offers the broadest library of hard-wired MSI macros. Including functions such as adders, counters, decoders, data and shift registers and multiplexers, MSI macros simplify and speed the design process. Compared to other software-based MSI macro functions, AMCC's hard-wired MSI macros offer higher speed and predictable repeatable performance. Typical MSI macro function and performance are provided in Figure 5.

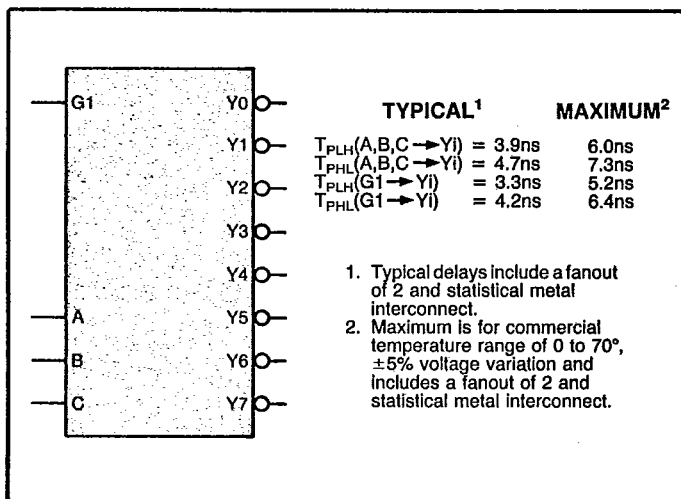
TYPICAL MSI MACRO
3-Line to 8-Line Decoder/Demultiplexer

FIGURE 5

PROPAGATION DELAYS

Q9000 Series circuit propagation delays result from a combination of factors, including:

- Macro-intrinsic propagation delay
- Input signal polarity
- Fanout loading
- Metal loading
- Junction temperature
- Supply voltage
- Process variation

The impact of all these factors for an individual macro is captured in the equation for computing maximum propagation delay:

$$T_{max} = (T_o + K * FO) * MF$$

where T_{max} is the maximum macro delay for either positive or negative edge transitions, T_o is the intrinsic macro delay, FO is fanout and metal load seen by the macro, K is a coefficient which translates the loading effect from capacitance to ns and MF is the multiplication factor reflecting the impact of temperature, process and voltage. Curves indicating the effects of temperature and voltage are provided in Figures 6 and 7. The process variation factor is approximately 1.4. For the total delay, individual macro propagation times along the signal path must be summed.

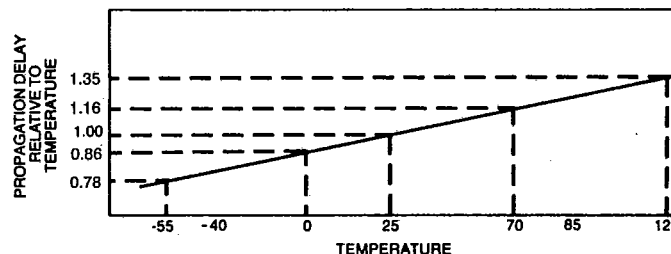
CMOS PROPAGATION DELAYS AS A
FUNCTION OF TEMPERATURE

FIGURE 6

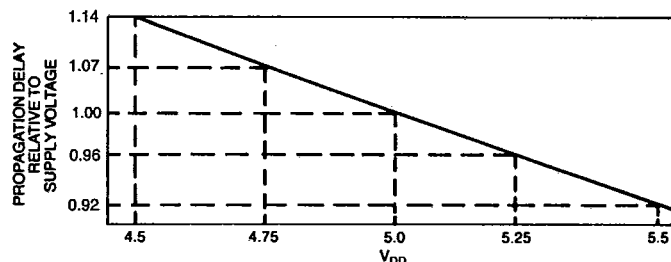
CMOS PROPAGATION DELAYS AS A
FUNCTION OF SUPPLY VOLTAGE

FIGURE 7

Prior to layout, the metal loading element of the multiplication factor is estimated using the front annotation software provided as part of AMCC's MacroMatrix™ design kit. The front annotation software provides statistical estimates of metal length based upon macro fanout. After layout, precise metal length data is available from the MacroMatrix back annotation software for use in final timing analysis.

I/O CAPABILITY**LOW POWER****I/O CAPABILITY**

The Q9000 Series I/O cells are configurable to provide a full range of interface options. Input, bi-directional and output functions are provided to meet both TTL and CMOS logic levels. A Schmitt Trigger macro option is available to enhance input signal definition. Direct access to and from internal logic is also available via selected interface macros.

Fully TTL threshold-compatible input macros contain buffers which translate signals to internal voltage operating levels. With an ability to sink 6 mA and source 6 mA, the Q9000 output macros offer LSTTL compatibility. Output drive of up to 24 mA is achievable by combining adjacent output buffers. Bi-directional TTL interface can be achieved within a single I/O cell.

The Q9000 Series arrays also support standard CMOS logic threshold levels. CMOS input macros recognize signals below 1.0 volts as logic level LOW and above 3.5 volts as logic level HIGH. CMOS output and bi-directional I/Os use macros identical to TTL. CMOS and TTL interface macros may be combined as desired on the array.

The Q9000 Series I/O cells are configurable to provide a full range of interface options.

FLEXIBLE I/O STRUCTURE

| INPUT | BI-DIRECTIONAL | OUTPUT |
|----------------------|---|----------------|
| TTL Inverting | TTL 3-state with Buffered Input and Output | True Buffer |
| TTL True | | 3-state Buffer |
| TTL Schmitt Trigger | TTL 3-state with Direct Input and Buffered Output | Open Drain |
| CMOS Inverting | | Totem Pole |
| CMOS True | | |
| CMOS Schmitt Trigger | | |
| Inverting Clock | | |
| True Clock | | |

TABLE 3

POWER PIN REQUIREMENTS

AMCC offers considerable flexibility in power and ground specification. To maintain high noise margins, the quantity of power connections indicated in Table 2 on page 1 are recommended. Each additional V_{DD} and V_{SS} occupies one I/O cell. For circuits with a high number of simultaneously switching outputs extra power and ground pads may be added to ensure noise immunity.

POWER DISSIPATION

AMCC's Q9000 Series arrays have been designed for high performance while maintaining low power dissipation. The CMOS array's power consumption has both passive and active constituents. Passive power consists of two components — leakage current which flows from the supply to ground and DC current which passes through both internal and I/O devices when in the ON state. Quiescent power due to leakage is on the order of a few microwatts, and generally considered negligible, while DC current through ON devices is usually less than 10% of total power consumption.

Physically, a CMOS device acts as a capacitor (C) storing a charge at a voltage (V), thereby holding an energy $\frac{1}{2} CV^2$. When the device switches, the stored energy is released and power is dissipated. Power consumption, therefore, is a linear function of operating frequency (f) but is also directly dependent upon the number of gates switching during a particular clock cycle. Total device power is represented by the equation:

$$\text{Power} = C \cdot V^2 \cdot f \cdot (\text{number of gates switching})$$

Active dissipation for Q9000 CMOS arrays is the sum of internal logic and I/O macro power. Internal power consumption is approximately 20 $\mu\text{W/gate-MHz}$ for utilized gates which switch during the clock cycle. Dominated by output macros, I/O power dissipation is a strong function of external capacitive loading (C_L). Output macro power dissipation is about 25 $\mu\text{W/I/O-MHz-pf}(C_L)$. Typical power dissipation for Q9000 Series arrays are plotted in Figure 8.

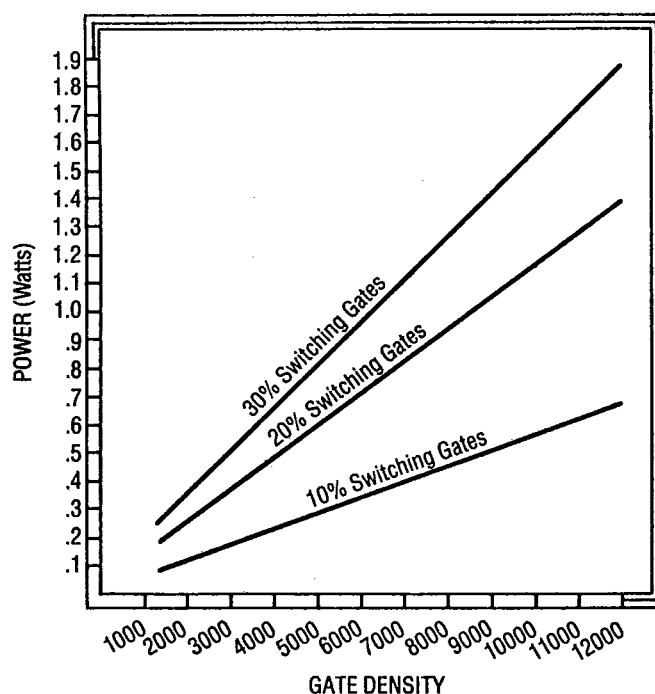
TYPICAL POWER DISSIPATION AT 30 MHz

FIGURE 8

Q9000 DESIGN SUPPORTT-42-11-09-
PACKAGING**DESIGN INTERFACE**

The AMCC circuit development interface has been structured to provide maximum flexibility with respect to customer involvement. AMCC provides fully supported macro libraries on several popular engineering workstations for on-site array development. The following workstation CAD tools are available as part of the AMCC MacroMatrix design kit.

WORKSTATION SUPPORT

- Schematic capture
- Logic simulation
- Engineering rule checks (ERC)
- Pre- and post-route timing verification

In addition, AMCC has developed a comprehensive set of CAD tools to assure "correct by construction", quick turnaround logic array designs.

AMCC CAD TOOLS

- Auto placement and routing
- Interactive pre-place, pre-route
- Test vector enhancement
- Test fault coverage grading
- Design rule & interconnect verification
- Post-route timing verification

These CAD tools are used by AMCC to complete a circuit design from an engineering workstation-generated schematic and simulation output.

AMCC-PROVIDED SERVICES

In addition to providing the required CAD capability to allow customer design of arrays, AMCC provides a number of services to support customer design.

- Logic conversion and simulation
- Custom macro development
- High-level engineering support
- Comprehensive training courses and documentation

PACKAGING

The Q9000 Series devices are available in any of the following package configurations. Requirements for special packaging will be evaluated on an individual basis. Plastic packages are available for high production volumes — consult AMCC.

| PACKAGING | | | | | | | |
|----------------------|--------------------|-----------------|--------------------|--------------------|--------------------|--------------------|-------------|
| PACKAGE PIN COUNT | PACKAGE TYPE | 2200 90 PADS | Q3400J 112 PADS | Q4900J 136 PADS | Q6200J 158 PADS | Q8000J 178 PADS | Q9300J |
| 24 | DIP | • | • | • | | | |
| 28 | DIP | • | • | • | | | |
| 40 | DIP | • | • | • | | | |
| 44 | LCC | • | • | • | | | |
| 48 | DIP | • | • | • | | | |
| 64 | LDFF LDCC | • • | • • | • • | • • | | |
| 68 | PGA LCC | • • | • • | • • | • • | • • | • • |
| 84 | PGA LDFF LCC | • • • | • • • | • • • | • • • | • • • | • • • |
| 100 | PGA LDCC | • • | • • | • • | • • | • • | • • |
| 120 | PGA | | • | • | • | • | • |
| 132 | LDCC | | | • | • | • | • |
| 144 | PGA | | | • | • | • | • |
| 172 | LDCC | | | | • | • | • |
| 180 | PGA | | | | • | • | • |
| 196 | LDCC PGA | | | | | | |

LDCC — Leaded Chip Carrier, LCC — Leadless Chip Carrier, DIP — Dual In-line Package, PGA — Pin Grid Array, LDFF — Leaded Flat Pack.

TABLE 4

APPLIED MICRO CIRCUITS 90 DE 0889002 0000365 7

OPERATING CONDITIONS

T-42-11-09

ABSOLUTE MAXIMUM RATING ($V_{SS} = 0V$)

| SYMBOL | PARAMETER | VALUE | UNIT |
|-----------|---------------------|-------------------------|------|
| V_{DD} | Supply Voltage | - 0.3 to 7.0 | V |
| V_{IN} | Input Voltage | - 0.3 to $V_{DD} + 0.3$ | V |
| V_{OUT} | Output Voltage | - 0.3 to $V_{DD} + 0.3$ | V |
| T_{STG} | Storage Temperature | - 65 to + 150 | °C |

TABLE 5

RECOMMENDED OPERATING CONDITIONS

| SYMBOL | PARAMETER | VALUE | UNIT |
|-----------|-----------------------|---------------|------|
| V_{DD} | Supply Voltage | + 5 \pm 10% | V |
| T_{OPR} | Operating Temperature | - 55 to + 125 | °C |

TABLE 6

TTL DC CHARACTERISTICS¹

| SYMBOL | PARAMETER | CONDITION | MIN | TYP | MAX | UNIT |
|----------|---|--------------------------------------|------------------|-----|----------------|---------|
| V_{IL} | Input Low Voltage | $V_{DD} = 4.5V$ | | | 0.8 | V |
| V_{IH} | Input High Voltage | $V_{DD} = 5.5V$ | 2.3 ⁵ | | | V |
| V_{T+} | Schmitt Trigger ² Positive Going Threshold | $V_{DD} = 5.5V$ | | | 2.6 | V |
| V_{T-} | Schmitt Trigger ² Negative Going Threshold | $V_{DD} = 4.5V$ | 0.4 | | | V |
| I_{IH} | Input High Current | $V_{DD} = 5.5V$ $V_{IN} = V_{DD}$ | | | 1 | μA |
| I_{IL} | Input Low Current | $V_{DD} = 5.5V$ $V_{IN} = V_{SS}$ | -1 | | | μA |
| | Input Low Current (Inputs with Pull-up Resistors) | | -100 | | | μA |
| V_{OL} | Output Low Voltage | $V_{DD} = 4.5V$ $I_{OL} = 6.0mA$ | | | 0.4 | V |
| V_{OH} | Output High Voltage | $V_{DD} = 4.5V$ $I_{OH} = -6.0mA$ | 2.4 | | | V |
| I_{DD} | Stand-By Current | $V_{IN} = V_{SS}$ or V_{DD} | | | 10 | μA |
| I_{OZ} | Tri-State Leakage Current | $V_{OH} = V_{SS}$ or V_{DD} | -1 | | 1 | μA |
| I_{OS} | Output Short ⁴ Circuit Current | $V_{DD} = 5.5V$ $V_O = V_{DD}$ | 32 | | 115 | mA |
| | | $V_{DD} = 5.5V$ $V_O = V_{SS}$ | -13 | | -40 | mA |
| C_{IN} | Input Capacitance | | | | 5 ³ | pf |

Notes:

- Specified at $V_{DD} = +5V \pm 10\%$ over military temperature range of - 55°C to + 125°C.
- Schmitt Trigger is non-inverting. For inverting Schmitt Trigger, V_{T+} is negative going threshold, while V_{T-} is positive going threshold.
- Not including package lead capacitance.
- For one output shorted with a maximum duration of one second. Only one output can be shorted at a time.
- For commercial specifications $V_{IH} = 2.0V$ min.

TABLE 7

CMOS DC CHARACTERISTICS¹

| SYMBOL | PARAMETER | CONDITION | MIN | TYP | MAX | UNIT |
|----------|---|--------------------------------------|------------------|-----|----------------|---------|
| V_{IL} | Input Low Voltage | $V_{DD} = 4.5V$ | | | 1 | V |
| V_{IH} | Input High Voltage | $V_{DD} = 5.5V$ | 3.7 ⁵ | | | V |
| V_{T+} | Schmitt Trigger ² Positive Going Threshold | $V_{DD} = 5.5V$ | | | 4.2 | V |
| V_{T-} | Schmitt Trigger ² Negative Going Threshold | $V_{DD} = 4.5V$ | 0.6 | | | V |
| I_{IH} | Input High Current | $V_{DD} = 5.5V$ $V_{IN} = V_{DD}$ | | | 1 | μA |
| I_{IL} | Input Low Current | $V_{DD} = 5.5V$ $V_{IN} = V_{SS}$ | -1 | | | μA |
| | Input Low Current (Inputs with Pull-up Resistors) | | -100 | | | μA |
| V_{OL} | Output Low Voltage | $V_{DD} = 4.5V$ $I_{OL} = 2.0mA$ | | | 0.2 | V |
| V_{OH} | Output High Voltage | $V_{DD} = 4.5V$ $I_{OH} = -2.0mA$ | 4.0 | | | V |
| I_{DD} | Stand-By Current | $V_{IN} = V_{SS}$ or V_{DD} | | | 10 | μA |
| I_{OZ} | Tri-State Leakage Current | $V_{OH} = V_{SS}$ or V_{DD} | -1 | | 1 | μA |
| I_{OS} | Output Short ⁴ Circuit Current | $V_{DD} = 5.5V$ $V_O = V_{DD}$ | 32 | | 115 | mA |
| | | $V_{DD} = 5.5V$ $V_O = V_{SS}$ | -13 | | -40 | mA |
| C_{IN} | Input Capacitance | | | | 5 ³ | pf |

Notes:

- Specified at $V_{DD} = +5V \pm 10\%$ over military temperature range of - 55°C to + 125°C.
- Schmitt Trigger is non-inverting. For inverting Schmitt Trigger, V_{T+} is negative going threshold, while V_{T-} is positive going threshold.
- Not including package lead capacitance.
- For one output shorted with a maximum duration of one second. Only one output can be shorted at a time.
- For commercial specifications $V_{IH} = 3.5V$ min.

TABLE 8

AC ELECTRICAL CHARACTERISTICS

| SYMBOL | PARAMETERS | | CONDITION | COMMERCIAL 0°C TO 70°C | | | MILITARY -55°C TO 125°C | | | UNIT |
|-------------|--|-------------|------------------------------------|------------------------|-----|-----|-------------------------|-----|-----|------|
| | | | | MIN | TYP | MAX | MIN | TYP | MAX | |
| t_{IPD} | Input Buffer Propagation Delay | Low to High | Fan Out = 2 | | 1.7 | | | 1.7 | | ns |
| | | High to Low | | | 3.2 | | | 3.2 | | ns |
| t_{OPD}^1 | Output Buffer Propagation Delay | Low to High | $C_L = 15\text{pf}$ | | 4.1 | | | 4.1 | | ns |
| | | High to Low | | | 4.0 | | | 4.0 | | ns |
| | | Low to High | $C_L = 50\text{pf}$ | | 7.1 | | | 7.1 | | ns |
| | | High to Low | | | 7.2 | | | 7.2 | | ns |
| t_{FPD} | Internal Equivalent Gate Delay | Low to High | 2-Input NAND Fanout = 2, 2mm Metal | | 1.2 | | | 1.2 | | ns |
| | | High to Low | | | 1.5 | | | 1.5 | | ns |
| F_{MAXT} | Max. Internal Flip/Flop Toggle Frequency | | | | 90 | | | 90 | | MHz |
| F_{IN}^2 | Max. Input Frequency at Package Pin | | | | 90 | | | 90 | | MHz |
| t_{PZH} | Enable Time to High Level (Bidirectional Output Buffer, Fig. 9) | | $C_L = 15\text{pf}$ | | 6.2 | | | 6.2 | | ns |
| | | | $C_L = 50\text{pf}$ | | 8.2 | | | 8.2 | | ns |
| t_{PZL} | Enable Time to Low Level (Bidirectional Output Buffer, Fig. 9) | | $C_L = 15\text{pf}$ | | 5.2 | | | 5.2 | | ns |
| | | | $C_L = 50\text{pf}$ | | 7.7 | | | 7.7 | | ns |
| t_{PHZ} | Disable Time from High Level (Bidirectional Output Buffer, Fig. 9) | | $C_L = 15\text{pf}$ | | 5.2 | | | 5.2 | | ns |
| | | | $C_L = 50\text{pf}$ | | 7.7 | | | 7.7 | | ns |
| t_{PLZ} | Disable Time from Low Level (Bidirectional Output Buffer, Fig. 9) | | $C_L = 15\text{pf}$ | | 6.2 | | | 6.2 | | ns |
| | | | $C_L = 50\text{pf}$ | | 8.2 | | | 8.2 | | ns |

TABLE 9

3-STATE ENABLE/DISABLE TIMING

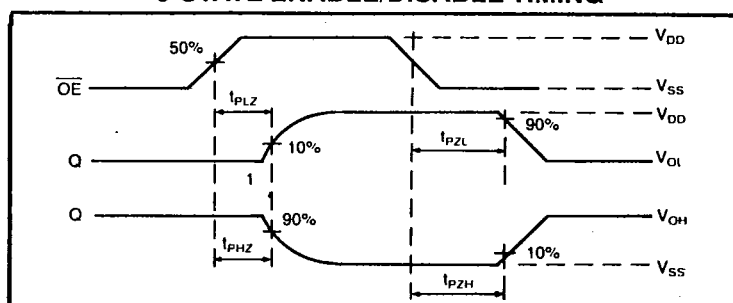


FIGURE 9

LOAD CIRCUIT FOR THREE-STATE OUTPUTS

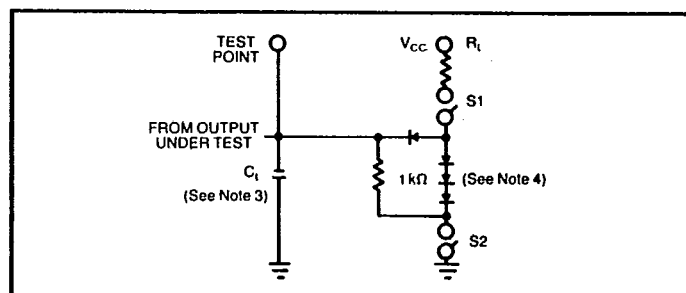


FIGURE 10

TEST CIRCUIT SWITCH TABLE

| TEST FUNCTIONS | S1 | S2 |
|------------------|--------|--------|
| tp _{ZH} | Open | Closed |
| tp _{ZL} | Closed | Open |
| tp _{HZ} | Closed | Closed |
| tp _{LZ} | Closed | Closed |

TABLE 10

Notes:

1. Standard TTL load circuit used, see Figure 10 (S1 & S2 closed)
2. Package selection will determine the maximum input frequency. Consult AMCC
3. CL includes probe and jig capacitance
4. All diodes are 1N916 or 1N3064