AN1081, AN1081S, AN6583

Single J-FET Input Operational Amplifiers

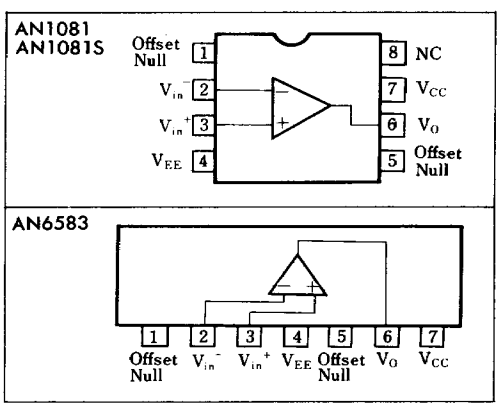
■ Outline

The AN1081, the AN1081S and the AN6583 are single operational amplifiers with input stages consisting of Pch J-FET adopting the ion implantation process, realizing high speed response, high input impedance and low input bias current. Therefore, they can be applied widely to general control equipment and medical equipment such as integrators, sample & hold circuits and high input impedance buffers.

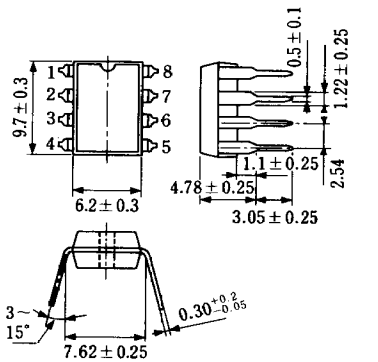
■ Features

- High slew rate : SR=11V/μs typ.
- Low input bias current : I_{Bias}=30pA typ.
- Low offset current : I_{IO}=5pA typ.
- High impedance : $10^{12}\Omega$
- High gain : Gv=106dB typ.
- Wide range of supply voltage : ±5V~±18V
- Built-in phase compensation circuit
- Offset null

■ Block Diagrams

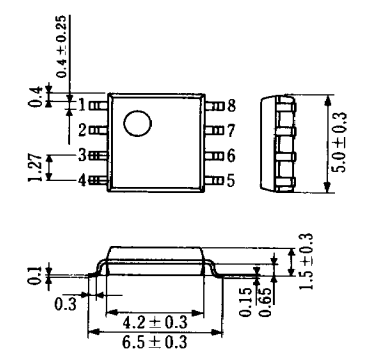


AN1081 Unit : mm



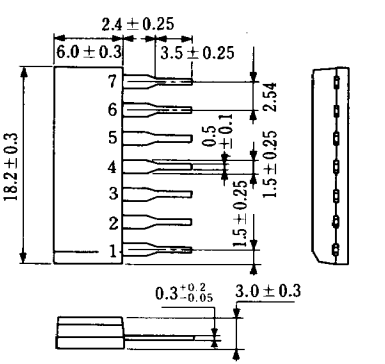
8-Lead DIL Plastic Package

AN1081S Unit : mm



8-Lead PANAFLAT Package(SO-8D)

AN6583 Unit : mm



7-Lead SIL Plastic Package

Panasonic

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■ Pin

〈AN1081, AN1081S〉

Pin No.	Pin Name
1	Offset Null
2	Invert Input
3	Non Invert Input
4	V_{EE}
5	Offset Null
6	Output
7	V_{CC}
8	NC

〈AN6583〉

Pin No.	Pin Name
1	Offset Null
2	Invert Input
3	Non Invert Input
4	V_{EE}
5	Offset Null
6	Output
7	V_{CC}

■ Absolute Maximum Ratings (Ta=25℃)

Item		Symbol	Rating	Unit
Voltage	Supply Voltage	V_{CC}	±18	V
	Differential Input Voltage	V_{ID}	±30	V
	Common-Mode Input Voltage	V_{ICM}	±15	V
Power Dissipation	AN1081, AN6583	P_D	500	mW
	AN1081S		360	
Operating Ambient Temperature		T_{opr}	−20～+75	℃
Storage Temperature	AN1081, AN6583	T_{stg}	−55～+150	℃
	AN1081S		−55～+125	

■ Electrical Characteristics (V_{CC}=15V, V_{EE}=−15V, Ta=25℃)

Item	Symbol	Test Circuit	Condition	min.	typ.	max.	Unit
Input Offset Voltage	$V_{I(offset)}$	1	$R_S \leqq 50\Omega$		2	10	mV
Input Offset Current	I_{IO}	1			5	200	pA
Input Bias Current	I_{Bias}	1			30	400	pA
Voltage Gain	G_V	1		88	106		dB
Maximum Output Voltage	$V_{O(max.)}$	2	$R_L \geqq 10k\Omega$	±12	±13.5		V
Maximum Output Voltage	$V_{O(max.)}$	2	$R_L \geqq 2k\Omega$	±10	±12		V
Common-Mode Input Voltage Range	V_{CM}	3		±10			V
Common-Mode Rejection Ratio	CMR	1		70	76		dB
Supply Voltage Rejection Ratio	SVR	1		70	76		dB
Power Consumption	P_C	4	$R_L=\infty$		60	95	mW
Slew Rate	SR	5	$R_L \geqq 2k\Omega$		11		V/μs
Unity-gain Band Width	$f_{(T)}$	6	$A_V=1$		3		MHz
Equivalent Input Noise Voltage	V_{ni}	7	$R_S=100\Omega$, B=10Hz～30kHz		4		μV_{rms}

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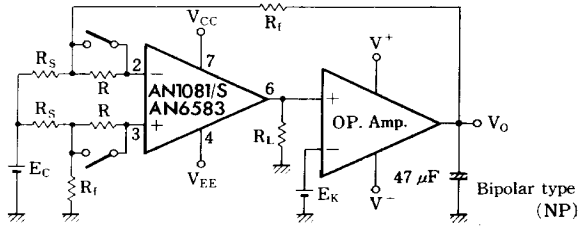
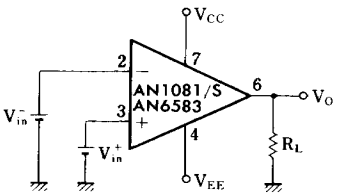
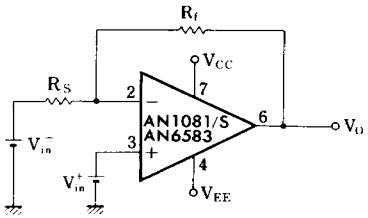
Test Circuit 1 ($V_{I(offset)}$, I_{IO}, I_{Bias}, G_V, CMR, SVR)



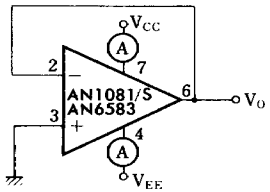
Test Circuit 2 ($V_{O(max.)}$)



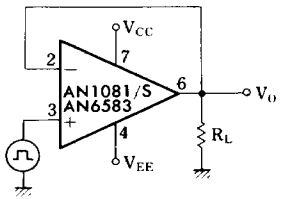
Test Circuit 3 (V_{CM})



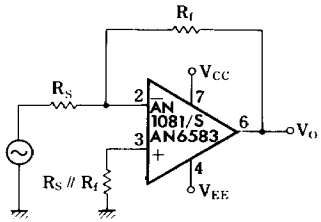
Test Circuit 4 (P_C)



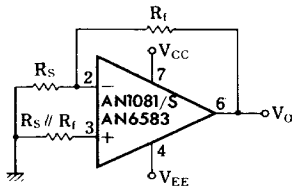
Test Circuit 5 (SR)



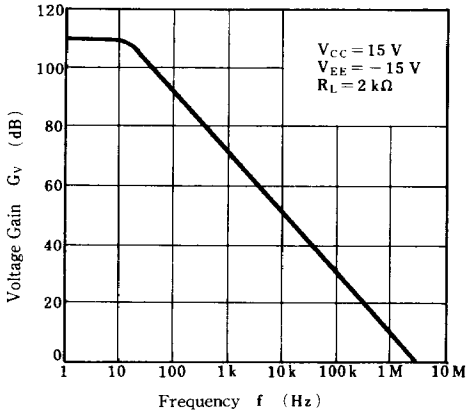
Test Circuit 6 ($f_{(T)}$)



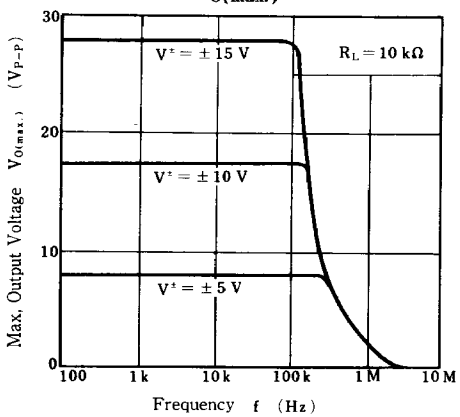
Test Circuit 7 (V_{ni})



$G_V - f$



$V_{O(max.)} - f$



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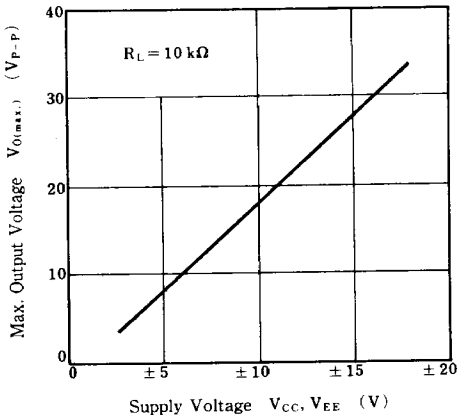
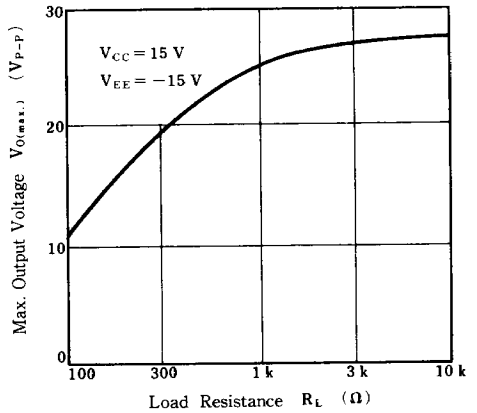
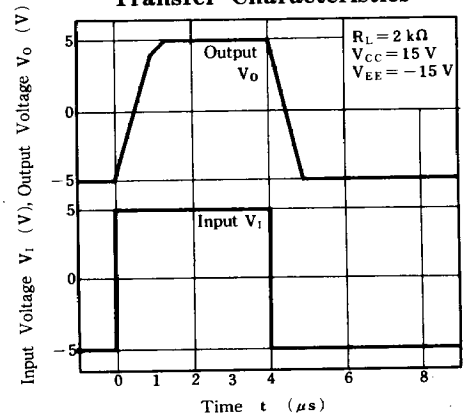
$V_{O(max.)} - V_{CC}$, V_{EE}



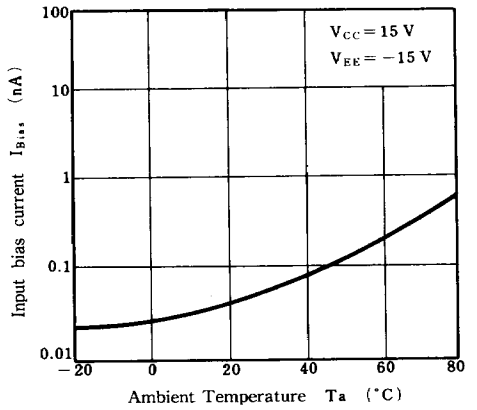
$V_{O(max.)} - R_L$



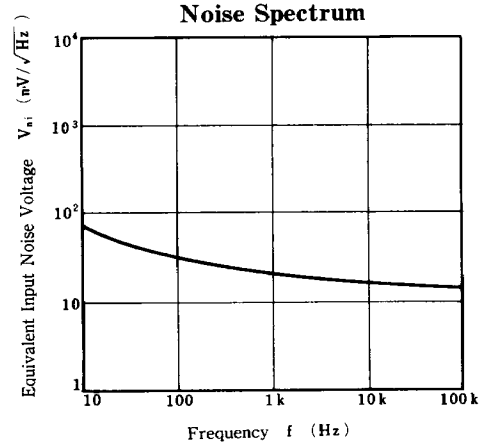
Transfer Characteristics



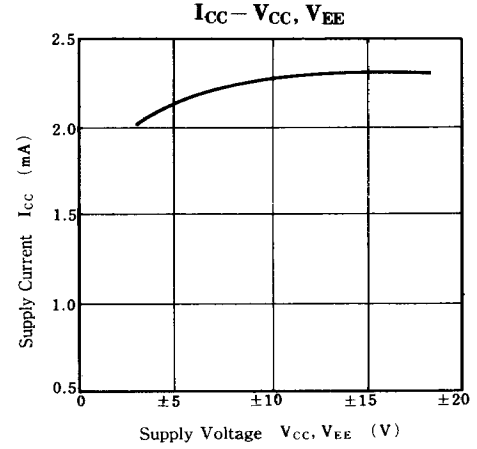
$I_{Bias} - Ta$



Noise Spectrum



$I_{CC} - V_{CC}$, V_{EE}



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