QL7100 QuickDSP Data Sheet

Combining Embedded DSP Blocks, Performance, Density, and Embedded RAM

1.0 Device Highlights

Clock Network

- 9 global clock networks
- 1 dedicated, 8 programmable
- 16 I/O (high drive) networks: 2 banks per I/O
- 20 Quad-net networks: 5 per quadrant

Programmable I/O

- High performance enhanced I/O: less than 3 ns Tco
- Programmable slew rate control
- Programmable I/O standards
- LVTTL, LVCMOS, PCI, GTL+, SSTL2, and SSTL3
- 8 independent I/O banks
- 3 register configuration: Input, Output, OE

Parameterized IP

- Free parameterized IP administered with a DSP Wizard
- Supports multiple and hierarchical IP instantiations

Applications

- Signal processing operators
- Signal processing functions
- Networking / communications for VoIP
- Speech / voice processing
- Channel coding

High Speed Customizable Logic

- 0.25u, 5 layer metal CMOS process
- 2.5 V Vcc, 2.5 / 3.3 V drive capable I/O
- 256 programmable I/O
- 960 Logic Cells
- 292,000 max system gates
- Muxed based architecture, non-volatile technology
- Completely customizable for any digital applications

Dual Port SRAM

- 36 blocks of dual-port SRAM
- 2,304 bit dual port high performance SRAM Blocks
- Total of 82,900 bits
- RAM / ROM / FIFO Wizard for automatic configuration
- Configurable and cascadable
- Array sizes of 2, 4, 9, and 18
- < 3 ns access times, 300+ MHz FIFO

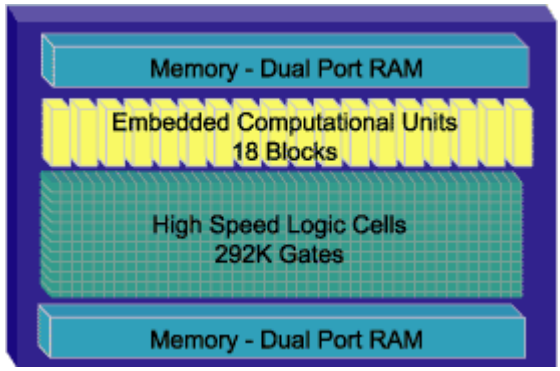

Figure 1: Embedded QuickDSP Block Diagram

2.0 AC Characteristics at Vcc = 2.5V, TA=25° C (K=1.00)

The AC Specifications, Logic Cell diagrams and waveforms are provided below.

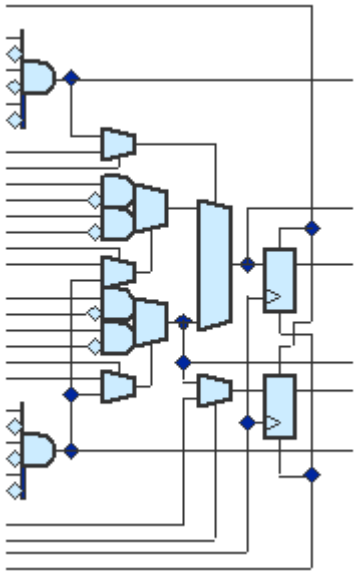

Figure 2: QuickDSP Logic Cell

Table 1: Logic Cells

Symbol	Parameter	Propagation delay (ns)
Logic Cells		**1**
tPD	Combinatorial delay: time taken by the combinatorial circuit to output	0.257
tSU	Setup time: the amount of time the synchronous input of the flip flop must be stable before the active clock edge	0.22
thl	Hold time: the amount of time the synchronous input of the flip flop must be stable after the active block edge	0
tCLK	Clock to out delay: the amount of time the synchronous input of the flip flop must be stable after the active block edge	0.255
tCWHI	Clock High Time: the length of time that the clock stays high	0.46
tCWLO	Clock Low Time: the length of time that the clock stays low	0.46
tSET	Set Delay: amount of time between when the flip flop is ”set” (high) and when Q is consequent “set” (high)	0.18
tRESET	Reset Delay: amount of time between when the flip flop is ”reset” (low) and when Q is consequent “reset” (low)	0.09
tSW	Set Width: length of time that the SET signal remains high (low if active low)	0.3
tRW	Reset Width: length of time that the RESET signal remains high (low if active low)	0.3

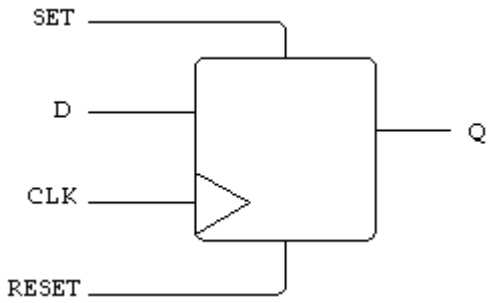

Figure 3: Logic Cell Flip Flop

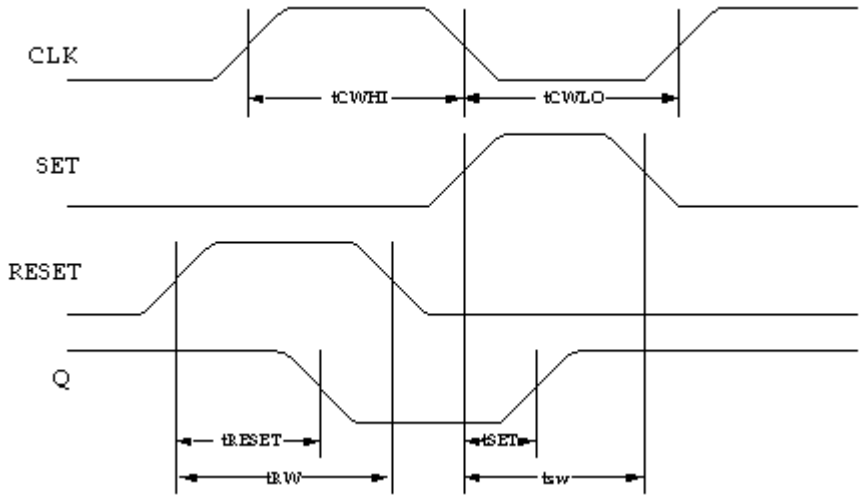

Figure 4: Logic Cell Flip Flop Timings - First Waveform

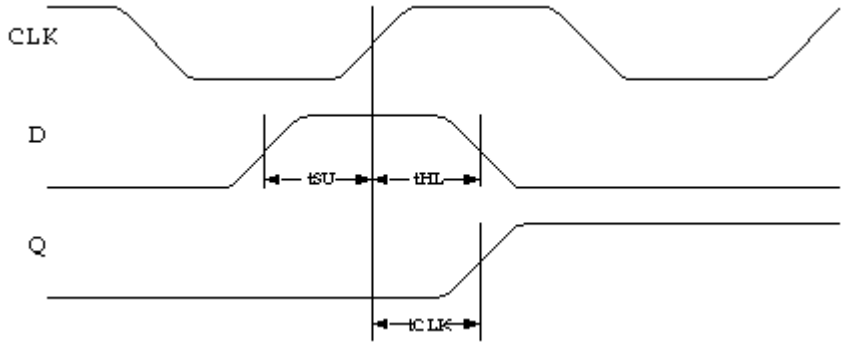

Figure 5: Logic Cell Flip Flop Timings - Second Waveform

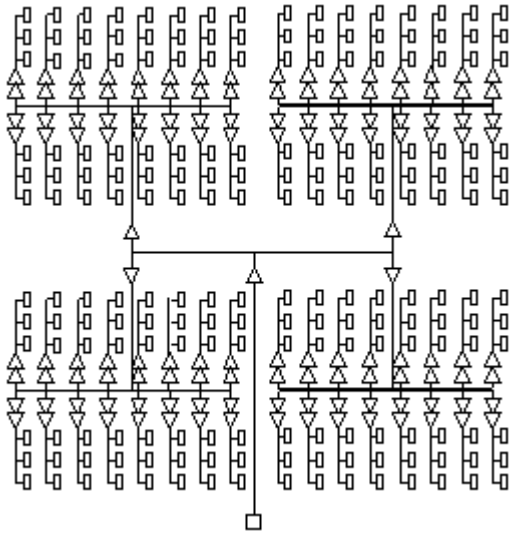

Figure 6: QuickDSP Global Clock Structure

Table 2: QuickDSP Clock Performance

	Clock Performance	
	Global	Dedicated
Macro	1.51 ns	1.59 ns
I/O	2.06 ns	1.73 ns
Skew	0.55 ns	0.14 ns

Table 3: QuickDSP Input Register Cell

Symbol Input Register Cell Only	Parameter	Propagation delay (ns)
tGCKP	Global clock pin delay	
GCKB	Global clock buffer delay	

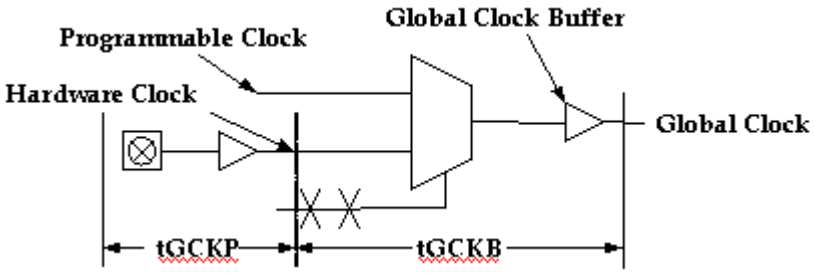

Figure 7: Global Clock Structure Schematic

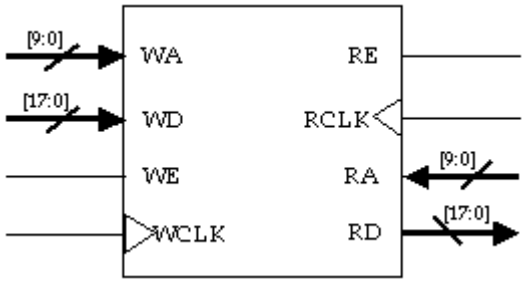

Figure 8: QuickRAM Module

Table 4: RAM Cell Synchronous Write Timing

Symbol	Parameter	Propagation delay (ns)
RAM Cell Synchronous Write Timing		**1**
TSWA	WA Setup Time to WCLK: the amount of time the WRITE ADDRESS must be stable before the active edge of the WRITE CLOCK	0.675
THWA	WA Hold Time to WCLK: the amount of time the WRITE ADDRESS must be stable after the active edge of the WRITE CLOCK	0
TSWD	WD Setup Time to WCLK: the amount of time the WRITE DATA must be stable before the active edge of the WRITE CLOCK	0.654
THWD	WD Hold Time to WCLK: the amount of time the WRITE DATA must be stable after the active edge of the WRITE CLOCK	0
TSWE	WE Setup Time to WCLK: the amount of time the WRITE ENABLE must be stable before the active edge of the WRITE CLOCK	0.623
THWE	WE Hold Time to WCLK: the amount of time the WRITE ENABLE must be stable after the active edge of the WRITE CLOCK	0
TWCRD	WCLK to RD (WA=RA) [5]: the amount of time between the active WRITE CLOCK edge and the time when the data is available at RD	4.38

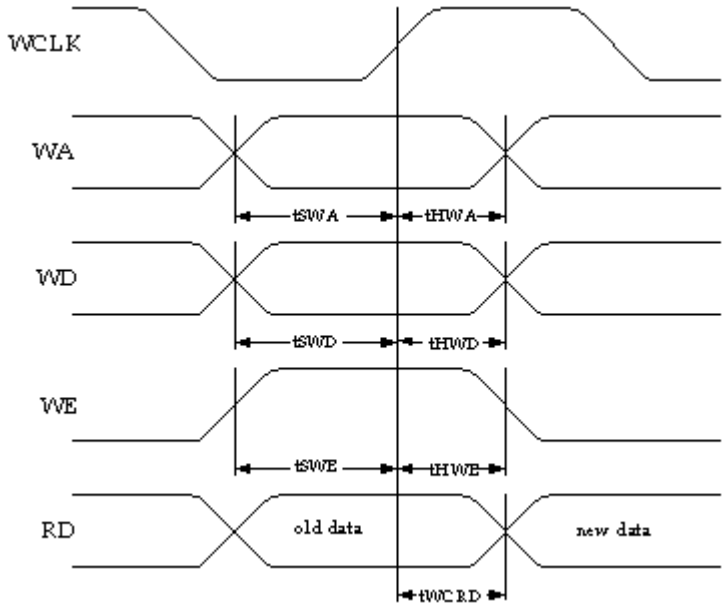

Figure 9: RAM Cell Synchronous Write Timing

Table 5: RAM Cell Synchronous & Asynchronous Read Timing

Symbol	Parameter	Propagation delay (ns)
RAM Cell Synchronous Read Timing		**1**
TSRA	RA Setup Time to RCLK: the amount of time the READ ADDRESS must be stable before the active edge of the READ CLOCK	0.686
THRA	RA Hold Time to RCLK: the amount of time the READ ADDRESS must be stable after the active edge of the READ CLOCK	0
TSRE	RE Setup Time to RCLK: the amount of time the READ ENABLE must be stable before the active edge of the READ CLOCK	0.243
THRE	RE Hold Time to RCLK: the amount of time the READ ENABLE must be stable after the active edge of the READ CLOCK	0
TRCRD	RCLK to RD [5]: the amount of time between the active READ CLOCK edge and the time when the data is available at RD	4.38
RAM Cell Synchronous Read Timing		
RPDRD	RA to RD [5]: amount of time between when the READ ADDRESS is input and when the DATA is output	2.06

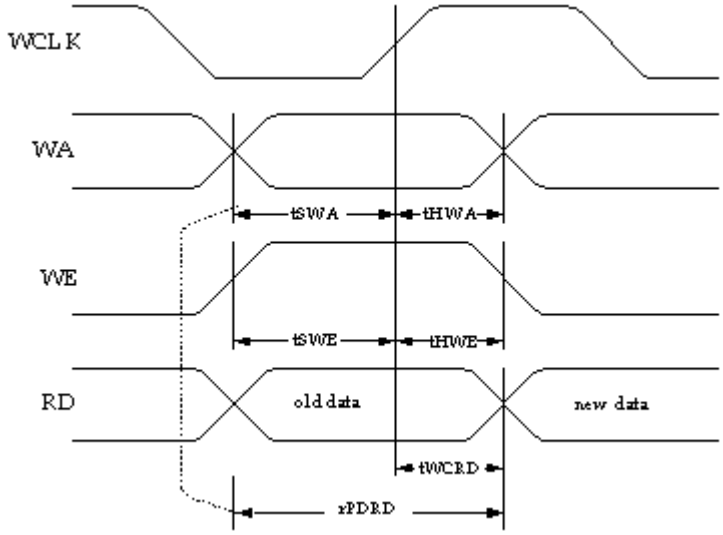

Figure 10: RAM Cell Synchronous & Asynchronous Read Timing

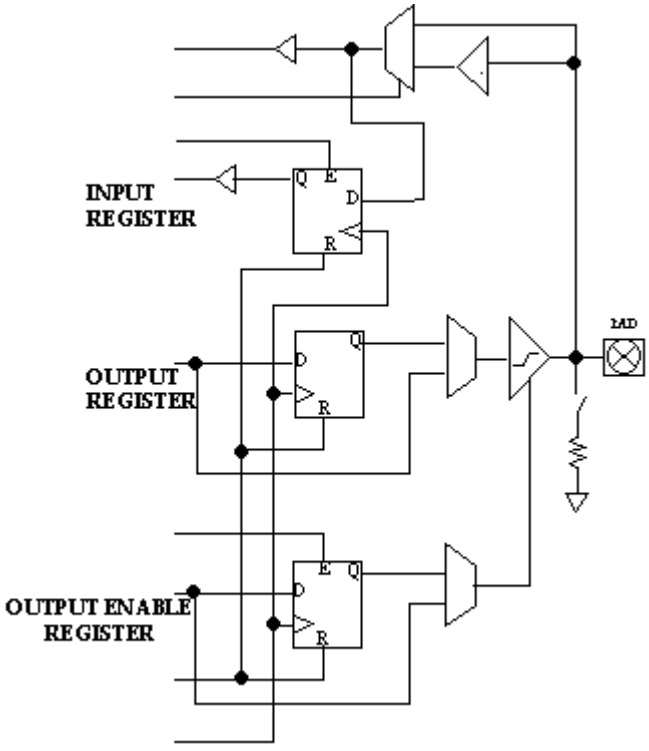

Figure 11: QuickDSP Cell I/O

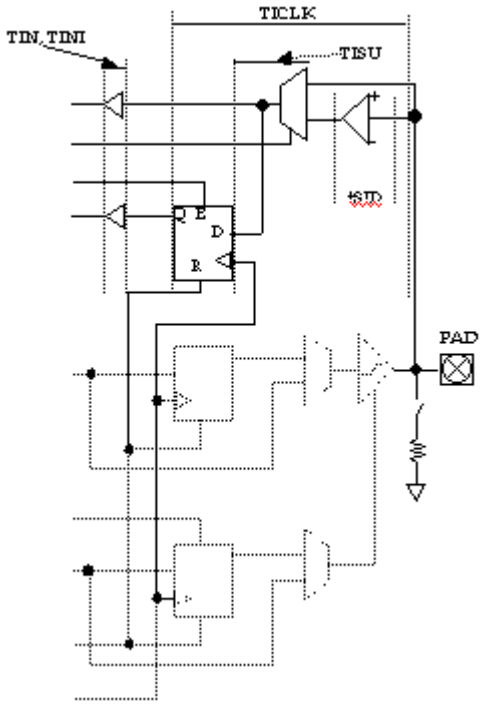

Figure 12: QuickDSP Input Register Cell

Table 6: Input Register Cell

Symbol	Parameter	Propagation delay (ns)
Input Register Cell Only		**1**
tISU	Input register setup time: the amount of time the synchronous input of the flip flop must be stable before the active clock edge	3.12
tIH	Input register hold time: the amount of time the synchronous input of the flip flop must be stable after the active clock edge	0
tICLK	Input register clock to Q: the amount of time taken by the flip flop to output after the active clock edge	1.08
tIRST	Input register reset delay: amount of time between when the flip flop is “reset”(low) and when Q is consequently “reset” (low)	0.99
tIESU	Input register clock enable setup time: the amount of time “enable” must be stable before the active clock edge	0.37
tIEH	Input register clock enable time: the amount of time “enable” must be stable after the active clock edge	0

Table 7: Standard Input Delays

Symbol Standard Input Delays	Parameter To get the total input delay and this delay to tISU	Propagation delay (ns) 1
tSID (LVTTL)	LVTTL input delay: Low Voltage TTL for 3.3V applications	0.34
tSID (LVCMOS2)	LVCMOS2 input delay: Low Voltage CMOS for 2.5V and lower applications	0.42
tSID (GTL+)	GTL+ input delay: Gunning Transceiver Logic	0.68
tSID (SSTL3)	SSTL3 input delay: Stub Series Terminated Logic for 3.3V	0.55
tSID (SSTL2)	SSTL2 input delay: Stub Series Terminated Logic for 2.5V	0.607

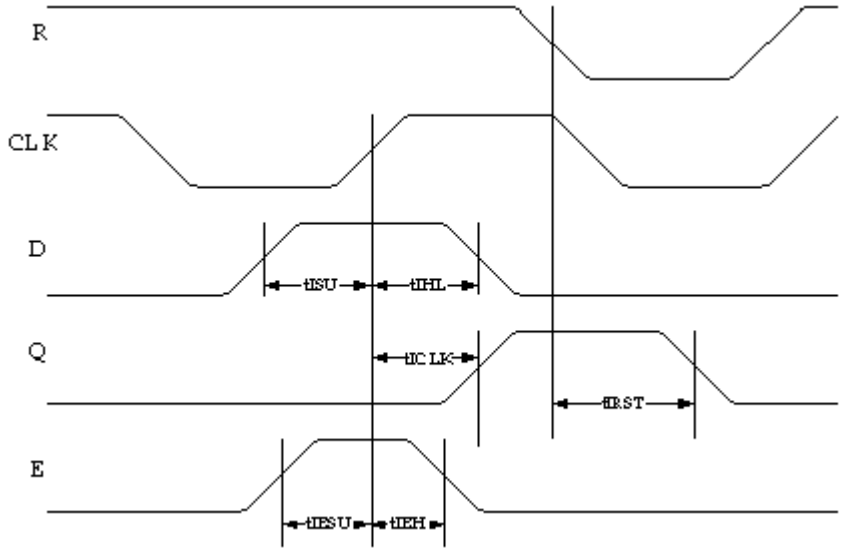

Figure 13: QuickDSP Input Register Cell Timing

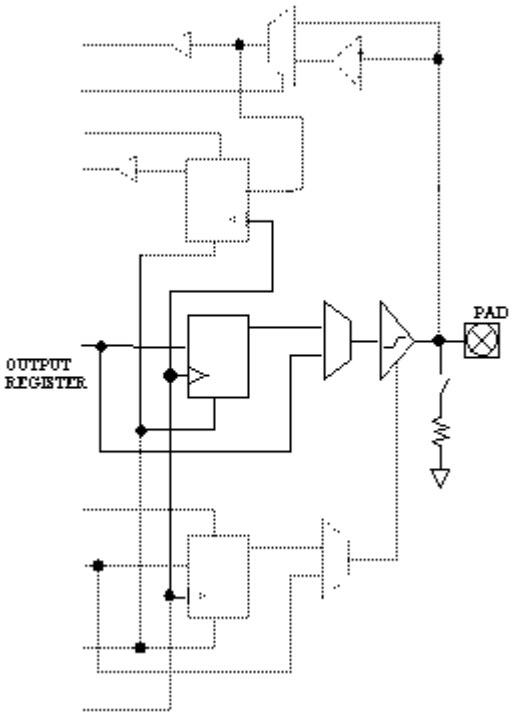

Figure 14: QuickDSP Output Register Cell

Table 8: QuickDSP Output Register Cell

Symbol	Parameter	Propagation delay (ns)
Output Register Cell Only		**1**
TOUTLH	Output Delay Low to High (10% of H)	0.40
TOUTHL	Output Delay High to Low (90% of H)	0.55
TPZH	Output Delay Tri-state to High (10% of Z)	
TPZL	Output Delay Tri-state to Low (90% of Z)	
TPHZ	Output Delay High to Tri-State	3.07
TPLZ	Output Delay Low to Tri-State	2.53

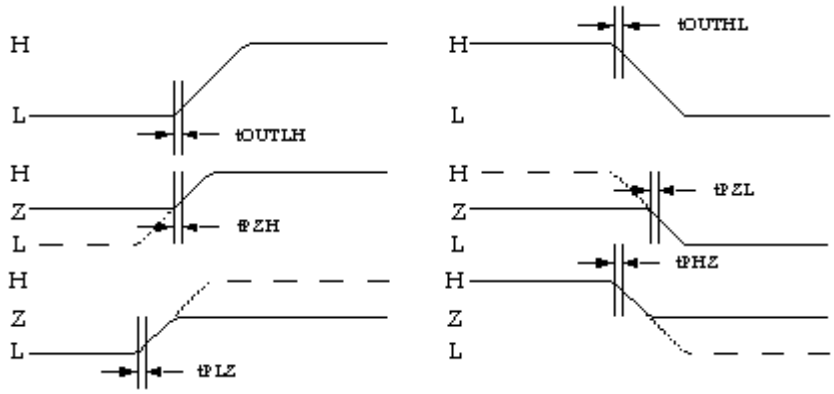

Figure 15: QuickDSP Output Register Cell Timing

Table 9: VCCIO = 3.3 V

	Fast Slew	Slow Slew
Rising Edge	2.8 V/ns	1.0 V/ns
Falling Edge	2.86 V/ns	1.0 V/ns

Table 10: VCCIO = 2.5 V

	Fast Slew	Slow Slew
Rising Edge	1.7 V/ns	0.6 V/ns
Falling Edge	1.9 V/ns	0.6 V/ns

3.0 DC Characteristics

The DC Specifications are provided in the tables below.

Table 11: Absolute Maximum Ratings

V_{CC} Voltage	-0.5 to 3.6V	**DC Input Current**	±20 mA
V_{CCIO} Voltage	-0.5 to 4.6V	**ESD Pad Protection**	±2000V
V_{REF} Voltage	2.7V	**Storage Temperature**	-65°C to +150°C
Input Voltage	-0.5V to V_{CCIO} +0.5V	**Maximum Lead Temperature**	300°C
Latch-up Immunity	±100 mA		

Table 12: Operating Range

Symbol	Parameter		Military		Industrial		Commercial		Unit
			Min	Max	Min	Max	Min	Max	
VCC	Supply Voltage		2.3	2.7	2.3	2.7	2.3	2.7	V
VCCIO	I/O Input Tolerance Voltage		2.3	3.6	2.3	3.6	2.3	3.6	V
TA	Ambient Temperature		-55		-40	85	0	70	°C
TC	Case Temperature			125					°C
K	Delay Factor	-4 Speed Grade	0.42	2.3	0.43	2.16	0.47	2.11	n/a
		-5 Speed Grade	0.42	1.92	0.43	1.80	0.46	1.76	n/a
		-6 Speed Grade	0.42	1.35	0.43	1.26	0.46	1.23	n/a
		-7 Speed Grade	0.42	1.22	0.43	1.14	0.46	1.11	n/a

Table 13: DC Input and Output Levels

	V_{REF}		V_{IL}		V_{IH}		V_{OL}	V_{OH}	I_{OL}	I_{OH}
	V_{MIN}	V_{MAX}	V_{MIN}	V_{MAX}	V_{MIN}	V_{MAX}	V_{MAX}	V_{MIN}	mA	mA
LVTTL	n/a	n/a	-0.3	0.8	2.0	V_{CCIO}-0.3	0.4	24.	2.0	-2.0
LVCMOS2	n/a	n/a	-0.3	0.7	1.7	V_{CCIO}-0.3	0.7	1.7	2.0	-2.0
GTL+	0.88	1.12	-0.3	V_{REF}-2.0	V_{REF}+2.0	V_{CCIO}-0.3	0.6	n/a	40	n/a
PCI	n/a	n/a	-0.3	0.3xV_{CC}	0.5xV_{CC}	V_{CCIO}-0.5	0.1xV_{CC}	0.9xV_C	1.5	-0.5
SSTL2	1.15	1.35	-0.3	V_{REF}-0.18	V_{REF}+0.18	V_{CCIO}+0.3	0.74	1.76	7.6	-7.6
SSTL3	1.3	1.7	-0.3	V_{REF}-0.2	V_{REF}+2.0	V_{CCIO}+0.3	1.10	1.90	9	-8

4.0 Pin Descriptions

Table 14: Pin Descriptions

Pin	Function	Description
TDI/RSI	Test Data In for JTAG /RAM init. Serial Data In	Hold HIGH during normal operation. Connects to serial PROM data in for RAM initialization. Connect to VCC if unused
TRSTB/RRO	Active low Reset for JTAG /RAM init. reset out	Hold LOW during normal operation. Connects to serial PROM reset for RAM initialization. Connect to GND if unused
TMS	Test Mode Select for JTAG	Hold HIGH during normal operation. Connect to VCC if not used for JTAG
TCK	Test Clock for JTAG	Hold HIGH or LOW during normal operation. Connect to VCC or ground if not used for JTAG
TDO/RCO	Test data out for JTAG /RAM init. clock out	Connect to serial PROM clock for RAM initialization. Must be left unconnected if not used for JTAG or RAM initialization
I/GCLK	High-drive input and/or global network driver	Can be configured as either or both
I/O	Input/Output pin	Can be configured as an input and/or output
VCC	Power supply pin	Connect to 2.5V supply
VCCIO	Input voltage tolerance pin	Connect to 3.3 volt supply if 3.3 volt input tolerance is required, otherwise connect to 2.5V supply
GND	Ground pin	Connect to ground
PLLIN	PLL clock input	Clock input for PLL
DEDCLK	Dedicated clock pin	Low skew global clock
GNDPLL	Ground pin for PLL	Connect to GND
INREF	Differential reference voltage	Connect to reference voltage or ground if used for non-differential input
PLLOUT	PLL output pin	Dedicated PLL output pin. Otherwise may be left unconnected
IOCTRL	Highdrive input	Can be used as highdrive input or clock to I/O register within the same bank. Tied low or high if unused

4.1 Recommended Unused Pin Terminations for the QuickDSP devices

All unused, general purpose I/O pins can be tied to VCC, GND or HIZ (high impedance) internally using the Configuration Editor. The option is given in the right-bottom corner of the Configuration window. The use the Configuration Editor go to: TOOLS/CONFIGURATION PINS.

The rest of the pins should be terminated at the board level in the following manner:

Table 15: Recommended Unused Pin Terminations

Signal Name	Recommended Termination
PLLOUT<x>	Unused PLL output pins must be connected to either VCC or GND so that their associated input buffer never floats. Utilized PLL output pins that route the PLL clock outside of the chip, do not need to be tied to either VCC or GND.
IOCTRL<y>	Any unused pins of this type must be connected to either VCC or GND.
CLK/PLLIN<x>	Any unused clock pins should be connected to VCC or GND.
PLLRST<x>	If a PLL module is not used, then the associated PLLRST<x> must be connected to VCC, under normal operation use it as needed.
INREF<y>	If an I/O bank does not require the use of INREF signal the pin should be connected to GND.

NOTE: *x -> number, y -> alphabetical character*

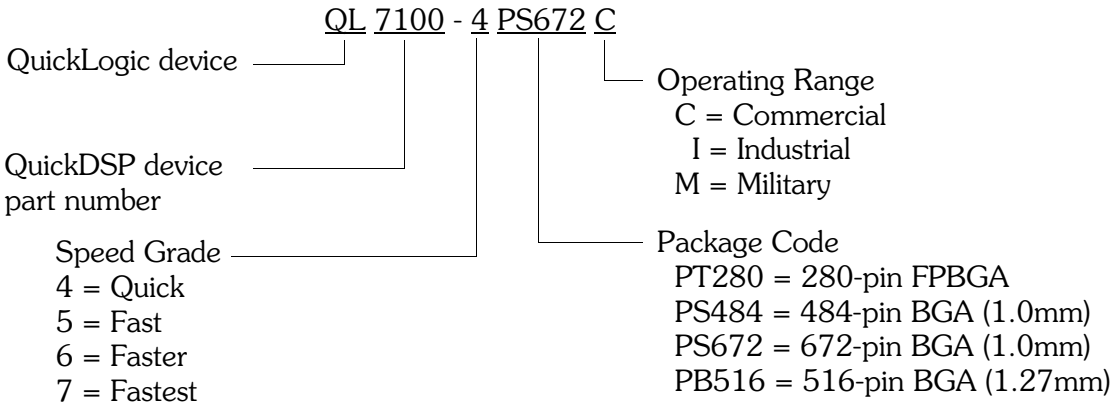

Figure 16: Ordering Information

5.0 208 PQFP Pinout Diagram

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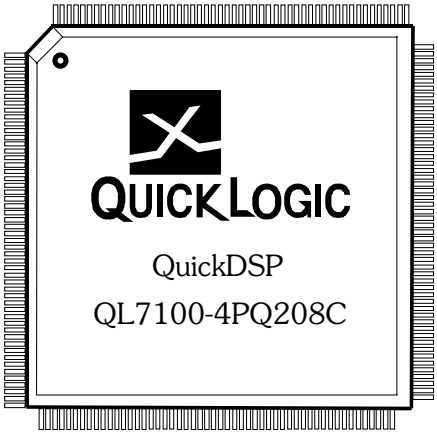

6.0 208 PQFP Pinout Table

Table 16: 208 PQFP Pinout Table

208 PQFP	Function	208 PQFP	Function	208 PQFP	Function	208 PQFP	Function	208 PQFP	Function	208 PQFP	Function
1	PLLRST(3)	36	IO(B)	71	IO(C)	106	VCCPLL(1)	141	IO(F)	176	IO(G)
2	VCCPLL(3)	37	IO(B)	72	VCCIO(C)	107	IO(E)	142	IO(F)	177	VCCIO(G)
3	GND	38	IO(B)	73	IO(C)	108	GND	143	IO(F)	178	GND
4	GND	39	IOCTRL(B)	74	IO(C)	109	IO(E)	144	IOCTRL(F)	179	IO(G)
5	IO(A)	40	INREF(B)	75	GND	110	IO(E)	145	INREF(F)	180	IO(G)
6	IO(A)	41	IOCTRL(B)	76	VCC	111	VCCIO(E)	146	VCC	181	IO(G)
7	IO(A)	42	IO(B)	77	IO(C)	112	IO(E)	147	IOCTRL(F)	182	VCC
8	VCCIO(A)	43	IO(B)	78	TRSTB	113	VCC	148	IO(F)	183	TCK
9	IO(A)	44	VCCIO(B)	79	VCC	114	IO(E)	149	IO(F)	184	VCC
10	IO(A)	45	IO(B)	80	IO(D)	115	IO(E)	150	VCCIO(F)	185	IO(H)
11	IOCTRL(A)	46	VCC	81	IO(D)	116	IO(E)	151	IO(F)	186	IO(H)
12	VCC	47	IO(B)	82	IO(D)	117	IOCTRL(E)	152	IO(F)	187	IO(H)
13	INREF(A)	48	IO(B)	83	GND	118	INREF(E)	153	GND	188	GND
14	IOCTRL(A)	49	GND	84	VCCIO(D)	119	IOCTRL(E)	154	IO(F)	189	VCCIO(H)
15	IO(A)	50	TDO	85	IO(D)	120	IO(E)	155	PLLOUT(3)	190	IO(H)
16	IO(A)	51	PLLOUT(1)	86	VCC	121	IO(E)	156	GNDPLL(0)	191	IO(H)
17	IO(A)	52	GNDPLL(2)	87	IO(D)	122	VCCIO(E)	157	GND	192	IOCTRL(H)
18	IO(A)	53	GND	88	IO(D)	123	GND	158	VCCPLL(0)	193	IO(H)
19	VCCIO(A)	54	VCCPLL(2)	89	VCC	124	IO(E)	159	PLLRST(0)	194	INREF(H)
20	IO(A)	55	PLLRST(2)	90	IO(D)	125	IO(E)	160	GND	195	VCC
21	GND	56	VCC	91	IO(D)	126	IO(E)	161	IO(G)	196	IOCTRL(H)
22	IO(A)	57	IO(C)	92	IOCTRL(D)	127	CLK(5),PLLIN (3)	162	VCCIO(G)	197	IO(H)
23	TDI	58	GND	93	INREF(D)	128	CLK(6)	163	IO(G)	198	IO(H)
24	CLK(0)	59	IO(C)	94	IOCTRL(D)	129	VCC	164	IO(G)	199	IO(H)
25	CLK(1)	60	VCCIO(C)	95	IO(D)	130	CLK(7)	165	VCC	200	IO(H)
26	VCC	61	IO(C)	96	IO(D)	131	VCC	166	IO(G)	201	IO(H)
27	CLK(2),PLLIN (2)	62	IO(C)	97	IO(D)	132	CLK(8)	167	IO(G)	202	IO(H)
28	CLK(3),PLLIN (1)	63	IO(C)	98	VCCIO(D)	133	TMS	168	IO(G)	203	VCCIO(H)
29	VCC	64	IO(C)	99	IO(D)	134	IO(F)	169	IOCTRL(G)	204	GND
30	CLK(4),DEDC LK,PLLIN(0)	65	IO(C)	100	IO(D)	135	IO(F)	170	INREF(G)	205	IO(H)
31	IO(B)	66	IO(C)	101	GND	136	IO(F)	171	IOCTRL(G)	206	PLLOUT(2)
32	IO(B)	67	IOCTRL(C)	102	PLLOUT(0)	137	GND	172	IO(G)	207	GND
33	GND	68	INREF(C)	103	GND	138	VCCIO(F)	173	IO(G)	208	GNDPLL(3)
34	VCCIO(B)	69	IOCTRL(C)	104	GNDPLL(1)	139	IO(F)	174	IO(G)		
35	IO(B)	70	IO(C)	105	PLLRST(1)	140	IO(F)	175	VCC		

7.0 280 PBGA Pinout Diagram

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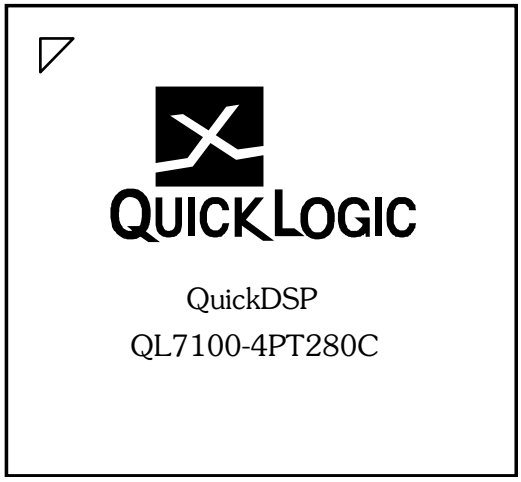

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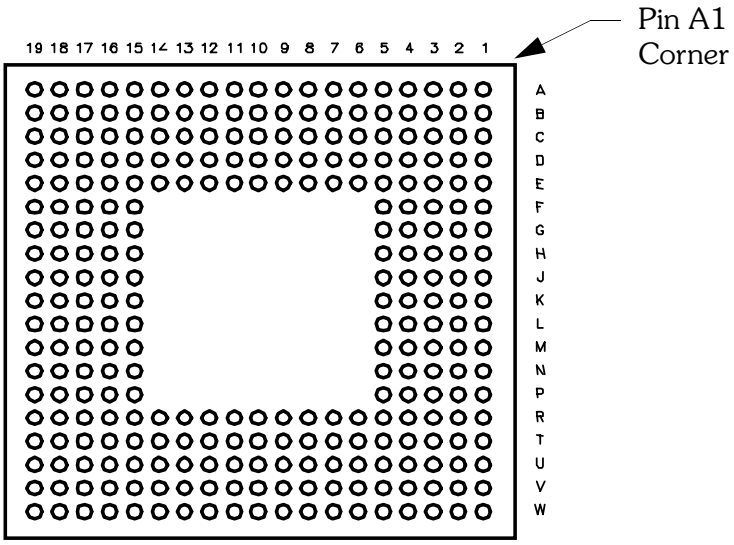


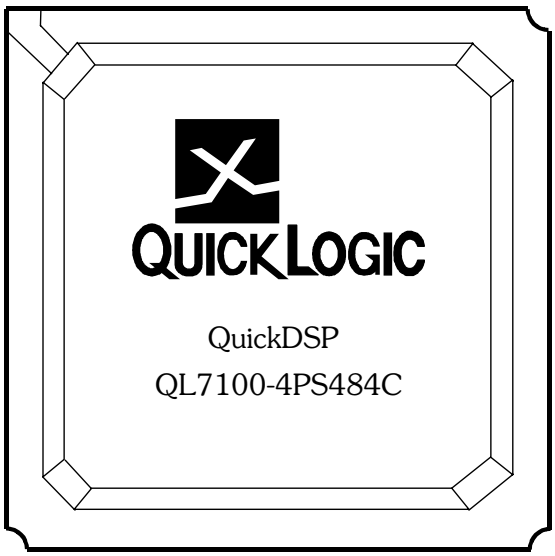
8.0 280 PBGA Pinout Table

Table 17: 280 PBGA Pinout Table

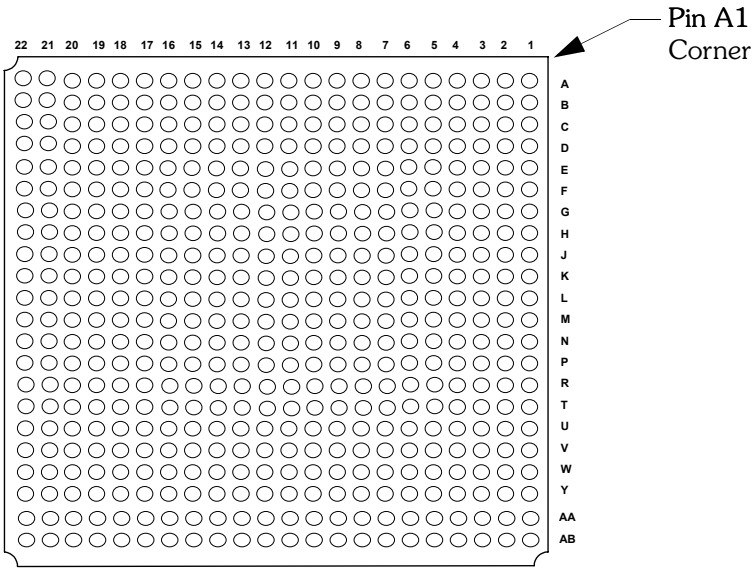
280 PBGA	Function	280 PBGA	Function	280 PBGA	Function	280 PBGA	Function	280 PBGA	Function	280 PBGA	Function
A1	PLLOUT<3>	C10	CLK<5>/PLLIN<3>	E19	IOCTRL<D>	K16	I/O<C>	R4	I/O<H>	U13	I/O<B>
A2	GNDPLL<0>	C11	VCCIO<E>	F1	INREF<G>	K17	I/O<D>	R5	GND	U14	IOCTRL<B>
A3	I/O<F>	C12	I/O<E>	F2	IOCTRL<G>	K18	I/O<C>	R6	GND	U15	VCCIO<B>
A4	I/O<F>	C13	I/O<E>	F3	I/O<G>	K19	TRSTB	R7	VCC	U16	I/O<B>
A5	I/O<F>	C14	I/O<E>	F4	I/O<G>	L1	I/O<H>	R8	VCC	U17	TDO
A6	IOCTRL<F>	C15	VCCIO<E>	F5	GND	L2	I/O<H>	R9	GND	U18	PLLRST<2>
A7	I/O<F>	C16	I/O<E>	F15	VCC	L3	VCCIO<H>	R10	GND	U19	I/O<B>
A8	I/O<F>	C17	I/O<E>	F16	IOCTRL<D>	L4	I/O<H>	R11	VCC	V1	PLLOUT<2>
A9	I/O<F>	C18	I/O<E>	F17	I/O<D>	L5	VCC	R12	VCC	V2	GNDPLL<3>
A10	CLK<7>	C19	I/O<E>	F18	I/O<D>	L15	GND	R13	VCC	V3	GND
A11	I/O<E>	D1	I/O<G>	F19	I/O<D>	L16	I/O<C>	R14	VCC	V4	I/O<A>
A12	I/O<E>	D2	I/O<G>	G1	I/O<G>	L17	VCCIO<C>	R15	GND	V5	I/O<A>
A13	I/O<E>	D3	I/O<F>	G2	I/O<G>	L18	I/O<C>	R16	I/O<C>	V6	IOCTRL<A>
A14	IOCTRL<E>	D4	I/O<F>	G3	IOCTRL<G>	L19	I/O<C>	R17	VCCIO<C>	V7	I/O<A>
A15	I/O<E>	D5	I/O<F>	G4	I/O<G>	M1	I/O<H>	R18	I/O<C>	V8	I/O<A>
A16	I/O<E>	D6	I/O<F>	G5	VCC	M2	I/O<H>	R19	I/O<C>	V9	I/O<A>
A17	I/O<E>	D7	I/O<F>	G15	VCC	M3	I/O<H>	T1	I/O<H>	V10	CLK<1>
A18	PLLRST<1>	D8	I/O<F>	G16	I/O<D>	M4	I/O<H>	T2	I/O<H>	V11	CLK<4>DEDCLK/PLLIN<0>
A19	GND	D9	CLK<8>	G17	I/O<D>	M5	VCC	T3	I/O<A>	V12	I/O<B>
B1	PLLRST<0>	D10	I/O<E>	G18	I/O<D>	M15	VCC	T4	I/O<A>	V13	I/O<B>
B2	GND	D11	I/O<E>	G19	I/O<D>	M16	INREF<C>	T5	I/O<A>	V14	INREF<B>
B3	I/O<F>	D12	I/O<E>	H1	I/O<G>	M17	I/O<C>	T6	IOCTRL<A>	V15	I/O<B>
B4	I/O<F>	D13	INREF<E>	H2	I/O<G>	M18	I/O<C>	T7	I/O<A>	V16	I/O<B>
B5	I/O<F>	D14	I/O<E>	H3	I/O<G>	M19	I/O<C>	T8	I/O<A>	V17	I/O<B>
B6	INREF<F>	D15	I/O<E>	H4	I/O<G>	N1	IOCTRL<H>	T9	I/O<A>	V18	GNDPLL<2>
B7	I/O<F>	D16	I/O<D>	H5	VCC	N2	I/O<H>	T10	I/O<A>	V19	GND
B8	I/O<F>	D17	I/O<D>	H15	VCC	N3	I/O<H>	T11	CLK<3>/PLLIN<1>	W1	GND
B9	TMS	D18	I/O<D>	H16	VCC	N4	I/O<H>	T12	I/O<B>	W2	PLLRST<3>
B10	CLK<6>	D19	I/O<D>	H17	I/O<D>	N5	VCC	T13	I/O<B>	W3	I/O<A>
B11	I/O<E>	E1	I/O<G>	H18	I/O<D>	N15	VCC	T14	I/O<B>	W4	I/O<A>
B12	I/O<E>	E2	I/O<G>	H19	I/O<D>	N16	I/O<C>	T15	I/O<B>	W5	I/O<A>
B13	IOCTRL<E>	E3	VCCIO<G>	J1	I/O<G>	N17	I/O<C>	T16	I/O<B>	W6	I/O<A>
B14	I/O<E>	E4	I/O<F>	J2	I/O<G>	N18	IOCTRL<C>	T17	VCCPLL<2>	W7	I/O<A>
B15	I/O<E>	E5	GND	J3	VCCIO<G>	N19	IOCTRL<C>	T18	I/O<B>	W8	I/O<A>
B16	I/O<E>	E6	VCC	J4	I/O<G>	P1	I/O<H>	T19	I/O<B>	W9	TDI
B17	VCCPLL<1>	E7	VCC	J5	GND	P2	I/O<H>	U1	I/O<A>	W10	CLK<2>/PLLIN<2>
B18	GNDPLL<1>	E8	VCC	J15	VCC	P3	IOCTRL<H>	U2	I/O<A>	W11	I/O<B>
B19	PLLOUT<0>	E9	VCC	J16	I/O<C>	P4	INREF<H>	U3	VCCPLL<3>	W12	I/O<B>
C1	I/O<F>	E10	GND	J17	VCCIO<D>	P5	VCC	U4	I/O<A>	W13	I/O<B>
C2	VCCPLL<0>	E11	GND	J18	I/O<D>	P15	GND	U5	VCCIO<A>	W14	IOCTRL<B>
C3	I/O<F>	E12	VCC	J19	I/O<D>	P16	I/O<C>	U6	INREF<A>	W15	I/O<B>
C4	I/O<F>	E13	VCC	K1	VCC	P17	I/O<C>	U7	I/O<A>	W16	I/O<B>
C5	VCCIO<F>	E14	GND	K2	TCK	P18	I/O<C>	U8	I/O<A>	W17	I/O<B>
C6	IOCTRL<F>	E15	GND	K3	I/O<G>	P19	I/O<C>	U9	VCCIO<A>	W18	I/O<B>
C7	I/O<F>	E16	I/O<D>	K4	I/O<G>	R1	I/O<H>	U10	CLK<0>	W19	PLLOUT<1>
C8	I/O<F>	E17	VCCIO<D>	K5	GND	R2	I/O<H>	U11	VCCIO<B>		
C9	VCCIO<F>	E18	INREF<D>	K15	GND	R3	VCCIO<H>	U12	I/O<B>		

9.0 484 PBGA Pinout Diagram

Top



Bottom



10.0 484 PBGA Pinout Table

Table 18: 484 PBGA Pinout Table

484 PBGA	Function	484 PBGA	Function	484 PBGA	Function	484 PBGA	Function	484 PBGA	Function	484 PBGA	Function
A1	NC	C17	NC	F11	VCCIO<H>	J5	I/O<A>	L21	NC	P15	VCC
A2	PLLRST<3>	C18	I/O<G>	F12	VCCIO<G>	J6	I/O<A>	L22	I/O<F>	P16	I/O<E>
A3	I/O<A>	C19	I/O<F>	F13	I/O<G>	J7	I/O<A>	M1	I/O<B>	P17	NC
A4	I/O<A>	C20	GNDPLL<0>	F14	VCCIO<G>	J8	VCC	M2	I/O<B>	P18	I/O<E>
A5	I/O<A>	C21	I/O<F>	F15	NC	J9	GND	M3	I/O<B>	P19	NC
A6	NC	C22	I/O<F>	F16	VCCIO<G>	J10	VCC	M4	CLK<3>/PLLIN<1>	P20	I/O<E>
A7	I/O<H>	D1	I/O<A>	F17	NC	J11	VCC	M5	NC	P21	I/O<E>
A8	IOCTRL<H>	D2	I/O<A>	F18	I/O<F>	J12	GND	M6	VCCIO<B>	P22	I/O<E>
A9	I/O<H>	D3	I/O<A>	F19	I/O<F>	J13	VCC	M7	CLK<1>	R1	I/O<B>
A10	NC	D4	I/O<A>	F20	IOCTRL<F>	J14	GND	M8	VCC	R2	INREF<B>
A11	NC	D5	I/O<A>	F21	I/O<F>	J15	VCC	M9	VCC	R3	I/O<B>
A12	TCK	D6	I/O<H>	F22	IOCTRL<F>	J16	I/O<F>	M10	GND	R4	I/O<B>
A13	I/O<G>	D7	NC	G1	NC	J17	VCCIO<F>	M11	GND	R5	I/O<B>
A14	I/O<G>	D8	I/O<H>	G2	NC	J18	I/O<F>	M12	GND	R6	NC
A15	I/O<G>	D9	NC	G3	I/O<A>	J19	I/O<F>	M13	GND	R7	I/O<B>
A16	NC	D10	I/O<H>	G4	I/O<A>	J20	I/O<F>	M14	GND	R8	GND
A17	I/O<G>	D11	I/O<H>	G5	I/O<A>	J21	I/O<F>	M15	GND	R9	VCC
A18	I/O<G>	D12	I/O<G>	G6	I/O<A>	J22	I/O<F>	M16	GND	R10	VCC
A19	I/O<F>	D13	I/O<G>	G7	GND	K1	TDI	M17	I/O<E>	R11	GND
A20	GND	D14	I/O<G>	G8	I/O<H>	K2	I/O<A>	M18	I/O<E>	R12	VCC
A21	PLLOUT<3>	D15	IOCTRL<G>	G9	I/O<H>	K3	I/O<A>	M19	I/O<E>	R13	VCC
A22	I/O<F>	D16	I/O<G>	G10	NC	K4	I/O<A>	M20	CLK<7>	R14	VCC
B1	I/O<A>	D17	I/O<G>	G11	I/O<G>	K5	I/O<A>	M21	CLK<5>/PLLIN<3>	R15	GND
B2	GND	D18	I/O<F>	G12	GND	K6	VCCIO<A>	M22	TMS	R16	I/O<D>
B3	GNDPLL<3>	D19	VCCPLL<0>	G13	NC	K7	NC	N1	NC	R17	VCCIO<E>
B4	GND	D20	I/O<F>	G14	NC	K8	VCC	N2	I/O<B>	R18	I/O<E>
B5	I/O<A>	D21	I/O<F>	G15	I/O<G>	K9	VCC	N3	I/O<B>	R19	I/O<E>
B6	I/O<H>	D22	I/O<F>	G16	GND	K10	GND	N4	NC	R20	I/O<E>
B7	I/O<H>	E1	IOCTRL<A>	G17	VCCIO<F>	K11	GND	N5	I/O<B>	R21	I/O<E>
B8	INREF<H>	E2	I/O<A>	G18	I/O<F>	K12	GND	N6	NC	R22	I/O<E>
B9	I/O<H>	E3	I/O<A>	G19	I/O<F>	K13	GND	N7	NC	T1	I/O<B>
B10	I/O<H>	E4	I/O<A>	G20	I/O<F>	K14	VCC	N8	VCC	T2	I/O<B>
B11	I/O<H>	E5	NC	G21	INREF<F>	K15	VCC	N9	VCC	T3	I/O<B>
B12	NC	E6	I/O<H>	G22	I/O<F>	K16	NC	N10	GND	T4	I/O<B>
B13	NC	E7	NC	H1	I/O<A>	K17	I/O<F>	N11	GND	T5	I/O<B>
B14	NC	E8	I/O<H>	H2	I/O<A>	K18	I/O<F>	N12	GND	T6	VCCIO<B>
B15	NC	E9	I/O<H>	H3	I/O<A>	K19	NC	N13	GND	T7	GND
B16	I/O<G>	E10	I/O<H>	H4	I/O<A>	K20	I/O<F>	N14	VCC	T8	I/O<C>
B17	I/O<G>	E11	VCC	H5	IOCTRL<A>	K21	I/O<F>	N15	VCC	T9	NC
B18	I/O<G>	E12	I/O<G>	H6	VCCIO<A>	K22	NC	N16	I/O<E>	T10	TRSTB
B19	PLLRST<0>	E13	I/O<G>	H7	I/O<H>	L1	CLK<4> DEDCLK/PLLIN<0>	N17	VCCIO<E>	T11	GND
B20	I/O<F>	E14	NC	H8	GND	L2	CLK<0>	N18	I/O<E>	T12	NC
B21	I/O<F>	E15	IOCTRL<G>	H9	VCC	L3	CLK<2>/PLLIN<2>	N19	I/O<E>	T13	I/O<D>
B22	I/O<F>	E16	I/O<G>	H10	VCC	L4	I/O<A>	N20	I/O<E>	T14	NC
C1	NC	E17	INREF<G>	H11	VCC	L5	I/O<A>	N21	I/O<E>	T15	I/O<D>
C2	I/O<A>	E18	NC	H12	GND	L6	I/O<A>	N22	I/O<E>	T16	GND
C3	VCCPLL<3>	E19	I/O<F>	H13	VCC	L7	GND	P1	NC	T17	I/O<E>
C4	PLLOUT<2>	E20	I/O<F>	H14	VCC	L8	GND	P2	I/O<B>	T18	I/O<E>
C5	I/O<A>	E21	NC	H15	GND	L9	GND	P3	I/O<B>	T19	NC
C6	NC	E22	I/O<F>	H16	I/O<F>	L10	GND	P4	I/O<B>	T20	NC
C7	I/O<H>	F1	I/O<A>	H17	I/O<F>	L11	GND	P5	I/O<B>	T21	IOCTRL<E>
C8	NC	F2	INREF<A>	H18	NC	L12	GND	P6	VCCIO<B>	T22	I/O<E>
C9	IOCTRL<H>	F3	NC	H19	I/O<F>	L13	GND	P7	I/O<B>	U1	IOCTRL<B>
C10	NC	F4	I/O<A>	H20	I/O<F>	L14	VCC	P8	VCC	U2	I/O<B>
C11	I/O<H>	F5	I/O<A>	H21	I/O<F>	L15	VCC	P9	GND	U3	IOCTRL<B>
C12	NC	F6	VCCIO<A>	H22	NC	L16	CLK<6>	P10	VCC	U4	I/O<B>
C13	I/O<G>	F7	VCCIO<H>	J1	I/O<A>	L17	VCCIO<F>	P11	GND	U5	I/O<B>
C14	NC	F8	I/O<H>	J2	I/O<A>	L18	I/O<F>	P12	VCC	U6	I/O<C>
C15	I/O<G>	F9	VCCIO<H>	J3	I/O<A>	L19	CLK<8>	P13	VCC	U7	VCCIO<C>
C16	I/O<G>	F10	I/O<H>	J4	I/O<A>	L20	I/O<F>	P14	GND	U8	NC

Table 18: 484 PBGA Pinout Table (Continued)

484 PBGA	Function	484 PBGA	Function	484 PBGA	Function	484 PBGA	Function	484 PBGA	Function	484 PBGA	Function
U9	VCCIO<C>	V8	I/O<C>	W7	NC	Y6	I/O<C>	AA5	I/O<C>	AB4	I/O<B>
U10	I/O<C>	V9	NC	W8	NC	Y7	I/O<C>	AA6	I/O<C>	AB5	I/O<B>
U11	VCCIO<C>	V10	I/O<C>	W9	NC	Y8	IOCTRL<C>	AA7	NC	AB6	I/O<C>
U12	VCCIO<D>	V11	NC	W10	NC	Y9	I/O<C>	AA8	INREF<C>	AB7	I/O<C>
U13	I/O<D>	V12	VCC	W11	I/O<C>	Y10	I/O<C>	AA9	NC	AB8	IOCTRL<C>
U14	VCCIO<D>	V13	NC	W12	NC	Y11	I/O<D>	AA10	I/O<C>	AB9	I/O<C>
U15	NC	V14	I/O<D>	W13	I/O<D>	Y12	NC	AA11	I/O<C>	AB10	I/O<C>
U16	VCCIO<D>	V15	I/O<D>	W14	NC	Y13	NC	AA12	I/O<D>	AB11	NC
U17	VCCIO<E>	V16	INREF<D>	W15	I/O<D>	Y14	I/O<D>	AA13	I/O<D>	AB12	I/O<D>
U18	I/O<E>	V17	I/O<D>	W16	NC	Y15	IOCTRL<D>	AA14	I/O<D>	AB13	I/O<D>
U19	I/O<E>	V18	I/O<E>	W17	NC	Y16	I/O<D>	AA15	I/O<D>	AB14	NC
U20	IOCTRL<E>	V19	I/O<E>	W18	I/O<E>	Y17	I/O<D>	AA16	NC	AB15	I/O<D>
U21	NC	V20	I/O<E>	W19	NC	Y18	I/O<E>	AA17	NC	AB16	IOCTRL<D>
U22	INREF<E>	V21	I/O<E>	W20	I/O<E>	Y19	PLLOUT<0>	AA18	I/O<D>	AB17	I/O<D>
V1	I/O<B>	V22	I/O<E>	W21	NC	Y20	PLLRST<1>	AA19	I/O<E>	AB18	I/O<D>
V2	I/O<B>	W1	I/O<B>	W22	I/O<E>	Y21	I/O<E>	AA20	GNDPLL<1>	AB19	I/O<E>
V3	I/O<B>	W2	I/O<B>	Y1	I/O<B>	Y22	I/O<E>	AA21	I/O<E>	AB20	GND
V4	I/O<B>	W3	I/O<B>	Y2	I/O<B>	AA1	TDO	AA22	I/O<E>	AB21	VCCPLL<1>
V5	I/O<B>	W4	I/O<B>	Y3	VCCPLL<2>	AA2	PLLOUT<1>	AB1	I/O<B>	AB22	I/O<E>
V6	NC	W5	I/O<B>	Y4	I/O<C>	AA3	GND	AB2	GNDPLL<2>		
V7	I/O<C>	W6	I/O<C>	Y5	I/O<C>	AA4	I/O<B>	AB3	PLLRST<2>		

11.0 516 PBGA Pinout Diagram

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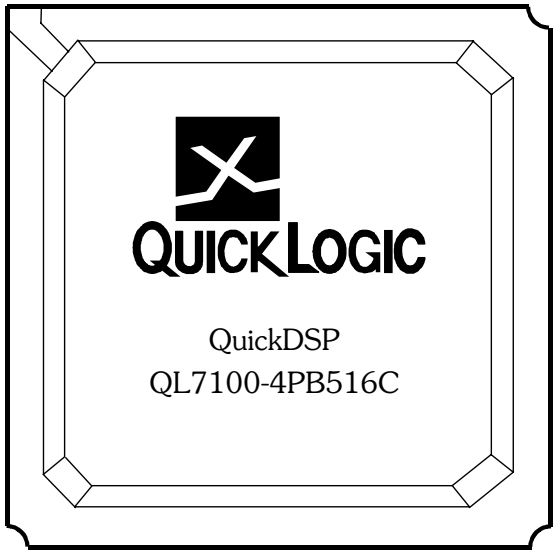
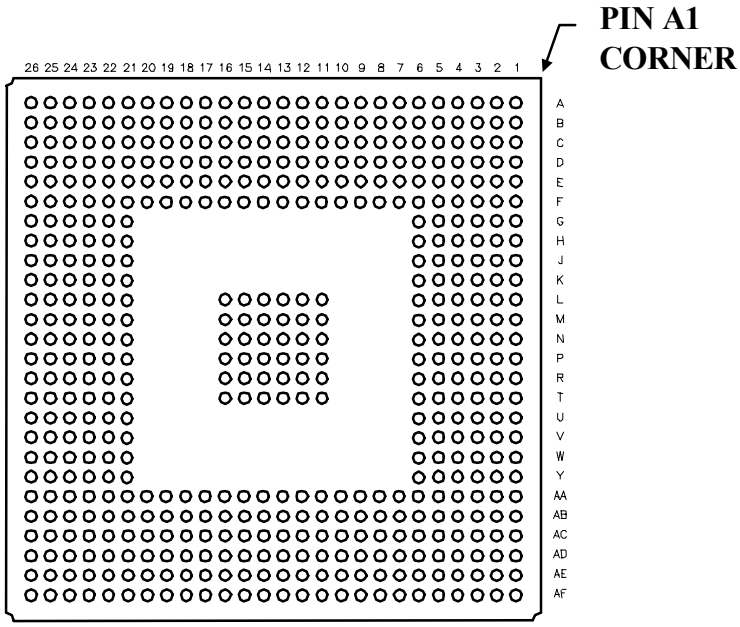


Bottom



12.0 516 PBGA Pinout Table

Table 19: 516 PBGA Pinout Table

516 PBGA	Function	516 PBGA	Function	516 PBGA	Function	516 PBGA	Function	516 PBGA	Function	516 PBGA	Function
A1	GND	C10	NC	E19	NC	J4	NC	N5	IO(G)	T16	GND
A2	IO(F)	C11	IO(F)	E20	IO(E)	J5	IO(G)	N6	GND	T21	VCC
A3	IO(F)	C12	NC	E21	NC	J6	VCCIO(G)	N11	GND	T22	VCC
A4	IO(F)	C13	CLK(7)	E22	NC	J21	VCCIO(D)	N12	GND	T23	NC
A5	NC	C14	IO(E)	E23	GNDPLL(1)	J22	IO(D)	N13	GND	T24	IO(C)
A6	IO(F)	C15	IO(E)	E24	IO(E)	J23	IO(D)	N14	GND	T25	NC
A7	IOCTRL(F)	C16	IO(E)	E25	IO(D)	J24	NC	N15	GND	T26	IO(C)
A8	IO(F)	C17	NC	E26	IO(D)	J25	IO(D)	N16	GND	U1	IO(H)
A9	IO(F)	C18	IO(E)	F1	IOCTRL(G)	J26	IO(D)	N21	GND	U2	IO(H)
A10	IO(F)	C19	IO(E)	F2	NC	K1	NC	N22	IO(D)	U3	NC
A11	NC	C20	IO(E)	F3	NC	K2	IO(G)	N23	IO(D)	U4	IO(H)
A12	IO(F)	C21	IO(E)	F4	NC	K3	IO(G)	N24	NC	U5	IO(H)
A13	IO(E)	C22	IO(E)	F5	IO(F)	K4	IO(G)	N25	IO(D)	U6	GND
A14	NC	C23	IO(E)	F6	GND	K5	NC	N26	IO(D)	U21	GND
A15	IO(E)	C24	IO(E)	F7	VCCIO(F)	K6	GND	P1	NC	U22	NC
A16	IO(E)	C25	IO(E)	F8	VCC	K21	GND	P2	IO(H)	U23	NC
A17	IO(E)	C26	IO(E)	F9	VCCIO(F)	K22	IO(D)	P3	IO(H)	U24	NC
A18	IOCTRL(E)	D1	IO(G)	F10	GND	K23	IO(D)	P4	VCC	U25	IO(C)
A19	IOCTRL(E)	D2	IO(G)	F11	VCC	K24	NC	P5	IO(H)	U26	IO(C)
A20	NC	D3	IO(F)	F12	VCCIO(F)	K25	NC	P6	VCCIO(H)	V1	IO(H)
A21	IO(E)	D4	NC	F13	GND	K26	NC	P11	GND	V2	IOCTRL(H)
A22	NC	D5	GNDPLL(0)	F14	VCCIO(E)	L1	IO(G)	P12	GND	V3	IOCTRL(H)
A23	IO(E)	D6	IO(F)	F15	VCC	L2	NC	P13	GND	V4	IO(H)
A24	IO(E)	D7	IO(F)	F16	VCC	L3	IO(G)	P14	GND	V5	NC
A25	PLLRST(1)	D8	NC	F17	GND	L4	IO(G)	P15	GND	V6	VCCIO(H)
A26	GND	D9	IO(F)	F18	VCCIO(E)	L5	VCC	P16	GND	V21	VCCIO(C)
B1	IO(F)	D10	IO(F)	F19	VCC	L6	VCC	P21	VCCIO(C)	V22	IO(C)
B2	PLLRST(0)	D11	IO(F)	F20	VCCIO(E)	L11	GND	P22	IO(C)	V23	NC
B3	IO(F)	D12	NC	F21	GND	L12	GND	P23	VCC	V24	IOCTRL(C)
B4	IO(F)	D13	TMS	F22	NC	L13	GND	P24	NC	V25	IO(C)
B5	IO(F)	D14	IO(E)	F23	NC	L14	GND	P25	NC	V26	IO(C)
B6	IO(F)	D15	IO(E)	F24	IO(D)	L15	GND	P26	TRSTB	W1	INREF(H)
B7	IOCTRL(F)	D16	NC	F25	NC	L16	GND	R1	NC	W2	IO(H)
B8	IO(F)	D17	IO(E)	F26	IO(D)	L21	VCC	R2	IO(H)	W3	NC
B9	IO(F)	D18	IO(F)	G1	NC	L22	IO(D)	R3	NC	W4	NC
B10	IO(F)	D19	CLK(8)	G2	INREF(G)	L23	IO(D)	R4	IO(H)	W5	VCC
B11	IO(F)	D20	IO(E)	G3	IO(G)	L24	NC	R5	VCC	W6	VCC
B12	IO(F)	D21	IO(E)	G4	IO(G)	L25	IO(D)	R6	VCC	W21	VCCIO(C)
B13	CLK(5),PLLIN(3)	D22	NC	G5	IO(G)	L26	IO(D)	R11	GND	W22	NC
B14	IO(E)	D23	VCCPLL(1)	G6	VCCIO(G)	M1	NC	R12	GND	W23	IO(C)
B15	IO(E)	D24	IO(E)	G21	VCCIO(D)	M2	NC	R13	GND	W24	IO(C)
B16	IO(E)	D25	IO(E)	G22	IO(D)	M3	NC	R14	GND	W25	INREF(C)
B17	IO(E)	D26	NC	G23	IO(D)	M4	NC	R15	GND	W26	IO(C)
B18	INREF(E)	E1	IO(G)	G24	NC	M5	IO(G)	R16	GND	Y1	IO(H)
B19	IO(E)	E2	IO(G)	G25	NC	M6	VCCIO(G)	R21	VCC	Y2	IO(H)
B20	NC	E3	NC	G26	INREF(D)	M11	GND	R22	IO(C)	Y3	NC
B21	IO(E)	E4	VCCPLL(0)	H1	NC	M12	GND	R23	NC	Y4	IO(H)
B22	IO(E)	E5	IO(F)	H2	IO(G)	M13	GND	R24	NC	Y5	IO(H)
B23	IO(E)	E6	IO(F)	H3	IOCTRL(G)	M14	GND	R25	NC	Y6	VCCIO(H)
B24	IO(E)	E7	IO(F)	H4	IO(G)	M15	GND	R26	IO(C)	Y21	VCCIO(C)
B25	IO(E)	E8	VCC	H5	IO(G)	M16	GND	T1	NC	Y22	NC
B26	PLLOUT(0)	E9	NC	H6	VCC	M21	VCCIO(D)	T2	IO(H)	Y23	IO(C)
C1	IO(F)	E10	IO(F)	H21	VCC	M22	VCC	T3	IO(H)	Y24	IO(C)
C2	NC	E11	IO(F)	H22	VCC	M23	NC	T4	IO(H)	Y25	NC
C3	IO(F)	E12	VCC	H23	IO(D)	M24	NC	T5	NC	Y26	IOCTRL(C)
C4	PLLOUT(3)	E13	IO(F)	H24	IOCTRL(D)	M25	IO(D)	T6	VCC	AA1	IO(H)
C5	IO(F)	E14	IO(F)	H25	IOCTRL(D)	M26	NC	T11	GND	AA2	IO(H)
C6	IO(F)	E15	IO(E)	H26	IO(D)	N1	TCK	T12	GND	AA3	NC
C7	IO(F)	E16	VCC	J1	NC	N2	NC	T13	GND	AA4	IO(A)
C8	INREF(F)	E17	CLK(6)	J2	IO(G)	N3	IO(G)	T14	GND	AA5	IO(A
C9	IO(F)	E18	IO(E)	J3	IO(G)	N4	IO(G)	T15	GND	AA6	GND

Table 19: 516 PBGA Pinout Table (Continued)

516 PBGA	Function	516 PBGA	Function	516 PBGA	Function	516 PBGA	Function	516 PBGA	Function	516 PBGA	Function
AA7	VCCIO(A)	AB6	NC	AC5	IO(A)	AD4	NC	AE3	IO(A)	AF2	IO(A)
AA8	VCC	AB7	NC	AC6	IO(A)	AD5	IO(A)	AE4	IO(A)	AF3	NC
AA9	VCCIO(A)	AB8	IO(A)	AC7	IO(A)	AD6	IO(A)	AE5	IO(A)	AF4	IO(A)
AA10	GND	AB9	IO(A)	AC8	IO(A)	AD7	IO(A)	AE6	IO(A)	AF5	IO(A)
AA11	VCC	AB10	IO(A)	AC9	IO(A)	AD8	IOCTRL(A)	AE7	INREF(A)	AF6	IOCTRL(A)
AA12	VCCIO(A)	AB11	VCC	AC10	NC	AD9	NC	AE8	NC	AF7	IO(A)
AA13	GND	AB12	IO(A)	AC11	IO(A)	AD10	IO(A)	AE9	IO(A)	AF8	IO(A)
AA14	VCCIO(B)	AB13	IO(A)	AC12	IO(A)	AD11	IO(A)	AE10	IO(A)	AF9	NC
AA15	VCC	AB14	CLK(3),PLLIN(1)	AC13	NC	AD12	TDI	AE11	IO(A)	AF10	IO(A)
AA16	VCC	AB15	VCC	AC14	CLK(1)	AD13	CLK(4), DEDCLK, PLLIN(0)	AE12	CLK(0)	AF11	IO(A)
AA17	GND	AB16	IO(B)	AC15	NC	AD14	IO(A)	AE13	IO(B)	AF12	CLK(2),PLLIN(2)
AA18	VCCIO(B)	AB17	NC	AC16	NC	AD15	NC	AE14	IO(B)	AF13	NC
AA19	VCC	AB18	IO(B)	AC17	IO(B)	AD16	IO(B)	AE15	NC	AF14	IO(B)
AA20	VCCIO(B)	AB19	VCC	AC18	IO(B)	AD17	NC	AE16	IO(B)	AF15	IO(B)
AA21	GND	AB20	NC	AC19	IO(B)	AD18	INREF(B)	AE17	IO(B)	AF16	IO(B)
AA22	VCCPLL(2)	AB21	IO(B)	AC20	IO(B)	AD19	IO(B)	AE18	IO(B)	AF17	IO(B)
AA23	IO(C)	AB22	GNDPLL(2)	AC21	IO(B)	AD20	IO(B)	AE19	IO(B)	AF18	IO(B)
AA24	IO(C)	AB23	IO(B)	AC22	TDO	AD21	IO(B)	AE20	IO(B)	AF19	IOCTRL(B)
AA25	IO(C)	AB24	IO(C)	AC23	PLLOUT(1)	AD22	IO(B)	AE21	IO(B)	AF20	IOCTRL(B)
AA26	NC	AB25	IO(C)	AC24	IO(B)	AD23	IO(B)	AE22	IO(B)	AF21	NC
AB1	IO(H)	AB26	IO(C)	AC25	NC	AD24	GND	AE23	IO(B)	AF22	IO(B)
AB2	NC	AC1	NC	AC26	IO(C)	AD25	IO(B)	AE24	IO(B)	AF23	IO(B)
AB3	IO(A)	AC2	IO(A)	AD1	IO(A)	AD26	IO(B)	AE25	PLLRST(2)	AF24	IO(B)
AB4	GNDPLL(3)	AC3	IO(A)	AD2	PLLOUT(2)	AE1	GND	AE26	IO(B)	AF25	IO(B)
AB5	VCCPLL(3)	AC4	IO(A)	AD3	PLLRST(3)	AE2	GND	AF1	IO(A)	AF26	IO(B)