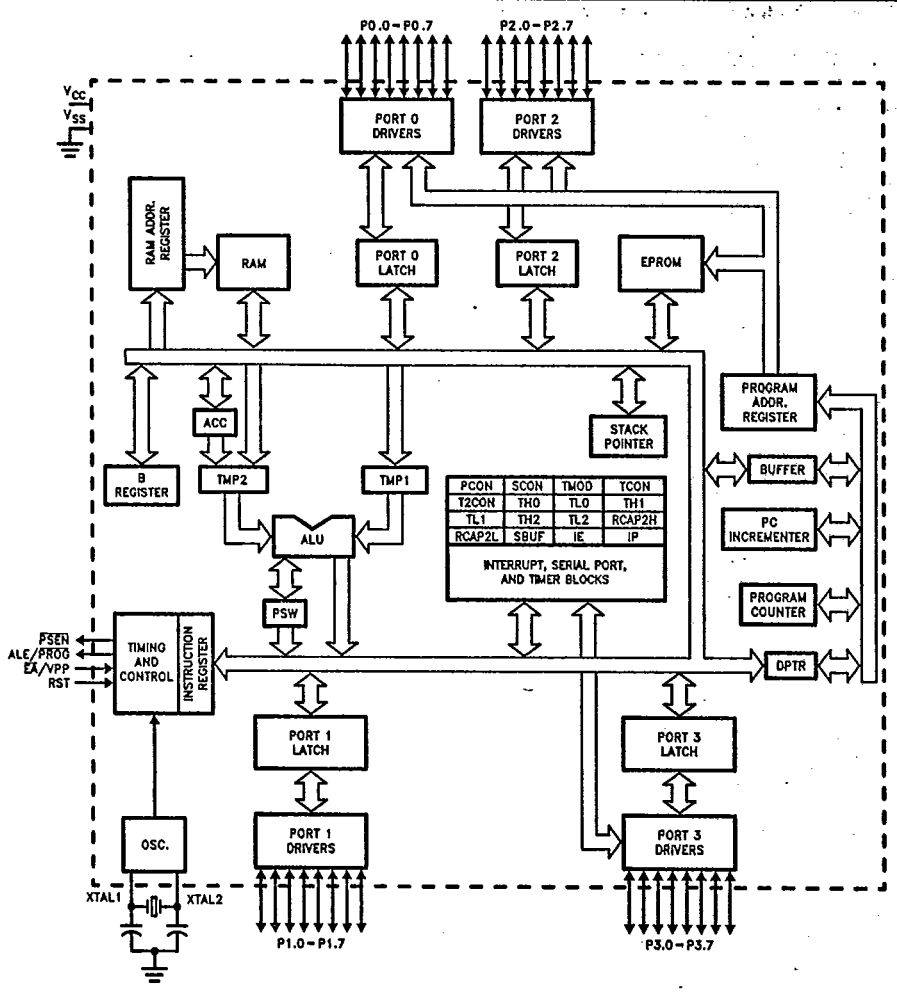
T-49-19-63

# 8752BH
# SINGLE-CHIP 8-BIT MICROCOMPUTER WITH 8K BYTES OF EPROM PROGRAM MEMORY

- 2-Bit Program Memory Lock
- 256 Bytes Data Ram
- Quick Pulse Programming™ Algorithm
- 12.75 Volt Programming Voltage
- Boolean Processor
- 32 Programmable I/O Lines
- Three 16-Bit Timer/Counters
- 6 Interrupt Sources
- Programmable Serial Channel
- Separate Transmit/Receive Baud Rate Capability
- 64K External Program Memory Space
- 64K External Data Memory Space




270429-1

**Figure 1. Block Diagram**



October 1990
Order Number: 270429-003

## PACKAGES

| Part | Prefix | Package Type |
|---|---|---|
| 8752BH | P | 40-Pin Plastic DIP |
| | D | 40-Pin CERDIP |
| | N | 44-Pin PLCC |

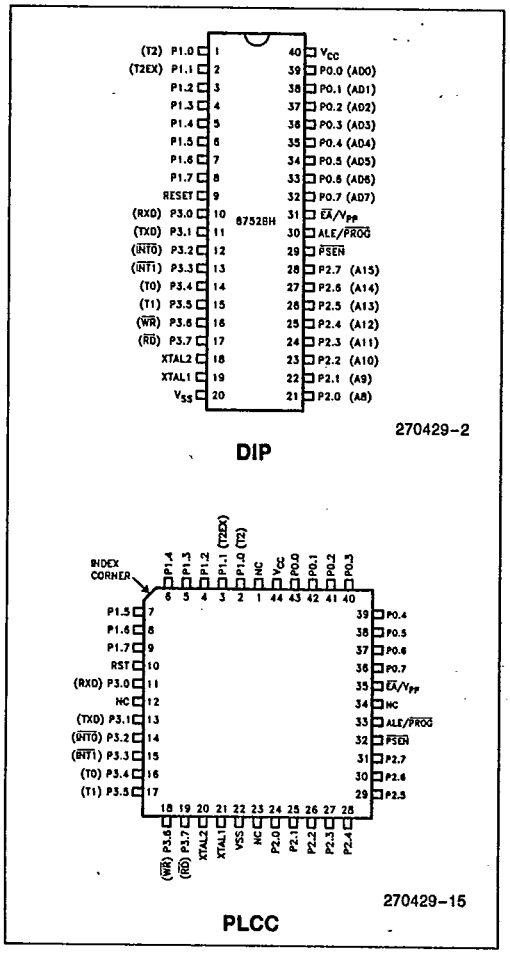



**Figure 2. Pin Connections**

## PIN DESCRIPTION

**$V_{CC}$:** Supply voltage.

**$V_{SS}$:** Circuit ground.

**Port 0:** Port 0 is an 8-bit open drain bidirectional I/O port. As an output port each pin can sink 8 LS TTL inputs. Port 0 pins that have 1s written to them float, and in that state can be used as high-impedance inputs.

Port 0 is also the multiplexed low-order address and data bus during accesses to external Program and Data Memory. In this application it uses strong internal pullups when emitting 1s, and can source and sink 8 LS TTL inputs.

Port 0 also receives the code bytes during EPROM programming, and outputs the code bytes during program verification. External pullups are required during program verification.

**Port 1:** Port 1 is an 8-bit bidirectional I/O port with internal pullups. The Port 1 output buffers can sink/source 4 LS TTL inputs. Port 1 pins that have 1s written to them are pulled high by the internal pullups, and in that state can be used as inputs. As inputs, Port 1 pins that are externally being pulled low will source current ($I_{IL}$, on the data sheet) because of the internal pullups.

Port 1 also receives the low-order address bytes during EPROM programming and program verification.

In addition, P1.0 and P1.1 serve the functions of the following special features of the MCS®-51 Family:

| Port Pin | Alternate Function |
|---|---|
| P1.0 | T2 (Timer/Counter 2 External Input) |
| P1.1 | T2EX (Timer/Counter 2 Capture/Reload Trigger) |

**Port 2:** Port 2 is an 8-bit bidirectional I/O port with internal pullups. The Port 2 output buffers can sink/source 4 LS TTL inputs. Port 2 pins that have 1s written to them are pulled high by the internal pullups, and in that state can be used as inputs. As inputs, Port 2 pins that are externally being pulled low will source current ($I_{IL}$, on the data sheet) because of the internal pullups.

Port 2 emits the high-order address byte during fetches from external Program Memory and during accesses to external Data Memory that use 16-bit addresses (MOVX @DPTR). In this application it uses strong internal pullups when emitting 1s. During accesses to external Data Memory that use 8-bit addresses (MOVX @Ri), Port 2 emits the contents of the P2 Special Function Register.

Port 2 also receives the high-order address bits during EPROM programming and program verification.

**Port 3:** Port 3 is an 8-bit bidirectional I/O port with internal pullups. The Port 3 output buffers can sink/source 4 LS TTL inputs. Port 3 pins that have 1s written to them are pulled high by the internal pullups, and in that state can be used as inputs. As inputs, Port 3 pins that are externally being pulled low will source current ($I_{IL}$, on the data sheet) because of the pullups.

Port 3 also serves the functions of various special features of the MCS®-51 Family, as listed below:

| Port Pin | Alternate Function |
|---|---|
| P3.0 | RXD (serial input port) |
| P3.1 | TXD (serial output port) |
| P3.2 | $\overline{INT0}$ (external interrupt 0) |
| P3.3 | $\overline{INT1}$ (external interrupt 1) |
| P3.4 | T0 (Timer 0 external input) |
| P3.5 | T1 (Timer 1 external input) |
| P3.6 | $\overline{WR}$ (external data memory write strobe) |
| P3.7 | $\overline{RD}$ (external data memory read strobe) |

**RST:** Reset input. A high on this pin for two machine cycles while the oscillator is running resets the device.

**ALE/$\overline{PROG}$:** Address Latch Enable output pulse for latching the low byte of the address during accesses to external memory. This pin is also the program pulse input (PROG) during EPROM programming on the 8752BH.

In normal operation ALE is emitted at a constant rate of 1/6 the oscillator frequency, and may be used for external timing or clocking purposes. Note, however, that one ALE pulse is skipped during each access to external Data Memory.

**$\overline{PSEN}$:** Program Store Enable is the Read strobe to External Program Memory.

When the device is executing code from external Program Memory, $\overline{PSEN}$ is activated twice each machine cycle, except that two $\overline{PSEN}$ activations are skipped during each access to External Data Memory.

**$\overline{EA}$/$V_{PP}$:** External Access enable. $\overline{EA}$ must be strapped to $V_{SS}$ in order to enable the device to fetch code from External Program Memory locations starting at 0000H up to FFFFH. Note, however, that if either of the Lock Bits are programmed, $\overline{EA}$ will be internally latched on reset.

$\overline{EA}$ should be strapped to $V_{CC}$ for internal program executions.

This pin also receives the 12.75V programming supply voltage ($V_{PP}$) during EPROM programming.

**XTAL1:** Input to the inverting oscillator amplifier.

**XTAL2:** Output from the inverting oscillator amplifier.

## OSCILLATOR CHARACTERISTICS

XTAL1 and XTAL2 are the input and output, respectively, of an inverting amplifier which can be configured for use as an on-chip oscillator, as shown in Figure 3. Either a quartz crystal or ceramic resonator may be used. More detailed information concerning the use of the on-chip oscillator is available in Applications Note AP-155, "Oscillators for Microcontrollers."

To drive the device from an external clock source, XTAL1 should be grounded, while XTAL2 is driven, as shown in Figure 4. There are no requirements on the duty cycle of the external clock signal, since the input to the internal clocking circuitry is through a divide-by-two flip-flop, but minimum and maximum high and low times specified on the Data Sheet must be observed.

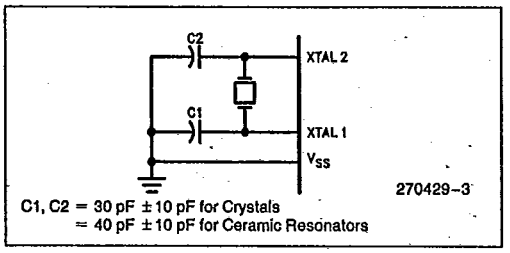



**Figure 3. Oscillator Connections**

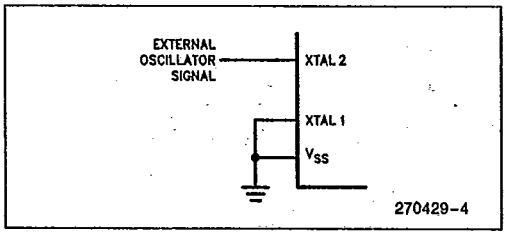



**Figure 4. External Clock Drive Configuration**

## DESIGN CONSIDERATIONS

Exposure to light when the 8752BH is in operation may cause logic errors. For this reason, it is suggested that an opaque label be placed over the window of the 8752BH when the die is exposed to ambient light.

Due to a timing problem in the Timer/Counter 2 interrupt circuitry, the device may vector to location 03H (External Interrupt 0 vector address). It happens when a low priority interrupt has been in progress for either 1 or 2 machine cycles and Timer/Counter 2 generates a priority 1 interrupt. Therefore, Timer/Counter 2 should only be assigned priority level 0.

If an 8752BH is replacing an 8751H in an existing design, the user should carefully compare both data sheets for DC or AC characteristic differences. Note that the $V_{IH}$ and $I_{IH}$ specifications for the EA pin differ significantly between the 8751H and 8752BH.

## ABSOLUTE MAXIMUM RATINGS*

Ambient Temperature Under Bias .....0°C to 70°C
Storage Temperature .....−65°C to +150°C
Voltage on $\overline{EA}$/$V_{PP}$ Pin to $V_{SS}$ ...−0.5V to +13.0V
Voltage on Any Other Pin to $V_{SS}$ ....−0.5V to +7V
Maximum $I_{OL}$ Per I/O Pin .....15 mA
Power Dissipation.....1.5W
(based on PACKAGE heat transfer limitations, not device power consumption)

NOTICE: This is a production data sheet. The specifications are subject to change without notice.

*WARNING: Stressing the device beyond the "Absolute Maximum Ratings" may cause permanent damage. These are stress ratings only. Operation beyond the "Operating Conditions" is not recommended and extended exposure beyond the "Operating Conditions" may affect device reliability.*

**Operating Conditions:** $T_A$ (under Bias) = 0°C to +70°C; $V_{CC}$ = 5V ±10%; $V_{SS}$ = 0V

## D.C. CHARACTERISTICS (Under Operating Conditions)

| Symbol | Parameter | Min | Max | Units | Test Conditions |
|---|---|---|---|---|---|
| $V_{IL}$ | Input Low Voltage (Except $\overline{EA}$) | −0.5 | 0.8 | V | |
| $V_{IL1}$ | Input Low Voltage $\overline{EA}$ | $V_{SS}$ | 0.7 | V | |
| $V_{IH}$ | Input High Voltage (Except XTAL2, RST, $\overline{EA}$) | 2.0 | $V_{CC}$+0.5 | V | |
| $V_{IH1}$ | Input High Voltage XTAL2, RST | 2.5 | $V_{CC}$+0.5 | V | XTAL1 = $V_{SS}$ |
| $V_{IH2}$ | Input High Voltage to $\overline{EA}$ | 4.5 | 5.5 | V | |
| $V_{OL}$ | Output Low Voltage (Note 3) (Ports 1, 2 and 3) | | 0.45 | V | $I_{OL}$ = 1.6 mA (Note 1) |
| $V_{OL1}$ | Output Low Voltage (Note 3) (Port 0, ALE/$\overline{PROG}$, $\overline{PSEN}$) | | 0.45 | V | $I_{OL}$ = 3.2 mA (Note 1, 2) |
| $V_{OH}$ | Output High Voltage (Ports 1, 2, 3, ALE/$\overline{PROG}$ and $\overline{PSEN}$) | 2.4 | | V | $I_{OH}$ = −80 µA |
| $V_{OH1}$ | Output High Voltage (Port 0 in External Bus Mode) | 2.4 | | V | $I_{OH}$ = −400 µA |
| $I_{IL}$ | Logical 0 Input Current (Ports 1, 2, 3 and RST) | | −500 | µA | $V_{IN}$ = 0.45V |
| $I_{IL1}$ | Logical 0 Input Current ($\overline{EA}$) | −10 | 500 | mA µA | $V_{IN}$ = $V_{SS}$ |
| $I_{IL2}$ | Logical 0 Input Current (XTAL2) | | −3.2 | mA | $V_{IN}$ = 0.45V XTAL1 = $V_{SS}$ |
| $I_{LI}$ | Input Leakage Current (Port 0) | | ±10 | µA | 0.45 < $V_{IN}$ < $V_{CC}$ |
| $I_{IH}$ | Logical 1 Input Current ($\overline{EA}$) | | 1 | mA | 4.5V < $V_{IN}$ < 5.5V |
| $I_{IH1}$ | Input Current to RST to activate Reset | | 500 | µA | $V_{IN}$ < ($V_{CC}$ − 1.5V) |
| $I_{CC}$ | Power Supply Current | | 175 | mA | All Outputs Disconnected |
| $C_{IO}$ | Pin Capacitance | | 10 | pF | Test freq = 1 MHz |

**NOTES:**
1. Capacitive loading on Ports 0 and 2 may cause spurious noise pulses to be superimposed on the $V_{OL}$s of ALE/$\overline{PROG}$ and Ports 1 and 3. The noise is due to external bus capacitance discharging into the Port 0 and Port 2 pins when these pins make 1-to-0 transitions during bus operations. In the worst cases (capacitive loading > 100 pF), the noise pulse on the ALE/$\overline{PROG}$ pin may exceed 0.8V. In such cases it may be desirable to qualify ALE with a Schmitt Trigger, or use an address latch with a Schmitt Trigger STROBE input.
2. ALE/$\overline{PROG}$ refers to a pin on the device. ALE refers to a timing signal that is output on the ALE/$\overline{PROG}$ pin.
3. Under steady state (non-transient) conditions, $I_{OL}$ must be externally limited as follows:
   Maximum $I_{OL}$ per port pin: 10 mA
   Maximum $I_{OL}$ per 8-bit port-
   Port 0: 26 mA
   Ports 1, 2, and 3: 15 mA
   Maximum total $I_{OL}$ for all output pins: 71 mA
   If $I_{OL}$ exceeds the test condition, $V_{OL}$ may exceed the related specification. Pins are not guaranteed to sink current greater than the listed test conditions.

## EXPLANATION OF THE AC SYMBOLS

Each timing symbol has 5 characters. The first character is always a 'T' (stands for time). The other characters, depending on their positions, stand for the name of a signal or the logical status of that signal. The following is a list of all the characters and what they stand for.

A:Address
C:Clock
D:Input Data
H:Logic level HIGH
I:Instruction (program memory contents)
L:Logic level LOW, or ALE
P:$\overline{\text{PSEN}}$
Q:Output data
R:$\overline{\text{RD}}$ signal
T:Time
V:Valid
W:$\overline{\text{WR}}$ signal
X:No longer a valid logic level
Z:Float

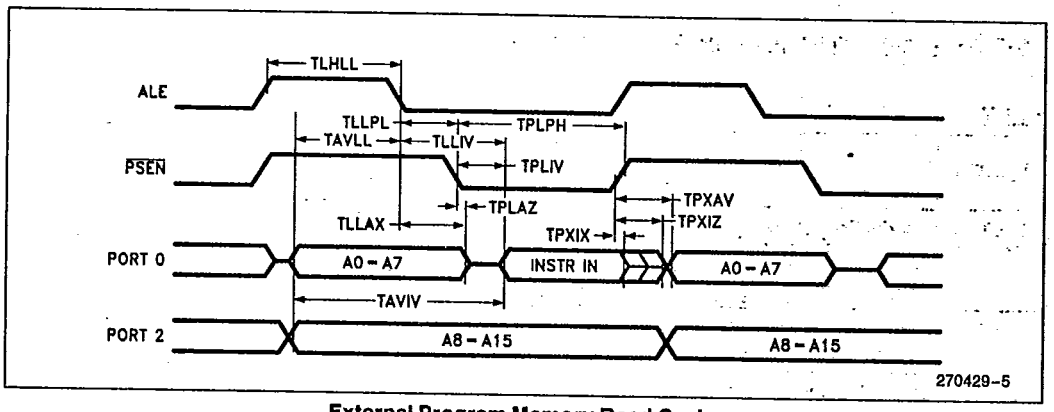
For example,

TAVLL = Time from Address Valid to ALE Low.
TLLPL = Time from ALE Low to PSEN Low.

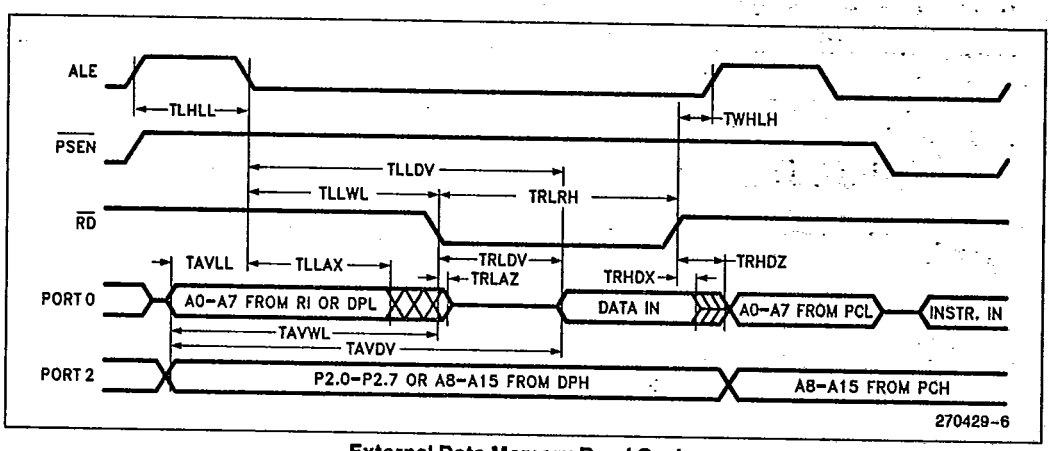
**A.C. CHARACTERISTICS** (Under Operating Conditions; Load Capacitance for Port 0, ALE/$\overline{\text{PROG}}$, and $\overline{\text{PSEN}}$ = 100 pF; Load Capacitance for All Other Outputs = 80 pF)

## EXTERNAL PROGRAM MEMORY CHARACTERISTICS

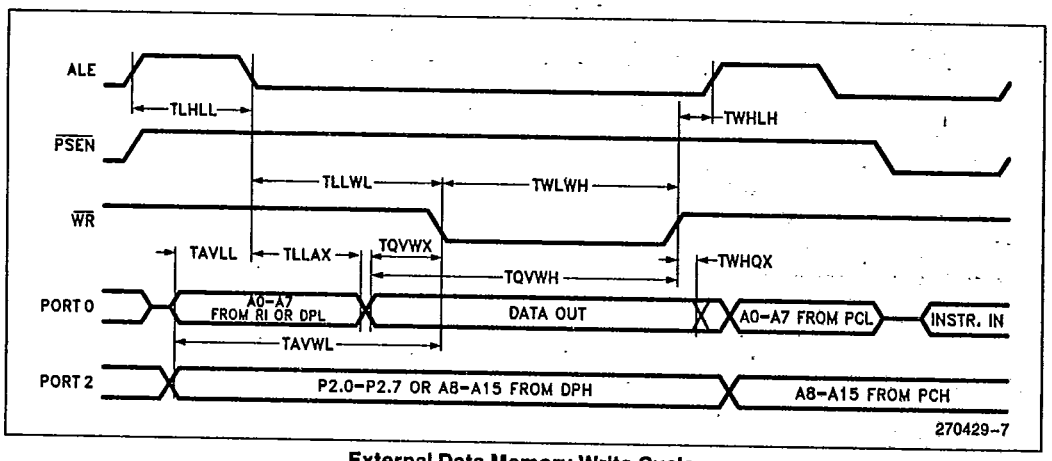
| Symbol | Parameter | 12 MHz Osc | | Variable Oscillator | | Units |
|---|---|---|---|---|---|---|
| | | Min | Max | Min | Max | |
| 1/TCLCL | Oscillator Frequency | | | 3.5 | 12.0 | MHz |
| TLHLL | ALE Pulse Width | 127 | | 2TCLCL−40 | | ns |
| TAVLL | Address Valid to ALE Low | 43 | | TCLCL−40 | | ns |
| TLLAX | Address Hold After ALE Low | 48 | | TCLCL−35 | | ns |
| TLLIV | ALE Low to Valid Instruction In | | 233 | | 4TCLCL−100 | ns |
| TLLPL | ALE Low to $\overline{\text{PSEN}}$ Low | 58 | | TCLCL−25 | | ns |
| TPLPH | $\overline{\text{PSEN}}$ Pulse Width | 215 | | 3TCLCL−35 | | ns |
| TPLIV | $\overline{\text{PSEN}}$ Low to Valid Instruction In | | 125 | | 3TCLCL−125 | ns |
| TPXIX | Input Instr Hold After $\overline{\text{PSEN}}$ | 0 | | 0 | | ns |
| TPXIZ | Input Instr Float After $\overline{\text{PSEN}}$ | | 63 | | TCLCL−20 | ns |
| TPXAV | $\overline{\text{PSEN}}$ to Address Valid | 75 | | TCLCL−8 | | ns |
| TAVIV | Address to Valid Instruction In | | 302 | | 5TCLCL−115 | ns |
| TPLAZ | $\overline{\text{PSEN}}$ Low to Address Float | | 20 | | 20 | ns |
| TRLRH | $\overline{\text{RD}}$ Pulse Width | 400 | | 6TCLCL−100 | | ns |
| TWLWH | $\overline{\text{WR}}$ Pulse Width | 400 | | 6TCLCL−100 | | ns |
| TRLDV | $\overline{\text{RD}}$ Low to Valid Data In | | 252 | | 5TCLCL−165 | ns |
| TRHDX | Data Hold After $\overline{\text{RD}}$ | 0 | | 0 | | ns |
| TRHDZ | Data Float After $\overline{\text{RD}}$ | | 97 | | 2TCLCL−70 | ns |
| TLLDV | ALE Low to Valid Data In | | 517 | | 8TCLCL−150 | ns |
| TAVDV | Address to Valid Data In | | 585 | | 9TCLCL−165 | ns |
| TLLWL | ALE Low to $\overline{\text{RD}}$ or $\overline{\text{WR}}$ Low | 200 | 300 | 3TCLCL−50 | 3TCLCL+50 | ns |
| TAVWL | Address to $\overline{\text{RD}}$ or $\overline{\text{WR}}$ Low | 203 | | 4TCLCL−130 | | ns |
| TQVWX | Data Valid to $\overline{\text{WR}}$ Transition | 23 | | TCLCL−60 | | ns |
| TQVWH | Data Valid to $\overline{\text{WR}}$ High | 433 | | 7TCLCL−150 | | ns |
| TWHQX | Data Held After $\overline{\text{WR}}$ | 33 | | TCLCL−50 | | ns |
| TRLAZ | $\overline{\text{RD}}$ Low to Address Float | | 0 | | 0 | ns |
| TWHLH | $\overline{\text{RD}}$ or $\overline{\text{WR}}$ High to ALE High | 43 | 123 | TCLCL−40 | TCLCL+40 | ns |




**External Program Memory Read Cycle**




**External Data Memory Read Cycle**

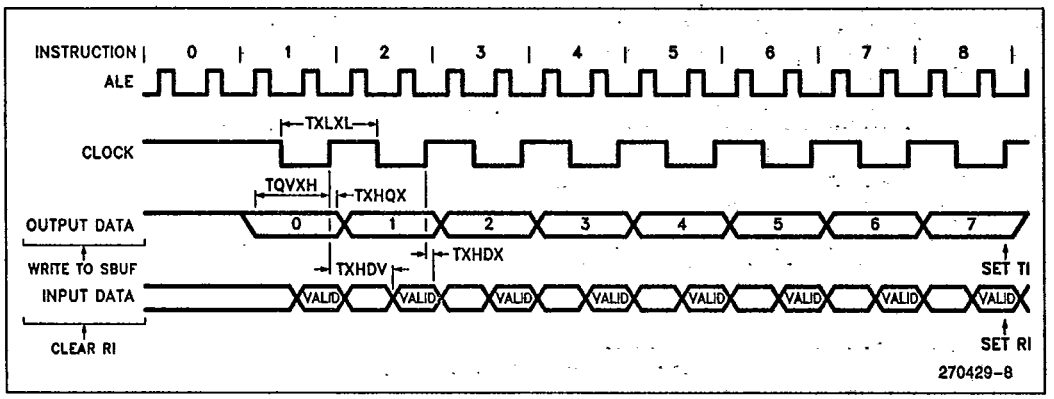



**External Data Memory Write Cycle**

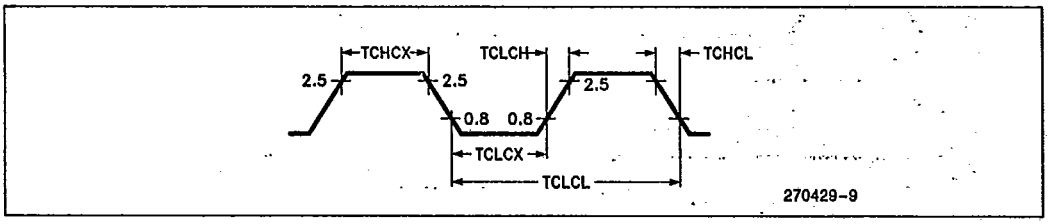
## SERIAL PORT TIMING—SHIFT REGISTER MODE

**TEST CONDITIONS** $T_A$ = 0°C to +70°C; $V_{CC}$ = 5V ±10%; $V_{SS}$ = 0V; Load Capacitance = 80 pF

| Symbol | Parameter | 12 MHz Osc | | Variable Oscillator | | Units |
|---|---|---|---|---|---|---|
| | | Min | Max | Min | Max | |
| TXLXL | Serial Port Clock Cycle Time | 1.0 | | 12TCLCL | | μs |
| TQVXH | Output Data Setup to Clock Rising Edge | 700 | | 10TCLCL−133 | | ns |
| TXHQX | Output Data Hold After Clock Rising Edge | 50 | | 2TCLCL−117 | | ns |
| TXHDX | Input Data Hold After Clock Rising Edge | 0 | | 0 | | ns |
| TXHDV | Clock Rising Edge to Input Data Valid | | 700 | | 10TCLCL−133 | ns |




**Shift Register Mode Timing Waveforms**

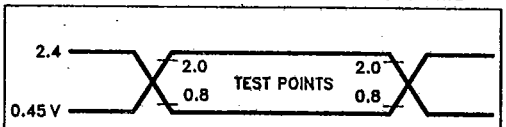



**External Clock Drive Waveforms**

## EXTERNAL CLOCK DRIVE

| Symbol | Parameter | Min | Max | Units |
|---|---|---|---|---|
| 1/TCLCL | Oscillator Frequency | 3.5 | 12 | MHz |
| TCHCX | High Time | 20 | | ns |
| TCLCX | Low Time | 20 | | ns |
| TCLCH | Rise Time | | 20 | ns |
| TCHCL | Fall Time | | 20 | ns |

## A.C. TESTING INPUT/OUTPUT WAVEFORMS

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AC inputs during testing are driven at 2.4V for a logic "1" and 0.45V for a logic "0". Timing measurements are made at 2.0V for a logic "1" and 0.8V for a logic "0".

## EPROM CHARACTERISTICS

Table 1 shows the logic levels for programming the Program Memory, the Encryption Table, and the Lock Bits and for reading the signature bytes.

### Programming the EPROM

To be programmed, the 8752BH must be running with a 4 to 6 MHz oscillator. (The reason the oscillator needs to be running is that the internal bus is being used to transfer address and program data to appropriate internal registers.) The address of an EPROM location to be programmed is applied to Port 1 and pins P2.0 - P2.4 of Port 2, while the code byte to be programmed into that location is applied to Port 0. The other Port 2 and 3 pins, and RST, $\overline{PSEN}$, and $\overline{EA}/V_{PP}$ should be held at the "Program" levels indicated in Table 1. ALE/$\overline{PROG}$ is pulsed low to program the code byte into the addressed EPROM location. The setup is shown in Figure 5.

Normally $\overline{EA}/V_{PP}$ is held at a logic high until just before ALE/$\overline{PROG}$ is to be pulsed. Then $\overline{EA}/V_{PP}$ is raised to $V_{PP}$, ALE/$\overline{PROG}$ is pulsed low, and then $\overline{EA}/V_{PP}$ is returned to a valid high voltage. The voltage on the $\overline{EA}/V_{PP}$ pin must be at the valid $\overline{EA}/V_{PP}$ high level before a verify is attempted. Waveforms and detailed timing specifications are shown in later sections of this data sheet.

Note that the $\overline{EA}/V_{PP}$ pin must not be allowed to go above the maximum specified $V_{PP}$ level for any amount of time. Even a narrow glitch above that voltage level can cause permanent damage to the device. The $V_{PP}$ source should be well regulated and free of glitches.

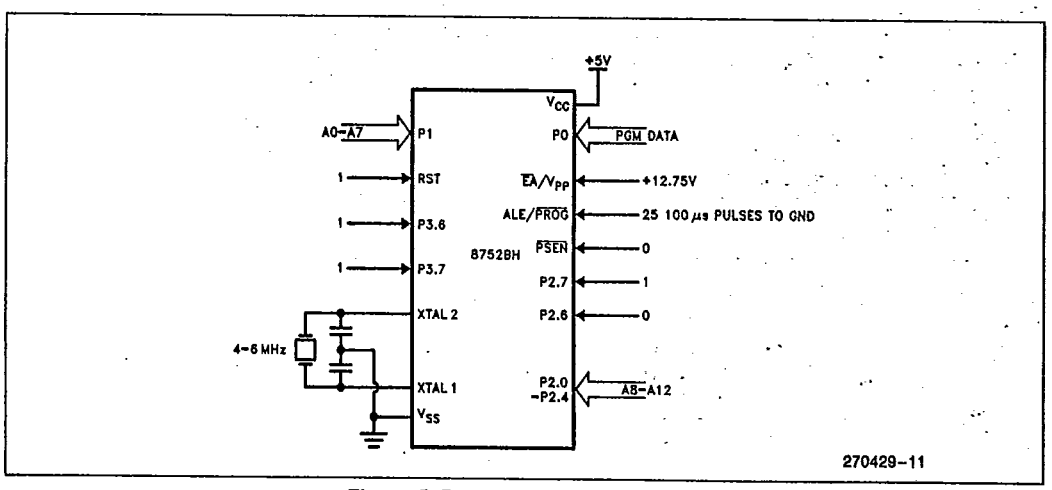


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**Figure 5. Programming the EPROM**

**Table 1. EPROM Programming Modes**

| MODE | RST | $\overline{PSEN}$ | ALE/$\overline{PROG}$ | $\overline{EA}$/$V_{PP}$ | P2.7 | P2.6 | P3.6 | P3.7 |
|---|---|---|---|---|---|---|---|---|
| Program Code Data | 1 | 0 | 0* | $V_{PP}$ | 1 | 0 | 1 | 1 |
| Verify Code Data | 1 | 0 | 1 | 1 | 0 | 0 | 1 | 1 |
| Program Encryption Table Use Addresses 0-1FH | 1 | 0 | 0* | $V_{PP}$ | 1 | 0 | 0 | 1 |
| Program Lock x=1 | 1 | 0 | 0* | $V_{PP}$ | 1 | 1 | 1 | 1 |
| Bits (LBx) x=2 | 1 | 0 | 0* | $V_{PP}$ | 1 | 1 | 0 | 0 |
| Read Signature | 1 | 0 | 1 | 1 | 0 | 0 | 0 | 0 |

**NOTES:**
"1" = Valid high for that pin
"0" = Valid low for that pin
"$V_{PP}$" = +12.75V ±0.25V
*ALE/$\overline{PROG}$ is pulsed low for 100 uS for programming. (Quick-Pulse Programming™)

## QUICK-PULSE PROGRAMMING™ ALGORITHM

The 8752BH can be programmed using the Quick-Pulse Programming™ Algorithm for microcontrollers. The features of the new programming method are a lower $V_{PP}$ (12.75 volts as compared to 21 volts) and a shorter programming pulse. It is possible to program the entire 8K Bytes of EPROM memory in less than 25 seconds with this algorithm!

To program the part using the new algorithm, $V_{PP}$ must be 12.75 ±0.25 Volts. ALE/$\overline{PROG}$ is pulsed low for 100 μseconds, 25 times as shown in Figure 6. Then, the byte just programmed may be verified. After programming, the entire array should be verified. The Program Lock features are programmed using the same method, but with the setup as shown in Table 1. The only difference in programming Lock features is that the Lock features cannot be directly verified. Instead, verification of programming is by observing that their features are enabled.

## PROGRAM VERIFICATION

If the Lock Bits have not been programmed, the on-chip Program Memory can be read out for verification purposes, if desired, either during or after the programming operation. The address of the Program Memory location to be read is applied to Port 1 and pins P2.0 - P2.4. The other pins should be held at the "Verify" levels indicated in Table 1. The contents of the addressed location will come out on Port 0. External pullups are required on Port 0 for this operation. (If the Encryption Array in the EPROM has been programmed, the data present at Port 0 will be Code Data XNOR Encryption Data. The user must know the Encryption Array contents to manually "unencrypt" the data during verify.)

The setup, which is shown in Figure 7, is the same as for programming the EPROM except that pin P2.7 is held at a logic low, or may be used as an active low read strobe.

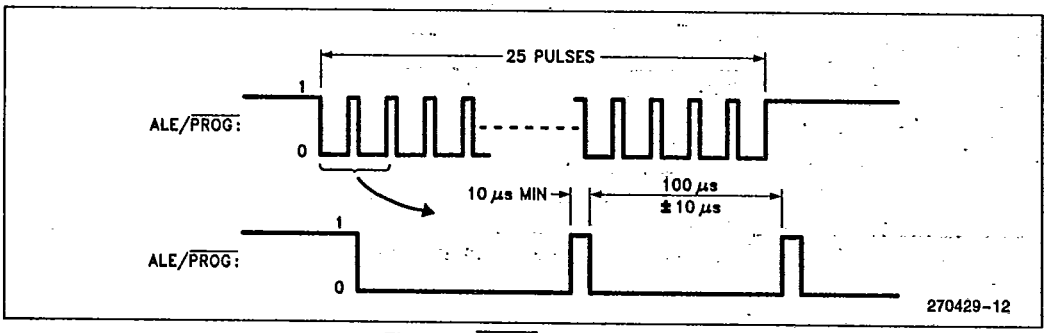



**Figure 6. $\overline{PROG}$ Waveforms**

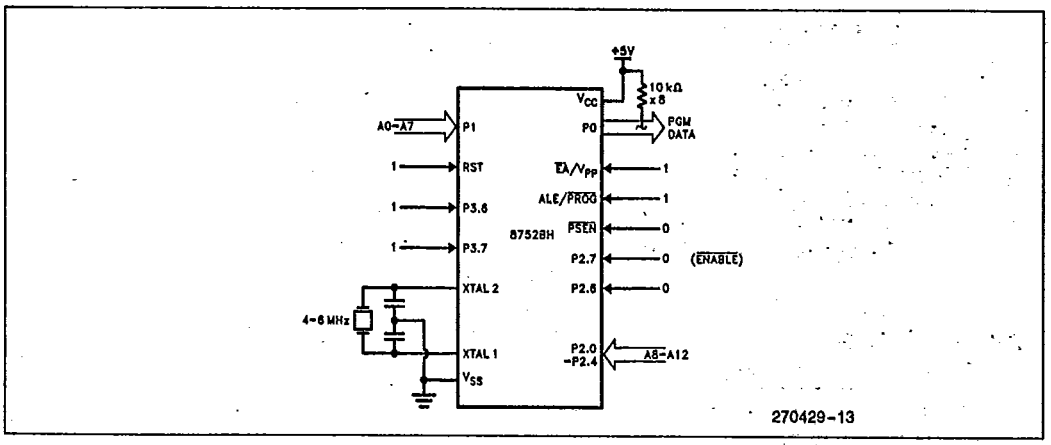



**Figure 7. Verifying the EPROM**

## PROGRAM MEMORY LOCK

The two-level Program Lock system consists of 2 Lock bits and a 32-byte Encryption Array which are used to protect the program memory against software piracy.

## ENCRYPTION ARRAY

Within the EPROM array are 32 bytes of Encryption Array that are initially unprogrammed (all 1s). Every time that a byte is addressed during a verify, 5 address lines are used to select a byte of the Encryption Array. This byte is then exclusive-NORed (XNOR) with the code byte, creating an Encrypted Verify byte. The algorithm, with the array in the unprogrammed state (all 1s), will return the code in its original, unmodified form.

It is recommended that whenever the Encryption Array is used, at least one of the Lock Bits be programmed as well.

## LOCK BITS

Also included in the EPROM Program Lock scheme are two Lock Bits which function as shown in Table 2.

Erasing the EPROM also erases the Encryption Array and the Lock Bits, returning the part to full unlocked functionality.

To ensure proper functionality of the chip, the internally latched value of the $\overline{EA}$ pin must agree with its external state.

**Table 2. Lock Bits and their Features**

| Lock Bits | | Logic Enabled |
|---|---|---|
| LB1 | LB2 | |
| U | U | Minimum Program Lock features enabled. (Code Verify will still be encrypted by the Encryption Array) |
| P | U | MOVC instructions executed from external program memory are disabled from fetching code bytes from internal memory, $\overline{EA}$ is sampled and latched on reset, and further programming of the EPROM is disabled |
| P | P | Same as above, but Verify is also disabled |
| U | P | Reserved for Future Definition |

P = Programmed
U = Unprogrammed

## READING THE SIGNATURE BYTES

The signature bytes are read by the same procedure as a normal verification of locations 030H and 031H, except that P3.6 and P3.7 need to be pulled to a logic low. The values returned are:

(030H) = 89H indicates manufactured by Intel
(031H) = 52H indicates 8752BH

## ERASURE CHARACTERISTICS

Erasure of the EPROM begins to occur when the 8752BH is exposed to light with wavelengths shorter than approximately 4,000 Angstroms. Since sunlight and fluorescent lighting have wavelengths in this range, exposure to these light sources over an extended time (about 1 week in sunlight, or 3 years in room-level fluorescent lighting) could cause inadvertent erasure. If an application subjects the device to this type of exposure, it is suggested that an opaque label be placed over the window.

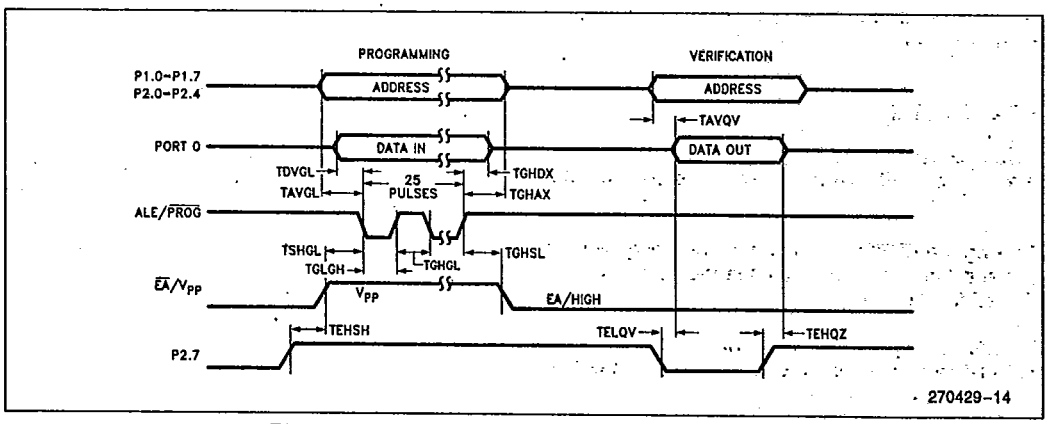
The recommended erasure procedure is exposure to ultraviolet light (at 2537 Angstroms) to an integrated dose of at lease 15 W-sec/cm. Exposing the EPROM to an ultraviolet lamp of 12,000 μW/cm rating for 30 minutes, at a distance of about 1 inch, should be sufficient.

Erasure leaves the array in an all 1s state.

## EPROM PROGRAMMING AND VERIFICATION CHARACTERISTICS

($T_A$ = 21°C to 27°C, $V_{CC}$ = 5.0V ±10%, $V_{SS}$ = 0V)

| Symbol | Parameter | Min | Max | Units |
|---|---|---|---|---|
| $V_{PP}$ | Programming Supply Voltage | 12.5 | 13.0 | V |
| $I_{PP}$ | Programming Supply Current | | 50 | mA |
| 1/TCLCL | Oscillator Frequency | 4 | 6 | MHz |
| TAVGL | Address Setup to $\overline{PROG}$ Low | 48TCLCL | | |
| TGHAX | Address Hold After $\overline{PROG}$ | 48TCLCL | | |
| TDVGL | Data Setup to $\overline{PROG}$ Low | 48TCLCL | | |
| TGHDX | Data Hold After $\overline{PROG}$ | 48TCLCL | | |
| TEHSH | P2.7 ($\overline{ENABLE}$) High to $V_{PP}$ | 48TCLCL | | |
| TSHGL | $V_{PP}$ Setup to $\overline{PROG}$ Low | 10 | | μs |
| TGHSL | $V_{PP}$ Hold After $\overline{PROG}$ | 10 | | μs |
| TGLGH | $\overline{PROG}$ Width | 90 | 110 | μs |
| TAVQV | Address to Data Valid | | 48TCLCL | |
| TELQV | $\overline{ENABLE}$ Low to Data Valid | | 48TCLCL | |
| TEHQZ | Data Float After $\overline{ENABLE}$ | 0 | 48TCLCL | |
| TGHGL | $\overline{PROG}$ High to $\overline{PROG}$ Low | 10 | | μs |




**EPROM Programming and Verification Waveforms**

## DATA SHEET REVISION HISTORY

The following are the key differences between this and the -002 version of the 8752BH data sheet.

1. Data sheet status changed from "Preliminary" to "Production".
2. Deleted LCC Package offering.
3. Revised Maximum Ratings warning and data sheet status notice.

The following are the key differences between this and the -001 version of the 8752BH data sheet.

1. PLCC pin connection diagram was added.
2. Package table was added.
3. Timer/Counter 2 Design Consideration was added.
4. Design Consideration was added referring to previous designs using the 8751H.
5. Note 3 was added to DC Characteristics to explain the maximum current specification.
6. Signature Byte was corrected.
7. Data Sheet Revision History was added.

intel

PRELIMINARY

T-49-19-63

# 8752BH

*EXPRESS*

■ **Extended Temperature Range** ■ **Burn-In**

The Intel EXPRESS system offers enhancements to the operational specifications of the MCS®-51 family of microcontrollers. These EXPRESS products are designed to meet the needs of those applications whose operating requirements exceed commercial standards.

The EXPRESS program includes the commercial standard temperature range with burn-in, and an extended temperature range with or without burn-in.

With the commercial standard temperature range operational characteristics are guaranteed over the temperature range of 0°C to 70°C. With the extended temperature range option, operational characteristics are guaranteed over the range of −40°C to +85°C.

The optional burn-in is dynamic, for a minimum time of 160 hours at 125°C with $V_{CC}$ = 5.5V ±0.25V, following guidelines in MIL-STD-883, Method 1015.

Package types and EXPRESS versions are identified by a one- or two-letter prefix to the part number. The prefixes are listed in Table 1.

For the extended temperature range option, this data sheet specifies the parameters which deviate from their commercial temperature range limits. The commercial temperature range data sheets are applicable for all parameters not listed here.

## Electrical Deviations from Commercial Specifications for Extended Temperature Range

D.C. and A.C. parameters not included here are the same as in the commercial temperature range data sheets.

## D.C. CHARACTERISTICS $T_A$ = −40°C to +85°C; $V_{CC}$ = 5V ±10%; $V_{SS}$ = 0V

| Symbol | Parameter | Min | Max | Unit | Test Conditions |
|---|---|---|---|---|---|
| $V_{IH}$ | Input High Voltage (Except XTAL2, RST, $\overline{EA}$) | 2.1 | $V_{CC}$ + 0.5 | V | |



January 1989
Order Number: 270650-002

**Table 1. Prefix Identification**

| Prefix | Package Type | Temperature Range | Burn-In |
|---|---|---|---|
| P | plastic | commercial | no |
| D | cerdip | commercial | no |
| N | PLCC | commercial | no |
| R | LCC | commercial | no |
| TD | cerdip | extended | no |
| QP | plastic | commercial | yes |
| LD | cerdip | extended | yes |

Please note:

- Commercial temperature range is 0°C to 70°C. Extended temperature range is −40°C to +85°C.
- Burn-in is dynamic, for a minimum time of 160 hours at 125°C, $V_{CC}$ = 5,5V ±0.25V, following guidelines in MIL-STD-883 Method 1015 (Test Condition D).

Examples: N8752BH indicates 8752BH in a PLCC package and specified for commercial temperature range, without burn-in. LD8752BH indicates 8752BH in a cerdip package and specified for extended temperature range with burn-in.

## DATA SHEET REVISION SUMMARY

The following are the key differences between this and the -001 version of the 8752BH Express data sheet:

1. $V_{IH}$ parameter changed to read "(Except XTAL2, RST, $\overline{EA}$)".
2. QD option removed.
3. Data Sheet Revision Summary added.