8101
Gigabit Ethernet Controller

99110

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Features

- ***Pin Compatible Upgrade of Seeq 8100***
- ***Combined Ethernet MAC and 8B10B PCS***
- ***Data Rate - 1000 Mbps***
- ***64-Bit @ 66 Mhz Interface to External Bus - 4 Gbps Bandwidth***
- ***10-Bit Interface to External PHY or SerDes Chip***
- ***16-Bit Interface to Internal Registers and Management Counters***
- ***Full RMON, SNMP, Ethernet Management Counter Support***
- ***Independent Receive and Transmit FIFO's with Programmable Watermarks***
  - ***Receive FIFO Size - 16K Bytes***
  - ***Transmit FIFO Size - 4K Bytes***
- ***AutoNegotiation Algorithm On Chip***
- ***Full Duplex Only***
- ***Flow Control per IEEE 802.3x***
- ***Automatic CRC Generation and Checking***
- ***Automatic Packet Error Discarding***
- ***Programmable Transmit Start Threshold***
- ***Interrupt Capability***
- ***Supports Fiber and Short Haul Copper Media***
- ***3.3v Power Supply, 5v Tolerant Inputs***
- ***Meets all applicable IEEE 802.3 and 802.3z Specifications***
- ***208L PQFP***

Description

The 8101 is a Ethernet controller for gigabit applications. The 8101 integrates the Media Access Control sublayer (MAC) and the Physical Coding Sublayer (PCS) for fiber and short haul copper media.

The 8101 is an improved version of the Seeq 8100. The 8101 is also pin compatible with the 8100 with the exception that the 8101 is powered from a 3.3V supply voltage. All inputs and outputs on the 8101 are 5V tolerant.

The 8101 consists of a full duplex Ethernet MAC, receive/transmit FIFO's, 32-bit System Interface, 8B10B encoder/decoder, 10-bit PHY Interface, and a 16-bit Register Interface.

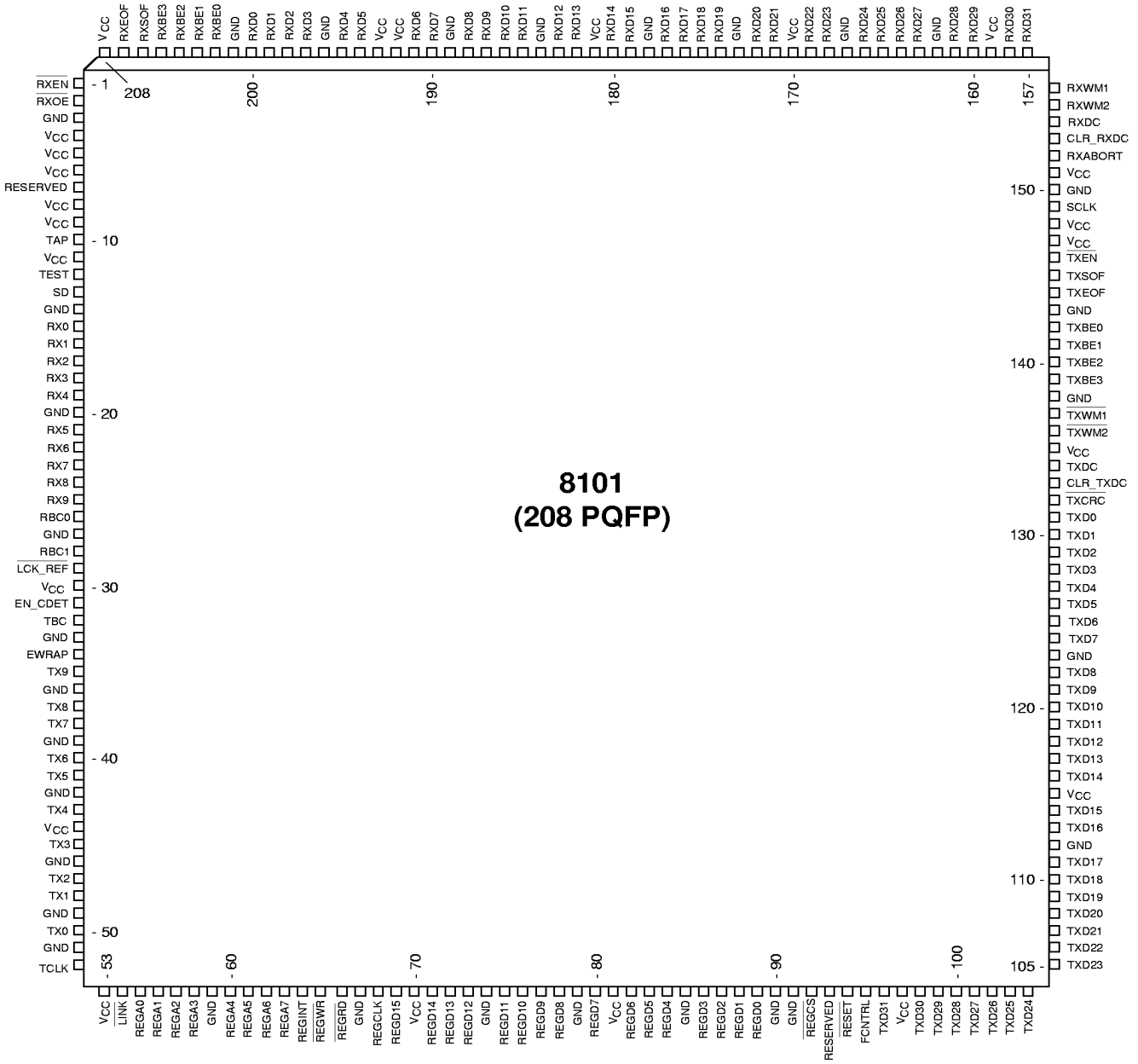
The 8101 also contains all the necessary circuitry to implement the flow control algorithm defined by IEEE 802.3x. Flow control messages can be sent automatically without any host intervention.

The 8101 contains 53 counters that completely satisfies the management objectives of the RMON Statistics Group MIB, (RFC 1757), SNMP Interfaces Group MIB (RFC 1213 & 1573), Ethernet-Like Group MIB (RFC 1643) and Ethernet MIB (IEEE 802.3z Clause 30).

The 8101 contains one hundred thirty six internal 16-bit registers that can be accessed though the Register Interface. These registers contain configuration inputs, status outputs, and management counter results.

The 8101 is ideal as an Ethernet controller for Gigabit Ethernet switch ports, uplinks, backbones, and adapter cards

Pin Configuration



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1.0 Pin Description

Pin #	Pin Name	I/O	Description
Power Supplies			
4 5 6 8 9 11 30 44 53 70 81 97 115 135 147 148 151 159 170 181 192 193 208	VCC[22:0]	—	**Positive Supply.** +3.3v +/-5% Volts.
3 14 20 27 33 36 39 42 46 49 51 59 67 74 79 85 90 91 112 123 138 143 150 162 167 173 178 184 189 196 201	GND[30:0]	—	**Ground.** 0 Volts.
10-Bit PHY Interface			
32	TBC	O	**Transmit Clock Output.** This 10-Bit PHY Interface output clocks transmit data out on TX[0:9] on rising edges. TBC is a 125 MHZ clock and is generated from TCLK.
50 48 47 45 43 41 40 38 37 35	TX[0:9]	O	**Transmit Data Output.** These 10-Bit PHY Interface outputs contain transmit data which are clocked out on rising edges of TBC.
28 26	RBC[1:0]	I	**Receive Clock Input.** These 10-Bit PHY Interface inputs clock in receive data on RX[0:9] on rising edges. RBC[1:0] are 62.5 MHZ clocks, 180° out of phase, used to clock in data on RX[0:9] at an effective 125 MHZ rate. For the device to acquire sync, the comma code must be input on RXD[0:9] on RBC1 rising edges.
15 16 17 18 19 21 22 23 24 25	RX[0:9]	I	**Receive Data Input**. These 10-Bit PHY Interface inputs contain receive data which are clocked in on rising edges of RBC[1:0].
31	EN_CDET	O	**Comma Detect Enable Output**. This 10-Bit PHY Interface output is asserted when either the receive 8B10B PCS state machine is in the loss of synchronization state or the EN_CDET bit is set in the internal Registers. This output is typically used to enable the comma detect function in an external Physical Layer device.

1.0 PIN DESCRIPTION (cont'd)

Pin #	Pin Name	I/O	Description
34	EWRAP	O	**Loopback Output Enable**. This 10-Bit PHY Interface output is asserted whenever the EWRAP bit is set in the internal Registers. This output is typically used to enable loopback in an external Physical Layer device.
29	LCK_REF	O	**Receiver Lock Output**. This 10-Bit PHY Interface output is asserted whenever the LCK_REF bit is set in the internal Registers. This output is typically used to enable the receive lock-to-reference mechanism in an external Physical Layer device.
System Interface			
149	SCLK	I	**System Interface Clock Input**. This input clocks data in and out of the receive and transmit FIFO's on TXD[31:0] and RXD[31:0], respectively. All System Interface inputs and outputs are also clocked in and out on rising edges of SCLK, with the exception of RXOE. SCLK clock frequency must be between 33-66 MHZ.
146	TXEN	I	**Transmit Enable Input.** This input has to be asserted active low to enable the current data word on TXD[31:0] to be clocked into the transmit FIFO. TXEN is clocked in on rising edges of system interface clock, SCLK.
96 98 99 100 101 102 103 104 105 106 107 108 109 110 111 113 114 116 117 118 119 120 121 122 124 125 126 127 128 129 130 131	TXD[31:0]	I	**Transmit Data Input**. This input bus contains the 32-bit data word that is clocked into the transmit FIFO on rising edges of the system interface clock, SCLK.
139 140 141 142	TXBE[3:0]	I	**Transmit Byte Enable Input.** These inputs determine which bytes of the current 32-bit word on TXD[31:0] contain valid data. TXBE[3:0] is clocked into the device on rising edges of the system interface clock, SCLK.
145	TXSOF	I	**Transmit Start Of Frame Indication.** This input has to be asserted active high on the same clock cycle when first word of the packet is being clocked in on TXD[31:0]. TXSOF is clocked into the device on rising edges of the system interface clock, SCLK.
144	TXEOF	I	**Transmit End Of Frame Indication.** This input has to be asserted active high on the same clock cycle when the last word of the packet is being clocked in on TXD[31:0]. TXEOF is clocked into the device on rising edges of the system interface clock, SCLK.
137	TXWM1	O	**Transmit FIFO Watermark 1 Output.** 1 = Transmit FIFO Data ≤ Transmit FIFO Watermark 1 Threshold 0 = Above Threshold TXWM1 is clocked out on rising edges of the system clock, SCLK.

1.0 PIN DESCRIPTION (cont'd)

Pin #	Pin Name	I/O	Description
136	$\overline{\text{TXWM2}}$	O	**Transmit FIFO Watermark 2 Output.** 1 = Transmit FIFO Data ≤ Transmit FIFO Watermark 2 Threshold 0 = Above Threshold $\overline{\text{TXWM2}}$ is clocked out on rising edges of the system clock, SCLK
134	TXDC	O	**Transmit Packet Discard Output.** 1 = Device Detects that Current Packet Being Input on the System Interface has an Error, Rest of Packet Ignored. 0 = No Discard TXDC is clocked out on rising edges of the system clock, SCLK. If Autoclear Mode is not enabled, this output is latched high and stays latched until cleared with the CLR_TXDC pin. If Autoclear Mode is enabled, this output is latched high and automatically clears itself low two clock cycles after the next TXEOF occurrence.
133	CLR_TXDC	I	**Clear TXDC Input.** 1 = TXDC Pin Cleared Low 0 = Not Cleared TXDC is clocked in on rising edges of the system clock, SCLK. This pin only clears TXDC when Autoclear Mode is disabled. When Autoclear Mode is enabled, this pin is ignored and TXDC is automatically cleared two clock cycles after the next TXEOF occurrence.
95	FCNTRL	I	**Flow Control Enable Input.** 1 = Transmitter Automatically Transmit a MAC Control Pause Frame 0 = Normal Operation FCNTRL is clocked in on rising edges of the system clock, SCLK.
132	$\overline{\text{TXCRC}}$	I	**Transmit CRC Enable Input.** 1 = No CRC 0 = CRC Calculated and Appended to Current Packet Being Inputted on System Interface $\overline{\text{TXCRC}}$ is clocked in on rising edges of the system clock, SCLK, and must be asserted on the same SCLK clock cycle as TXSOF.
1	$\overline{\text{RXEN}}$	I	**Receive Enable Input.** This input has to be asserted active low to enable the current data word to be clocked out of the receive FIFO on RXD[31:0]. $\overline{\text{RXEN}}$ is clocked in on rising edges of system interface clock, SCLK.
2	$\overline{\text{RXOE}}$	I	**Receive Output Enable Input.** 1 = Receive Outputs High Impedance (RXD[31:0], RXBE[3:0], RXSOF, RXEOF) 0 = Receive Outputs Active

1.0 PIN DESCRIPTION (cont'd)

Pin #	Pin Name	I/O	Description
157 158 160 161 163 164 165 166 168 169 171 172 174 175 176 177 179 180 182 183 185 186 187 188 190 191 194 195 197 198 199 200	RXD[31:0]	O	**Receive Data Input**. This output bus contains the 32-bit data word that is clocked out of the receive FIFO on rising edges of the system interface clock, SCLK.
205 204 203 202	RXBE[3:0]	O	**Receive Byte Enable Output.** These outputs determine which bytes of the current 32-bit word on RXD[31:0] contain valid data. RXBE[3:0] is clocked out of the device on rising edges of the system interface clock, SCLK.
206	RXSOF	O	**Receive Start Of Frame Indication.** This output is asserted active high on the same clock cycle when the first word of the packet is being read out of the receive FIFO on RXD[31:0]. RXSOF is clocked out of the device on rising edges of the system interface clock, SCLK.
207	RXEOF	O	**Receive End Of Frame Indication.** This output is asserted active high on the same clock cycle when the last word of the packet is being read out of the receive FIFO on RXD[31:0]. RXEOF is clocked out of the device on rising edges of the system interface clock, SCLK.
156	RXWM1	O	**Receive FIFO Watermark 1 Output.** 1 = Receive FIFO Data > Receive FIFO Watermark 1 Threshold 0 = Equal to or Below Threshold RXWM1 is clocked out on rising edges of the system clock, SCLK. Data is valid on RXD[31:0] when either RXWM1 or RXWM2 is asserted high, independent of $\overline{\text{RXEN}}$.
155	RXWM2	O	**Receive FIFO Watermark 2 Output.** 1 = Receive FIFO > Receive FIFO Watermark 2 Threshold Or Complete Packet Loaded Into Receive FIFO 0 = Equal to or Below Threshold and no EOF in FIFO RXWM2 is clocked out on rising edges of the system clock, SCLK. Data is valid on RXD[31:0] when either RXWM1 or RXWM2 is asserted high, independent of $\overline{\text{RXEN}}$.

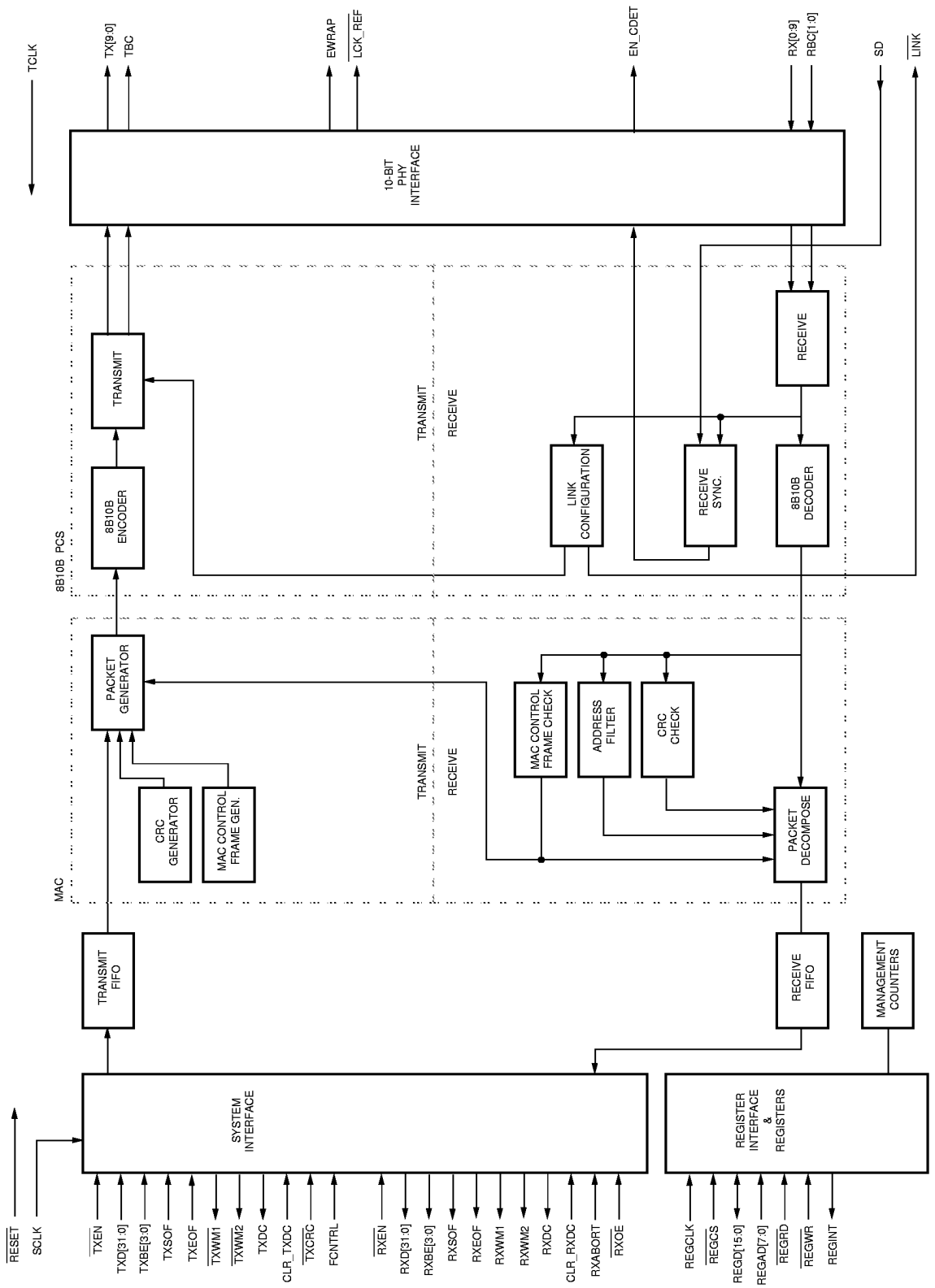
1.0 PIN DESCRIPTION (cont'd)

Pin #	Pin Name	I/O	Description
154	RXDC	O	**Receive Packet Discard Output.** 1 = Device Detects that Current Packet Being Output on the System Interface has an Error and Should be Discarded. 0 = No Discard Packet being output on System Interface can be discarded by asserting the RXABORT pin or automatically discarded if AUTORXAB bit is set. RXDC is clocked out on rising edges of the system clock, SCLK. If Autoclear Mode is not enabled, this output is latched high and stays latched until cleared with the CLR_RXDC pin. If Autoclear Mode is enabled, this output is latched high and automatically clears itself low two clock cycles after the next RXEOF occurrence. RXDC can also be cleared with RXABORT if programmed to do so.
153	CLR_RXDC	I	**Clear RXDC Input.** 1 = RXDC Pin Cleared Low 0 = Not Cleared CLR_RXDC is clocked in on rising edges of the system clock, SCLK. This pin only clears RXDC when Autoclear Mode is disabled. When Autoclear Mode is enabled, this pin is ignored and RXDC is automatically cleared two clock cycles after the next RXEOF occurrence.
152	RXABORT	I	**Receive FIFO Data Abort Input.** 1 = Abort & Discard Receive Packet Being Read Out On RXD[31:0] 0 = No Discard RXABORT is clocked in on rising edges of the system clock, SCLK.
Register Interface			
92	$\overline{\text{REGCS}}$	I	**Register Interface Chip Select Input.** This input has to be asserted active low to enable reading and writing of data on REGD[15:0] and REGA[7:0]. This input is clocked in on rising edges of REGCLK.
68	REGCLK	I	**Register Interface Clock Input**. This input clocks data in and out on REGD[15:0], REGA[7:0], REGRD, and REGWR on rising edges. REGCLK frequency must be between 5-40 MHz.
69 71 72 73 75 76 77 78 80 82 83 84 86 87 88 89	REGD[15:0]	I/O	**Register Interface Data Bus**. This bus is a bidirectional 16-bit data path to and from the internal registers. Data is read/written from/to the internal registers on rising edges of the register clock, REGCLK.
63 62 61 60 58 57 56 55	REGA[7:0]	I	**Register Interface Address Input.** These inputs provide the address for the specific internal register to be accessed. These inputs are clocked into the device on rising edges of REGCLK.
66	$\overline{\text{REGRD}}$	I	**Register Interface Read Input.** When this input is asserted active low, the accessed internal register is read out, i.e. data is outputted from the register. This input is clocked into the device on rising edges of REGCLK.

1.0 PIN DESCRIPTION (cont'd)

Pin #	Pin Name	I/O	Description
65	$\overline{\text{REGWR}}$	I	**Register Interface Write Input.** When this input is asserted active low, the accessed internal register is written to, i.e. data is inputted to the register. This input is clocked into the device on rising edges of REGCLK.
64	REGINT	O	**Register Interface Interrupt Output.** This output is asserted active high when certain interrupt bits in the registers are set, and it remains latched high until all interrupt bits are read and cleared.
Miscellaneous			
52	TCLK	I	**Transmit Clock Input**. This 125 MHZ input clock is used by the 8B10B PCS Section and generates the 125 MHZ transmit output clock, TBC, used to output data on the 10-Bit PHY Interface.
54	$\overline{\text{LINK}}$	O	**Receive Link Output.** 1 = No Link 0 = Receive Link Synchronized & Configured.
13	SD	I	**Signal Detect Input** 1 = Data Detected on Receive 10-Bit PHY Interface is Valid 0 = Data Not Valid, 8B10B PCS Receiver Forced to Loss of Sync State This pin is ignored (assumed high) unless it is enabled by setting the SD enable bit in the Configuration 3 Register.
94	$\overline{\text{RESET}}$	I	**Reset Input.** 1 = Normal 0 = Device Reset, FIFO's Cleared, Counters Cleared, Register Bits Set to Defaults
10	TAP	I	**Tristate All Pin Input.** This pin is used for testing purposes only. 1 = All Output and Bidirectional Pins Placed in High Impedance State 0 = Normal Operation
12	TEST	I	**Test Mode Input.** This pin is reserved for factory test and must be tied low for proper operation.
7 93	RESERVED		**Reserved.** These pins are reserved and must be left floating.

2.0 Block Diagram



8101 Block Diagram

3.0 Functional Description

3.1 GENERAL

The 8101 is a complete Media Access Controller (MAC sublayer) with integrated coding logic for fiber and short haul copper media (8B10B PCS sublayer) for 1000 Mbps Gigabit Ethernet systems. The 8101 has six main sections: System Interface, FIFO's, MAC, 8B10B PCS, 10-Bit PHY Interface, and Register Interface. A block diagram is shown in Figure 1.

The 8101 has a transmit data path and a receive data path. The transmit data path goes in the System Interface and out the 10-Bit PHY Interface, as shown in the top half of Figure 1. The receive data path goes in the 10-Bit PHY Interface and out the System Interface, as shown in the bottom half of Figure 1.

On the transmit data path, data is input into the System Interface from an external bus. The data is then sent to the transmit FIFO. The transmit FIFO provides temporary storage of the data until it is sent to the transmit MAC section. The transmit MAC takes the data and formats it into an Ethernet packet per IEEE 802.3 specifications and shown in Figure 2. The Ethernet packet then goes to the 8B10B PCS section. The 8B10B PCS section encodes the data and adds the appropriate framing delimiters to create a 10-Bit PHY frame as specified in IEEE 802.3z and shown in Figure 3. The encoded data then goes to the 10-Bit PHY Interface for transmission to an external PHY chip. The transmit side also generates MAC Control frames and includes logic for AutoNegotiation.

On the receive data path, the 10-Bit PHY Interface receives incoming encoded data from an external PHY chip. The incoming encoded data must be encoded in the 10-Bit PHY format specified in IEEE 802.3z and shown in Figure 3. The incoming encoded data is then sent to the receive 8B10B PCS block which strips off the framing delimiters, decodes the data, and converts the encoded data into an

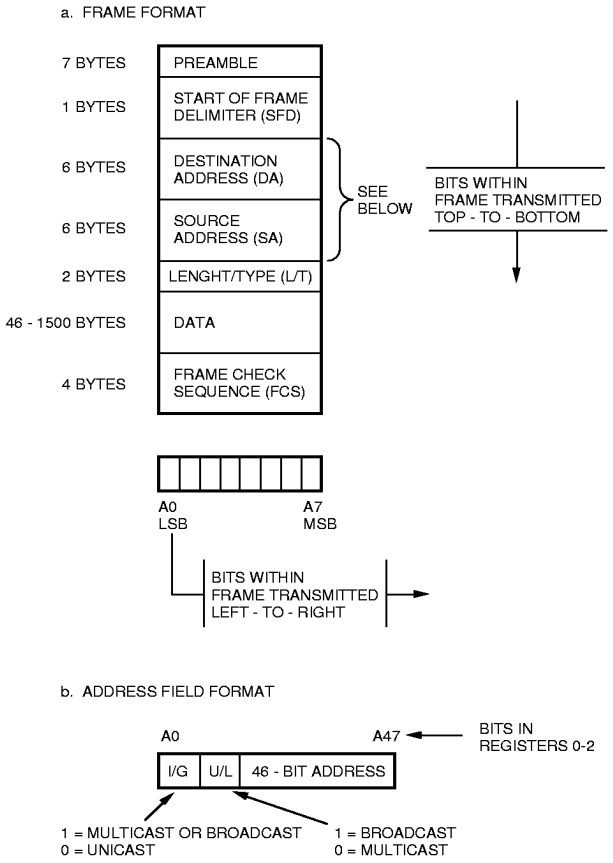


Figure 2. Ethernet MAC Frame Format

Ethernet packet per IEEE 802.3 specifications and shown in Figure 2. The Ethernet packet data is then sent to the receive MAC section. The receive MAC section decomposes the packet, checks the validity of the packet against certain error criteria and address filters, and checks for MAC Control frames. The receive MAC then sends valid packets to the receive FIFO. The receive FIFO provides temporary storage of data until it is demanded by the System Interface. The System Interface outputs the data to an external bus.

The Register Interface is a separate bidirectional 16-bit data bus through which configuration inputs can be set, status outputs can be read, and management counters can be accessed from the internal registers.

Each block plus the operating modes are described in more detail in the following sections.

3.2 ETHERNET FRAME FORMAT

3.2.1 General

Information in an Ethernet network is transmitted and received in packets or frames. The basic function of the 8101 is to process Ethernet frames. An Ethernet frame is defined in IEEE 802.3 and consists of a preamble, start of frame delimiter (SFD), destination address (DA), source address (SA) , length/type field (L/T), data, frame check sequence (FCS), and interpacket gap (IPG). The format for the Ethernet frame is shown in Figure 2.

An Ethernet frame is specified by IEEE 802.3 to have a minimum length of 64 bytes and a maximum length of 1518 bytes, exclusive of the preamble and SFD. Packets which are less than 64 bytes or greater than 1518 bytes are referred to as undersize and oversize packets, respectively.

3.2.2 Preamble & SFD

The preamble & SFD is a combined 64-bit field consisting of 62 alternating 1's and 0's followed by a 11 end of preamble indicator. The first 56-bits of 1's and 0's are considered to be the preamble, and the last 8-bits of 10101011 are considered to be the SFD (Start of Frame Delimiter).

3.2.3 Destination Address

The destination address is a 48-bit field containing the address of the station(s) to which the frame is directed. The format of the address field is the same as defined in IEEE 802.3 and shown in Figure 2b. The destination address can be either a unicast address to a specific station, a multicast address to a group of stations, or a broadcast address to all stations. The first and second bits determine whether an address is unicast, multicast or broadcast, and the remaining 46-bits are the actual address bits, as shown in Figure 2b.

3.2.4 Source Address

The source address is a 48-bit field containing the specific station address from which the frame originated. The format of the address field is the same as defined in IEEE 802.3 and shown in Figure 2b.

3.2.5 Length/Type Field

The 16-bit length/type field takes on the meaning of either packet length or packet type, depending on its numeric value, as described in Table 1.

Table 1. Length/Type Field Definition

Length/Type Field Value (Decimal)	Length or Type	Definition
0-1500	Length	Total Number of Bytes In Data Field minus any padding
1501-1517	Neither	Undefined
≥1518	Type	Frame Type

3.2.6 Data

The data is a 46-1500 byte field containing the actual data to be transmitted between two stations. If the actual data is less than 46 bytes, extra 0's are added to increase the data field to the 46 byte minimum size. Adding these extra 0's is referred to as padding.

3.2.7 Frame Check Sequence

The frame check sequence (FCS), is a 32-bit cyclic redundancy check (CRC) value computed on the entire frame, exclusive of preamble & SFD. The FCS algorithm is defined in IEEE 802.3. The FCS is appended to the end of the frame and is used to determine frame validity.

3.2.8 Interpacket Gap

The interpacket gap (IPG) is the time interval between packets. The minimum IPG value is defined to be 96 bits, where 1 bit = 1nS for Gigabit Ethernet. There is no maximum IPG limit.

3.3 SYSTEM INTERFACE

3.3.1 General

The System Interface is a 64-bit wide data interface consisting of separate 32-bit data bus for transmit and a separate 32-bit data bus for receive.

3.3.2 Data Format and Bit Order

The format of the data word on TXD[31:0] and RXD[31:0] and its relationship to the MAC frame format and 10-Bit PHY Interface format is shown in Figure 3. Note that the device can be programmed to append an additional 32-bit status word to the end of the receive packet; refer to the Receive Status Word section for more details on this status word.

The byte ordering of the TXD and RXD data bits is programmable by setting the endian select bit in the Configuration 4 register. The byte order shown in Figure 3 is with little endian format mode (default). If the device is placed in big endian format, then the byte order shown in Figure 3 is reversed, i.e. DA[0:7] occurs on pins RXD[24:31], DA[24:31] occurs on pins RXD[0:7], etc. All bytes in the frame are affected by the endian select bit, including the receive status word if appended. The difference between little endian and big endian format is illustrated in Figure 4.

3.3.3 Transmit Timing

The transmit portion of the System Interface consists of 45 signals: 32 transmit data input bits (TXD[31:0]), one transmit enable ($\overline{TXEN}$), four transmit byte enable inputs (TXBE[3:0]), two transmit start of frame and end of frame inputs ($\overline{TXSOF}$ and $\overline{TXEOF}$), two transmit FIFO watermark outputs (TXWM1 and TXWM2), one transmit discard output (TXDC), one transmit discard clear input (CLR_TXDC), one transmit CRC enable input ($\overline{TXCRC}$), and one flow control enable input (FCNTRL). All receive and transmit data is clocked in/out on rising edges of the system clock, SCLK. SCLK must operate between 33-66 MHZ.

The SCLK input needs to be continuously input to the device at 33-66 MHz. When $\overline{TXEN}$ is deasserted, the transmit interface is not selected and subsequently, no input data is accepted by the device from the transmit System Interface inputs. When $\overline{TXEN}$ is asserted, a data word on the TXD[31:0] input is clocked into the transmit FIFO on each rising edge of the SCLK clock input. Multiple packets may be clocked in on one $\overline{TXEN}$ assertion. TXD[31:0] input data is 32-bit wide packet data whose format and relationship to the MAC packet and 10-Bit PHY data is described in Figure 3.

The transmit byte enable inputs, TXBE[3:0], determine which bytes of the 32-bit TXD[31:0] data word contain valid data. TXBE[3:0] are clocked in on rising edges of SCLK along with each TXD[31:0] data word. The correspondence between the byte enable inputs and the valid bytes of each data word on TXD[31:0] is defined in Table 2. Any logic combination of TXBE[3:0] inputs is allowed, with the one exception that TXBE[3:0] must not be 0000 on the SCLK cycle when TXSOF or TXEOF is asserted.

Table 2. Byte Enable Pin vs. Valid Byte Position

TXBE/RXBE Pins	Valid Bytes on TXD/RXD Pins
TXBE3/RXBE3	TXD[31:24]/RXD[31:24]
TXBE2/RXBE2	TXD[23:16]/RXD[23:16]
TXBE1/RXBE1	TXD[15:8]/RXD[15:8]
TXBE0/RXBE0	TXD[7:0]/RXD[7:0]

The transmit start of frame and end of frame inputs, TXSOF and TXEOF, indicate to the device which data words start and end the Ethernet data packet, respectively. These signals are input on the same SCLK rising edge as the first and last word of the data packet.

The transmit watermark outputs, $\overline{TXWM1}$ and $\overline{TXWM2}$, indicate when the transmit FIFO has exceeded the programmable watermark thresholds. The watermarks will be asserted or deasserted by the device on rising edges of SCLK, depending on the fullness of the transmit FIFO. Refer to the transmit FIFO section for more details on these watermarks.

TXDC is a transmit packet discard output. TXDC is asserted every time the transmission of the packet being input on the System Interface was halted and packet discarded due to some error. This signal is latched active high and can be cleared by either asserting the clearing signal, CLR_TXDC, or cleared automatically if the device is placed in the AutoClear mode. See the Packet Discard section for more details on discards and TXDC.

$\overline{TXCRC}$ is an input which can enable the internal generation and appending of the 4 byte CRC value onto the end of the data packet. $\overline{TXCRC}$ is sampled on rising edges of SCLK and has to be asserted at the beginning of the packet, coincident with TXSOF, to cause the removal or addition of the CRC to that packet. CRC generation can also be enabled by setting the transmit CRC enable bit in the Configuration 1 register. The interaction between the $\overline{TXCRC}$ pin and CRC enable bit is defined in Table 3.

FCNTRL is an input which will cause the automatic generation and transmission of a MAC Control Pause frame. FCNTRL is input on rising edges of SCLK. See the MAC Control Frame section for more details about this feature.

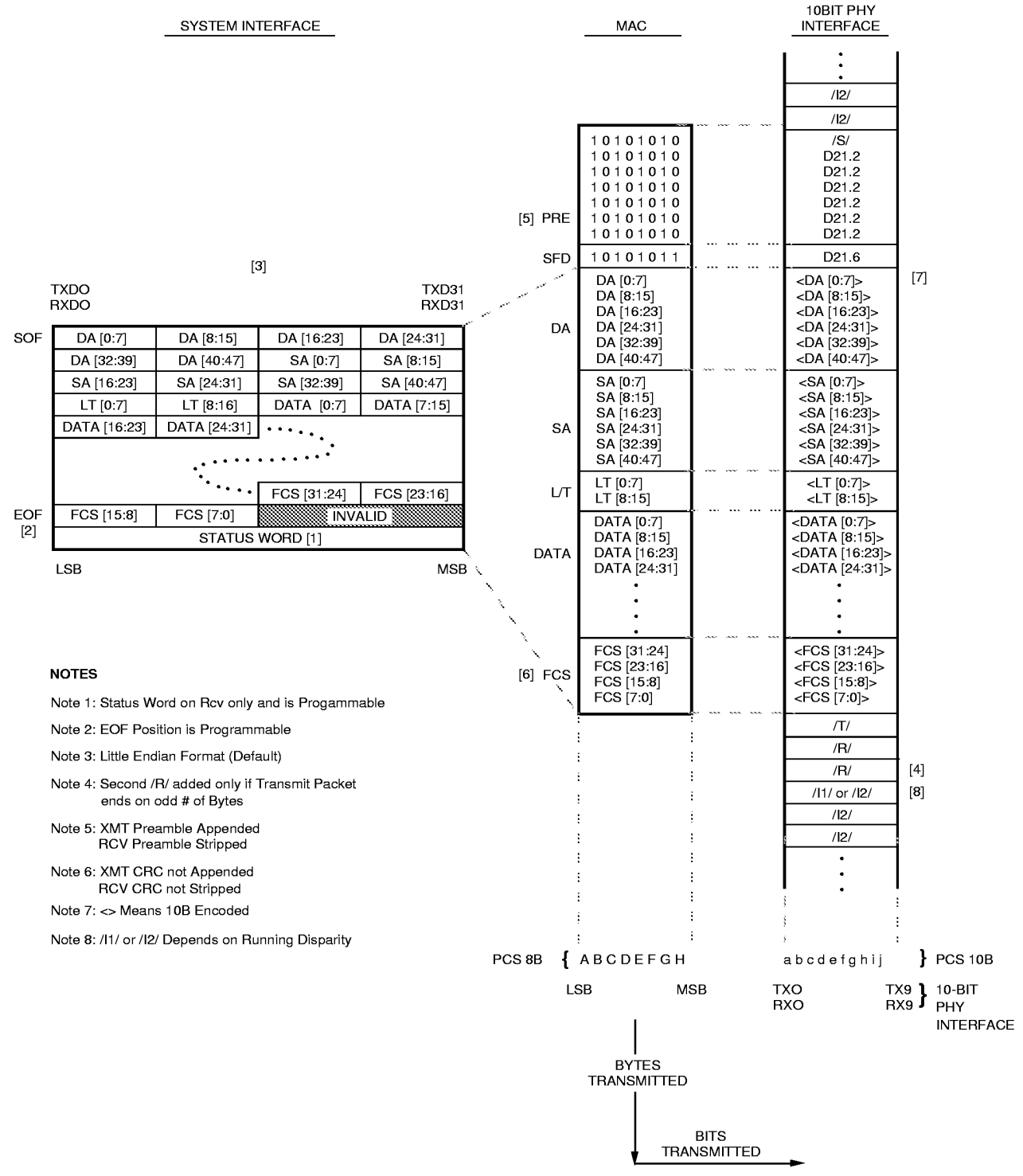


Figure 3. Frame Formats and Bit Ordering

3.3.4 Receive Timing

The receive portion of the System Interface consists of 45 signals: 32 receive output data bits (RXD[31:0]), one receive enable input (RXEN), four receive byte enable outputs (RXBE[3:0]), two receive start of frame and end of frame outputs (RXSOF and RXEOF), two receive FIFO watermark outputs (RXWM1 and RXWM2), one receive discard output (RXDC), one receive discard clear input (CLR_RXDC), one receive packet abort input (RXABORT),and one receive output enable (RXOE). All receive and transmit data is clocked in/out with the system clock, SCLK. SCLK must operate between 33-66 MHz.

The SCLK input needs to be continuously input at 33-66 Mhz. When RXEN is deasserted, the receive interface is not selected and subsequently, no data from the receive FIFO can be output over the System Interface. If the receive watermarks are asserted while RXEN is deasserted, the next data word from the receive FIFO appears on the RXD[31:0] outputs and stays there until RXEN is asserted. When RXEN is asserted, a data word from the receive FIFO is clocked out onto the RXD[31:0] outputs after each rising edge of the SCLK input. Once the entire packet has been clocked out, then no more data is clocked out on RXD[31:0] until RXEN is deasserted and reasserted, thus allowing extra dribble SCLK clock cycles to occur after the end of packet. RXD[31:0] output data is 32-bit wide packet data whose format and relationship to the MAC packet and 10-Bit PHY data is described in Figure 3.

The receive byte enable outputs, RXBE[3:0], determine which bytes of the 32-bit RXD[31:0] data word contain valid data. RXBE[3:0] are clocked out on rising edges of SCLK along with each RXD[31:0] data word. Note that RXBE[3:0]=1111 for all words of the packet except the last word; the last word of the packet may end on any one of the four byte boundaries of the 32-bit data word. The correspondence between the byte enable inputs and the valid data bytes of each data word on RXD[31:0] is defined in Table 2.

The receive start of frame and end of frame outputs, RXSOF and RXEOF, indicate which words start and end the Ethernet data packet, respectively. These signals are generally clocked out on the same SCLK rising edge as the first and last word of the data packet, respectively. However their exact position relative to the data packet is dependent on the programming of the EOF position bit and status word option bits in the Configuration 1 register. The exact RXSOF and RXEOF position for combinations of these two bits is depicted in Figure 5. More details about the definition of these bits can be found in the Configuration 1 Register Bit Definition, and more details about the status word can be found in the Receive Status Word section.

The receive watermarks, RXWM1 and RXWM2, indicate when the receive FIFO has exceeded the programmable watermark thresholds. The watermarks will be asserted or deasserted on rising edges of SCLK, depending on the fullness of the receive FIFO. Refer to Receive FIFO section for more details on these watermarks.

RXDC is a receive packet discard output. RXDC is asserted every time the reception of a packet being output over the System Interface was halted and the packet discarded due to some error. This signal is latched active high and can be cleared by either asserting the clearing signal, CLR_RXDC, or cleared automatically if the device is placed in the AutoClear mode. See the Packet Discard section for more details on discards and RXDC.

The RXABORT input, when asserted, will discard the current packet being output on the System Interface. When a packet is discarded by asserting RXABORT, the remaining contents of that packet in the receive FIFO are flushed. The process of flushing a receive packet from the receive FIFO with the RXABORT pin requires extra SCLK cycles equal to the (packet length in bytes)/8 + 6. Refer to

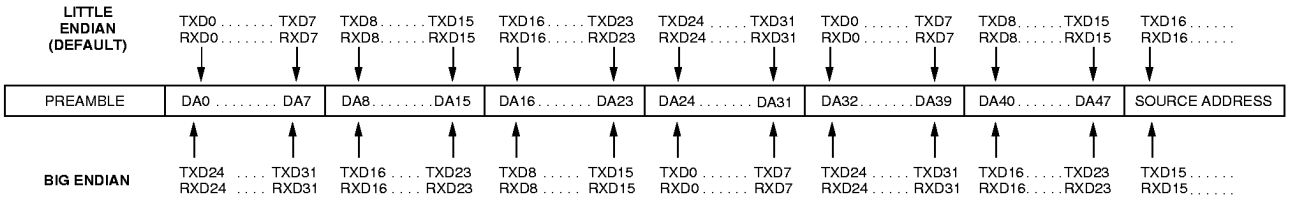


Figure 4. Little Endian vs. Big Endian Format

the Packet Discard section for more information about discarded packets. The device can be programmed to ignore the RXABORT pin by clearing the discard RXABORT enable bit in the Configuration 2 register. The device can also be programmed to discard either the data packet and its status word or just the data packet itself exclusive of its status word by setting the RXABORT definition bit in the Configuration 3 register.

$\overline{RXOE}$ is an output enable input which, when asserted, will place certain receive outputs in the high impedance state. The output pins affected by $\overline{RXOE}$ are RXD[31:0], RXBE[3:0], RXSOF, and RXEOF.

3.3.5 Bus Width

The receive word width can be changed from 32-bits to 16-bits by appropriately setting the bus word width select bit in the Configuration 4 register. When the bus width is configured to 16-bits, the receive System Interface data outputs appear on RXD[15:0] and the data words are now 16-bits wide instead of 32-bits wide. Note that the transmit word width can be adjusted by appropriately setting the transmit byte enable inputs, TXBE[3:0], as described in Table 2.

3.3.6 System Interface Disable

The system interface can be disabled by setting the system interface disable bit in the Configuration 3 register. When the System Interface is disabled, the device (1) places all System Interface outputs in high impedance state (i.e. $\overline{TXWM1/2}$, TXDC, RXD, RXBE, RXSOF, RXEOF, $\overline{RXWM1/2}$, RXDC), (2) ignores all inputs (i.e. SCLK, $\overline{TXEN}$, TXD, TXBE, TXSOF, TXEOF, CLR_TXDC, FCNTRL, $\overline{TXCRC}$, $\overline{RXEN}$, $\overline{RXOE}$, CLR_RXDC, RXABORT), and (3) transmits /C/ ordered sets with the remote fault bits RF[1:0]=10 over the 10-Bit PHY Interface outputs.

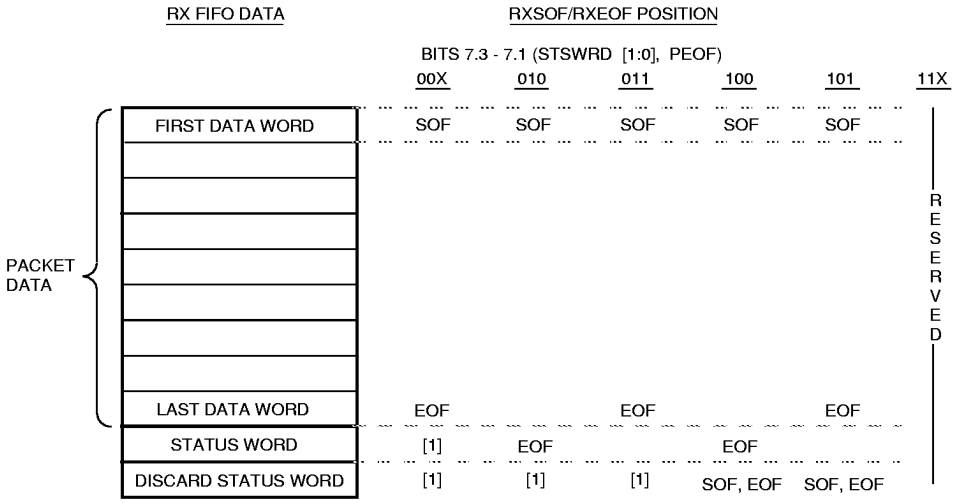
3.4 TRANSMIT MAC

3.4.1 General

The transmit MAC (Media Access Control) section generates an Ethernet MAC frame from transmit FIFO data by (1) generating preamble & SFD, (2) padding undersize packet with 0's to meet minimum packet size requirements, (3) calculating and appending CRC value, and (4) maintaining a minimum interpacket gap between packets. Each of the above four operations can be individually disabled and altered, if desired. The transmit MAC then sends the fully formed Ethernet packet to the 8B10B PCS block for encoding. The transmit MAC section also generates MAC Control frames.

3.4.2 Preamble & SFD Generation

The transmit MAC normally appends the preamble and SFD to the packet. The device can be programmed to ***not*** *append the preamble & SFD to the transmit packet by clearing the transmit preamble enable bit in the Configuration 1 register.*



NOTE 1: STATUS WORDS DO NOT EXIST WITH THIS BIT COMBINATION

Figure 5. RXSOF/RXEOF Position

3.4.3 AutoPad

The transmit MAC normally AutoPad's packets. AutoPadding is the process of automatically adding enough zeroes on packets with data fields less than 46 bytes to make the data field exactly 46 bytes in length and meet the 46 byte minimum data field requirement of IEEE 802.3. The device can be programmed to ***not*** *AutoPad by clearing the AutoPad bit in the Configuration 1 register.*

3.4.4 CRC Generation

The transmit MAC normally appends the CRC value to the packet. The device can be programmed to ***not*** *append the CRC value to the end of the packet from the transmit FIFO by asserting the* $\overline{TXCRC}$ *pin or by appropriately setting the transmit CRC enable bit in the Configuration 1 register, as described in Table 3.*

Table 3. TXCRC Bit & $\overline{TXCRC}$ Pin Logic

TXCRC Bit 7.5 1 = Append 0 = No Append	$\overline{TXCRC}$ Pin 1 = No Append 0 = Append	CRC Appended to End of Packet?
1	1	Yes
1	0	Yes
0	1	No
0	0	Yes

3.4.5 Interpacket Gap

If packets from the transmit FIFO arrive at the transmit MAC sooner than the minimum interpacket gap time (referred to as IPG), the transmit MAC will add enough time between packets to equal the minimum IPG value. The default IPG time is set to 96 bits (1 bit=1ns), but the IPG can be programmed to other values by appropriately setting the transmit IPG select bits in the Configuration 1 register and also summarized in Table 4.

Table 4. Transmit IPG Selection

IPG Select Bits 7.[9:7]	IPG (Bits)	Comments
111	96	IEEE Min Spec
110	112	
101	80	
100	64	
011	192	2x IEEE Min Spec
010	384	4x IEEE Min Spec
001	768	8x IEEE Min Spec
000	32	

3.4.6 MAC Control Frame Generation

The transmit MAC can automatically generate and transmit MAC Control Pause frames. MAC Control Pause frames are used for flow control. This function is described in more detail in the MAC Control Frame section.

3.5 RECEIVE MAC

3.5.1 General

The receive MAC (Media Access Control) section decomposes Ethernet packets received from the receive 8B10B PCS section by (1) stripping off the preamble & SFD, (2) stripping off the CRC, (3) checking the destination address against the address filters to determine packet validity, (4) checking frame validity against the discard conditions, and (5) checking the length/type field for MAC Control frames. Each of the above five operations can be individually disabled and altered, if desired. The receive MAC then sends valid packets to the receive FIFO for storage.

3.5.2 Preamble & SFD Stripping

The transmit MAC normally strips the preamble and SFD from the receive packet. The device can be programmed to ***not*** *strip the preamble & SFD by setting the receive preamble enable bit in the Configuration 1 register. When this bit is set, the preamble & SFD are left on the receive packet and are stored in the receive FIFO as a part of the packet.*

3.5.3 CRC Stripping

The receive MAC normally strips the FCS from the receive packet. The device can be programmed to ***not*** *strip the FCS field by setting the receive CRC enable bit in the Configuration 1 register. When this bit is set, the last 4-bytes of the packet containing the CRC value are left on the receive packet and are stored in the receive FIFO as part of the packet.*

3.5.4 Unicast Address Filter

Unicast packets are filtered by comparing the destination address of the receive packet against the 48-bit value stored in the three MAC Address 1-3 registers. When the destination address of a unicast packet matches the value stored in this register, the unicast packet is deemed valid and passed to the receive FIFO; otherwise, the packet is rejected. The correspondence between the bits in the MAC Address register and the incoming bits in the destination address of the receive packet is defined in the MAC Address register definition table.

The device can be programmed to always reject unicast packets by setting the reject unicast packet bit in the Configuration 2 register. When this bit is set, all unicast packets are rejected regardless of their address.

The reception of MAC Control frames is unaffected by any of the unicast packet address filtering functions and is controlled by other bits described in the MAC Control Frame section.

3.5.5 Multicast Address Filter

Multicast packets can be filtered by processing the destination address with the multicast address filter function. The multicast address filter function computes the CRC on the incoming DA and produces a 6-bit number that is compared against the 64 values stored in the MAC Address Filter 1-4 registers. When the multicast packet destination address passes the address filter, the packet is deemed valid and passed to the receive FIFO; otherwise, the packet is rejected.

The multicast address filter requires 64 address filter bits to be written into the Address Filter 1-4 registers. The multicast address filtering algorithm is as follows:

(1) Compute a separate 32-bit CRC on the destination address field using the same IEEE 802.3 defined method that computes the transmit CRC.

(2) Use bits 0-3 of the destination address FCS to select one of the bytes in the 64-bit address filter, as shown in Table 5.

(3) Use bits 4-6 of the destination address FCS to select one of the bits within the byte selected in (2) as shown in Table 5.

(4) If the bit selected in (3) is a "1", the destination address passes the filter; otherwise, the address fails the filter and the packet is rejected and discarded.

Note that if all 64-bits of the address filter are programmed to all 1's, then the address filter passes all multicast addresses.

The device can be programmed to reject multicast packets by setting the reject multicast packet bit in the Configuration 2 register. When this bit is set, all multicast packets are rejected regardless of their address.

The reception of MAC Control frames is unaffected by any of the multicast packet address filtering functions and is controlled by other bits described in the MAC Control Frame section

Table 5. Multicast Address Filter Map

FCS Bits [0:2]	Address Filter Byte	FCS Bits [3:5]	Address Filter Bit
000	F0[7:0]	000	Fx[0]
001	F1[7:0]	001	Fx[1]
010	F2[7:0]	010	Fx[2]
011	F3[7:0]	011	Fx[3]
100	F4[7:0]	100	Fx[4]
101	F5[7:0]	101	Fx[5]
110	F6[7:0]	110	Fx[6]
111	F7[7:0]	111	Fx[7]

F[7:0] are bytes in Address Filter 1-4 Registers.
Fx[7:0] are bits within each byte in Address Filter 1-4 Registers.
Bits 0-5 are the six least significant bits of the CRC.

3.5.6 Broadcast Address Filter

The device does not do any filtering on broadcast packets. However, the device can be programmed to reject broadcast packets by setting the reject broadcast packet bit in the Configuration 2 register. When this bit is set, all broadcast packets are rejected regardless of their address.

The reception of MAC Control frames is unaffected by any of the broadcast packet address filtering functions and is controlled by other bits described in the MAC Control Frame section

3.5.7 Reject Or Accept All Packets

The device can be programmed to accept or reject all packets regardless of type or whether the packet passes the address filter by setting the accept all packet or reject all packet bits, respectively, in the Configuration 2 register.

The reception of MAC Control frames is unaffected by these bits and is controlled by other bits described in the MAC Control Frame section.

3.5.8 Frame Validity Checks

The receive MAC determines the validity of each receive packet by checking for (1) valid FCS, (2) oversize packet, and (3) undersize packet.

*Valid FCS is determined by computing the CRC value on the incoming receive packet per IEEE 802.3 specifications and comparing it against the actual CRC value in the FCS field of the received packet. If the values are not the same, the frame is determined to be invalid and the packet is discarded. Refer to the Packet Discard section for more information about discards. The device can be programmed to **not** discard a packet with bad FCS by clearing the discard CRC error bit in the Configuration 2 register.*

*Oversize packets are packets whose length is greater than the maximum packet size. If a received packet is an oversize packet, then the packet is determined to be invalid and it is discarded. Refer to the Packet Discard section for more information about discards. The maximum packet size can be programmed to be either 1518 bytes, 1522 bytes, or 1535 bytes, exclusive of preamble & SFD, by appropriately setting the maximum packet size bit in the Configuration 3 register. The device can be programmed to **not** discard an oversize packet and thus allow packets of unlimited length by clearing the discard oversize packet bit in the Configuration 2 register.*

*Undersize packets are packets whose length is less than the minimum packet size. Minimum packet size is defined to be 64 bytes, exclusive of preamble & SFD. If a received packet is an undersize packet, then the frame is determined to be invalid and it is discarded. Refer to the Packet Discard section for more information about discards. The device can be programmed to **not** discard an undersize packet by clearing the discard oversize packet bit in the Configuration 2 register.*

3.5.9 Maximum Packet Size

The maximum packet size used for receive MAC frame validity checking can be programmed to be one of four values by appropriately setting the receive MAC maximum packet size select bits in the Configuration 3 register and the discard oversize packet enable bit in the Configuration 2 register as shown in Table 6. This selection is also described in the register descriptions for those registers.

The bits shown in Table 6 affect the receive MAC section only; the maximum packet size for the management counters is determined by other bits as described in the Counters section.

Table 6. Receive Maximum Packet Size Selection

Receive Max Packet Size Select Bits		Max Packet Size (bytes)
Discard Oversize Packet, Bit 8.7	RX MAC Max Packet Size Select, Bits 9.[5:4]	
0	xx	unlimited
1	10	1535
1	01	1522
1	00	1518

3.5.10 MAC Control Frame Check

The length/type field is checked to detect whether the packet is a valid MAC Control frame. Refer to the MAC Control Frame section for more details on MAC Control frames.

3.6 TRANSMIT FIFO

3.6.1 General

The transmit FIFO acts as a temporary buffer between the System Interface and transmit MAC section. The transmit FIFO size is 4K bytes. Data is clocked into the transmit FIFO with the 33-66 MHZ System Interface clock, SCLK. Data is automatically clocked out of the transmit FIFO with the 125 MHZ 8B10B PCS clock whenever (1) a full packet has been loaded into the FIFO (evidenced by an EOF being written into the FIFO on the System Interface), or (2) the FIFO data exceeds the transmit FIFO AutoSend threshold. There are two programmable watermark outputs, $\overline{TXWM1}$ and $\overline{TXWM2}$, which aid in managing the data flow into the transmit FIFO.

3.6.2 AutoSend

The AutoSend feature causes a packet in the transmit FIFO to be automatically transmitted once transmit FIFO data exceeds a certain threshold.

The transmit AutoSend threshold is programmable over the lower 2K byte of the transmit FIFO. The AutoSend threshold can be programmed with the six transmit

AutoSend threshold bits that reside in the Transmit FIFO Threshold register. Once the data in the FIFO exceeds this threshold, then the packet is automatically transmitted to the 8B10B PCS section and out the 10-Bit PHY Interface. A packet will also be automatically transmitted if an EOF is written into the transmit FIFO for that packet, regardless of the autosend threshold setting.

All of the bit settings for the transmit autosend threshold are evenly distributed over the lower 1/2 of the transmit FIFO range, except for the 000000 setting. The 000000 setting automatically starts transmission when the transmit FIFO is full, thus facilitating the transmission of oversize packets. Refer to the Transmit FIFO Threshold Register description for more details on the autosend bit settings.

3.6.3 Watermarks

There are two transmit watermarks for the transmit FIFO. These two watermarks are output on the $\overline{TXWM1}$ and $\overline{TXWM2}$ pins. These watermarks are asserted when the transmit FIFO data exceeds the thresholds associated with the watermarks.

The transmit watermark thresholds for $\overline{TXWM1}$ and $\overline{TXWM2}$ can be programmed over the entire 4K FIFO range. Each of the watermark thresholds are independently programmed with five bits that reside in the Transmit FIFO Threshold register. Once the data in the FIFO exceeds the threshold of either watermark, then the respective watermark pin on either $\overline{TXWM1}$ or $\overline{TXWM2}$ is asserted active low. The watermarks stay asserted until the data in the FIFO goes below the respective thresholds.

3.6.4 TX Underflow

The transmit FIFO underflow condition occurs when the TX FIFO is empty but the MAC still is requesting data to complete the transmission of a packet. If the transmit FIFO underflows, then (1) packet transmission to the 8B10B PCS is halted, (2) a /V/ code is appended to the end of the partially transmitted packet, and (3) any new data for the partially transmitted packet is discarded. Refer to the Packet Discard section for more information about discards.

3.6.5 TX Overflow

The transmit FIFO overflow condition occurs when the TX FIFO is full but additional data is still being written into it from the System Interface. If the transmit FIFO overflows, then (1) the input to the TX FIFO is blocked and will not accept any more data from System Interface until TX FIFO space is freed up, (2) the data already stored in the the TX FIFO for the partially loaded last packet is transmitted with a /V/ code appended to the end of the packet to indicate an error, and (3) any new data for the partially loaded last packet is discarded. Refer to the Packet Discard section for more information about discards.

3.6.6 Link Down FIFO Flush

When the link is down (also referred to as Link Fail and defined by either receiver has lost sync or AutoNegotiation process not yet completed), the transmitter at the 10-Bit PHY Interface is occupied with sending either idle or AutoNegotiation codes (/I/ or /C/). As a result, data cannot exit the transmit FIFO to the transmit MAC section. If data continues to be input to the transmit FIFO from the System Interface while the device is in Link Fail, the transmit FIFO may overflow. Enabling the link down FIFO flush feature will cause the data exiting the transmit FIFO to be automatically discarded when the device is in Link Fail, thus preventing any possible overflow of the transmit FIFO. The link down FIFO flush mode can be enabled by setting the link down FIFO flush bit in the Configuration 4 register.

3.6 RECEIVE FIFO

3.6.1 General

The receive FIFO acts as a temporary buffer between the receive MAC section and System Interface. The receive FIFO size is 16K bytes. Data is clocked into the receive FIFO with the 125 MHZ 8B10B PCS clock. Data is clocked out of the receive FIFO with the 33-66 MHZ System Interface clock, SCLK. There are two programmable watermark outputs, RXWM1 and RXWM2, which aid in managing the data flow out of the receive FIFO.

3.6.2 Watermarks

There are two watermarks for the receive FIFO. These two watermarks are output on the RXWM1 and RXWM2 pins. These watermarks are asserted when the receive FIFO data exceeds the thresholds associated with the watermarks.

The receive watermark thresholds for RXWM1 and RXWM2 can be programmed over the entire 16K byte receive FIFO range. Each of the watermark thresholds are independently programmed with eight bits that reside in the Receive FIFO Threshold register. Once the data in the FIFO exceeds the threshold of either watermark, then the respective watermark pin on either RXWM1 or RXWM2 is asserted active high. RXWM2 is also asserted if a complete packet is loaded into the receive FIFO from the 8B10B PCS section. The watermarks stay asserted until the data in the FIFO goes below the respective thresholds and RXWM2 will also stay asserted until all end of packets (EOF) have been read out of the receive FIFO. Once the EOFs has been read out of the receive FIFO, the watermarks cannot go active again until $\overline{RXEN}$ is deasserted.

3.6.3 RX Overflow

The receive FIFO overflow condition occurs when the receive RX FIFO is full and additional data is still being written into it from the MAC. If the receive FIFO overflows, then (1) the input to the RX FIFO is blocked and will not accept any more data from the 8B10B PCS until RX FIFO space is freed up, (2) the data already stored in the RX FIFO for the partially loaded last packet is normally discard, and (3) any new data for the partially loaded last packet is also normally discarded. Refer to the Packet Discard section for more information about discards. The device can be programmed to ***not*** *discard a packet corrupted by overflow by clearing the discard overflow packet bit in the Configuration 2 register.*

3.6.4 RX Underflow

The receive FIFO underflow condition occurs when the RX FIFO is empty but data is still being attempted to be read out of the FIFO over the System Interface. If the RX FIFO underflows, then (1) any data read out of the RX FIFO while the underflow condition persists is invalid, (2) any new data for the partially loaded last packet will be stored in the RX FIFO and will not be discarded.

3.7 8B10B PCS

3.7.1 Transmit

The transmit 8B10B PCS section accepts Ethernet formatted packet data from the transmit MAC and (1) encodes the data with the 8B10B encoder, (2) adds the start of packet delimiter, (3) adds the end of packet delimiter, (4) adds idle code stream, and (5) formats the packet according to the 10B PHY format defined in IEEE 802.3z and shown in Figure 3. The 8B10B encoded data stream is then sent to the transmit 10-bit PHY Interface for transmission.

The transmit 8B10B PCS section also generates the AutoNegotiation code stream when the device is in the AutoNegotiation process.

3.7.2 Receive

The receive 8B10B PCS section takes the 8B10B encoded packet data from the incoming 10-Bit PHY Interface and (1) acquires and maintains word synchronization, (2) strips off the start of packet delimiter, (3) strips off the end of packet delimiter, (4) strips off the idle code stream, (5) decodes the data with the 8B10B decoder, and (6) converts the packet to the Ethernet packet format shown in Figure 2. The Ethernet packet is then sent to the receive MAC for processing.

The receive 8B10B PCS section also decodes the AutoNegotiation code stream when the device is in the AutoNegotiation process.

3.7.3 8B10B Encoder

The 8B10B encoder converts each data byte of a packet into a unique 10-bit word as defined in IEEE 802.3z and shown in Table 7 (in abbreviated form).

The encoder also converts the start of packet delimiter, end of packet delimiter, idle code streams, and AutoNegotiation code streams into unique 10B code words. These unique 10B code words are referred to as ordered sets. Table 8 describes the ordered sets defined and used by IEEE 802.3z.

The 8B10B encoder also keeps the running disparity of the outgoing 10B word as close as possible to 0. Running disparity is the difference between the number of 1's and 0's transmitted on the outgoing bit stream. The algorithm for calculating running disparity is defined in 802.3z. After each 10B word is transmitted, the running disparity is recalculated. If the current running disparity is negative, then the next 10B word is chosen from the "Current RD-" column Table 7 (in abbreviated form). If the current running disparity is positive, then the next 10B word is chosen from the "Current RD+" column in Table 7.

Table 7. 8B10B Coding Table

8B Bytes		10B Codes	
Data Byte Name	Bits HGFEDCBA	CurrentRD- abcdei fghj	CurrentRD+ abcdei fghj
D0.0	000 00000	100111 0100	011000 1011
D1.0	000 00001	011101 0100	100010 1011
D2.0	000 00010	101101 0100	010010 1011
D3.0	000 00011	110001 1011	110001 0100
- - - - -	- - - - -	- - - - -	- - - - -
D28.7	111 11100	001110 1110	001110 0001
D29.7	111 11101	101110 0001	010001 1110
D30.7	111 11110	011110 0001	100001 1110
D31.7	111 11111	101011 0001	010100 1110

3.7.4 8B10B Decoder

The 8B10B decoder performs the reverse process of that described above in the 8B10B Encoder section. The 8B10B decoder converts each 10-bit word back into an 8-bit byte using the code conversion tables defined in IEEE 802.3z and shown in Table 7 (in abbreviated form) and Table 8. The 8B10B decoder also checks the running disparity of the incoming 10B word to insure that it is correct.

If the 8B10B decoder detects a 10B word that is not valid (not in Table 7), detects an ordered set that is not valid (not in Table 8), or detects an error in the running disparity, then a PCS codeword error results. Packets with PCS codeword errors are normally discarded. Refer to the Packet Discard section for more details on discards. The device can be programmed to ***not*** *discard packets with PCS codeword errors by clearing the discard codeword enable bit in the Configuration 2 register.*

Table 8. 10B Defined Ordered Sets

10B Code Sym.	Description	10B Codes	Begin RD	End RD
/C1/	Link Configuration 1	/K28.5/ [2] /D21.5/ config_word1 config_word2	+ or -	flip [1]
/C2/	Link Configuration 2	/K28.5/ [2] /D2.2/ config_word1 config_word2	+ or -	same [1]
/C/	Link Configuration	Alternating /C1/ & /C2/	------	------
/I1/	Idle 1	/K28.5/ /D5.6/	+	-
/I2/	Idle 2	/K28.5/ /D16.2/	-	-
/I/	Idle	/I1/ or /I2/	------	------
/S/	Start of Packet Delimiter (SPD)	/K27.7/	+ or -	same
/T/	End of Packet Delimiter (EPD)	/K29.7/	+ or -	same
/R/		/K23.7/	+ or -	same
/V/	Error (Void)	/K30.7/	+ or -	same

[1] RD determined on the /K/ and /D/ characters only, not the config_word.

[2] config_word 1/2 contain the 16-Bit AutoNegotiation data word. See the AutoNegotiation section for details.

3.7.5 Start of Packet

Start of packet is indicated by a unique Start of Packet Delimiter, referred to as SPD. The SPD consists of a single /S/ code inserted at the beginning of the packet in place of the first preamble octet, as defined in the IEEE 802.3z and shown in Figure 3. The /S/ code is defined in Table 8.

The transmit 8B10B PCS section inserts an /S/ code at the beginning of each transmit packet in place of the first 10B word of the preamble.

The receive 8B10B PCS section constantly monitors the incoming 10B bit stream. If an /S/ code is detected, then start of packet indication is given to the receive MAC, and a preamble octet is substituted in place of the /S/ code at the beginning of the packet. If the 8B10B PCS receiver detects the transition from the Idle pattern (/I/ code stream) to non-Idle pattern without an intervening /S/ code, then the packet is assumed to have a bad SPD. Packets with bad SPD are normally discarded as codeword errors. Refer to the Packet Discard section for more details on discards. The device can be programmed to ***not*** *discard packets with PCS codeword errors by clearing the discard codeword enable bit in the Configuration 2 register.*

3.7.6 End Of Packet

End of packet is indicated by a the End of Packet Delimiter, referred to as EPD. The EPD consists of two codes, called /T/ and /R/, inserted at the end of the packet, as defined in IEEE 802.3z and shown in Table 8, and also shown in Figure 3. To maintain synchronization on the proper word boundaries, an outgoing packet must also have an even number of 10-bit words transmitted. If the packet has an odd number of 10-bit words transmitted after the /T/R/ codes, then an extra /R/ code is inserted after the /T/R/ (now a /T/R/R/) to meet the even word requirement as defined in IEEE 802.3z and shown in Figure 3.

The transmit 8B10B PCS section appends either the /T/R/ or /T/R/R/ codes to the end of each transmit packet.

The receive 8B10B PCS section constantly monitors the incoming 10B bit stream. If the /T/R/ codes are detected, then end of packet indication is given to the receive MAC, and the /T/R/ or /T/R/R/ codes are stripped off from the end of the packet. If the 8B10B PCS receiver detects the transition from non-Idle pattern to Idle pattern (/I/ code stream) without intervening /T/R/ codes, then the packet is assumed to have a bad EPD. Packets with bad EPD are discarded if the device is programmed to do so. Refer to the Packet Discard section for more details on discards. The device can be programmed to ***not*** *discard packets with PCS errors by clearing the discard codeword enable bit in the Configuration 2 register.*

3.7.7 Idle

The interpacket gap time is filled with a continuous stream of codes referred to as the idle pattern. The idle pattern consists of a continuous stream of /I2/ codes, as defined in IEEE 802.3z and shown in Figure 3. The running disparity during idle is defined to be negative. So, if the running disparity after the last /R/ code of a packet is positive, a single /I1/ code must be transmitted as the first idle code to make the running disparity negative. All subsequent idle codes must be /I2/, as defined in IEEE 802.3z and shown in Figure 3. The /I1/ and /I2/ codes are defined in Table 8.

The transmit 8B10B PCS section inserts a continuous stream of /I1/I2/I2/I2/..... or /I2/I2/I2/I2/..... codes between packets.

The receive 8B10B PCS section constantly monitors the incoming 10B bit stream. If an /I2/ or /I1/ code is detected, then an end of packet indication is given to the receive MAC and the /I1/ and /I2/ codes are stripped off from the packet.

3.7.8 Receive Word Synchronization

In order to correctly decode the incoming encoded data, the 8B10B PCS receiver must identify the word boundaries of the incoming data stream. The process of detecting these word boundaries is referred to as word synchronization. The receiver uses a state machine compatible with the algorithm defined in IEEE 802.3z to acquire and maintain word synchronization. The comma code is used to acquire and maintain receive word synchronization, as specified by IEEE 802.3z. The comma code consists of a unique 7 bit pattern that only appears in the defined ordered sets shown in Table 8, and the comma code does not appear in the normal data words or across data word boundaries.

Word synchronization is signaled to an external PHY device by asserting the EN_CDET pin when the 8B10B PCS receiver has lost word synchronization. Word synchronization status can also be determined by reading the receive word sync detect bit in the Status 1 register.

3.7.9 AutoNegotiation

The AutoNegotiation algorithm uses the /C/ ordered sets, as defined in Table 8, to configure the link for correct operation. Refer to the AutoNegotiation section for more details on this process.

3.8 10-BIT PHY INTERFACE

3.8.1 General

The 10-Bit PHY Interface is a standardized interface between the 8B10B PCS section and an external Physical Layer device. The 10-Bit PHY Interface meets all the requirements outlined in IEEE 802.3z. The device can directly connect, without any external logic, to any Physical Layer device which also complies with the IEEE 802.3z 10-Bit Interface specifications. The 10-Bit PHY Interface frame format is defined in IEEE 802.3z and shown in Figure 3.

The 10-Bit PHY Interface consists of twenty six signals: ten transmit data output bits (TX[0:9]), transmit clock output (TBC), ten receive data input bits (RX[0:9]), two receive clock inputs (RBC0 and RBC1), comma detect enable output (EN_CDET), loopback output (EWRAP), and a receiver lock output (LCK_REF).

3.8.2 Data Format and Bit Order

The format and bit order of the data word on TX[0:9] and RX[0:9] and its relationship to the MAC frame and the System Interface data words is shown in Figure 3. Note that Figure 3 assumes that the device is in Little Endian format (default). If the device is in Big Endian Format, the byte order of the System Interface data word is reversed. See the System Interface section for more details if needed.

3.8.3 Transmit

On the transmit side, the TBC output clock is generated from the TCLK input clock and runs continuously at 125 MHz. Data on TX[0:9] is clocked out of the device on rising edges of the TBC clock output.

3.8.4 Receive

On the receive side, RX[0:9] data is clocked in on rising edges of the RBC[1:0] input clocks. RBC1 and RBC0 are required to be at a frequency of 62.5 MHz and be 180° out of phase. The data on RX[0:9] is clocked in at 125 MHZ by using alternate rising edges of the RBC[1:0] clocks to latch in the data on RX[0:9]. The incoming data on RX[0:9] is also required to be word aligned to the RBC1 clock, that is, the words that contain comma codes must be clocked in with the RBC1 clock, as specified in IEEE 802.3z.

The comma detect output, EN_CDET, is asserted when the receiver in the 8B10B PCS section has lost word synchronization. EN_CDET can also be asserted by setting the EN_CDET pin assert bit in the Configuration 3 register. The EN_CDET output can be used to enable the bit synchronization process in an external Physical Layer device.

The device does not have a pin designated for the standardized comma detect input, COM_DET, because the receive 8B10B PCS section has all the necessary logic to acquire word synchronization from the contents of the receive data stream alone.

3.8.5 Lock To Reference

The LCK_REF output is controlled exclusively by setting the LCK_REF pin assert bit in the Configuration 3 register. This output is typically used to enable the PLL locking process in an external Physical Layer device.

3.8.6 PHY Loopback

The EWRAP output pin is controlled exclusively by setting the EWRAP pin assert bit in the Configuration 3 register. This output is typically used to enable a loopback function in an external Physical Layer device.

When the EWRAP pin is asserted, the signal detect input pin, SD, from an external Physical Layer Device may be in an unknown state. To counteract this, the signal detect pin enable bit in the Configuration 3 register should also be written to a "0" when the EWRAP assert bit is written to a "1".

3.8.7 Signal Detect

There is an additional signal detect input pin, SD, which indicates to the device that the receive data detected on RXD[0:9] contains valid data. If SD is asserted high, the input data is assumed valid and the receive 8B10B PCS section is unaffected. If SD is deasserted low, the data is assumed to be invalid and the receive 8B10B PCS section is forced into the loss of sync state. Although SD is not part of the IEEE defined 10-Bit PHY Interface, it is typically sourced from an external Physical Layer device.

The device powers up with the SD pin disabled, that is, SD has no affect on the receive word synchronization state machine. To enable the SD pin, the SD pin enable bit must be set in the Configuration 3 register.

There is also a signal detect status bit in the Status 1 register which reflects the state of the SD input pin. If SD is high, then the signal detect status bit is forced high; if the SD pin is low, then the signal detect status bit is also forced low.

3.8.8 TBC Disable

The transmit side of the 10-bit PHY interface can be disabled if the TBC disable bit is set in the Configuration 4 register. When this bit is set, the TBC and TX[0:9] outputs are placed in high impedance state.

3.9 PACKET DISCARD

3.9.1 General

The device can be programmed to discard receive and transmit packets when certain error conditions are detected. The detection ot these error conditions can occur in the MAC, FIFO, or 8B10B PCS sections.

3.9.2 Transmit Discards

Transmit packets will be automatically discarded if certain error conditions are detected. These error conditions are described in Table 9. When a discard error is a detected for a transmit packet, any remaining data for that packet being input from the System Interface is ignored, a /V/ code is appended to the end of the packet to indicate an error to a remote station, and TXDC is asserted if the packet was being input from the System Interface when the discard occurred.

Table 9. Transmit Discard Conditions

Discard Condition	Description
Transmit FIFO Underflow	TX FIFO empty. Packet transmission to 8B10B PCS halted. Partially transmitted packet is terminated with a /V/ code followed by normal /I/ codes.
Transmit FIFO Overflow	TX FIFO full. No more data accepted from the System Interface. Partially transmitted packet is terminated with a /V/ code followed by normal /I/ codes.

3.9.3 Receive Discards

Receive packets can be discarded if certain error conditions are detected. These error conditions are described in Table 10. The discard behavior is dependent on whether the packet is being output on the System Interface or not when the discard condition is detected. If the packet containing the error is not being output on the System Interface when the discard condition is detected (referred to as internal discard), the packet is discarded, that is, all data from the packet containing the error is flushed from the receive FIFO. If the packet containing the error is being output on the System Interface when the discard condition is detected (referred to as external discard), the error condition is indicated by the assertion of the RXDC pin. The packet can then be discarded by asserting the RXABORT pin, or the packet can be automatically discarded if the automatic AutoAbort bit is set in the Configuration 3 register. For both internal and external discarded packets, the appended status word is updated to reflect the discard error condition.

Each of the receive discard conditions can be individually removed as a discard condition by appropriately setting the discard bits in the Configuration 2 register. When these bits are set, a packet that is afflicted with the error condition indicated by that bit will not be discarded.

The device can be programmed to send status words for discarded packets to the receive FIFO. See the Receive Status Word Section for more details on status word configuration.

Note that receive FIFO underflow is not listed as a discard condition in Table 10. That is, packets are not discarded when corrupted by receive FIFO underflow. However, receive FIFO underflow does cause the assertion of RXDC.

Table 10. Receive Discard Conditions

Discard Condition	Description
Receive FIFO Overflow	Receive FIFO full. No more data accepted from the 8B10B PCS.
CRC Error	Receive packet has CRC Error
Undersize Packet	Receive packet is less than 64 bytes, exclusive of preamble & SFD
Oversize Packet	Receive packet is greater than maximum packet size, exclusive of preamble & SFD
PCS Codeword Error	Receive packet contains at least one word with 8B10B PCS coding error.
RXABORT Pin	RXABORT pin was asserted while the receive packet was read out on the System Interface. The process of flushing a receive packet with RXABORT pin requires extra SCLK cycles equal to the [(packet length in bytes)/8 + 6].

3.9.4 Discard Output Indication

When a discard condition is detected on a packet that is being received or transmitted over the System Interface, the TXDC and RXDC output pins are asserted to indicate that the discard error was detected. TXDC and RXDC are normally latched high when a discard takes place. TXDC and RXDC can be cleared low by asserting the clearing pins, CLR_TXDC and CLR_RXDC, respectively. When the CLR_TXDC and CLR_RXDC pins are asserted, the TXDC and RXDC outputs are cleared two SCLK after the clearing signal was asserted.

3.9.5 AutoClear Mode

TXDC and RXDC can be made to automatically self clear by putting the device in the AutoClear mode. The AutoClear mode is enabled by setting the AutoClear enable bit in the Configuration 3 register. When the device is in the AutoClear mode, TXDC and RXDC are automatically cleared three SCLK cycles after the next end of the packet occurs (TXEOF and RXEOF).

3.9.6 AutoAbort Mode

When the AutoClear mode is enabled, the device can also be made to automatically abort the current packet on the System Interface in the receive FIFO when a discard condition is detected and RXDC is asserted. This is referred to as AutoAbort mode. The AutoAbort mode is enabled by setting the AutoAbort bit in the Configuration 3 register.

3.10 RECEIVE STATUS WORD

3.10.1 General

A 32-bit status word can be appended to the end of each good receive data packet and stored in the receive FIFO. This status word contains a byte count and error information for the receive data packet.

3.10.2 Format

The format for the status word is shown in Table 11. The top 16-bits contain the actual byte count for the packet, and the bottom 16-bits contain the status information related to the packet. Note that the endian select bit will affect the byte order of the status word in the same way that it affects normal data byte order on the System Interface.

The byte count value in the status word is the total number of actual bytes in the received packet minus the preamble & SFD bytes and CRC bytes. The byte count is independent of whether the preamble or CRC has been stripped by the receive MAC. If the packet overflows the receive FIFO, then the byte count will stop counting at the moment that the receive FIFO overflow has been detected and the remaining bytes on incoming packet will not be counted.

3.10.3 Append Options

The status word is normally appended to the end of all good receive packets. However, the device can also be programmed to either (1) store a status word in the receive FIFO for discarded packets as well as append a status word to the end of good (non-discarded) packets, or (2) not append any status word at all. These status word options can be selected by appropriately setting the receive status word append bits in the Configuration 1 register.

3.10.4 Status Word for Discarded Packets

When the device is programmed to add a status word for discarded packets, only the status word is stored in the receive FIFO for each discarded packet. The status word for a discarded packet contains an indication of the error that caused the discard. If the receive FIFO is full and more than one consecutive packet was discarded, then one more status word is stored in the receive FIFO for the next consecutive group of discarded packets, and a bit is set in the status word indicating that multiple status words have been discarded. When a status word has the multiple discard bit set, then the other status bits reflect the status of the second discarded packet only.

3.10.5 Status Word for RXABORT Packets

When the RXABORT pin is asserted, both the packet data and its associated status word are normally flushed from the receive FIFO. The device can be programmed to allow the RXABORT pin to discard the packet data only and leave the status word for the aborted packet in the receive FIFO by setting the RXABORT definition bit in the Configuration 3 register.

3.11 AUTONEGOTIATION

3.11.1 General

The AutoNegotiation algorithm is a negotiation sequence between two stations over the 10-Bit PHY Interface that (1) establishes a good link between two stations, and (2) configures both stations for the same mode of operation. The AutoNegotiation algorithm in the 8101 meets all specifications defined in IEEE 802.3z.

AutoNegotiation uses a stream of /C/ ordered sets to pass an AutoNegotiation data word to and from a remote station. The /C/ ordered set stream consists of an alternating sequence of /C1/ and /C2/ ordered sets. The /C1/ and /C2/ ordered sets are composed of two unique 10B code words plus a 16-bit AutoNegotiation data word, as defined in IEEE 802.3z and shown in Figure 6.

The AutoNegotiation algorithm is initiated by any of the following conditions: (1) device reset, (2) AutoNegotiation restart bit set, (3) /C/ ordered sets received from remote end, or (4) device reacquires receive word synchroniza-

Table 11. Receive Status Word Definition

RXD31 … RXD16

BC15	BC14	BC13	BC12	BC11	BC10	BC9	BC8	BC7	BC6	BC5	BC4	BC3	BC2	BC1	BC0
										MPKT	CWRD	OSIZE	USIZE	OVFL	CRC

RXD15 … RXD0

Symbol	Name	Definition	Position on RXD[31:0][1]
BC[15:0]	Byte Count	Contains Actual Byte Count of Receive Packet	RXD[31:16]
---	---	Reserved	RXD[15:6]
MPKT	Multiple Packet Reject	1 = RX FIFO full and multiple consecutive packets were discarded. Status word indicates error condition for first packet of discarded group.	RXD5
CWRD	Codeword Error	1 = Receive Packet Has PCS Coding Error	RXD4
OSIZE	Oversize Packet	1 = Receive Packet is Greater Than Maximum Size	RXD3
USIZE	Undersize Packet	1 = Receive Packet is Less Than Minimum Size	RXD2
OVFL	Receive FIFO Overflow	1 = Receive FIFO is Full and Has Received Additional Data	RXD1
CRC	CRC Error	1 = Receive Packet has a CRC Error	RXD0

Note 1: This byte order is for to little endian format. Big endian format will reverse this byte order.

tion. Once a negotiation has been initiated, the device uses the contents of the AutoNegotiation Base Page Transmit register to advertise its capabilities to a remote device. The remote device does the same, and the capabilities read back from the remote device are stored in the AutoNegotiation Base Page Receive register. The device's advertised capabilities can then be externally compared to the capabilities received from the remote device, and the device can then be configured for a compatible mode of operation. The 8101 also has Next Page capability. For a complete description of the AutoNegotiation algorithm in the device, refer to IEEE 802.3z clause 37 specification.

If the 8B10B PCS receiver has lost word synchronization, the device needs to acquire synchronization before AutoNegotiation words can be successfully received. While it is in the loss of synchronization state, the transmitter outputs /C/ ordered sets with the remote fault bits set to RF[1:0]=01 to indicate the link failure condition to the remote end. Once the 8B10B PCS receiver has acquired word synchronization, then the negotiation process is ready to begin.

3.11.2 Next Page

The device also has the Next Page capability defined in IEEE 802.3z. The Next Page feature allows the transfer of additional 16-bit data words between stations during a negotiation sequence in addition to the original base page message information. These additional 16-bit data words are referred to as next pages and can contain any arbitrary data.

If a next page is to be transmitted, the next page bit must be written to NP=1 in the AutoNegotiation Base Page Transmit register to indicate this to the remote station. Conversely, if a remote station wants the send a next page to the device, it will set the next page bit NP=1 in the base page, which is stored in the AutoNegotiation Base Page Receive register. The next pages to be transmitted to the remote station have to be written into the AutoNegotiation Next Page Transmit register in order to be transmitted. The next pages received from the remote station are stored in the AutoNegotiation Next Page Receive register. Both stations must have the Next Page functionality for a successful next page transfer. Next Page operation is complicated; refer to IEEE 802.3z for a full description of how this feature works.

There are status bits related to Next Page operation. See the Negotiation Status section for details.

3.11.3 Negotiation Status

There are bits in the Status 1 register which indicate the status of AutoNegotiation. These bits are summarized in Table 12 and are also described in more detail in the Status 1 register description. Some of the bits related to AutoNegotiation can programmed to set interrupt, as described in the Status 1 register description.

Table 12. AutoNegotation Status Bits

Bit No.	Bit Name	What Bit Indicates
11.11	LINK	Link is up, AutoNegotation has compeleted.
11.7	AN_NP	One TX and one RX Next Page has been exchanged.
11.6	AN_TX_NP	One Next Page has been transmitted.
11.5	AN_RX_NP	One Next Page has been received.
11.4	AN_RX_BP	Base Page has been received.
11.3	AN_REM_RST	AutoNegotiation was restarted by remote station.

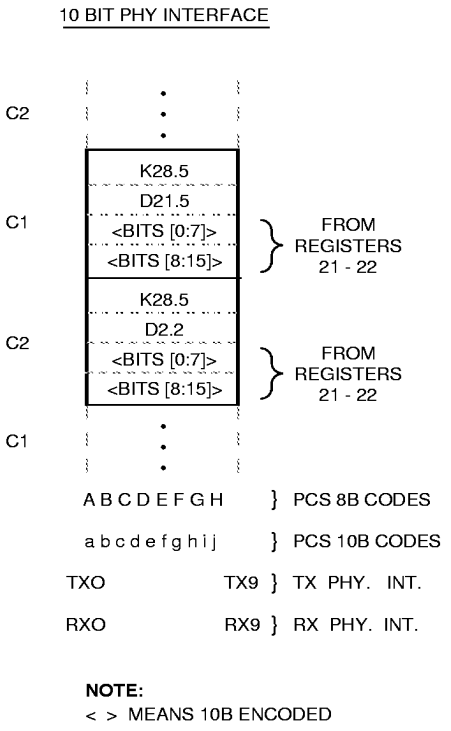


Figure 6. AutoNegotiation Data Format

3.11.4 AutoNegotiation Restart

The AutoNegotiation algorithm can be restarted by setting the AutoNegotiation restart bit in the Configuration 1 register. The AutoNegotiation restart bit clears itself automatically once the AutoNegotiation process starts transmitting /C/ ordered sets.

3.11.5 AutoNegotiation Enable

The AutoNegotiation algorithm can be enabled by setting the AutoNegotiation disable bit in the Configuration 3 register. When AutoNegotiation is disabled, the transmitter will output /I/ ordered sets.

3.11.6 Link Indication

The successful completion of the AutoNegotiation process (and by definition the receiver has also acquired word synchronization) is indicated by (1) asserting the $\overline{LINK}$ pin active low, and (2) setting the link detect status bit in the Status 1 Register. The $\overline{LINK}$ output can drive an LED from VCC or GND and also drive another digital input.

3.12 FLOW CONTROL

Flow control refers to the ability to cause a remote station to temporarily halt sending packets in order to prevent packet loss in a congested system. The 8101 uses MAC Control frames for flow control, per IEEE 802.3x specifications. Refer to the MAC Control Frame section for more details on the MAC Control Frame flow control scheme.

3.13 MAC CONTROL FRAMES

3.13.1 General

MAC Control frames are packets which pass signaling information between stations and are specified in IEEE 802.3 Clause 31. MAC Control frames are used primarily for flow control.

MAC Control frames defined in IEEE 802.3 Clause 31 are differentiated from other packets by having the unique value of **8808H** in the length/type field. MAC Control frames have the same packet format as normal Ethernet packets except the Data field is composed of an opcode field and a parameter field. The opcode field contains an opcode command, the parameter field contains a value associated with the opcode command. The only opcode command defined to date by IEEE 802.3x is the Pause opcode; the parameter field for the Pause opcode defines the pause time. MAC Control frames with the Pause opcode, referred to as Pause frames, are only allowed to have a destination address equal to a specific reserved multicast address or the address of the receive station itself. The value of the reserved multicast address is **01-80-C2-00-00-01H.**

The 8101 normally treats MAC Control frames according to the IEEE 802.3 Clause 31 algorithm. When the receive MAC detects a MAC Control frame with a Pause opcode and with the destination address equal to the reserved multicast address or the address stored in the MAC Address 1-3 registers, then the transmitter is paused for a time equal to the number of pause times specified in the parameter field. Each unit of pause time equals 512 bits (512 nS for Gigabit). If a Pause frame is received while another packet is being transmitted, then the transmission is completed for the current packet being transmitted, and then the transmitter is paused. If there are other packets in the transmit FIFO, their transmission will be delayed until the pause timer has expired. MAC Control frames are not normally passed into the receive FIFO; they are terminated in the receive MAC.

The 8101 also has incorporated some additional features to facilitate MAC Control frame operation. These features are described in the following sections.

3.13.2 Automatic Pause Frame Generation

Pause frames can be automatically generated when either (1) the FCNTRL pin is asserted, or (2) The receive FIFO data exceeds the MAC Control Autosend threshold. These automatically generated Pause frames, referred to as autogenerated Pause frames, will be internally generated and transmitted over the 10-Bit PHY Interface. The transmission of autogenerated Pause frames is not affected by the reception of a receive Pause frame; receive Pause frames only inhibit the transmission of regular packets from the transmit FIFO.

If a packet transmission is in progress when an autogenerated Pause frame is to be transmitted, the device will wait until the transmission of that packet has completed and then transmit the autogenerated Pause frame before any other subsequent packets in the TX FIFO are transmitted. When the first autogenerated Pause frame begins transmission, an internal timer will start whose value is equal to the pause_time value in the pause frame (and obtained from Flow Control Register 2). If the FCNTRL pin is still asserted or the MAC Control Frame Autosend threshold is still exceeded when the internal pause timer expires, then another autogenerated Pause frame will be transmitted. This process will continue to repeat itself as long as FCNTRL remains asserted or the MAC Control Frame Autosend threshold is exceeded. When FCNTRL is deasserted and the MAC Control Autosend threshold is not exceeded, then one last autogenerated Pause frame of pause_time=0 will be transmitted. To compensate for latency, the internal pause timer will be internally shorten itself by 32 units from the value programmed into the Flow Control 2 register.

The device can be programmed to eliminate the last autogenerated Pause frame with pause_time = 0 by clearing low the MAC Control frame end pause bit in the Flow Control 1 register.

The structure of the autogenerated Pause frame is described in Figure 7. Note that the source address and pause_time parameter fields are programmable through internal registers as shown in Figure 7.

The FNTRL pin and the MAC Control Autosend threshold can be individually disabled, that is, they can be programmed to no longer initiate the transmission of autogenerated Pause frames. The FCNTRL pin is default enabled but it can be disabled by setting the FCNTRL pin disable bit in Configuration 3 register. The MAC Control Autosend is default disabled, but can be enabled by appropriately setting the MAC Control Autosend threshold bits in the Flow Control 1 register.

3.13.3 Transmitter Pause Disable

*Receive Pause frames normally pause the transmitter. Receive Pause frames can be programmed to **not** pause the transmitter by clearing the MAC Control frame enable bit in the Flow Control 1 Register. When this bit cleared low, received Pause frames do not affect the transmitter.*

3.13.4 Passthrough to FIFO

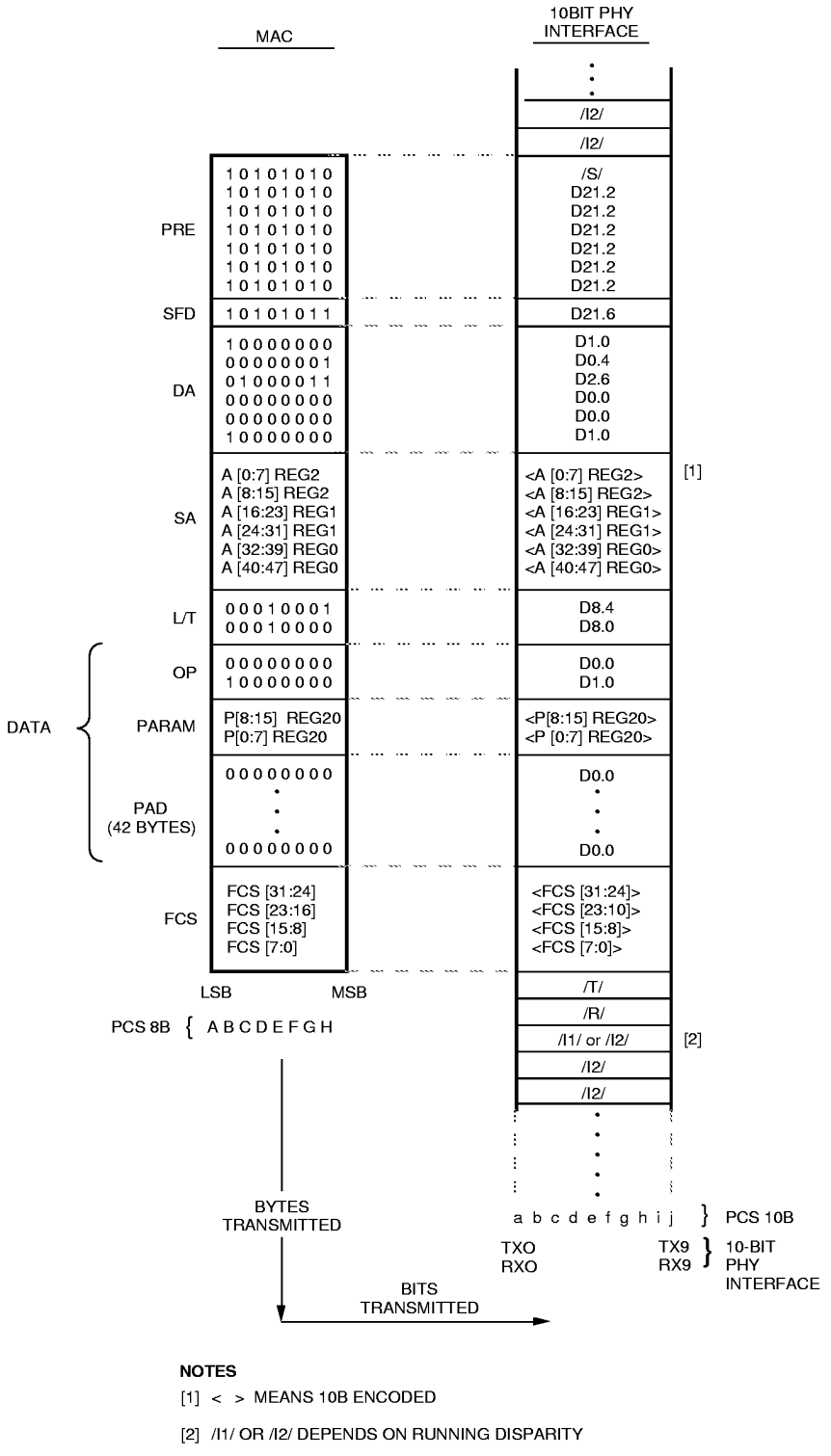
*Receive Pause frames are normally discarded and not passed to the receive FIFO. Receive Pause frames **can** be passed to the receive FIFO by appropriately setting the MAC Control frame passthrough bits in the Flow Control 1 register. These bits allow either all MAC Control frames or non-Pause frames only or Pause frames only to be passed to the receive FIFO.*

3.13.5 Reserved Multicast Address Disable

Receive Pause frames are normally rejected as invalid if they do not have the reserved multicast address in the destination address field. Receive Pause frames can be accepted without regard to the contents of the destination address field by appropriately setting the MAC Control frame address filter bit in the Flow Control 1 register. When this bit is cleared low, any value in the destination address field will be accepted as a valid address.

3.13.6 MAC Control Frame AutoSend

The transmission of autogenerated Pause frames can also be triggered by the level of data in the receive FIFO. This feature is referred to as MAC Control Frame AutoSend. The AutoSend feature can be enabled by appropriately setting the MAC Control Frame AutoSend bits in the Flow Control 1 register. When MAC Control Frame AutoSend is enabled, autogenerated Pause frames will be transmitted when the receive FIFO data exceeds a programmable threshold level, called the MAC Control AutoSend threshold. The MAC Control AutoSend threshold can be set with the four MAC Control frame autosend bits in the Flow Control 1 register. The automatic Pause frame generation mechanism is described in more detail in a previous section.



NOTES

[1] < > MEANS 10B ENCODED

[2] /I1/ OR /I2/ DEPENDS ON RUNNING DISPARITY

Figure 7. Autogenerated Pause Frame Format

3.14 RESET

The device has four resets. All four resets are described in Table 13. The device should be ready for normal operation 1 µS after the reset sequence has been completed for that bit.

Table 13. Reset Description

Name	Initiated By	Reset Action
Device Reset	1. RESET Pin Asserted Low	Reset Datapath
		Flush Transmit FIFO
	2. RST Bit in Config. 1	Flush Receive FIFO
		Reset Bits to Defaults
		Reset Counters to 0
Transmit Reset	TXRST Bit in Config 1	Reset Transmit Data Path
		Flush Transmit FIFO
		Reset TX Counters to 0
Receive Reset	RXRST Bit Config. 1	Reset Receive Data seperate path
		Flush Receive FIFO
		Reset RX Counters to 0
AutoNe-gotiation Restart	ANRST Bit in Config. 1	Starts AutoNegotiation Sequence
Counter Reset	CTRRST Bit in Config. 1	Reset Counters to 0

3.15 COUNTERS

3.15.1 General

The 8101 has a set of 53 management counters. Each counter is responsible for tabulating the number of times a specific event occurs. A complete list of all counters along with their definitions is shown in Table 15. These counters provide the necessary statistics to completely support the following specifications:

(1) RMON Statistics Group (IETF RFC1757)
(2) SNMP Interfaces Group (IETF RFC1213 & 1573)
(3) Ethernet-Like MIB (IETF RFC1643)
(4) Ethernet MIB (IEEE 802.3z Clause 30)

All counters are 32-bits wide. Each 32-bit counter result can be obtained by performing a read operation from two adjacent 16-bit register address locations over the Register Interface. The address locations for each counter are shown in both Table 15 and Table 17. For the two 16-bit register locations associated with each 32-bit counter, the register with the lower value address always contains the least significant 16-bits of the counter result. Thus, C0 of the lower value address register is the counter LSB; C15 of the higher value address register is the counter MSB.

When a counter read operation is initiated, the 32-bit counter result to be accessed is transferred to two internal 16-bit holding registers. These holding registers freeze and store the counter result for the duration of the read operation while allowing the internal counter to continue to increment if needed. The timing and delay associated with reading the counters is described in the Register Interface section and Register Interface Timing Characteristics.

When a counter is read out, the count can be automatically reset to zero or it can remain unchanged (programmable). Counters can be configured to either stop counting when they reach their maximum count or rollover (programmable).

Each counter has an associated status bit which is set when the counter becomes half full. These status bits can be individually programmed to assert interrupt.

The counter set in Table 15 includes the packet and octet statistics for transmit side as well as receive. The RMON specs literally state that packet and octet counters should only tabulate received information. This is sometimes interpreted to mean both transmitted and received information because Ethernet was originally a shared media protocol. As such, packet and octet counters for both transmit and receive are available in the device, and the transmit and receive packet and octets counts can be summed together if desired.

The exact correspondence of the actual MIB objects from the IETF and IEEE specifications to the actual 8101 counters locations is described in the Applications section and is shown there in Tables 45-48.

3.15.2 Counter Half Full

Each 32-bit counter has a half full status output bit associated with that counter. The half full bits are stored in the Counter Half Full 1-4 registers. These half full bits are set when the counter value reaches 80000000H (i.e. MSB bit goes from a 0 to a 1), so they go high when the counter becomes half full.

The counter half full bits will latch themselves when they go high, and each bit will stay latched high until either (1) the bit is read out, or (2) the counter register which the bit is associated with is read out. Counter half full bits are also interrupt bits; that is, the setting of any counter half full bit can be programmed to cause the assertion of the interrupt pin, REGINT. When a counter half full bit is cleared low by a read, the interrupt caused by that bit is also cleared. Note that REGINT stays asserted until all interrupt bits are

cleared. Each counter half full bit can be individually programmed to assert (or not assert) interrupt by appropriately setting the mask bit associated with that counter half full bit in Counter Half full Mask 1-4 registers.

3.15.3 Counter Reset On Read

The counter value is normally unaffected by a read operation on that counter. However, the counters can be programmed to automatically reset the count to zero when read out by appropriately setting the counter reset on read bit in the Configuration 3 Register.

When the counter reset on read bit is set high, a counter is reset to zero whenever any one of the two 16-bit counter registers associated with a 32-bit counter is read out. There is an internal holding register inside the device which stores the entire 32-bit counter result so that the 32-bit result will be correctly read out as long as two successive 16-bit counter register reads are performed from the same counter.

When the counter reset on read bit is cleared low (default), the count inside the counters is unaffected by a read as long as the counter is not at maximum count. If a counter is at maximum count, itís count is always reset to zero when it is read out.

3.15.4 Counter Rollover

The counters normally rollover to zero when they exceed their maximum count (i.e. receive an increment when counter is at maximum count). The counters can be programmed to freeze and stop counting once they reach their maximum count by setting the counter rollover bit in the Configuration 3 register.

3.15.5 Counter Maximum Packet Size

The maximum packet size used for the management counter statistics can be programmed to be one of four values by appropriately setting the counter packet size select bits in the Configuration 4 register. This selection is described in the register descriptions for those registers and is also summarized in Table 14.

The bits in Table 14 affect the maximum packet size for the counters only; the maximum packet size for the MAC section is determined by other bits as described in the Receive MAC section.

Table 14. Counter Maximum Packet Size Selection

Counter Max Packet Size Select Bits 10.[7:6]	Max Packet Size (bytes)
11	Unlimited
10	1535
01	1522
00	1518

3.15.6 Counter Reset

All counters can be reset to all zeroes by setting the counter reset bit in the Configuration 1 register. Asserting the device reset pin RESET will also reset the counters to zero.

Table 15. Counter Definition

Ctr. #	Counter Name (MIB Object Name)	Counter Description			
		RX/ TX	Definition	Size (Bits)	Register Address REGAD[7:0] (Lo/Hi)
RMON Statistics Group MIB (RFC 1757)					
1	etherStatsDropEvents	RX	Packets with receive FIFO overflow error.	32	10000000 10000001
2	etherStatsOctets	RX	Bytes, exclusive of preamble, in good or bad packets. Bytes in packets with bad SFD are excluded. [6]	32	10000010 10000011
3	etherStatsPkts	RX	All packets, good or bad. [6]	32	10000100 10000101
4	etherStatsBroadcastPkts	RX	Broadcast packets, good only. [6]	32	10000110 10000111
5	etherStatsMulticastPkts	RX	Multicast packets, good only. [6]	32	10001000 10001001

Table 15. Counter Definition (cont'd)

Ctr. #	Counter Name (MIB Object Name)	Counter Description			
		RX/ TX	Definition	Size (Bits)	Register Address REGAD[7:0] (Lo/Hi)
6	etherStatsCRCAlignErrors	RX	Packets of legal-length with CRC error or alignment error. There are no alignment errors in 8B10B Gigabit Ethernet, so this counter will only count CRC errors for legal length packets.	32	10001010 10001011
7	etherStatsUndersizePkts	RX	Packets of length <64 bytes with no other errors.	32	10001100 10001101
8	etherStatsOversizePkts	RX	Packets of length > Max_Packet_Length with no other errors.	32	10001110 10001111
9	etherStatsFragments	RX	Packets of length < 64 bytes with CRC error or alignment error. There are no alignment errors in 8B10B Gigabit Ethernet, so this counter will only count CRC errors with length < 64.	32	10010000 10010001
10	etherStatsJabber	RX	Packets of length > Max_Packet_Length with CRC error or alignment error. There is no jabber function in Gigabit Ethernet, so this counter is undefined	32	10010010 10010011
11	etherStatsCollisions	TX/ RX	CRS asserted and one or more collsions occurred. Since device is Full Duplex only, this counter is undefined.	32	10010100 10010101
12	etherStatsPkts64Octets	RX	Packets of length = 64 bytes, good or bad. [6]	32	10010110 10010111
13	etherStatsPkts65to127Octets	RX	Packets of length between 65-127 bytes, inclusive, good or bad. [6]	32	10011000 10011001
14	etherStatsPkts128to255Octets	RX	Packets of length between 128-255 bytes, inclusive, good or bad. [6]	32	10011010 10011011
15	etherStatsPkts256to511Octets	RX	Packets of length between 256 and 511 bytes, inclusive, good or bad. [6]	32	10011100 10011101
16	etherStatsPkts512to1023Octets	RX	Packets of length between 512 and 1023 bytes, inclusive, good or bad. [6]	32	10011110 10011111
17	etherStatsPkts1024to1518Octets	RX	Packets of length between 1024 and Max_Packet_Length, inclusive, good or bad. [6]	32	10100000 10100001
18	etherStatsOctets_TX	TX	Bytes, exclusive of preamble, in good or bad packets. [6]	32	10100010 10100011
19	etherStatsPkts_TX	TX	All packets, good or bad. [6]	32	10100100 10100101
20	etherStatsBroadcastPkts_TX	TX	Broadcast packets, good only. [6]	32	10100110 10100111

Table 15. Counter Definition (cont'd)

Ctr. #	Counter Name (MIB Object Name)	Counter Description			
		RX/ TX	Definition	Size (Bits)	Register Address REGAD[7:0] (Lo/Hi)
21	etherStatsMulticastPkts_TX	TX	Multicast packets, good only. [6]	32	10101000 10101001
22	etherStatsPkts64Octets_TX	TX	Packets of length = 64 bytes, good or bad. [6]	32	10101010 10101011
23	etherStatsPkts65to127Octets_TX	TX	Packets of length between 65-127 bytes, inclusive, good or bad. [6]	32	10101100 10101101
24	etherStatsPkts128to255Octets_TX	TX	Packets of length between 128-255 bytes, inclusive, good or bad. [6]	32	10101110 10101111
25	etherStatsPkts256to511Octets_TX	TX	Packets of length between 256 and 511 bytes, inclusive, good or bad. [6]	32	10110000 10110001
26	etherStatsPkts512to1023Octets_TX	TX	Packets of length between 512 and 1023 bytes, inclusive, good or bad. [6]	32	10110010 10110011
27	etherStatsPkts1024to1518Octets_TX	TX	Packets of length between 1023 and Max_Packet _Length, inclusive, good or bad. [6]	32	10110100 10110101
SNMP Interfaces Group MIB (RFC 1213 & 1573)					
28	ifInOctets	RX	Bytes, including preamble, in good or bad packets.	32	10110110 10110111
29	ifInUcastPkts	RX	Unicast packets, good only.	32	10111000 10111001
	ifInMulticastPkts	RX	Multicast packets, good only. Equivalent to "etherStatsMulticastPkts"		Use Ctr. #5
	ifInBroadcastPkts	RX	Broadcast packets, good only. Equivalent to "etherStatsBroadcastPkts"		Use Ctr. #4
	ifInNUcastPkts	RX	Broadcast and multicast packets, good only. Equivalent to "etherStatsBroadcastPkts + etherStatsMulticastPkts"		Use Ctr. #4+5
	ifInDiscards	RX	Packets with receive FIFO overflow error. Equivalent to "etherStatsDropEvents"		Use Ctr. #1
	ifInErrors	RX	All packets, bad only. Equivalent to "etherStatsCRCAlignError + etherStatsUndersizePkts + etherStatsOversizePkts"		Use Ctr. #6+7+8
30	ifOutOctets	TX	Bytes, including preamble, in good or bad packets.	32	10111010 10111011
31	ifOutUcastPkts	TX	Unicast packets, good and bad.	32	10111100 10111101
32	ifOutMulticastPkts	TX	Multicast packets, good and bad.	32	10111110 10111111

Table 15. Counter Definition (cont'd)

Ctr. #	Counter Name (MIB Object Name)	Counter Description			
		RX/ TX	Definition	Size (Bits)	Register Address REGAD[7:0] (Lo/Hi)
33	ifOutBroadcastPkts	TX	Broadcast packets, good and bad.	32	11000000 11000001
	ifOutNUcastPkts	TX	Broadcast and multicast packets, good and bad. Equivalent to "ifOutMulticastPkts + ifOutBroadcastPkts"		Use Ctr. #32+33
34	ifOutDiscards	TX	Packets with transmit FIFO underflow error.	32	11000010 11000011
35	ifOutErrors	TX	All Packets, bad only, exclusive of legal-length errors.	32	11000100 11000101
Ethernet-Like Group MIB (RFC 1643)					
36	dot3StatsAlignmentErrors	RX	Packets with alignment error only. There are no alignment errors in 8B10B Gigabit Ethernet, so this counter is undefined.	32	11000110 11000111
	dot3StatsFCSErrors	RX	Packets with CRC error only. Equivalent to "etherStatsCRCAlignErrors"		Use Ctr. #6
38	dot3StatsSingleCollisionFrames	TX	Packets successfully transmitted after one and only one collision (ie: attempt value=2). Since device is Full Duplex only, this counter is undefined.	32	11001010 11001011
39	dot3StatsMultipleCollisionFrames	TX	Packets successfully transmitted after more than one collision (ie: 2<attempt value<16). Since device is Full Duplex only, this counter is undefined.	32	11001100 11001101
40	dot3StatsSQETestErrors	RX	Number of times SQE was asserted. There is no SQE for Gigabit Ethernet, so this counter is undefined.	32	11001110 11001111
41	dot3StatsDeferredTransmissions	TX	Packets deferred, i.e. packets whose transmission was delayed due to busy medium, on first attempt only. Since device is Full Duplex only, this counter is undefined.	32	11010000 11010001
42	dot3StatsLateCollisions	TX	Packets that encounter a late collision, i.e. encountered collisions more than 512 bit times into transmitted packet. A late collision is counted twice, as a collision and a late collision. Since device is Full Duplex only, this counter is undefined.	32	11010010 11010011

Table 15. Counter Definition (cont'd)

Ctr. #	Counter Name (MIB Object Name)	Counter Description			
		RX/ TX	Definition	Size (Bits)	Register Address REGAD[7:0] (Lo/Hi)
43	dot3StatsExcessiveCollisions	TX	Packets not successfully transmitted after more than 15 collisions (ie: attempt value=16). Since device is Full Duplex only, this counter is undefined.	32	11010100 11010101
	dot3StatsInternalMacTransmitErrors	TX	Packets with transmit FIFO underflow error. Equivalent to "ifOutDiscards"		Use Ctr. #34
44	dot3StatsCarrierSenseErrors	TX	Carrier sense dropout errors, i.e. number of times that carrier sense is not asserted or deasserted during packet transmission, without a collision. This counter is only incremented once per packet, regardless of the number of dropout errors in the packet There is no CRS loopback in 8B10B Ethernet, so this counter is undefined	32	11010110 11010111
	dot3StatsFrameTooLongs	RX	Packets of length > Max_Packet_Length with no other errors. Equivalent to "etherStatsOversizePkts"		Use Ctr. #8
	dot3StatsInternalMacReceiveErrors	RX	Packets with receive FIFO overflow error. Equivalent to "etherStatsDropEvents"		Use Ctr. #1
Ethernet MIB (IEEE 802.3z Clause 30)					
	aFramesTransmittedOK	TX	All packets, good only. Equivalent to "etherStatsPkts_TX - ifOutErrors"		Use Ctr. #19-35
	aSingleCollisionFrames	TX	Packets successfully transmitted after one and only one collision (ie: attempt value=2). Equivalent to "dot3StatsSingleCollisionFrames"		Use Ctr. #38
	aMultipleCollisionFrames	TX	Packets successfully transmitted after more than one collision (ie: 2<attempt value<16). Equivalent to "dot3StatsMultipleCollisionFrames"		Use Ctr. #39
	aFramesReceivedOK	RX	All packets, good only. Equivalent to "ifInUcastPkts + etherStatsBroadcastPkts + etherStatsMulticastPkts"		Use Ctr. #29+4+5
	aFrameCheckSequenceErrors	RX	Packets with CRC error only. Equivalent to "dot3StatsFCSErrors"		Use Ctr. #37
	aAlignmentErrors	RX	Packets with alignment error only. Equivalent to "dot3StatsAlignmentErrors"		Use Ctr. #36

Table 15. Counter Definition (cont'd)

Ctr. #	Counter Name (MIB Object Name)	Counter Description			
		RX/ TX	Definition	Size (Bits)	Register Address REGAD[7:0] (Lo/Hi)
45	aOctetsTransmittedOK	TX	Bytes, exclusive of preamble, in good packets only.	32	11011000 11011001
	aFramesWithDeferredXmissions	TX	Packets deferred, i.e. packets whose transmission was delayed due to busy medium, on first attempt only. Equivalent to "dot3StatsDeferredTransmissions"		Use Ctr. #41
	aLateCollisions	TX	Packets that encounter a late collision, i.e. encountered collisions more than 512 bit times into transmitted packet. A late collision is counted twice, as a collision and a late collision. Equivalent to "dot3StatsLateCollisions"		Use Ctr. #42
	aFrameAbortedDueToXSCollisions	TX	Packets not successfully transmitted after more than 15 collisions (ie: attempt value=16). Equivalent to "dot3StatsExcessiveCollisions"		Use Ctr. #43
	aFrameAbortedDueToIntMACXmitError	TX	Packets with transmit FIFO underflow error. Equivalent to "ifOutDiscards"		Use Ctr. #34
	aCarrierSenseErrors	TX	Carrier sense dropout errors, i.e. number of times that carrier sense is not asserted or deasserted during packet transmission, without a collision. This counter is only incremented once per packet, regardless of the number of dropout errors in the packet Equivalent to "dot3StatsCarrierSenseErrors"		Use Ctr. #44
46	aOctetsReceivedOK	RX	Bytes, exclusive of preamble in good packets only.	32	11011010 11011011
	aFramesLostDueToIntMACRcvrError	RX	Packets with receive FIFO overflow error. Equivalent to "etherStatsDropEvents"		Use Ctr. #1
	aMulticastFrameXmittedOK	TX	TX Multicast packets, good only. Equivalent to "etherStatsMulticastPkts_TX"		Use Ctr. #21
	aBroadcastFramesXmittedOK	TX	TX Broadcast packets, good only. Equivalent to "etherStatsBroadcastPkts_TX"		Use Ctr. #20
47	aFramesWithExcessiveDefferal	TX	Packets with excessive deferral, i.e. packets waiting for transmission longer than two max packet times. Since device is Full Duplex only, this counter is undefined.	32	11011100 11011101
	aMulticastFramesReceivedOK	RX	Multicast packets, good only. Equivalent to "etherStatsMulticastPkts"		Use Ctr. #5
	aBroadcastFramesReceivedOK	RX	Broadcast packets, good only. Equivalent to "etherStatsBroadcastPkts"		Use Ctr. #4

Table 15. Counter Definition (cont'd)

Ctr. #	Counter Name (MIB Object Name)	Counter Description			
		RX/ TX	Definition	Size (Bits)	Register Address REGAD[7:0] (Lo/Hi)
48	aInRangeLengthErrors	RX	Packets of legal-length whose actual length is different from length/type field value.	32	11011110 11011111
49	aOutOfRangeLengthField	RX	Packets with length/type field value > Max_Packet_Length.	32	11100000 11100001
	aFrameTooLongErrors	RX	Packets of length > Max_Packet_Length with no other errors. Equivalent to "etherStatsOversizePkts"		Use Ctr. #8
	aSQETestErrors	RX	Number of times SQE was asserted. Equivalent to "dot3StatsSQETestError"		Use Ctr. #40
50	aSymbolErrorDuringCarrier	RX	One or more symbol errors received from a PHY during packet reception, exclusive of collision. This counter is only incremented once per packet, regardless of the number of symbol errors in that packet.	32	11100010 11100011
	aMACControlFramesTransmitted	TX	Valid MAC Control packets. Equivalent to "aPauseMACCtrlFramesTransmitted"		Use Ctr. #52
	aMACControlFramesReceived	RX	Valid MAC Control packets. Equivalent to "aPauseMACCtrlFramesReceived"		Use Ctr. #53
51	aUnsupportedOpcodesReceived	RX	Valid MAC Control packets with non-Pause opcode.	32	11100100 11100101
52	aPauseMACCtrlFramesTransmitted	TX	Valid MAC Control packets with Pause opcode.	32	11100110 11100111
53	aPauseMACCtrlFramesReceived	RX	Valid MAC Control packets with Pause opcode.	32	11101000 11101001

1. Bad RX packet = legal-length error, CRC error , receive FIFO overflow, symbol error.
   Where: CRC Error is bad FCS with an integral number of octets.
   Alignment Error is bad FCS with non-integral number of octets.
   Symbol Error is an invalid codeword or a /V/.
2. Bad TX packet = legal-length error, transmit FIFO underflow.
3. Legal-length packet is between 64 and Max_Packet_Length in bytes. Preamble is not included in length count.
4. Max_Packet_Length for the counters can be programmed to be either 1518, 1522, 1535, or unlimited bytes. 1518 is default for both transmit and receive.
5. The counter result is stored in two 16-bit registers. Thus, there are two register addresses for each counter. Of the two registers for a given counter, the register with the lower value address contains the least significant counter bits.
6. The RMON specs explicitly states that packet and octet counters should only tabulate received information. This is sometimes interpreted to mean both transmitted and received information because Ethernet was originally a shared media. As such, transmit packet and octet counters are also available in counters 18-27 and can be summed with receive packet and octet counts ifdesired.

3.16 LOOPBACK

A diagnostic loopback mode can be enabled by setting the loopback enable bit in the Configuration 4 register. When the loopback mode is enabled, the transmit data that is input to the transmit System Interface and output from the 8B10B Encoder is internally looped back into the receive 8B10B Decoder and is available to be read from the receive System Interface.

3.17 TEST MODES

The TEST pin is reserved for factory test. TEST must be tied low for normal operation.

All inputs and outputs can be made to go to the high impedance state by asserting the TAP pin active high. This pin is intended for device and board diagnostic testing.

3.18 REGISTER INTERFACE

3.18.1 General

The Register Interface is a 16-bit bidirectional data interface that allows access to the internal registers. The Register Interface consists of twenty nine signals: sixteen bidirectional data I/O bits (REGD[15:0]), eight register address inputs (REGA[7:0]), one chip select input (REGCS), one clock input (REGCLK), one read select input (REGRD), one write select input (REGWR), and one interrupt output (REGINT). The REGCLK, clock frequency must be between 5-40 Mhz.

All register accesses are done on a single rising edge of the REGCLK clock. To access a register through the Register Interface, REGCS needs to be asserted active low and is sampled on rising edges of REGCLK. On that same rising edge of REGCLK, the address of the register that will be accessed is clocked in on REGA[7:0]. On that same rising edge of REGCLK, either REGRD or REGWR also needs to be asserted active low and one of these will be clocked into the device; which signal is asserted will determine whether this is a read or write cycle. If the cycle is a write cycle, then data to be written to a specific register will be clocked in on the rising edge of the same clock that clocked in the other inputs. If the cycle is a read cycle, then data will be output on REGD[15:0] after some delay after the rising edge of REGCLK that clocked in the input information. REGCS can remain low for multiple REGCLK cycles so that many registers can be read or written to in one REGCS assertion.

During read cycles, the delay from REGCLK to data valid on REGD[15:0] pins is a function of which register is being accessed. Data read from any register, exclusive of the Counter 1-53 registers, appears on the REGD[15:0] pins in one REGCLK cycle. Data read from the Counter 1-53 registers takes at most 6 REGCLK cycles to be available on REGD[15:0] for the first 16-bits of counter result, and at most 3 REGCLK cycles for the second 16-bits of the counter result. Refer to the Register Interface Timing Characteristics for more details.

3.18.2 Bit Types

The Register Interface is bidirectional, and there are many types of bits in the registers. The bit type definitions are summarized in Table 16. Write bits (W) are inputs during a write cycle and are logic 0 during read cycle. Read bits

Table 16. Register Bit Type Definition

Sym.	Name	Definition	
		Write Cycle	Read Cycle
W	Write	Input	No Operation Output Not Valid
R	Read	No Operation, Input Ignored	Output
R/W	Read/ Write	Input	Ouput
R/W SC	Read/ Write Self Clearing	Input Clears Itself After Operation Completed	Ouput
R/LL R/LLI	Read/ Low with Interrupt	No Operation Latching	Output Input Ignored When Bit Goes Low, Bit Latched & Interrupt Asserted (If Not Masked) When Bit Is Read Bit Updated and Interrupted Cleared
R/LH R/LHI	Read/ Latching High with Interrupt	No Operation, Input Ignored	Output When Bit Goes High, Bit Latcched & Interrupt Assert (If Not Masked) When Bit Is Read, Bit Updated and Interrupt Cleared
R/LT R/LTI	Read/ Latching on Transition with Interrupt	No Operation, Input Ignored	Output When Bit Transitions, Bit Latched and Interrupt Asserted (if Not Masked) When Bit Is Read, Bit Updated and Interrupt Cleared

(R) are outputs during a read cycle and ignored and high impedance during a write cycle. Read/Write bits (R/W) are actually write bits which can be read out during a read cycle. R/WSC bits are R/W bits that are self clearing after a set period of time or after a specific event has completed. R/LL bits are read bits that latch themselves when they go low, and they stay latched low until read. After they are read, they are reset high. R/LH bits are the same as R/LL bits except that they latch high. R/LT are read bits that latch themselves whenever they make a transition or change value, and they stay latched until they are read. After R/LT bits are read, they are updated to their current value. R/LLI, R/LHI, and R/LTI bits function the same as R/LL, R/LH and R/LT bits, respectively, except they also assert interrupt if programmed to do so (not masked). Interrupt bits are described in more detail in the Interrupt section.

3.18.3 Interrupt

An interrupt is triggered when certain output status bits change state. These bits are called interrupt bits and are designated as R/LLI, R/LHI, and R/LTI bits as descriibed in the previous section. The interrupt bits reside in the Status 1 and Counter Half Full 1-4 registers. Interrupt bits automatically latch themselves and assert the interrupt pin, REGINT, when they latch themselves. Interrupt bits stay latched until they are read. When interrupt bits are read, the interrupt pin REGINT is deasserted and the interrupt bits that caused the interrupt to happen are updated to their current value. Each interrupt bit can be individually masked and subsequently be removed as an interrupt bit by setting the appropriate mask register bits in the Status 1 Mask and Counter Half Full Mask 1-4 registers.

3.18.4 Register Structure

The device has 136 internal 16-bit registers. Twenty two registers are available for setting configuration inputs and reading status outputs, the remaining 114 registers are associated with the management cunters. The location of all registers is described in the register addressing table in Table 17. A register bit map is shown in Table 18. The definition of each bit of each register is described in Tables 19-43.

4.0 Registers

Table 17. Register Address Table

Register #	Register Address (REGAD[7:0] Pins)	Register Name
0	00000000	MAC Address 1
1	00000001	MAC Address 2
2	00000010	MAC Address 3
3	00000011	MAC Address Filter 1
4	00000100	MAC Address Filter 2
5	00000101	MAC Address Filter 3
6	00000110	MAC Address Filter 4
7	00000111	Configuration 1
8	00001000	Configuration 2
9	00001001	Configuration 3
10	00001010	Configuration 4
11	00001011	Status 1
12-13	00001100 - 00001101	Reserved
14	00001110	Status Mask 1
15-16	00001111 - 00010000	Reserved
17	00010001	Transmit FIFO Threshold
18	00010010	Receive FIFO Threshold
19	00010011	Flow Control 1
20	00010100	Flow Control 2
21	00010101	AutoNegotiation Base Page Transmit
22	00010110	AutoNegotiation Base Page Receive
23	00010111	AutoNegotiation Next Page Transmit
24	00011000	AutoNegotiation Next Page Receive
25-31	00011001- 00011111	Reserved
32	00100000	Device ID
33-111	00011001 - 01101111	Reserved
112-115	01110000 - 01110011	Counter Half Full 1-4
116-119	01110100 - 01110111	Reserved
120-123	01111000 - 01111011	Counter Half Full Mask 1-4
124-127	01111100 - 01111111	Reserved
128-129	10000000 - 10000001	Counter 1 - etherStatsDropEvents
130-131	10000010 - 10000011	Counter 2 - etherStatsOctets
132-133	10000100 - 10000101	Counter 3 - etherStatsPkts
134-135	10000110 - 10000111	Counter 4 - etherStatsBroadcastPkts
136-137	10001000 - 10001001	Counter 5 - etherStatsMulticastPkts
138-139	10001010 - 10001011	Counter 6 - etherStatsCRCAlignErrors

Table 17. Register Address Table (cont'd)

Register #	Register Address (REGAD[7:0] Pins)	Register Name
140-141	10001100 - 10001101	Counter 7 - etherStatsUndersizePkts
142-143	10001110 - 10001111	Counter 8 - etherStatsOversizePkts
144-145	10010000 - 10010001	Counter 9 - etherStatsFragments
146-147	10010010 - 10010011	Counter 10 - etherStatsJabber
148-149	10010100 - 10010101	Counter 11 - etherStatsCollisions
150-151	10010110 - 10010111	Counter 12 - etherStatsPkts64Octets
152-153	10011000 - 10011001	Counter 13 - etherStatsPkts65to127Octets
154-155	10011010 - 10011011	Counter 14 - etherStatsPkts128to255Octets
156-157	10011100 - 10011101	Counter 15 - etherStatsPkts256to511Octet
158-159	10011110 - 10011111	Counter 16 - etherStatsPkts512to1023Octets
160-161	10100000 - 10100001	Counter 17 - etherStatsPkts1024to1518Octets
162-163	10100010 - 10100011	Counter 18 - etherStatsOctets_TX
164-165	10100100 - 10100101	Counter 19 - etherStatsPkts_TX
166-167	10100110 - 10100111	Counter 20 - etherStatsBroadcastPkts_TX
168-169	10101000 - 10101001	Counter 21 - etherStatsMulticastPkts_TX
170-171	10101010 - 10101011	Counter 22 - etherStatsPkts64Octets_TX
172-173	10101100 - 10101101	Counter 23 - etherStatsPkts65to127Octets_TX
174-175	10101110 - 10101111	Counter 24 - etherStatsPkts128to255Octets_TX
176-177	10110000 - 10110001	Counter 25 - etherStatsPkts256to511Octets_TX
178-179	10110010 - 10110011	Counter 26 - etherStatsPkts512to1023Octets_TX
180-181	10110100 - 10110101	Counter 27 - etherStatsPkts1024to1518Octets_TX
182-183	10110110 - 10110111	Counter 28 - ifInOctets
184-185	10111000 - 10111001	Counter 29 - ifInUcastPkts
186-187	10111010 - 10111011	Counter 30 - ifOutOctets
188-189	10111100 - 10111101	Counter 31 - ifOutUcastPkts
190-191	10111110 - 10111111	Counter 32 - ifOutMulticastPkts
192-193	11000000 - 11000001	Counter 33 - ifOutBroadcastPkts
194-195	11000010 - 11000011	Counter 34 - ifOutDiscards
196-197	11000100 - 11000101	Counter 35 - ifOutErrors
198-199	11000110 - 11000111	Counter 36 - dot3StatsAlignmentErrors
200-201	11001000 - 11001001	Reserved
202-203	11001010 - 11001011	Counter 38 - dot3StatsSingleCollisionFrames
204-205	11001100 - 11001101	Counter 39 - dot3StatsMultipleCollisionFrames
206-207	11001110 - 11001111	Counter 40 - dot3StatsSQETestErrors
208-209	11010000 - 11010001	Counter 41 - dot3StatsDeferredTransmissions
210-211	11010010 - 11010011	Counter 42 - dot3StatsLateCollisions
212-213	11010100 - 11010101	Counter 43 - dot3StatsExcessiveCollisions
214-215	11010110 - 11010111	Counter 44 - dot3StatsCarrierSenseErrors

Table 17. Register Address Table (cont'd)

Register #	Register Address (REGAD[7:0] Pins)	Register Name
216-217	11011000 - 11011001	Counter 45 - aOctetsTransmittedOK
218-219	11011010 - 11011011	Counter 46 - aOctetsReceivedOK
220-221	11011100 - 11011101	Counter 47 - aFramesWithExcessiveDefferal
222-223	11011110 - 11011111	Counter 48 - aInRangeLengthErrors
224-225	11100000 - 11100001	Counter 49 - aOutOfRangeLengthField
226-227	11100010 - 11100011	Counter 50 - aSymbolErrorDuringCarrier
228-229	11100100 - 11100101	Counter 51 - aUnsupportedOpcodesReceived
230-231	11100110 - 11100111	Counter 52 - aPauseMACCtrlFramesTransmitted
232-233	11101000 - 11101001	Counter 53 - aPauseMACCtrlFramesReceived
234-255	11101010 - 11111111	Reserved

Table 18. Register Bit Map

Addr	Register Name	x.15	x.14	x.13	x.12	x.11	x.10	x.9	x.8	x.7	x.6	x.5	x.4	x.3	x.2	x.1	x.0
0	MAC Address 1-3	A47	A46	A45	A44	A43	A42	A41	A40	A39	A38	A37	A36	A35	A34	A33	A32
1		A31	A30	A29	A28	A27	A26	A25	A24	A23	A22	A21	A20	A19	A18	A17	A16
2		A15	A14	A13	A12	A11	A10	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0
		R/W 0	R/W 0	R/W 0	R/W 0	R/W 0	R/W 0	R/W 0	R/W 0	R/W 0	R/W 0	R/W 0	R/W 0	R/W 0	R/W 0	R/W 0	R/W 0
3	MAC Address Filter 1-4	F7[7]	F7[6]	F7[5]	F7[4]	F7[3]	F7[2]	F7[1]	F7[0]	F6[7]	F6[6]	F6[5]	F6[4]	F6[3]	F6[2]	F6[1]	F6[0]
4		F5[7]	F5[6]	F5[5]	F5[4]	F5[3]	F5[2]	F5[1]	F5[0]	F4[7]	F4[6]	F4[5]	F4[4]	F4[3]	F4[2]	F4[1]	F4[0]
5		F3[7]	F3[6]	F3[5]	F3[4]	F3[3]	F3[2]	F3[1]	F3[0]	F2[7]	F2[6]	F2[5]	F2[4]	F2[3]	F2[2]	F2[1]	F2[0]
6		F1[7]	F1[6]	F1[5]	F1[4]	F1[3]	F1[2]	F1[1]	F1[0]	F0[7]	F0[6]	F0[5]	F0[4]	F0[3]	F0[2]	F0[1]	F0[0]
		R/W 0	R/W 0	R/W 0	R/W 0	R/W 0	R/W 0	R/W 0	R/W 0	R/W 0	R/W 0	R/W 0	R/W 0	R/W 0	R/W 0	R/W 0	R/W 0
7	Configuration 1	RST	RXRST	TXRST	ANRST	CTRRST	APAD	IPG2	IPG1	IPG0	TXPRMBL	TXCRC	RXPRMBL	RXCRC	STSWRD1	STSWRD0	PEOF
		R/WSC 0	R/WSC 0	R/WSC 0	R/WSC 0	R/SCW 0	R/W 1	R/W 1	R/W 1	R/W 1	R/W 1	R/W 1	R/W 0	R/W 0	R/W 1	R/W 0	R/W 1
8	Configuration 2	REJUCST	REJMCST	REJBCST	REJALL	ACPTALL	DIS_OVF	DIS_CRC	DIS_USIZE	DIS_OSIZE	DISCWRD	DIS_RXAB	0	0	0	0	0
		R/W 0	R/W 0	R/W 0	R/W 0	R/W 0	R/W 1	R/W 1	R/W 1	R/W 1	R/W 1	R/W 1	R/W 0	R/W 0	R/W 0	R/W 0	R/W 0
9	Configuration 3	0	0	AUTOCLR	AUTORXAB	CTR_RD	CTR_ROLL	EWRAP	LCKREF	CDET	AN_EN	RMXPKT1	RMXPKT0	RXAB_DEF	SINTF_DIS	FCNTRL_DIS	SD_EN
		R/W 0	R/W 0	R/W 0	R/W 0	R/W 1	R/W 0	R/W 0	R/W 0	R/W 0	R/W 1	R/W 0	R/W 0	R/W 0	R/W 0	R/W 0	R/W 0
10	Configuration 4	ENDIAN	BUSSIZE	0	LPBK	LNKDN	TBC_DIS	0	0	CMXPKT1	CMXPKT0	0	0	0	0	0	0
		R/W 0	R/W 0	R/W 0	R/W 0	R/W 0	R/W 0	R/W 0	R/W 0	R/W 0	R/W 0	R/W 0	R/W 0	R/W 0	R/W 0	R/W 0	R/W 0
11	Status 1	RSYNC			SD	LINK				AN_NP	AN_TX_NP	AN_RX_NP	AN_RX_BP	AN_RMTRST			
		R/LTI 0			R 0	R/LTI 0				R/LHI 0	R 0	R 0	R 0	R/LHI 0			
14	Status Mask 1	MASK_ RSYNC	1	1	1	MASK_ LINK	1	1	1	MASK_ AN_NP	1	1	1	MASK_ AN_RMTRST	1	1	1
		R/W 1	R/W 1	R/W 1	R/W 1	R/W 1	R/W 1	R/W 1	R/W 1	R/W 1	R/W 1	R/W 1	R/W 1	R/W 1	R/W 1	R/W 1	R/W 1
17	Transmit FIFO Threshold	TWM1[4]	TWM1[3]	TWM1[2]	TWM1[1]	TWM1[0]	TWM2[4]	TWM2[3]	TWM2[2]	TWM2[1]	TWM2[0]	TASND5	TASND4	TASND3	TASND2	TASND1	TASND0
		R/W 1	R/W 0	R/W 0	R/W 0	R/W 0	R/W 1	R/W 1	R/W 0	R/W 0	R/W 0	R/W 1	R/W 0	R/W 0	R/W 0	R/W 0	R/W 0
18	Receive FIFO Threshold	RWM1[7]	RWM1[6]	RWM1[5]	RWM1[4]	RWM1[3]	RWM1[2]	RWM1[1]	RWM1[0]	RWM2[7]	RWM2[6]	RWM2[5]	RWM2[4]	RWM2[3]	RWM2[2]	RWM2[1]	RWM2[0]
		R/W 0	R/W 0	R/W 0	R/W 0	R/W 0	R/W 0	R/W 0	R/W 0	R/W 1	R/W 1	R/W 0	R/W 0	R/W 0	R/W 0	R/W 0	R/W 0

Table 18. Register Bit Map (cont'd)

Addr	Register Name	x.15	x.14	x.13	x.12	x.11	x.10	x.9	x.8	x.7	x.6	x.5	x.4	x.3	x.2	x.1	x.0
19	Flow Control 1	MCNTRL	MCPASS1	MCPASS0	MCFLTR	MCENDPS	MCASND3	MCASND2	MCASND1	MCASND0	0	0	0	0	0	0	0
		R/W 1	R/W 0	R/W 0	R/W 1	R/W 1	R/W 0	R/W 0	R/W 0	R/W 0	R/W 0	R/W 0	R/W 0	R/W 0	R/W 0	R/W 0	R/W 0
20	Flow Control 2	P15	P14	P13	P12	P11	P10	P9	P8	P7	P6	P5	P4	P3	P2	P1	P0
		R/W 1	R/W 1	R/W 1	R/W 1	R/W 0	R/W 0	R/W 0	R/W 0	R/W 0	R/W 0	R/W 0	R/W 0	R/W 0	R/W 0	R/W 0	R/W 0
21	AutoNegotiation Base Page Transmit	NP	ACK	RF2	RF1	0	0	0	PS_DIR	PS	HDX	FDX	0	0	0	0	0
		R/W 0	R/W 0	R/W 0	R/W 0	R/W 0	R/W 0	R/W 0	R/W 0	R/W 1	R/W 0	R/W 1	R/W 0	R/W 0	R/W 0	R/W 0	R/W 0
22	AutoNegotiation Base Page Receive	NP	ACK	RF2	RF1	0	0	0	PS_DIR	PS	HDX	FDX	0	0	0	0	0
		R 0	R 0	R 0	R 0	R 0	R 0	R 0	R 0	R 0	R 0	R 0	R 0	R 0	R 0	R 0	R 0
23	AutoNegotiation Next Page Transmit	NP	ACK	PAGETYPE	ACK2	TOGGLE	MSG10	MSG9	MSG8	MSG7	MSG6	MSG5	MSG4	MSG3	MSG2	MSG1	MSG0
		R/W 0	R/W 0	R/W 0	R/W 0	R/W 0	R/W 0	R/W 0	R/W 0	R/W 0	R/W 0	R/W 0	R/W 0	R/W 0	R/W 0	R/W 0	R/W 0
24	AutoNegotiation Next Page Receive	NP	ACK	PAGETYPE	ACK2	TOGGLE	MSG10	MSG9	MSG8	MSG7	MSG6	MSG5	MSG4	MSG3	MSG2	MSG1	MSG0
		R 0	R 0	R 0	R 0	R 0	R 0	R 0	R 0	R 0	R 0	R 0	R 0	R 0	R 0	R 0	R 0
32	Device ID	PART3	PART2	PART1	PART0	HREV3	HREV2	HREV1	HREV0					SREV3	SREV2	SREV1	SREV0
		R 0	R 0	R 0	R 1	R X	R X	R X	R X					R X	R X	R X	R X
112 113 114 115	Counter Half Full 1-4	HFULL15	HFULL14	HFULL13	HFULL12	HFULL11	HFULL10	HFULL9	HFULL8	HFULL7	HFULL6	HFULL5	HFULL4	HFULL3	HFULL2	HFULL1	HFULL0
		R/LHI 0	R/LHI 0	R/LHI 0	R/LHI 0	R/LHI 0	R/LHI 0	R/LHI 0	R/LHI 0	R/LHI 0	R/LHI 0	R/LHI 0	R/LHI 0	R/LHI 0	R/LHI 0	R/LHI 0	R/LHI 0
120 121 122 123	Counter Half Full Mask 1-4	MASK_ HFULL15	MASK_ HFULL14	MASK_ HFULL13	MASK_ HFULL12	MASK_ HFULL11	MASK_ HFULL10	MASK_ HFULL9	MASK_ HFULL8	MASK_ HFULL7	MASK_ HFULL6	MASK_ HFULL5	MASK_ HFULL4	MASK_ HFULL3	MASK_ HFULL2	MASK_ HFULL1	MASK_ HFULL0
		R/W 1	R/W 1	R/W 1	R/W 1	R/W 1	R/W 1	R/W 1	R/W 1	R/W 1	R/W 1	R/W 1	R/W 1	R/W 1	R/W 1	R/W 1	R/W 1
126	Counter 1	C15	C14	C13	C12	C11	C10	C9	C8	C7	C6	C5	C4	C3	C2	C1	C0
⋮	⋮		⋮				⋮				⋮				⋮		
233	Counter 53	C15	C14	C13	C12	C11	C10	C9	C8	C7	C6	C5	C4	C3	C2	C1	C0
		R 0	R 0	R 0	R 0	R 0	R 0	R 0	R 0	R 0	R 0	R 0	R 0	R 0	R 0	R 0	R 0

Table 19. Register 0 (MAC Address 1 Register) Definition

0.15	0.14	0.13	0.12	0.11	0.10	0.9	0.8
A47	A47	A45	A44	A43	A42	A41	A40
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

0.7	0.6	0.5	0.4	0.3	0.2	0.1	0.0
A39	A38	A37	A36	A35	A34	A33	A32
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Symbol	Name	Definition	R/W	Def.
0.15	A47	MAC Address, 1st Word	This is 1st of 3 Words That Comprise the 48-Bit MAC Address. The MAC Address is Used for (1) Receive Unicast Address Filtering of the DA, and (2) as the SA for Automatic Generated MAC Control Pause Frames. A0 corresponds to the first bit transmitted or received by the MAC section (DA[0] or SA[0] in Figure 3).	R/W	0
0.14	A46			R/W	0
0.13	A45			R/W	0
0.12	A44			R/W	0
0.11	A43			R/W	0
0.10	A42			R/W	0
0.9	A41			R/W	0
0.8	A40			R/W	0
0.7	A39			R/W	0
0.6	A38			R/W	0
0.5	A37			R/W	0
0.4	A36			R/W	0
0.3	A35			R/W	0
0.2	A34			R/W	0
0.1	A33			R/W	0
0.0	A32			R/W	0

x.15 Bit Occurs On REGD15 Pin

Table 20. Register 1 (MAC Address 2 Register) Definition

1.15	1.14	1.13	1.12	1.11	1.10	1.9	1.8
A31	A30	A29	A28	A27	A26	A25	A24
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

1.7	1.6	1.5	1.4	1.3	1.2	1.1	1.0
A23	A22	A21	A20	A19	A18	A17	A16
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Symbol	Name	Definition	R/W	Def.
1.15	A31	MAC Address, 2nd Word	This is 2nd of 3 Words That Comprise the 48-Bit MAC Address. The MAC Address is Used for (1) Receive Unicast Address Filtering of the DA, and (2) as the SA for Automatic Generated MAC Control Pause Frames. A0 corresponds to the first bit transmitted or received by the MAC section (DA[0] or SA[0] in Figure 3).	R/W	0
1.14	A30			R/W	0
1.13	A29			R/W	0
1.12	A28			R/W	0
1.11	A27			R/W	0
1.10	A26			R/W	0
1.9	A25			R/W	0
1.8	A24			R/W	0
1.7	A23			R/W	0
1.6	A22			R/W	0
1.5	A21			R/W	0
1.4	A20			R/W	0
1.3	A19			R/W	0
1.2	A18			R/W	0
1.1	A17			R/W	0
1.0	A16			R/W	0

x.15 Bit Occurs On REGD15 Pin

Table 21. Register 2 (MAC Address 3 Register) Definition

2.15	2.14	2.13	2.12	2.11	2.10	2.9	2.8
A15	A14	A13	A12	A11	A10	A9	A8
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

2.7	2.6	2.5	2.4	2.3	2.2	2.1	2.0
A7	A6	A5	A4	A3	A2	A1	A0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Symbol	Name	Definition	R/W	Def.
2.15	A15	MAC Address, 3rd Word	This is 3rd of 3 Words That Comprise the 48-Bit MAC Address. The MAC Address is Used for (1) Receive Unicast Address Filtering of the DA, and (2) as the SA for Automatic Generated MAC Control Pause Frames. A0 corresponds to the first bit transmitted or received by the MAC section (DA[0] or SA[0] in Figure 3).	R/W	0
2.14	A14			R/W	0
2.13	A13			R/W	0
2.12	A12			R/W	0
2.11	A11			R/W	0
2.10	A10			R/W	0
2.9	A9			R/W	0
2.8	A8			R/W	0
2.7	A7			R/W	0
2.6	A6			R/W	0
2.5	A5			R/W	0
2.4	A4			R/W	0
2.3	A3			R/W	0
2.2	A2			R/W	0
2.1	A1			R/W	0
2.0	A0			R/W	0

x.15 Bit Occurs On REGD15 Pin

Table 22. Register 3 (MAC Address Filter 1 Register) Definition

3.15	3.14	3.13	3.12	3.11	3.10	3.9	3.8
F7[7]	F7[6]	F7[5]	F7[4]	F7[3]	F7[2]	F7[1]	F7[0]
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

3.7	3.6	3.5	3.4	3.3	3.2	3.1	3.0
F6[7]	F6[6]	F6[5]	F6[4]	F6[3]	F6[2]	F6[1]	F6[0]
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Symbol	Name	Definition	R/W	Def.
3.15	F7[7]	MAC Address	This is 1st of 4 Words That Comprise the 64-Bit	R/W	0
3.14	F7[6]	Filter	MAC Address Filter.	R/W	0
3.13	F7[5]			R/W	0
3.12	F7[4]		The MAC Address Filter is Used for Filtering the	R/W	0
3.11	F7[3]		Destination Address on Multicast Packets.	R/W	0
3.10	F7[2]			R/W	0
3.9	F7[1]			R/W	0
3.8	F7[0]			R/W	0
3.7	F6[7]			R/W	0
3.6	F6[6]			R/W	0
3.5	F6[5]			R/W	0
3.4	F6[4]			R/W	0
3.3	F6[3]			R/W	0
3.2	F6[2]			R/W	0
3.1	F6[1]			R/W	0
3.0	F6[0]			R/W	0

x.15 Bit Occurs On REGD15 Pin

Table 23. Register 4 (MAC Address Filter 2 Register) Definition

4.15	4.14	4.13	4.12	4.11	4.10	4.9	4.8
F5[7]	F5[6]	F5[5]	F5[4]	F5[3]	F5[2]	F5[1]	F5[0]
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

4.7	4.6	4.5	4.4	4.3	4.2	4.1	4.0
F4[7]	F4[6]	F4[5]	F4[4]	F4[3]	F4[2]	F4[1]	F4[0]
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Symbol	Name	Definition	R/W	Def.
4.15	F5[7]	MAC Address	This is 2nd of 4 Words That Comprise the 64-Bit	R/W	0
4.14	F5[6]	Filter	MAC Address Filter.	R/W	0
4.13	F5[5]			R/W	0
4.12	F5[4]		The MAC Address Filter is Used for Filtering the	R/W	0
4.11	F5[3]		Destination Address on Multicast Packets.	R/W	0
4.10	F5[2]			R/W	0
4.9	F5[1]			R/W	0
4.8	F5[0]			R/W	0
4.7	F4[7]			R/W	0
4.6	F4[6]			R/W	0
4.5	F4[5]			R/W	0
4.4	F4[4]			R/W	0
4.3	F4[3]			R/W	0
4.2	F4[2]			R/W	0
4.1	F4[1]			R/W	0
4.0	F4[0]			R/W	0

x.15 Bit Occurs On REGD15 Pin

Table 24. Register 5 (MAC Address Filter 3 Register) Definition

5.15	5.14	5.13	5.12	5.11	5.10	5.9	5.8
F3[7]	F3[6]	F3[5]	F3[4]	F3[3]	F3[2]	F3[1]	F3[0]
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

5.7	5.6	5.5	5.4	5.3	5.2	5.1	5.0
F2[7]	F2[6]	F2[5]	F2[4]	F2[3]	F2[2]	F2[1]	F2[0]
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Symbol	Name	Definition	R/W	Def.
5.15	F3[7]	MAC Address	This is 3rd of 4 Words That Comprise the 64-Bit	R/W	0
5.14	F3[6]	Filter	MAC Address Filter.	R/W	0
5.13	F3[5]			R/W	0
5.12	F3[4]		The MAC Address Filter is Used for Filtering the	R/W	0
5.11	F3[3]		Destination Address on Multicast Packets.	R/W	0
5.10	F3[2]			R/W	0
5.9	F3[1]			R/W	0
5.8	F3[0]			R/W	0
5.7	F2[7]			R/W	0
5.6	F2[6]			R/W	0
5.5	F2[5]			R/W	0
5.4	F2[4]			R/W	0
5.3	F2[3]			R/W	0
5.2	F2[2]			R/W	0
5.1	F2[1]			R/W	0
5.0	F2[0]			R/W	0

x.15 Bit Occurs On REGD15 Pin

Table 25. Register 6 (MAC Address Filter 4 Register) Definition

6.15	6.14	6.13	6.12	6.11	6.10	6.9	6.8
F1[7]	F1[6]	F1[5]	F1[4]	F1[3]	F1[2]	F1[1]	F1[0]
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

6.7	6.6	6.5	6.4	6.3	6.2	6.1	6.0
F0[7]	F0[6]	F0[5]	F0[4]	F0[3]	F0[2]	F0[1]	F0[0]
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Symbol	Name	Definition	R/W	Def.
6.15	F1[7]	MAC Address	This is 4th of 4 Words That Comprise the 64-Bit	R/W	0
6.14	F1[6]	Filter	MAC Address Filter.	R/W	0
6.13	F1[5]			R/W	0
6.12	F1[4]		The MAC Address Filter is Used for Filtering the	R/W	0
6.11	F1[3]		Destination Address on Multicast Packets.	R/W	0
6.10	F1[2]			R/W	0
6.9	F1[1]			R/W	0
6.8	F1[0]			R/W	0
6.7	F0[7]			R/W	0
6.6	F0[6]			R/W	0
6.5	F0[5]			R/W	0
6.4	F0[4]			R/W	0
6.3	F0[3]			R/W	0
6.2	F0[2]			R/W	0
6.1	F0[1]			R/W	0
6.0	F0[0]			R/W	0

x.15 Bit Occurs On REGD15 Pin

Table 26. Register 7 (Configuration 1 Register) Definition

7.15	7.14	7.13	7.12	7.11	7.10	7.9	7.8
RST	RXRST	TXRST	ANRST	CTRRST	APAD	IPG2	IPG1
R/WSC	R/WSC	R/WSC	R/WSC	R/WSC	R/W	R/W	R/W

7.7	7.6	7.5	7.4	7.3	7.2	7.1	7.0
IPG0	TXPRMBL	TXCRC	RXPRMBL	RXCRC	STSWRD1	STSWRD0	PEOF
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Symbol	Name	Definition	R/W	Def.
7.15	RST	Reset	1 = Chip Reset, Self Clearing in 1 uS 0 = Normal	R/W SC	0
7.14	RXRST	Receive Reset	1 = Receive Data Path Reset, Self Clears When Start New Packet Detected. 0 = Normal	R/W SC	0
7.13	TXRST	Transmit Reset	1= Transmit Data, Data Reset, Self Clearing in 1 uS 0 = Normal	R/W SC	0
7.12	ANRST	AutoNegotiation Restart	1 = AutoNegotiation Algorithm Restarted, Self Clearing After AutoNegotiation Process Starts 0 = No Reset	R/W SC	0
7.11	CTRRST	Counter Reset	1 = All Counters Reset to 0, Self Clearing in 1 uS 0 = No Reset	R/W SC	0
7.10	APAD	AutoPad Enable	1 = All Undersize Transmit Pkts Padded to 64 Bytes 0 = No Autopad	R/W	1
7.9 7.8 7.7	IPG2 IPG1 IPG0	Transmit Interpacket Gap Select	111 = Tranmsit IPG is 96 Bits (IEEE spec Min) 110 = Transmit IPG is 122 Bits 101 = Transmit IPG is 80 Bits 100 = Transmit IPG is 64 Bits 011 = Transmit IPG is 192 Bits - (2 x IEEE spec Min) 010 = Transmit IPG is 384 Bits - (4 x IEEE spec Min) 001 = Transmit IPG is 768 Bits - (8 x IEEE spec Min) 000 = Transmit IPG is 32 Bits	R/W	1 1 1
7.6	TXPRMBL	Transmit Preamble Enable	1 = Preamble Added To Beginning Of Transmit Pkt 0 = Preamble Not Added	R/W	1
7.5	TXCRC	Transmit CRC Enable	1 = CRC Calculated And Added To End Of Xmt Pkt 0 = CRC Not Added	R/W	1
7.4	RXPRMBL	Receive Preamble Enable	1 = Preamble is Stored in RX FIFO With Rest of Pkt 0 = Preamble Stripped Off	R/W	0
7.3	RXCRC	Receive CRC Enable	1 = CRC is Stored in RX FIFO With Rest of Pkt 0 = CRC Stripped Off	R/W	0
7.2 7.1	STSWRD1 STSWRD0	Receive Status Word Append Select	11 = Reserved 10 = Receive Status Word for Non-Discarded Pkt's And Discarded Pkt's 01 = Receive Status Word for Non-Discarded Pkt's 00 = No Receive Status Word	R/W	1 0
7.0	PEOF	Receive EOF Position Select	1 = Receive EOF At End Of Packet Data 0 = Receive EOF At End Of Receive Status Word	R/W	1

x.15 Bit Occurs On REGD15 Pin

Table 27. Register 8 (Configuration 2 Register) Definition

8.15	8.14	8.13	8.12	8.11	8.10	8.9	8.8
REJUCST	REJMCST	REJBCST	REJALL	ACPTALL	DIS_OVF	DIS_CRC	DIS_USIZE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
8.7	8.6	8.5	8.4	8.3	8.2	8.1	8.0
DIS_OSIZE	DIS_CWRD	DIS_RXAB	0	0	0	0	0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Symbol	Name	Definition	R/W	Def.
8.15	REJUCST	Receive Unicast Packets Reject	1 = Receiver Rejects All Unicast Pkts 0 = Accept Ucst Pkt if DA = Value in Registers [0:2]	R/W	0
8.14	REJMCST	Receive Multicast Packets Reject	1 = Receiver Rejects All Multicast Pkts 0 = Accept Mcst Pkt if DA Passes MAC Address Filter	R/W	0
8.13	REJBCST	Receive Broadcast Packets Reject	1 = Receiver Rejects All Broadcast Pkts 0 = Accept Bcst Pkt	R/W	0
8.12	REJALL	Receive All Packet Reject	1 = Receive Rejects All Packets 0 = Normal	R/W	0
8.11	ACPTALL	Receive All Packets Enable	1 = Receiver Accepts All Pkt Regardless Of Address (Not Including MAC Control Frames) 0 = Normal	R/W	0
8.10	DIS_OVF	Discard Overflow Packet Enable	1 = Discard Receive Pkt With Receive FIFO Overflow Error 0 = No Discard	R/W	1
8.9	DIS_CRC	Discard CRC Error Packet Enable	1 = Discard Receive Pkt With CRC Error 0 = No Discard	R/W	1
8.8	DIS_USIZE	Discard Undersize Packet Enable	1 = Discard Receive Undersize Pkt 0 = No Discard	R/W	1
8.7	DIS_OSIZE	Discard Oversize Packet Enable	1 = Discard Receive Oversize Pkt 0 = No Discard Note: Setting this Bit to 0 Allows Max Packet Size to be Unlimited in Length	R/W	1
8.6	DIS_CWRD	Discard Codeword Err Packet Enable	1 = Discard Receive Pkt That Contains PCS Codeword Error 0 = No Discard	R/W	1
8.5	DIS_RXAB	Discard RXABORT Packet Enable	1 = Discard Receive Pkt That Are Aborted With RXABORT 0 = No Discard (i.e. RXABORT Pin is Disabled)	R/W	1
8.4 thru 8.0			Reserved. Must be Left at Default Value or Written to 0 for Proper Operation.	R/W	0 0 0 0

x.15 Bit Occurs On REGD15 Pin

Table 28. Register 9 (Configuration 3 Register) Definition

9.15	9.14	9.13	9.12	9.11	9.10	9.9	9.8
0	0	AUTOCLR	AUTORXAB	CTR_RD	CTR_ROLL	EWRAP	LCKREF
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
9.7	9.6	9.5	9.4	9.3	9.2	9.1	9.0
CDET	AN_EN	RMXPKT1	RMXPKT2	RXAB_DEF	SINTF_DIS	FCNTRL_DIS	SD_EN
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Symbol	Name	Definition	R/W	Def.
9.15 9.14			Reserved. Must be Left at Default Value or Written to 0 for Proper Operation.	R/W	0 0
9.13	AUTOCLR	Autoclear Mode Enable	1 = TXDC & RXDC Automatically Cleared at Next EOF 0 = TXDC and RXDC cleared by CLR_TXDC and CLR_RXDC pins, respectively	R/W	0
9.12	AUTORXAB	AutoAbort Enable	1 = Current Packet Aborted and RXDC Automatically Cleared at Next EOF 0 = No Abort	R/W	0
9.11	CTR_RD	Counter Reset On Read Enable	1 = Counters Reset to 0 When Read 0 = Counters Not Reset When Read (Only If Count < Max Count)	R/W	1
9.10	CTR_ROLL	Counter Rollover Enable	1 = Counters Rollover to 0 After Max Count 0 = Counters Stop at Max Count	R/W	0
9.9	EWRAP	EWRAP Pin Assert	1 = EWRAP Pin is Asserted Active High 0 = Deassert	R/W	0
9.8	LCKREF	$\overline{\text{LCKREF}}$ Pin Assert	1 = $\overline{\text{LCKREF}}$ Pin is Asserted 0 = Deassert	R/W	0
9.7	CDET	EN_CDET Pin Assert	1 = EN_CDET Pin is Asserted Active High 0 = EN_CDET Pin is Controlled by Receive PCS State Machine	R/W	0
9.6	AN_EN	AutoNegotiation Enable	1 = AutoNegotiation Algorithm Enabled 0 = Disable	R/W	1
9.5 9.4	RMXPKT1 RMXPKT0	Receive MAC Maximum Packet Size Select	11 = Reserved 10 = 1535 Bytes 01 = 1522 Bytes 00 = 1518 Bytes Note: Max Packet Size will be unlimited if bit 8.7 = 0	R/W	0 0
9.3	RXAB_DEF	RXABORT Pin Definition	1 = RXABORT Pin and Autoabort Feature Discards Data 0 = RXABORT Pin and Autoabort Feature Discards Data And Status Word	R/W	0
9.2	SINTF_DIS	System Interface Disable	1 = System Interface Disabled (See System Interf. Section) 0 = Normal	R/W	0
9.1	FCNTRL_DIS	FCNTRL Pin Disable	1= FCNTRL Pin Disabled, i.e., Doesn't cause Autogenerated Pause Frame Transmission 0 = Enabled	R/W	0
9.0	SD_EN	Signal Detect Pin Enable	1 = Enabled 0 = SD Pin Disabled, i.e., Internal SD always Asserted, Doesn't Affect Receive Word Synchronization	R/W	0

x.15 Bit Occurs On REGD15 Pin

Table 29. Register 10 (Configuration 4 Register) Definition

10.15	10.14	10.13	10.12	10.11	10.10	10.9	10.8
ENDIAN	BUSSIZE	0	LPBK	LNKDN	TBC_DIS	0	0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

10.7	10.6	10.5	10.4	10.3	10.2	10.1	10.0
CMXPKT1	CMXPKT0	0	0	0	0	0	0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Symbol	Name	Definition	R/W	Def.
10.15	ENDIAN	Endian Select	1 = RXD/TXD Data In Big Endian Format 0 = RXD/TXD Data In Little Endian Format	R/W	0
10.14	BUSSIZE	Bus Size Word Width	1 = Receive System Bus Word Width is 16-Bits 0 = Receive System Bus Word Width is 32-Bits	R/W	0
10.13			Reserved. Muse be Left at Default Value or Written to 0 for Proper Device Operation	R/W	0
10.12	LPBK	Loopback Enable	1 = Loopback Mode Enabled 0 = Normal	R/W	0
10.11	LNKDN	Link Down FIFO Flush Enable	1 = When Receive Link is Down, Data Exiting the TX FIFO is Discarded 0 = Normal	R/W	0
10.10	TBC_DIS	TX Disable	1 = TBC, TX [0:9] Outputs Disabled (High Impedance) 0 = Enabled	R/W	0
10.9 10.8			Reserved. Muse be Left at Default Value or Written to 0 for Proper Device Operation	R/W	0 0
10.7 10.6	CMXPKT1 CMXPKT0	Counter Max Packet Size Select	11 = Unlimited 10 = 1535 bytes 01 = 1522 bytes 00 = 1518 bytes	R/W	0 0
10.5 thru 10.0			Reserved. Muse be Left at Default Value or Written to 0 for Proper Device Operation	R/W	0

x.15 Bit Occurs on REGD15 Pin

Table 30. Register 11 (Status 1 Register) Definition

11.15	11.14	11.13	11.12	11.11	11.10	11.9	11.8
RSYNC			SD	LINK			
R/LTI			R	R/LTI			

11.7	11.6	11.5	11.4	11.3	11.2	11.1	11.0
AN_NP	AN_TX_NP	AN_RX_NP	AN_RX_BP	AN_RMTRST			
R/LHI	R	R	R	R/LHI			

Bit	Symbol	Name	Definition	R/W	Def.
11.15	RSYNC	Receive Word Synchronization Detect	1 = Receive 8B10B PCS has Acquired Word Synchronization 0 = Not Synchronized	R/LTI	0
11.14 11.13			Reserved		
11.12	SD	Signal Detect Pin Status	1 = SD Input Pin High 0 = SD Input Pin Low	R	0
11.11	LINK	Link Detect Status	1 = Link Pass (Rcvr in Sync, Autonegotation Done) 0 = Link Fail	R/LTI	0
11.10 11.9 11.8			Reserved		
11.7	AN_NP	AutoNegotiation Next Page Status	1 = One Next Page Exchange Done (Both RX & TX) 0 = Not Done	R/LHI	0
11.6	AN_TX_NP	AutoNegotiation TX Next Page Status	1 = Transmission of Next Page Done 0 = Not Done	R	0
11.5	AN_RX_NP	AutoNegotiation RX Next Page Status	1 = Reception of Next Page Done, Next Page Valid 0 = Not Done	R	0
11.4	AN_RX_BP	AutoNegotiation RX Base Page Status	1 = Reception of Base Page Done, Base Page Valid 0 = Not Done	R	0
11.3	AN_RMTRST	AutoNegotiation Remote Restart Status	1 = AutoNegotiation Restarted Because Remote End Sent Restart Codes or Invalid Characters 0 = Normal	R/LHI	0
11.2 11.1 11.0			Reserved		

x.15 Bit Occurs On REGD15 Pin

Table 31. Register 14 (Status Mask 1 Register) Definition

14.15	14.14	14.13	14.12	14.11	14.10	14.9	14.8
MASK_ RSYNC	1	1	1	MASK_ LINK	1	1	1
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

14.7	14.6	14.5	14.4	14.3	14.2	14.1	14.0
MASK_ AN_NP	1	1	1	MASK_ AN_RMTRST	1	1	1
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Symbol	Name	Definition	R/W	Def.
14.15	MASK_ RSYNC	Interrupt Mask - Receive Word Synchronization Detect	1 = Mask Interrupt For RSYNC In Register 11 0 = No Mask	R/W	1
14.14 14.13 14.12			Reserved. Must be Left at Default Value or Written to 1 for Proper Device Operation	R/W	1
14.11	MASK_ LINK	Interrupt Mask - Link Status Detect	1 = Mask Interrupt For LINK In Register 11 0 = No Mask	R/W	1
14.10 14.9 14.8			Reserved. Must be Left at Default Value or Written to 1 for Proper Device Operation	R/W	1
14.7	MASK_ AN_NP	Interrupt Mask - AutoNegotiation Next Page Status	1 = Mask Interrupt For AN_NP In Register 11 0 = No Mask	R/W	1
14.6 14.5 14.4			Reserved. Must be Left at Default Value or Written to 1 for Proper Device Operation	R/W	1
14.3	MASK_ AN_RMTRST	Interrupt Mask - AutoNegotiation Remote Restart Status	1 = Mask Interrupt For AN_RMTRST in Register 11 0 = No Mask	R/W	1
14.2 14.1 14.0			Reserved. Must be Left at Default Value or Written to 1 for Proper Device Operation	R/W	1

x.15 Bit Occurs On REGD15 Pin

Table 32. Register 17 (Transmit FIFO Threshold Register) Definition

17.15	17.14	17.13	17.12	17.11	17.10	17.9	17.8
TWM1[4]	TWM1[3]	TWM1[2]	TWM1[1]	TWM1[0]	TWM2[4]	TWM2[3]	TWM2[2]
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

17.7	17.6	17.5	17.4	17.3	17.2	17.1	17.0
TWM2[1]	TWM2[0]	TASND5	TASND4	TASND3	TASND2	TASND1	TASND0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Symbol	Name	Definition	R/W	Def.
17.15 17.14 17.13 17.12 17.11	TWM1[4] TWM1[3] TWM1[2] TWM1[1] TWM1[0]	Transmit FIFO Watermark 1 Threshold	Range = 0-1024 Words (0-4096 Bytes) Increment = 32 Words (128 Bytes) 11111 = Reserved, Do Not Use 11110 = 992 Words, in FIFO (3968 Bytes) 11101 = 960 Words, in FIFO (3840 Bytes) ⋮ ⋮ ⋮ 00001 = 64 Words In FIFO (256 Bytes) 00000 = 32 Words In FIFO (128 Bytes)	R/W	1 0 0 0 0
17.10 17.9 17.8 17.7 17.6	TWM2[4] TWM2[3] TWM2[2] TWM2[1] TWM2[0]	Transmit FIFO Watermark 2 Threshold	Range = 0-1024 Words (0-4096 Bytes) Increment = 32 Words (128 Bytes) 11111 = Reserved, Do Not Use 11110 = 992 Words, in FIFO (3968 Bytes) 11101 = 960 Words, in FIFO (3840 Bytes) ⋮ ⋮ ⋮ 00001 = 64 Words In FIFO (256 Bytes) 00000 = 32 Words In FIFO (128 Bytes)	R/W	1 1 0 0 0
17.5 17.4 17.3 17.2 17.1 17.0	TASND5 TASND4 TASND3 TASND2 TASND1 TASND0	Transmit FIFO Autosend Threshold	Range = 0-1024 Words (0-4096 Bytes) Increment = 8 Words (32 Bytes) 111111 = Reserved do not use 111110 = Transmit Starts When 504 Words In FIFO ⋮ ⋮ ⋮ 000010 = Transmit Starts When 24 Words In FIFO 000001 = Transmit Starts When 16 Words In FIFO 000000 = Transmit Starts When 992 Words In FIFO Note 1: An EOF written into FIFO will also start transmission of that packet regardless of the autosend threshold setting. Note 2: The 000000 setting lets the FIFO fill up before transmission starts, facilitating transmission of oversize packets.	R/W	1 0 0 0 0 0

x.15 Bit Occurs On REGD15 Pin

Table 33. Register 18 (Receive FIFO Threshold Register) Definition

18.15	18.14	18.13	18.12	18.11	18.10	18.9	18.8
RWM1[7]	RWM1[6]	RWM1[5]	RWM1[4]	RWM1[3]	RWM1[2]	RWM1[1]	RWM1[0]
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
18.7	18.6	18.5	18.4	18.3	18.2	18.1	18.0
RWM2[7]	RWM2[6]	RWM2[5]	RWM2[4]	RWM2[3]	RWM2[2]	RWM2[1]	RWM2[0]
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Symbol	Name	Definition	R/W	Def.
18.15 18.14 18.13 18.12 18.11 18.10 18.9 18.8	RWM1[7] RWM1[6] RWM1[5] RWM1[4] RWM1[3] RWM1[2] RWM1[1] RWM1[0]	Receive FIFO Watermark 1 Threshold	Range = 0-4096 Words (0-16386 Bytes) Increment = 16 Words (64 Bytes) 11111111 = Reserved, Do Not Use 11111110 = 4080 Words in FIFO (16320 Bytes) 11111110 = 4064 Words in FIFO (16256 Bytes) ⋮ ⋮ ⋮ 00000001 = 32 Words In FIFO (128 Bytes) 00000000 = 16 Words In FIFO (64 Bytes)	R/W	0 0 0 0 0 0 0 0
18.7 18.6 18.5 18.4 18.3 18.2 18.1 18.1	RWM2[7] RWM2[6] RWM2[5] RWM2[4] RWM2[3] RWM2[2] RWM2[1] RWM2[0]	Receive FIFO Watermark 2 Threshold	Range = 0-4096 Words (0-16386 Bytes) Increment = 16 Words (64 Bytes) 11111111 = Reserved, Do Not Use 11111110 = 4080 Words in FIFO (16320 Bytes) 11111110 = 4064 Words in FIFO (16256 Bytes) ⋮ ⋮ ⋮ 00000001 = 32 Words In FIFO (128 Bytes) 00000000 = 16 Words In FIFO (64 Bytes)	R/W	1 1 0 0 0 0 0 0

x.15 Bit Occurs On REGD15 Pin

Table 34. Register 19 (Flow Control 1 Register) Definition

19.15	19.14	19.13	19.12	19.11	19.10	19.9	19.8
MCNTRL	MCPASS1	MCPASS0	MCFLTR	MCENDPS	MCASND3	MCASND2	MCASND1
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

19.7	19.6	19.5	19.4	19.3	19.2	19.1	19.0
MCASND0	0	0	0	0	0	0	0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Symbol	Name	Definition	R/W	Def.
19.15	MCNTRL	MAC Control Frame Enable	1 = Valid Receive MAC Control Frames Cause Transmitter To Pause (Flow Control Enabled) 0 = Transmitter Not Paused (Flow Control Disable)	R/W	1
19.14 19.13	MCPASS1 MCPASS0	MAC Control Frame Passthrough Enable	11 = Valid MAC Control Frame That Have Pause Opcode are Passed thru to Rcv FIFO 10 = Valid MAC Control Frames That Have any Opcode are passed thru to Rcv FIFO 01 = Valid MAC Control Frames That Have nonPause Opcode are Passed Thru to Rcv FIFO 00 = MAC Control Frames are Not Passed Thru to Rcv FIFO	R/W	0 0
19.12	MCFLTR	MAC Control Frame Address Filter Enable	1 = Use Reserved Multicast Address or Station Address as the DA To Determine MAC Control Pause Frame Validity 0 = Use Any Address as the DA to Determine MAC Control Pause Frame Validity	R/W	1
19.11	MCENDPS	MAC Control Frame End Pause Enable	1 = When FNCTRL Deasserted, Send Transmit MAC Control Frame With pause_time=0 0 = Normal	R/W	1
19.10 19.9 19.8 19.7	MCASND3 MCASND2 MCASND1 MCASND0	MAC Control Frame AutoSend Threshold	These Bits Determine the Receive FIFO Threshold Which Will Cause the Automatic Transmission of Pause Frames. Autogenerated Pause Frame Transmission is also Affected by the FCNTRL Pin and Bit 9.1. 1111 = 15360 Bytes ⋮ ⋮ 0010 = 2048 Bytes 0001 = 1024 Bytes 0000 = Disabled, i.e. RX FIFO Data Does Not Cause Autogenerated Pause Frame Transmission.	R/W	0 0 0 0
19.6 thru 19.0			Reserved. Must be Left at Defaults or Written to 0 for Proper Operation.	R/W	0

x.15 Bit Occurs On REGD15 Pin

Table 35. Register 20 (Flow Control 2 Register) Definition

20.15	20.14	20.13	20.12	20.11	20.10	20.9	20.8
P15	P14	P13	P12	P11	P10	P9	P8
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
20.7	20.6	20.5	20.4	20.3	20.2	20.1	20.0
P7	P6	P5	P4	P3	P2	P1	P0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Symbol	Name	Definition	R/W	Def.
20.15	P15	Pause Time	The contents of this register are inserted into the pause_time parameter field of all autogenerated transmit MAC Control Pause frames. Upon successful reception of these autogenerated Pause frames, a remote device will not transmit data for a time interval equal to the decimal value of this register times 512 nS. P0 is LSB. Any Pause Time Value ≤ 32_H Will Be Sent As 32_H.	R/W	1
20.14	P14			R/W	1
20.13	P13			R/W	1
20.12	P12			R/W	1
20.11	P11			R/W	0
20.10	P10			R/W	0
20.9	P9			R/W	0
20.8	P8			R/W	0
20.7	P7			R/W	0
20.6	P6			R/W	0
20.5	P5			R/W	0
20.4	P4			R/W	0
20.3	P3			R/W	0
20.2	P2			R/W	0
20.1	P1			R/W	0
20.0	P0			R/W	0

x.15 Bit Occurs On REGD15 Pin

Table 36. Register 21 (AutoNegotiation Base Page Transmit) Definition

21.15	21.14	21.13	21.12	21.11	21.10	21.9	21.8
NP	ACK	RF2	RF1	0	0	0	PS_DIR
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

21.7	21.6	21.5	21.4	21.3	21.2	21.1	21.0
PS	HDX	FDX	0	0	0	0	0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Symbol	Name	Definition	R/W	Def.
21.15	NP	Next Page Enable	1 = Next Page Exists 0 = No Next Page	R/W	0
21.14	ACK	Acknowledge	1 = Received AutoNegotiation Word Recognized 0 = Not Recognized Note: Writing this bit has no affect on device operation, transmitted bit is controlled by internal state machine	R/W	0
21.13 21.12	RF2 RF1	Remote Fault	11 = AutoNegotiation Error 10 = Offline 01 = Link Failure 00 = No Error, Link OK	R/W	0 0
21.11 21.10 21.9			Reserved For Future IEEE Use	R/W	0 0 0
21.8 21.7	PS_DIR PS	Pause Capable	11 = Capable of Rcv Pause Only 10 = Capable of Xmt Pause Only 01 = Capable of Xmt and Rcv Pause 00 = Not Capable	R/W	0 1
21.6	HDX	Half Duplex Capable	1 = Capable of Half Duplex 0 = Not Capable	R/W	0
21.5	FDX	Full Duplex Capable	1 = Capable Of Full Duplex 0 = Not Capable	R/W	1
21.4 21.3 21.2 21.1 21.0			Reserved For Future IEEE Use	R/W	0 0 0 0 0

x.15 Bit Occurs On REGD15 Pin

Table 37. Register 22 (AutoNegotiation Base Page Receive Register) Definition

22.15	22.14	22.13	22.12	22.11	22.10	22.9	22.8
NP	ACK	RF2	RF1	0	0	0	PS_DIR
R	R	R	R	R	R	R	R

22.7	22.6	22.5	22.4	22.3	22.2	22.1	22.0
PS	HDX	FDX	0	0	0	0	0
R	R	R	R	R	R	R	R

Bit	Symbol	Name	Definition	R/W	Def.
22.15	NP	Next Page Enable	1 = Next Page Exists 0 = No Next Page	R	0
22.14	ACK	Acknowledge	1 = Received AutoNegotiation Word Recognized 0 = Not Recognized	R	0
22.13 22.12	RF2 RF1	Remote Fault	11 = AutoNegotiation Error 10 = Offline 01 = Link Failure 00 = No Error, Link OK	R	0
22.11 22.10 22.9			Reserved For Future IEEE Use	R	0 0 0
22.8 22.7	PS_DIR PS	Pause Capable	11 = Capable of Rcv Pause Only 10 = Capable of Xmt Pause Only 01 = Capable of Xmt and Rcv Pause Only 00 = Not Capable	R	0 0
22.6	HDX	Half Duplex Capable	1 = Capable of Half Duplex 0 = Not Capable	R	0
22.5	FDX	Full Duplex Capable	1 = Capable Of Full Duplex 0 = Not Capable	R	0
22.4 22.3 22.2 22.1 22.0			Reserved For Future IEEE Use	R	0 0 0 0 0

x.15 Bit Occurs On REGD15 Pin

Table 38. Register 23 (AutoNegotiation Next Page Transmit Register) Definition

23.15	23.14	23.13	23.12	23.11	23.10	23.9	23.8
NP	ACK	PAGETYPE	ACK2	TOGGLE	MSG10	MSG9	MSG8
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
23.7	23.6	23.5	23.4	23.3	23.2	23.1	23.0
MSG7	MSG6	MSG5	MSG4	MSG3	MSG2	MSG1	MSG0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Symbol	Name	Definition	R/W	Def.
23.15	NP	Next Page Enable	1 = Additional Next Page Exists 0 = This is Last Next Page	R/W	0
23.14	ACK	Acknowledge	1 = Received AutoNegotiation Word Recognized 0 = Not Recognized Note: Writing this bit has no affect on device operation, transmitted bit is controlled by internal state machine	R/W	0
23.13	PAGE TYPE	Page Type	1 = Message Page 0 = Unformatted Page	R/W	0
23.12	ACK2	Acknowledge 2	1 = Able to Comply With the Received Message 0 = Not Able to Comply	R/W	0
23.11	TOGGLE	Toggle Bit	1 = Value of the Toggle Bit in Previous Transmitted AutoNegotiation Word was 0 0 = Value of the Toggle Bit in Previous Transmitted AutoNegotiation Word was 1 Note: Writing this bit has no affect on device operation, transmitted bit is controlled by internal state machine	R/W	0
23.10 23.9 23.8 23.7 23.6 23.5 23.4 23.3 23.2 23.1 23.0	MSG10 MSG9 MSG8 MSG7 MSG6 MSG5 MSG4 MSG3 MSG2 MSG1 MSG0	Message	These Bits Carry the 11-bit Message Associated With this Next Page. Refer to IEEE 802.3z Specifications for details on the format and definition of these bits.	R/W	0 0 0 0 0 0 0 0 0 0 0

x.15 Bit Occurs On REGD15 Pin

Table 39. Register 24 (AutoNegotiation Next Page Receive Register) Definition

24.15	24.14	24.13	24.12	24.11	24.10	24.9	24.8
NP	ACK	PAGETYPE	ACK2	TOGGLE	MSG10	MSG9	MSG8
R	R	R	R	R	R	R	R
24.7	24.6	23.5	24.4	24.3	24.2	24.1	24.0
MSG7	MSG6	MSG5	MSG4	MSG3	MSG2	MSG1	MSG0
R	R	R	R	R	R	R	R

Bit	Symbol	Name	Definition	R/W	Def.
24.15	NP	Next Page Enable	1 = Additional Next Page Exists 0 = This is Last Next Page	R	0
24.14	ACK	Acknowledge	1 = Received AutoNegotiation Word Recognized 0 = Not Recognized	R	0
24.13	PAGETYPE	Page Type	1 = Message Page 0 = Unformatted Page	R	0
23.12	ACK2	Acknowledge 2	1 = Able to Comply With the Received Message 0 = Not Able to Comply	R	0
23.11	TOGGLE	Toggle Bit	1 = Value of the Toggle Bit in Previous Transmitted AutoNegotiation Word was 0 0 = Value of the Toggle Bit in Previous Transmitted AutoNegotiation Word was 1	R	0
24.10 24.9 24.8 24.7 24.6 24.5 24.4 24.3 24.2 24.1 24.0	MSG10 MSG9 MSG8 MSG7 MSG6 MSG5 MSG4 MSG3 MSG2 MSG1 MSG0	Message	These Bits Carry the 11-bit Message Associated With this Next Page. Refer to IEEE 802.3z Specifications for details on the format and definition of these bits.	R	0 0 0 0 0 0 0 0 0 0 0

x.15 Bit Occurs On REGD15 Pin

Table 40. Register 32 (Device ID Register) Definition

32.15	32.14	32.13	32.12	32.11	32.10	32.9	32.8
PART3	PART2	PART1	PART0	HREV3	HREV2	HREV1	HREV0
R	R	R	R	R	R	R	R

32.7	32.6	32.5	32.4	32.3	32.2	32.1	32.0
				SREV3	SREV2	SREV1	SREV0
				R	R	R	R

Bit	Symbol	Name	Definition	R/W	Def.
32.15 32.14 32.13 32.12	PART3 PART2 PART1 PART0	Part Number	This field contains a 4-bit number that uniquely identifies the device as the 8101.	R	0 0 0 1
32.11 32.10 32.9 32.8	HREV3 HREV2 HREV1 HREV0	Hardware Revision Number	This field contains a 4-bit number that identifies that a revision was made to the device and the revision did not affect any Register bit definitions.	R	X X X X
32.7 32.6 32.5 32.4			Reserved For Future Use.		
32.3 32.2 32.1 32.1	SREV3 SREV2 SREV1 SREV0	Software Revision Number	This field contains a 4-bit number that identifies that a revision was made to the device and the revision did affect Register bit definitions.	R	X X X X

x.15 Bit Occurs On REGD15 Pin

Table 41. Register 112-115 (Counter Half Full 1-4 Registers) Definition

xxx.15	xxx.14	xxx.13	xxx.12	xxx.11	xxx.10	xxx.9	xxx.8
HFULL15	HFULL14	HFULL13	HFULL12	HFULL11	HFULL10	HFULL9	HFULL8
R/LHI	R/LHI	R/LHI	R/LHI	R/LHI	R/LHI	R/LHI	R/LHI

xxx.7	xxx.6	xxx.5	xxx.4	xxx.3	xxx.2	xxx.1	xxx.0
HFULL7	HFULL6	HFULL5	HFULL4	HFULL3	HFULL2	HFULL1	HFULL0
R/LHI	R/LHI	R/LHI	R/LHI	R/LHI	R/LHI	R/LHI	R/LHI

Bit	Symbol	Name	Definition	R/W	Def.
xxx.15	HFULL15	Counter Half Full Detect	These bits indicate when a counter is near overflow as measured by being half full. These four registers contain 53 counter half full detect bits, one bit for each of the 53 counters. Bit 0 in Counter Half Full Register 0 corresponds to Counter 1 as listed in Table 17; Bit 15 in Counter Half Full Register 0 corresponds to Counter 16; Bit 4 of Counter Half Full Register 4 corresponds to Counter 53. 1 = Counter has Reached a Count of 80000000_H, i.e. Half Full. 0 = Count < 80000000_H	R/LHI	0
xxx.14	HFULL14				0
xxx.13	HFULL13				0
xxx.12	HFULL12				0
xxx.11	HFULL11				0
xxx.10	HFULL10				0
xxx.9	HFULL9				0
xxx.8	HFULL8				0
xxx.7	HFULL7				0
xxx.6	HFULL6				0
xxx.5	HFULL5				0
xxx.4	HFULL4				0
xxx.3	HFULL3				0
xxx.2	HFULL2				0
xxx.1	HFULL1				0
xxx.0	HFULL0				0

xxx=112-115
xxx.15 Bit Occurs On REGD15 Pin

Table 42. Registers 120-123 (Counter Half Full Mask 1-4 Registers) Definition

xxx.15	xxx.14	xxx.13	xxx.12	xxx.11	xxx.10	xxx.9	xxx.8
MASK_ HFULL15	MASK_ HFULL14	MASK_ HFULL13	MASK_ HFULL12	MASK_ HFULL11	MASK_ HFULL10	MASK_ HFULL9	MASK_ HFULL8
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

xxx.7	xxx.6	xxx.5	xxx.4	xxx.3	xxx.2	xxx.1	xxx.0
MASK_ HFULL7	MASK_ HFULL6	MASK_ HFULL5	MASK_ HFULL4	MASK_ HFULL3	MASK_ HFULL2	MASK_ HFULL1	MASK_ HFULL0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Symbol	Name	Definition	R/W	Def.
xxx.15	MASK_HFULL15	Counter Half Full Detect Mask	The bits will mask (disable) the interrupt caused by the counter half full detect bits. These four registers contain 53 mask bits, one bit for each of the 53 half full detect bits. Bit 0 in Counter Half Full Mask Register 0 masks the interrupt caused by the half full detect bit for Counter 1; Bit 15 in Counter Half Full Mask Register 0 corresponds to Counter 16; Bit 4 in Counter Half Full Mask Register 3 corresponds to Counter 53. 1 = Mask (Disable) the Interrupt Caused by Counter Half Full Detect Bit N 0 = No Mask	R/W	1
xxx.14	MASK_HFULL14				1
xxx.13	MASK_HFULL13				1
xxx.12	MASK_HFULL12				1
xxx.11	MASK_HFULL11				1
xxx.10	MASK_HFULL10				1
xxx.9	MASK_HFULL9				1
xxx.8	MASK_HFULL8				1
xxx.7	MASK_HFULL7				1
xxx.6	MASK_HFULL6				1
xxx.5	MASK_HFULL5				1
xxx.4	MASK_HFULL4				1
xxx.3	MASK_HFULL3				1
xxx.2	MASK_HFULL2				1
xxx.1	MASK_HFULL1				1
xxx.0	MASK_HFULL0				1

xxx=112-115
xxx.15 Bit Occurs On REGD15 Pin

Table 43. Registers 128-233 (Counter 1-53 Registers) Definition

xxx.15	xxx.14	xxx.13	xxx.12	xxx.11	xxx.10	xxx.9	xxx.8
C15	C14	C13	C12	C11	C10	C9	C8
R	R	R	R	R	R	R	R

xxx.7	xxx.6	xxx.5	xxx.4	xxx.3	xxx.2	xxx.1	xxx.0
C7	C6	C5	C4	C3	C2	C1	C0
R	R	R	R	R	R	R	R

Bit	Symbol	Name	Definition	R/W	Def.
xxx.15	C15	Counter Result Value	These 106 registers contain the results of the 53 32-bit management counters. Each 32-bit counter result value resides in two 16-bit registers. For the two registers associated with each counter, the register with the lower value address always contains the least significant 16-bits of the counter result. C0 of the lower value address is the counter LSB; C15 of the higher value address is the counter MSB. The definition and register address for each counter is shown in Table 15. The register address for each counter is also shown in Table 17.	R	0
xxx.14	C14			R	0
xxx.13	C13			R	0
xxx.12	C12			R	0
xxx.11	C11			R	0
xxx.10	C10			R	0
xxx.9	C9			R	0
xxx.8	C8			R	0
xxx.7	C7			R	0
xxx.6	C6			R	0
xxx.5	C5			R	0
xxx.4	C4			R	0
xxx.3	C3			R	0
xxx.2	C2			R	0
xxx.1	C1			R	0
xxx.0	C0			R	0

xxx=128-233
xxx.15 Bit Occurs On REGD15 Pi

5.0 Application Information

5.1 EXAMPLE SCHEMATICS

A typical example of a Gigabit Ethernet switch port using the 8101 is shown in Figure 8.

5.2 PHY INTERFACE

5.2.1 External Physical Layer Devices

The 10-Bit PHY Interface will directly couple to any external Physical Layer device which complies with the IEEE 802.3z or the 10-Bit ANSI X3.230 Interface standards. In a typical configuration, the 8101 will be connected to an external SerDes chip, as shown in Figure 8. A list of SerDes chips whose specifications are compatible with and can directly connect to the 8101 is shown in Table 44.

Table 44. Compatible SerDes Chips

Vendor	Device No.
Vitesse	VSC7135
Hewlett-Packard	HDMP-1636 HDMP-1646
Sony	CXB1589Q
AMCC	52052
TriQuint	TQ9506

5.2.2 PCB Layout

The 10-Bit PHY interface clocks data at a very high rate, 125 MHz. The setup and hold times on the timing signals are very small. The outputs are specified assuming a maximum load of 10 pf, a very small number. As such, it is imperative that the SerDes or other Physical Layer device be placed as close as possible to the 8101, preferably within 1". In addition, care should be taken to eliminate any extra loading on all the 10-Bit PHY Interface signal lines. Also, the clock and data lines in both receive and transmit directions should be routed along the same paths so that they have similar parasitics and delays so as to not degrade setup and hold times. Termination is not necessary if these precautions are taken.

5.3 SYSTEM INTERFACE

5.3.1 Watermarks

There are two independent watermarks on both transmit and receive FIFO's. The usage of these watermarks is unspecified and is left to the discretion of the system designer. Below are three examples of watermark usage based on transferring data in (1) complete packets, (2) fixed block sizes, or (3) variable block sizes.

The first example is to transfer data to/from the 8101 in completed packets. In this case, only one watermark is needed. Either transmit watermark could be chosen for this application, but on the receive side, RXWM2 should be chosen because it gets asserted when a complete packet is loaded into the RX FIFO. The transmit and receive watermark thresholds should preferably be set to a value equal to or larger than the maximum size packet (1518 bytes or greater). On the transmit side, data would be written into the TX FIFO in complete packet bursts when the system requires. On the receive side, data would be read out of the RX FIFO beginning when $\overline{RXWM2}$ is asserted and stopped when RXEOF is asserted.

The second example is to transfer data to/from the 8101 in fixed block sizes (64 bytes at a time, for example). In this case, only one watermark is needed. Either transmit watermark could be chosen for this application, but on the

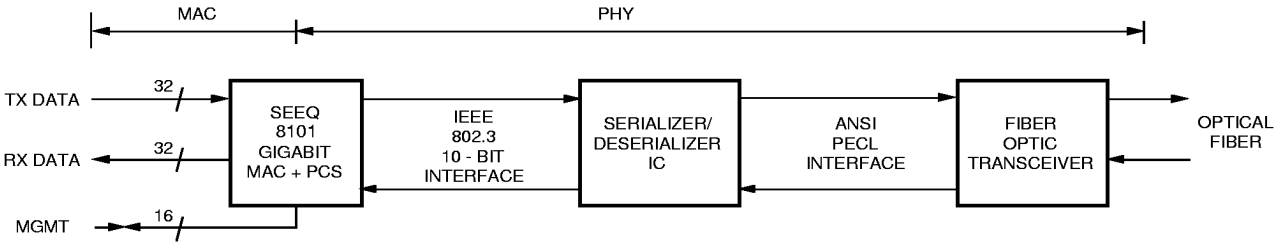


Figure 8. Gigabit Ethernet Port Using the 8101

receive side, RXWM2 should be chosen because it gets asserted when a complete packet is loaded into the RX FIFO. The transmit watermark threshold would be set to a low value (64 bytes for example), and the receive watermark thresholds would preferably be set to a value equal to or larger than the fixed cell size (64 bytes in this example). On the transmit side, data would be written into the TX FIFO in fixed block size bursts when the system requires. When the transmit watermark gets deasserted, another block would have to be written into the TX FIFO. On the receive side, data would be read out of the RX FIFO beginning whenever RXWM2 is asserted and stoped when the fixed block has been read out (64 bytes in this example) or RXEOF has been asserted.

A third example is to transfer data to/from the 8101 in variable cell sizes. In this case, two watermarks would be needed. The TXWM1 and RXWM1 watermark thresholds would be set to some low value (64 bytes for example), while the TXWM2 and RXWM2 watermark thresholds would be set to some high value (1024 bytes for example). On the transmit side, data would be written into the TX FIFO when the system requires. If TXWM2 is asserted, then data input would have to be halted; if TXWM1 is deasserted, data input would have to be resumed. In this way, the TX FIFO contents are kept between the high and low watermark thresholds which potentially increses the external system loading efficiency. Similarly, on the receive side, data would have to be read out of the RX FIFO when RXWM2 is asserted. If RXWM1 is deasserted, data output would have to be halted (or if RXEOF has been asserted); if RXWM2 is asserted, then data output would have to be resumed. In this way, the RX FIFO contents are kept between the high and low watermarks.

The transmit and receive watermarks can also be used to indicate that the FIFO is full or empty (or almost full or almost empty), if desired.

5.3.2 PCB Layout

Since the data rate of the System Interface can be as high as 66 MHz, care should be taken in keeping PCB trace lengths of all critical signals as small as possible, preferably less than 2" in length. If this guideline is followed, termination is not necessary.

5.4 RESET

While the device is being reset, it transmits valid 10B symbols out of the 10-Bit PHY Interface on TXD[0:9] and TBC. If the device is reset with the RESET pin for a long period of time, these 10B symbols may and be mistakenly decoded as valid packet information and fill up the memory in a remote device. The reset procedure outlined in Table 45 will avoid this situation and is recommended for use when the RESET pin is asserted for long periods of time. When the reset bit is used for device reset, the above situation is avoided because the reset bit is self clearing in 1 uS.

Table 45. Reset Procedure

#	Step	Comment
1	Write Bit 10.10=1	Stop transmission of data out of 10-Bit PHY Interface to SerDes
2	Wait for >20 mS	Insure that the remote device receiver detects that the link has been broken so it won't decode 10B data as valid.
3	Assert RESET=0.	Start reset period.
4	Wait >10 uS.	Allow enough time for all circuits in device to be reset.
5	Deassert RESET=1	Stop Reset Period
6	Write Bit 10.10 = 0	Turn on 10-Bit PHY Interface. Returns Device to Normal Operation.

5.5 LOOPBACK

The 8101 has a loopback mode, but most external SerDes devices connected to the 8101 10-Bit PHY Interface also have a loopback mode. Sometimes, it is desirable to use the SerDes loopback mode instead of the 8101 loopback mode because the SerDes loopback mode will test a larger

and/or different section of the system circuitry. When the SerDes loopback mode is used, it is recommended that the procedure outlined in Table 46 be followed.

Table 46. SerDes Loopback Procedure

#	Step	Comment
1	Write Bit 8.12=1	Ignore all receive data until the loopback mode is ready for operation.
2	Write Bit 9.9=1	Enable the external SerDes loopback mode.
3	Write Bit 9.0=0	Ignore the Signal Detect output from optical transceiver because the receive optical data may be invalid.
4	Write Bit 10.10=1	Stop transmission of data out of 10-Bit PHY Interface to cause the SerDes & 8101 to lose sync so that they will properly resync to the new data stream.
5	Wait > 200 uS	Allow time for the SerDes & 8101 receivers to lose sync.
6	Write Bit 10.10=0	Turn on transmitter so that the SerDes and 8101 receivers can gain sync.
7	Wait > 200 uS	Allow time for the SerDes & 8101 receivers to gain sync.
8	Write Bit 8.12=0	Stop ignoring receive data, turn on the receive MAC.
9	Do loopback tests	
10	Write Bit 9.9=0 Write Bit 9.0=1 (if SD pin is used)	Turn off SerDes loopback mode, enable Signal Detect function (if used).
11	Write Bit 7.12=1.	Restarts AutoNegotiation. Device is ready for normal operation when Auto-Negotation completed.

5.6 AUTONEGOTIATION

5.6.1 AutoNegotiation at Powerup

When the device is powered up, the AutoNegotiation algorithm must handshake with the remote device to configure itself for a common mode of operation. To insure smooth and proper AutoNegotiation operation at powerup, it is recommended that the procedure outlined in Table 47 be followed.

Table 47. AutoNegotiation Powerup Procedure

#	Step	Comment
1	Wait for Pin SD=1 (If SD is not used, go to next step)	Waits for valid data from the optical transceiver
2	Write Bit 7.15=1	Resets the device
3	Write Bit 21.[15:0]	Sets up the advertised capabilities for Auto-Negotiation.
4	Write the remaining registers as needed.	Sets up the device for the desired operation.
5	Write Bit 7.12=1	Restarts AutoNegotiation
7	Wait > 50 mS	Wait for AutoNegotiation to complete.
8	Read Bit 11.11 twice. If 0, then done. If 1, repeat #5-8 (up to seven times)	Determine if Auto-Negotiation done and Link Pass. If Link Pass, device ready for operation. If Link Fail, retry again seven more times. If no Link Pass after seven times, disable ANEG and try manual Link Pass.
9	Write 9.6=0	Disable AutoNegotiation
10	Write Bit 7.12=1	Clears all internal Auto-Negotiation circuitry.
11	Wait > 100mS	Wait for manual Link Pass
12	Read Bit 11.11 twice. If 0, go to first step. If 1, done.	If manual Link Pass, then device ready for operation. If Link Fail, then redo procedure until Link Pass is achieved.

5.6.2 Negotiating with a Non-AutoNegotiation Able Device

When the 8101 has AutoNegotiation enabled and the remote device to which it is connected to has AutoNegotiation disabled (or doesnít have AutoNegotiation capability at all), then the 8101 will stay in the Link Fail state and continually restart AutoNegotiation because it cannot complete a negotiation sequence successfully. Conversely, the remote device will go to the Link Pass state because it sees the AutoNegotiation words transmitted to it as valid idle symbols. For proper operation between two devices, the 8101 and remote device must both be either set with AutoNegotiation enabled or set with AutoNegotiation disabled.

5.7 MANAGEMENT COUNTERS

5.7.1 Relationship to IETF and IEEE Specs

The 8101 management counters provide the necessary statistics to completely support the following IETF and IEEE specifications:

(1) IETF RFC 1757: RMON Statistics Group
(2) IETF RFC 1213: SNMP Interfaces Group
(3) IETF RFC 1643: Ethernet-Like MIB
(4) IEEE 802.3/Cl. 30: Ethernet MIB

A complete list of the counters along with their definitions was already defined in Table 15. A map of the actual MIB objects from the above specifications to the specific counters on the 8101 is shown below in Tables 48-51.

5.7.2 TX Packet and Octet Counters

The 8101 counter set includes packet and octet counters for the transmit packets as well as receive. The RMON specs literally state that packet and octet counters should only tabulate received information. This is sometimes interpreted to mean both transmitted and received information because Ethernet was originally a shared media protocol. As such, the tables below only point to receive packet and octet counters, but the transmit packet and octet counters are also available in counters #17-26 and can be summed with the receive packet and octet counts if desired.

5.8 POWER SUPPLY DECOUPLING

There are twenty three VCC's (VCC[22:0]) and thirty one GND's (GND[30:0]) on the device.

All GND's should also be connected to a large ground plane. If the GND's vary in potential by even a small amount, noise and latchup can result. The GNDís should be kept to within 50 mV of each other.

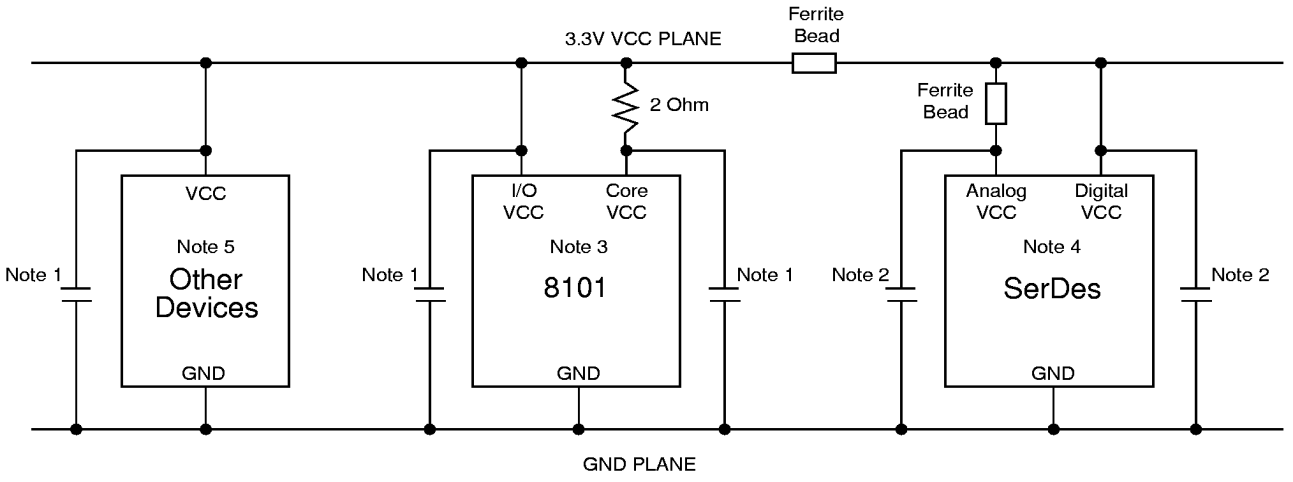
Some of the VCC pins on the 8101 go to the internal core logic, and the remaining VCC's go to the I/O buffers. The core and I/O VCC's should be isolated from each other to minimize jitter on the 10-Bit PHY Interface. It is recommended that all of the I/O VCC's be directly connected to a large VCC plane. It is also recommended that the core VCC's (Pins 70, 97, 135, 147, 193) be isolated from the I/O VCC's with a 2 ohm resistor between the VCC plane and the device core VCC pins, as shown in Figure 9. The 2 ohm resistor will reduce the amount of noise coupling from the I/O VCC's to the core VCC's. A resistor is recommended over a ferrite bead because the inductance of a ferrite bead can induce noise spikes at the device pins. Decoupling capacitors should then be placed between the device VCC pins and GND plane, as shown in Figure 9 and described below.

The external SerDes device that is typically connected to the 10-Bit PHY Interface can also be very sensitive to noise from the VCC plane. Recommendations from the manufacturer of the SerDes chip used should be followed. Generically, it has been found from practice that the SerDes should be isolated from all devices on the PCB with a ferrite bead between the VCC plane and all of the SerDes VCC pins, as shown in Figure 9. In addition, it has been found from practice that the analog and digital VCC pins on the SerDes device should be isolated from each other with a ferrite bead placed between the analog SerDes VCC pins and the digital SerDes VCC pins, as shown in Figure 9. Decoupling capacitors should then be placed between the SerDes device VCC pins and GND plane, as shown in Figure 9 and described below.

For the 8101 and other digital devices, there should be a pair of 0.1 uF and 0.001 uF decoupling capacitors con-

nected between VCC and GND for every four sets of VCC/GND pins placed as close as possible to the device pins, preferably within 0.5" and evenly distributed around all four sides of the devices. For the external SerDes device, there should be a pair of 0.1/0.001 uF capacitors for every two sets of VCC/GND pins. The 0.1 uf and 0.001 uf capacitors reduce the low and high frequency noise, respectively, on the VCC at the device.

The PCB layout and power supply decoupling discussed above should provide sufficient decoupling to achieve the following when measured at the device: (1) The resultant AC noise voltage measured across each VCC/GND set should be less than 100 mVpp, (2) All VCCís should be within 50 mVpp of each other, and (3) All GNDís should be within 50 mVpp of each other.



Note 1. Recommended to have 0.1/0.001uF pair for every four (4) VCC's less than 0.5" from device VCC/GND pins, evenly distributed around all four sides of the devices.

Note 2. Same as Note 1 except every two (2) VCC's.

Note 3. Core VCC pins are 70, 97, 135, 147, and 193. All remaining VCC pins are I/O VCC's.

Note 4. These are generic recommendations for SerDes. Follow any specific recommendations from SerDes manufacturer.

Note 5. This is a generic recommendation for other digital devices. Follow any specific recommendations from device manufacturers

Figure 9. Decoupling Recommendations

Table 48.
MIB Objects vs. Counter Location
For RMON Statistics Group MIB
(RFC 1757)

MIB Objects	Counter Location	
	Ctr. #	Reg. Addr. (Lo/Hi)
etherStatsDropEvents	1	10000000 10000001
etherStatsOctets	2	10000010 10000011
etherStatsPkts	3	10000100 10000101
etherStatsBroadcastPkts	4	10000110 10000111
etherStatsMulticastPkts	5	10001000 10001001
etherStatsCRCAlignErrors	6	10001010 10001011
etherStatsUndersizePkts	7	10001100 10001101
etherStatsOversizePkts	8	10001110 10001111
etherStatsFragments	9	10010000 10010001
etherStatsJabber	10	10010010 10010011
etherStatsCollisions	11	10010100 10010101
etherStatsPkts64Octets	12	10010110 10010111
etherStatsPkts65to127Octets	13	10011000 10011001
etherStatsPkts128to255Octets	14	10011010 10011011
etherStatsPkts256to511Octets	15	10011100 10011101
etherStatsPkts512to1023Octets	16	10011110 10011111
etherStatsPkts1024to1518Octets	17	10100000 10100001

Table 49.
MIB Objects vs. Counter Location
For SNMP Interface Group MIB
(RFC 1213 & 1573)

MIB Objects	Counter Location	
	Ctr. #	Reg. Addr. (Lo/Hi)
ifInOctets	28	10110110 10110111
ifInUcastPkts	29	10111000 10111001
ifInMulticastPkts	5	10001000 10001001
ifInBroadcastPkts	4	10000110 10000111
ifInNUcastPkts	5 + 4	10001000 10001001 + 10000110 10000111
ifInDiscards	1	10000000 10000001
ifInErrors	6 + 7 + 8	10001010 10001011 + 10001100 10001101 + 10001110 10001111
ifOutOctets	30	10111010 10111011
ifOutUcastPkts	31	10111100 10111101
ifOutMulticastPkts	32	10111110 10111111
ifOutBroadcastPkts	33	11000000 11000001
ifOutNUcastPkts	32 +33	10111110 10111111 + 11000000 11000001
ifOutDiscards	34	11000010 11000011
ifOutErrors	35	11000100 11000101

Table 50.
MIB Objects vs. Counter Location
For Ethernet-Like Group MIB
(RFC 1643)

MIB Objects	Counter Location	
	Ctr. #	Reg. Addr. (Lo/Hi)
dot3StatsAlignmentErrors	36	11000110 11000111
dot3StatsFCSErrors	6	10001010 10001011
dot3StatsSingleCollisionFrames	38	11001010 11001011
dot3StatsMultipleCollisionFrames	39	11001100 11001101
dot3StatsSQETestErrors	40	11001110 11001111
dot3StatsDeferredTransmissions	41	11010000 11010001
dot3StatsLateCollisions	42	11010010 11010011
dot3StatsExcessiveCollisions	43	11010100 11010101
dot3StatsInternalMacTransmitErrors	34	11000010 11000011
dot3StatsCarrierSenseErrors	44	11010110 11010111
dot3StatsFrameTooLongs	8	10001110 10001111
dot3StatsInternalMacReceiveErrors	1	10000000 10000001

Table 51.
MIB Objects vs. Counter Location
For Ethernet MIB
(IEEE 802.3z Clause 30)

MIB Objects	Counter Location	
	Ctr. #	Reg. Addr. (Lo/Hi)
aFramesTransmittedOK	19-35	10100100 10100101 - 11000100 11000101
aSingleCollisionFrames	38	11001010 11001011
aMultipleCollisionFrames	39	11001100 11001101
aFramesReceivedOK	29 + 4+5	10111000 10111001 + 10000110 10000111 + 10001000 10001001
aFrameCheckSequenceErrors	6	10001010 10001011
aAlignmentErrors	36	11000110 11000111
aOctetsTransmittedOK	45	11011000 11011001
aFramesWithDeferredXmissions	41	11010000 11010001
aLateCollisions	42	11010010 11010011
aFrameAbortedDueToXSCollisions	43	11010100 11010101
aFrameAbortedDueToIntMACXmitError	34	11000010 11000011
aCarrierSenseErrors	44	11010110 11010111
aOctetsReceivedOK	46	11011010 11011011
aFramesLostDueToIntMACRcvrError	1	10000000 10000001

Table 51. (cont'd)
MIB Objects vs. Counter Location
For Ethernet MIB
(IEEE 802.3z Clause 30)

MIB Objects	Counter Location	
	Ctr. #	Reg. Addr. (Lo/Hi)
aMulticastFrameXmittedOK	21	10101000 10101001
aBroadcastFramesXmittedOK	20	10100110 10100111
aFramesWithExcessiveDefferal	47	11011100 11011101
aMulticastFramesReceivedOK	5	10001000 10001001
aBroadcastFramesReceivedOK	4	10000110 10000111
aInRangeLengthErrors	48	11011110 11011111
aOutOfRangeLengthField	49	11100000 11100001
aFrameTooLongErrors	8	10001110 10001111
aSQETestErrors	40	11001110 11001111
aSymbolErrorDuringCarrier	50	11100010 11100011
aMACControlFramesTransmitted	52	11100110 11100111
aMACControlFramesReceived	53	11101000 11101001
aUnsupportedOpcodesReceived	51	11100100 11100101
aPauseMACCtrlFramesTransmitted	52	11100110 11100111
aPauseMACCtrlFramesReceived	53	11101000 11101001

6.0 Specifications

6.1 ABSOLUTE MAXIMUM RATINGS

Absolute maximum ratings are limits beyond which may cause permanent damage to the device or affect device reliability. All voltages are specified with respect to GND, unless otherwise specified.

VCC Supply Voltage ..... -.3V to 4.0V
All Inputs and Outputs ..... -.3V to 5.5V
Package Power Dissipation ..... 2.2 Watt @ 70°C
Storage Temperature ..... -65° to +150°C
Temperature Under Bias ..... -10° to + 85°C
Lead Temperature (Soldering, 10 Sec) .....260°C
Body Temperature (Soldering, 30 Sec) .....220°C

6.2 DC ELECTRICAL CHARACTERISTICS

Unless otherwise noted, all test conditions are as follows:

1. TA= 0 to +70° C
2. VCC= 3.3V +/-5%
3. SCLK = 66 Mhz +/- 0.01%,
4. TCLK = 125 Mhz +/- 0.01%

SYM	PARAMETER	LIMIT			UNIT	CONDITIONS
		MIN	TYP	MAX		
VIL	Input Low Voltage			0.8	Volt	
VIH	Input High Voltage	2		5.5	Volt	
IIL	Input Low Current			-1	µA	VIN=GND
IIH	Input High Current			1	µA	VIN=VCC
VOL	Output Low Voltage	GND		0.4	Volt	IOL=-4 mA All Except $\overline{\text{LINK}}$
		GND		1	Volt	IOL=-20 mA $\overline{\text{LINK}}$
VOH	Output High Voltage	2.4		VCC	Volt	IOL=4 mA All Except $\overline{\text{LINK}}$
		VCC –1.0		VCC	Volt	IOL=20 mA $\overline{\text{LINK}}$
CIN	Input Capacitance			5	pF	
ICC	VCC Supply Current			300	mA	No output load

6.3 AC ELECTRICAL CHARACTERISTICS

Unless otherwise noted, all test conditions are as follows:

1. TA = 0 to +70°C
2. VCC = 3.3V +/-5%
3. SCLK = 66 Mhz +/- 0.01%,
4. TCLK = 125 Mhz +/- 0.01%
5. Input conditions:
   All Inputs: tr,tf <= 4nS, 0.8V to 2.0V
6. Output Loading
   TBC, TX[0:9]: 10pF
   LINK: 50pF
   All Other Digital Outputs: 30pF
7. Measurement Points:
   Data Active to Hi-Z: 200mV Change
   Data Hi-Z to Active: 200mV Change
   All inputs and outputs: 1.5 Volts

INPUT CLOCK TIMING CHARACTERISTICS

Refer To Figure 10 For Timing Diagram

SYM	PARAMETER	LIMIT			UNIT	CONDITIONS
		MIN	TYP	MAX		
t_1	SCLK Cycle Time	1/33		1/66	1/Mhz	
t_2	SCLK Duty Cycle	40		60	%	
t_3	TCLK Period	7.9992	8	8.0008	nS	
t_4	TCLK High Time	3.6		4.4	nS	
t_5	TCLK Low Time	3.6		4.4	nS	
t_6	TCLK to TBC Delay	0		8	nS	
t_7	REGCLK Cycle Time	1/5		1/40	1/Mhz	
t_8	REGCLK Duty Cycle	40		60	%	

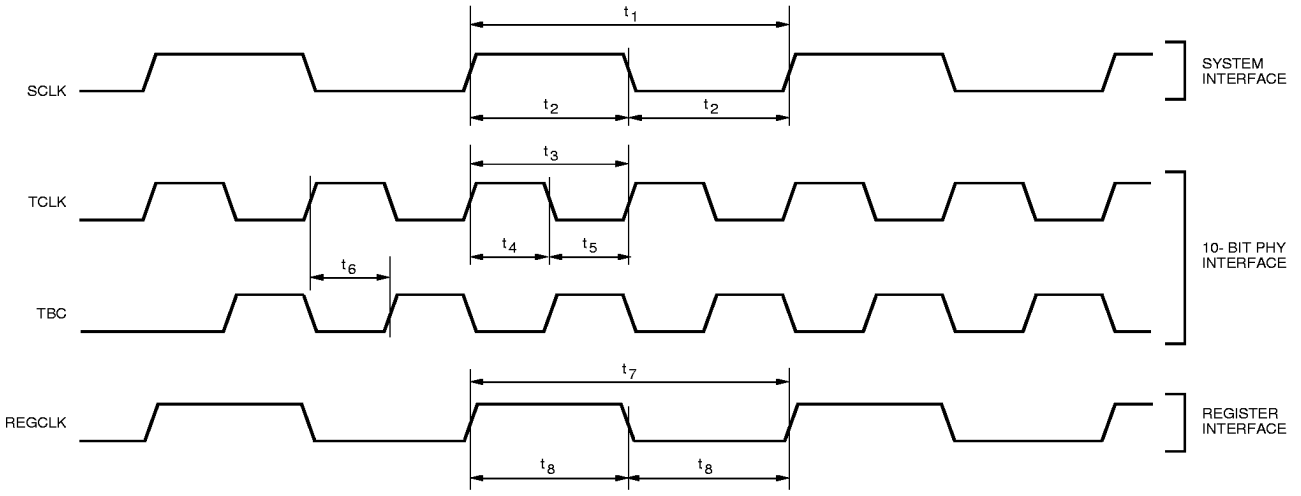
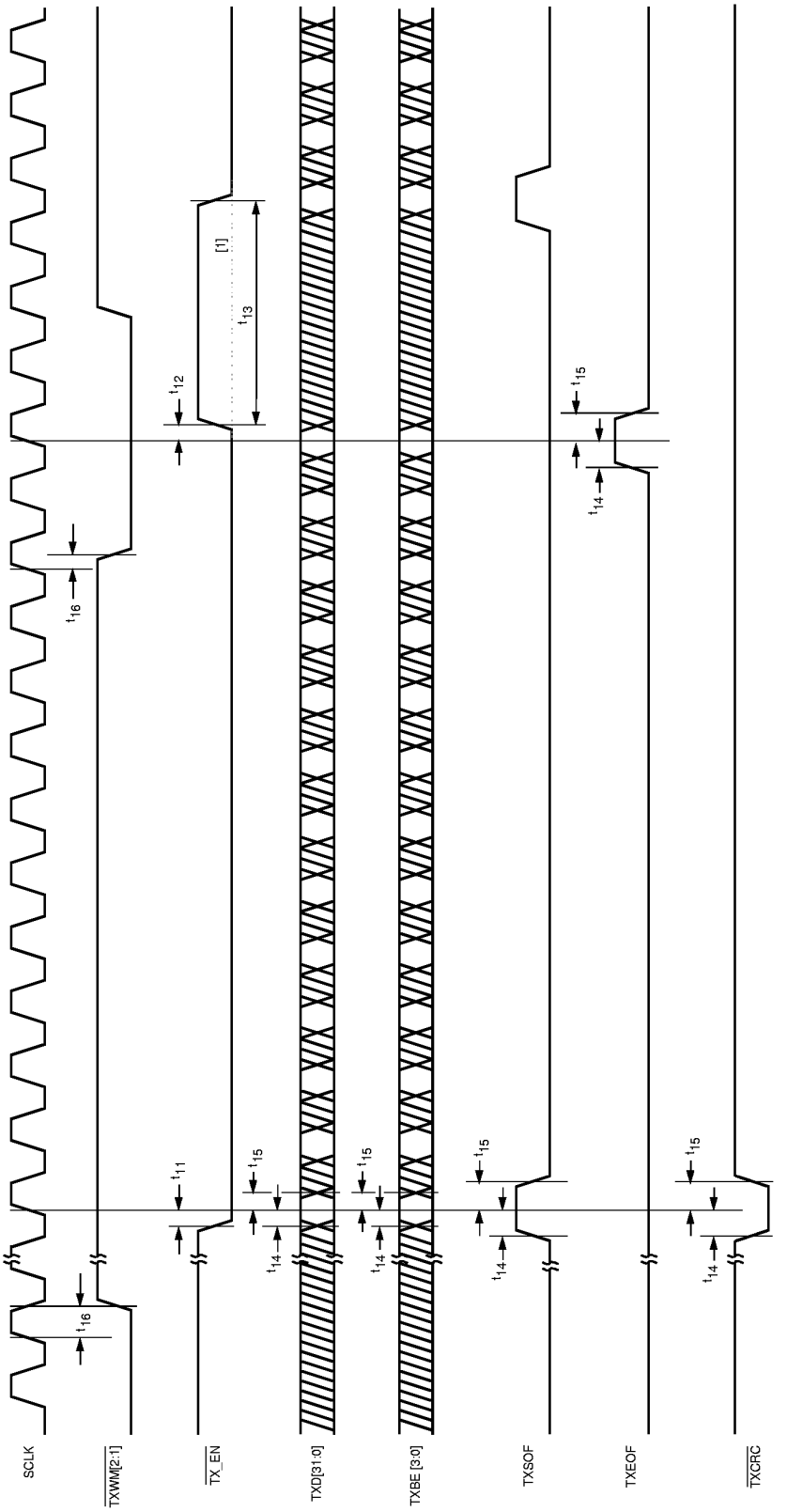


Figure 10. Input Clock Timing

TRANSMIT SYSTEM INTERFACE TIMING CHARACTERISTICS

Refer To Figure 11 For Timing Diagram

SYM	PARAMETER	LIMIT MIN	LIMIT TYP	LIMIT MAX	UNIT	CONDITIONS
t_{11}	$\overline{\text{TXEN}}$ Setup Time	5			nS	
t_{12}	$\overline{\text{TXEN}}$ Hold Time	0			nS	
t_{13}	$\overline{\text{TXEN}}$ Deassert Time	1 SCLK Cycle			nS	
t_{14}	TXD, TXBE, $\overline{\text{TXSOF}}$, TXEOF, and TXCRC Setup Time	5			nS	
t_{15}	TXD, TXBE, $\overline{\text{TXSOF}}$, TXEOF, and TXCRC Hold Time	0			nS	
t_{16}	$\overline{\text{TXWM}}$ Delay Time	0		8	nS	
t_{17}	$\overline{\text{TXWM}}$ Rise/Fall Time			4	nS	



Note 1: Back to back packet transmission allowed without TXEN deassertion.

Figure 11. Transmit System Interface Timing

RECEIVE SYSTEM INTERFACE TIMING CHARACTERISTICS

Refer To Figures 12-14 For Timing Diagram

SYM	PARAMETER	LIMIT			UNIT	CONDITIONS
		MIN	TYP	MAX		
t_{31}	$\overline{\text{RXEN}}$ Setup Time	5			nS	
t_{32}	$\overline{\text{RXEN}}$ Hold Time	1			nS	
t_{33}	$\overline{\text{RXEN}}$ Deassert Time	3 SCLK Cycles			nS	
t_{34}	RXD, RXBE, RXSOF, RXEOF, and RXWM Delay Time	0		8	nS	
t_{35}	RXD, RXBE, RXSOF, RXEOF, and RXWM Rise/Fall Time			4	nS	
t_{41}	RXABORT Setup Time	5			nS	
t_{42}	RXABORT Hold Time	0			nS	
t_{43}	RXABORT Assert to RXWM Deassert Delay	0		1 SCLK Cycles + 8 nS	nS	
t_{46}	$\overline{\text{RXOE}}$ Deassert to Data Hi-Z Delay	0		15	nS	
t_{47}	$\overline{\text{RXOE}}$ Assert To Data Active Delay	0		15	nS	

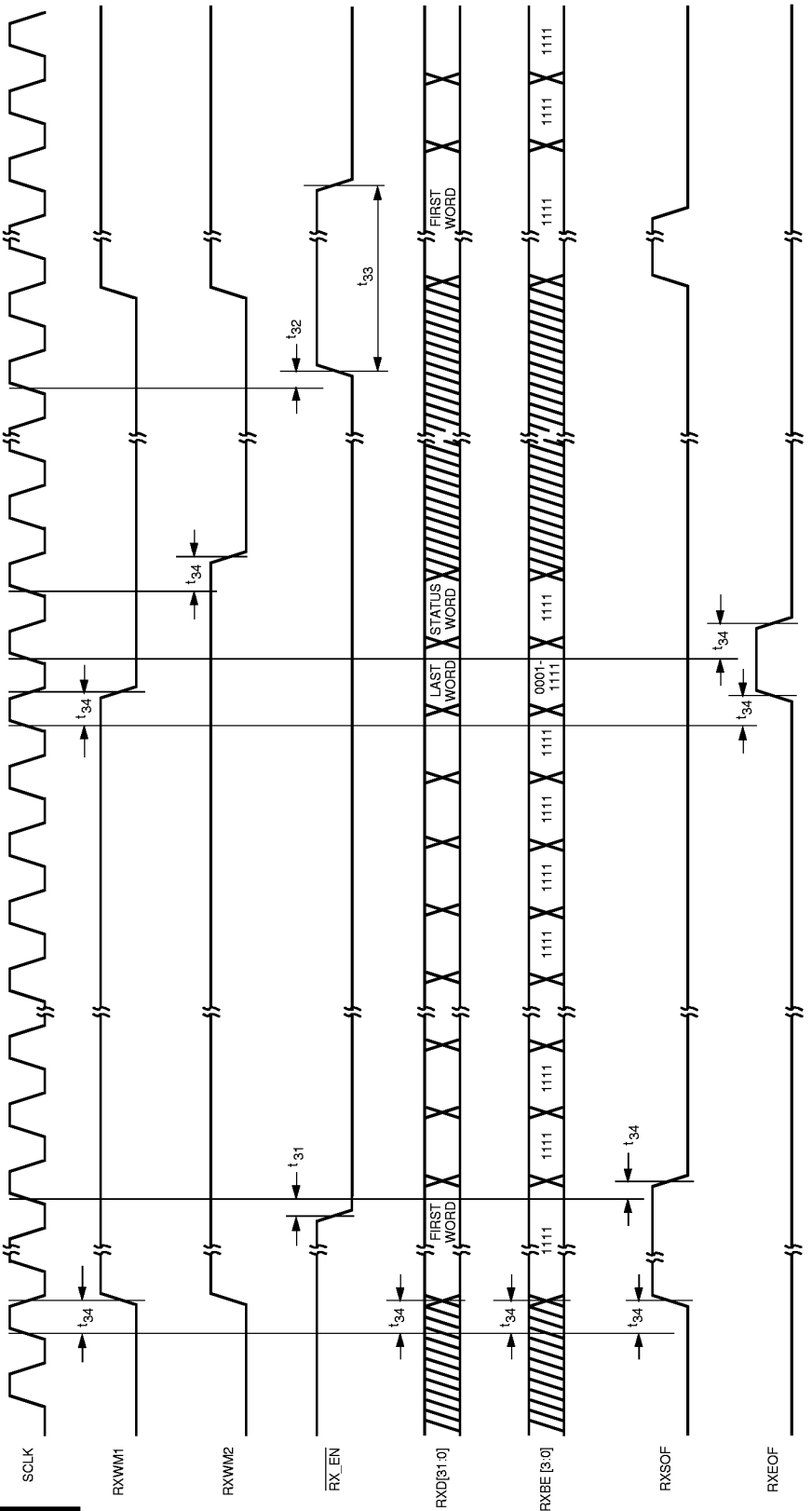


Figure 12. Receive System Interface Timing

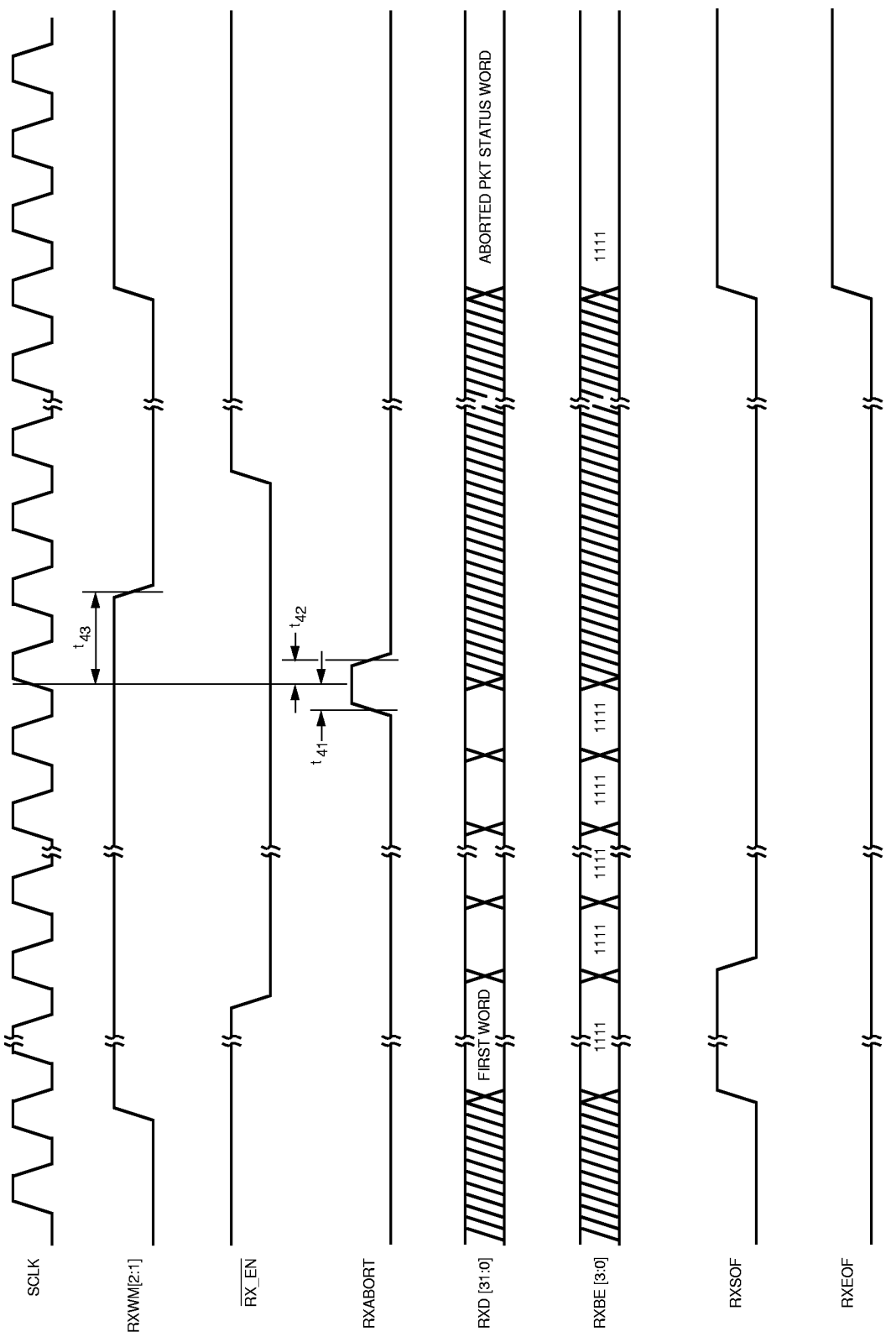


Figure 13. Receive System Interface RXABORT Timing

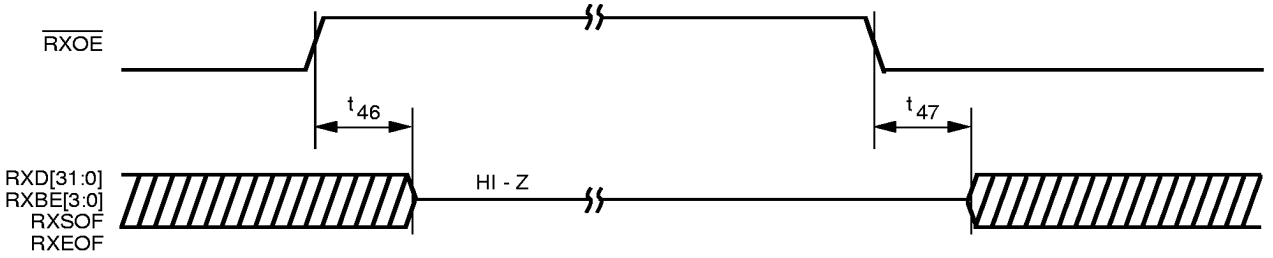


Figure 14. Receive System Interface $\overline{\text{RXOE}}$ Timing

SYSTEM INTERFACE TXDC/RXDC TIMING CHARACTERISTICS

Refer To Figure 15 For Timing Diagram

SYM	PARAMETER	LIMIT			UNIT	CONDITIONS
		MIN	TYP	MAX		
t_{51}	TXDC/RXDC Assert Delay Time	0		8	nS	
t_{52}	TXDC/RXDC Deassert Delay Time	0		2 SCLK Cycle + 8 nS	nS	AutoClear Mode Off
		0		3 SCLK Cycle + 8 nS	nS	AutoClear Mode On
t_{53}	CLR_TXDC/RXDC Setup Time	5			nS	
t_{54}	CLR_TXDC/RXDC Hold Time	0			nS	
t_{55}	TXDC/RXDC Rise and Fall Time			4	nS	

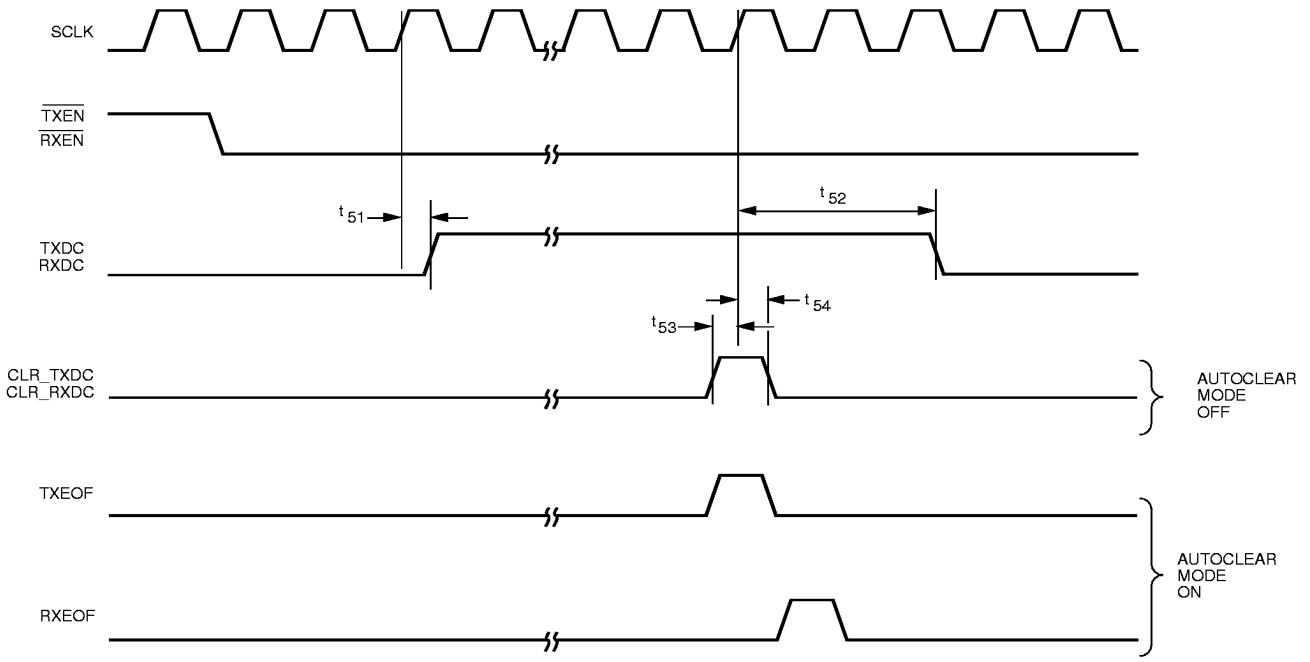


Figure 15. System Interface RXDC/TXDC Timing

TRANSMIT 10-BIT PHY INTERFACE TIMING CHARACTERISTICS

Refer To Figure 16 For Timing Diagram

SYM	PARAMETER	LIMIT			UNIT	CONDITIONS
		MIN	TYP	MAX		
t_{61}	TBC Period	7.992	8	8.008	nS	
t_{62}	TBC High Time	3.2		4.8	nS	
t_{63}	TBC Low Time	3.2		4.8	nS	
t_{64}	TX[0:9] Data Valid Before TBC Rising Edge	2.0			nS	Assumes TBC Duty Cycle = 40 - 60%
t_{65}	TX[0:9] Data Valid After TBC Rising Edge	1.0			nS	Assumes TBC Duty Cycle = 40 - 60%
t_{66}	TBC, TX[0:9] Rise and Fall Time	0.7		2.4`	nS	

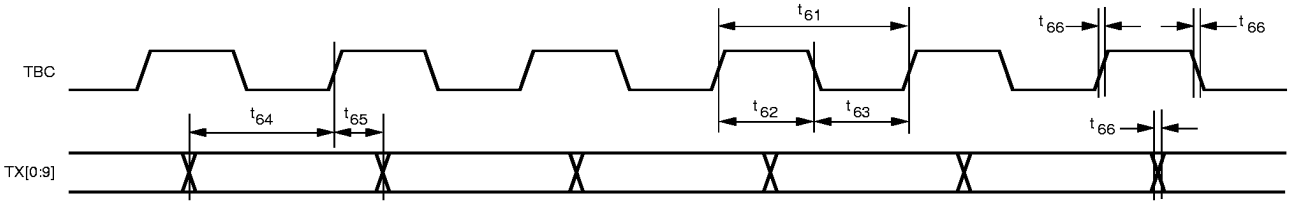


Figure 16. Transmit 10-Bit PHY Interface Timing

RECEIVE 10-BIT PHY INTERFACE TIMING CHARACTERISTICS

Refer To Figure 17 For Timing Diagram

SYM	PARAMETER	LIMIT			UNIT	CONDITIONS
		MIN	TYP	MAX		
t_{71}	RBC Frequency	62.4937	62.5	62.5063	Mhz	
t_{72}	RBC High Time	6.4		9.6	nS	
		6.4		128	nS	During Synchronization
t_{73}	RBC Low Time	6.4		9.6	nS	
		6.4		128	nS	During Synchronization
t_{74}	RBC Skew	7.5		8.5	nS	
t_{75}	RX[0:9] Setup Time	2.5			nS	
t_{76}	RX[0:9] Hold Time	1.5			nS	
t_{77}	RBC, RX[0:9] Rise and Fall Time	0.7		2.4	nS	

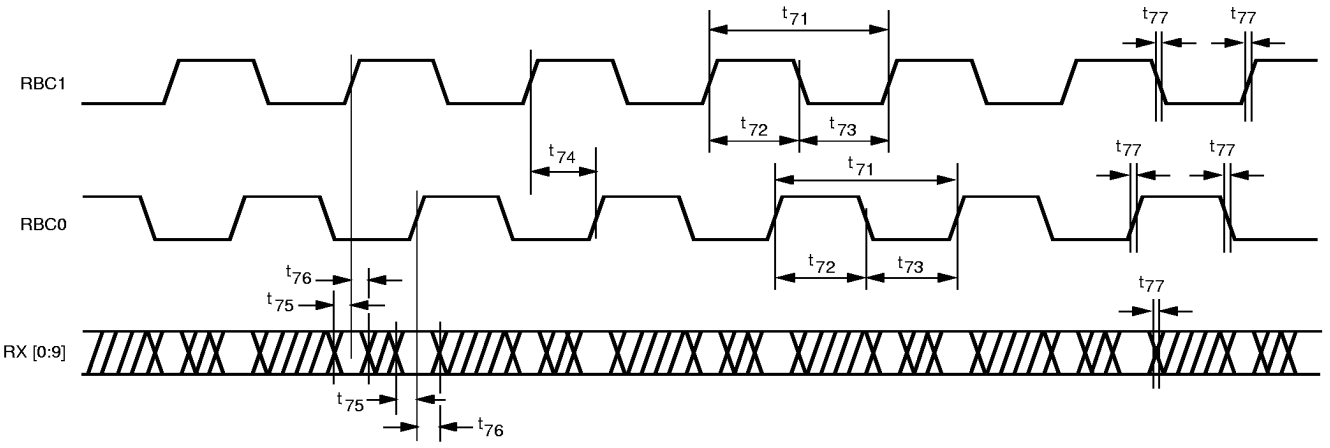


Figure 17. Receive 10-Bit PHY Interface Timing

REGISTER INTERFACE TIMING CHARACTERISTICS

Refer To Figure 18 and 19 For Timing Diagram

SYM	PARAMETER	LIMIT MIN	LIMIT TYP	LIMIT MAX	UNIT	CONDITIONS
t_{81}	$\overline{REGCS}$, $\overline{REGWR}$, $\overline{REGRD}$, REGA, REGD Setup Time	10			nS	
t_{82}	$\overline{REGCS}$, $\overline{REGWR}$, $\overline{REGRD}$, REGA, REGD Hold Time	1			nS	
t_{83}	REGCLK to REGD Active Delay			10	nS	Read Cycle. All Registers Except Counter Registers 1-53
				6 REGCLK Cycles +10 nS	nS	Read Cycle. Counter Registers 1-53, 1st 16-bit of Counter Result
				3 REGCLK Cycles +10 nS	nS	Read Cycle. Counter Registers 1-53, 2nd 16-bits of Counter Result
t_{84}	REGCLK to REGD HI-Z Delay	0		10	nS	
t_{85}	REGCLK to REGINT Assert Delay	0		20	nS	
t_{86}	REGCLK to REGINT Deassert Delay	0		20	nS	

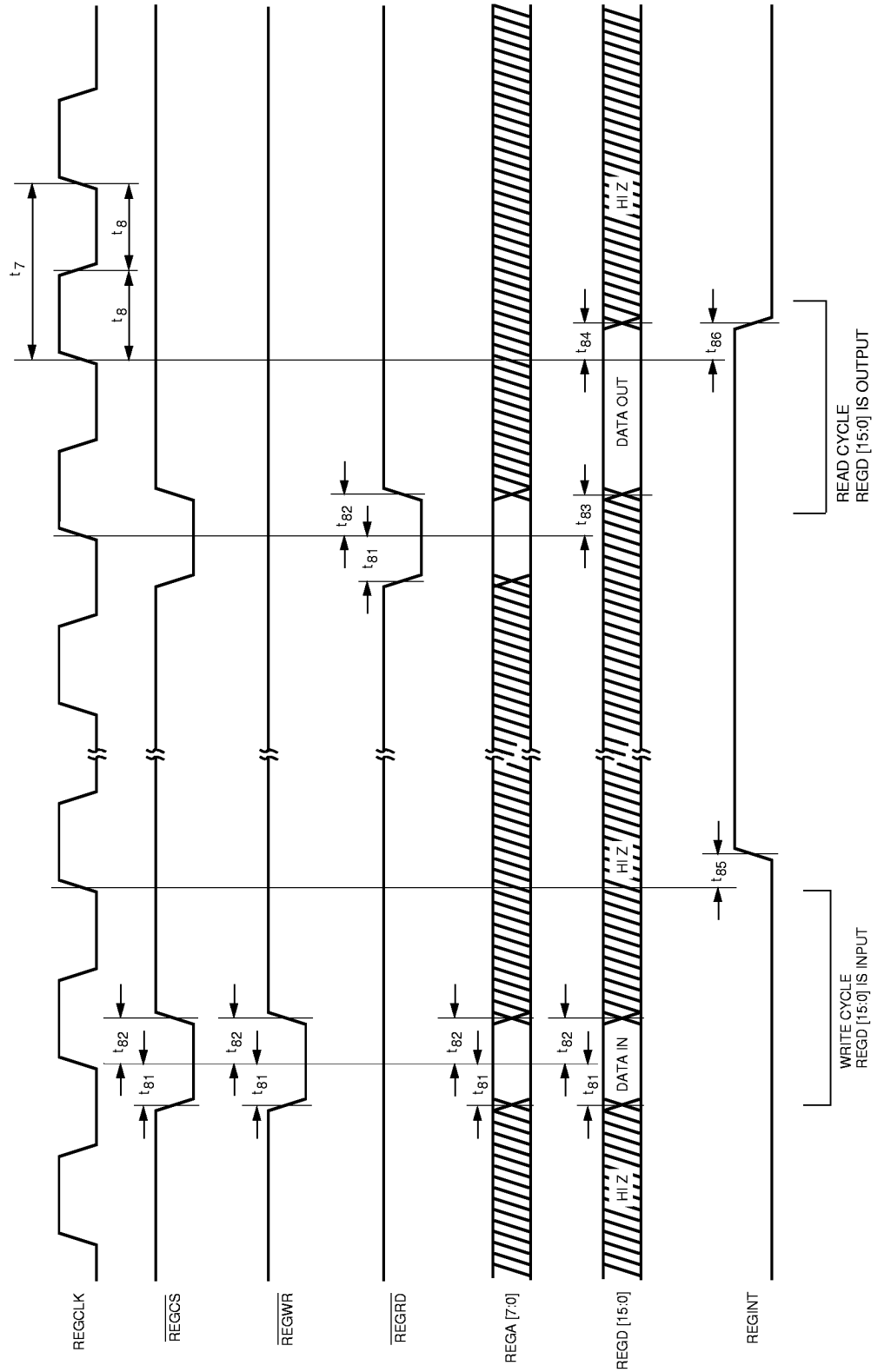


Figure 18. Register Interface Timing (Excluding Counter Read Cycle)

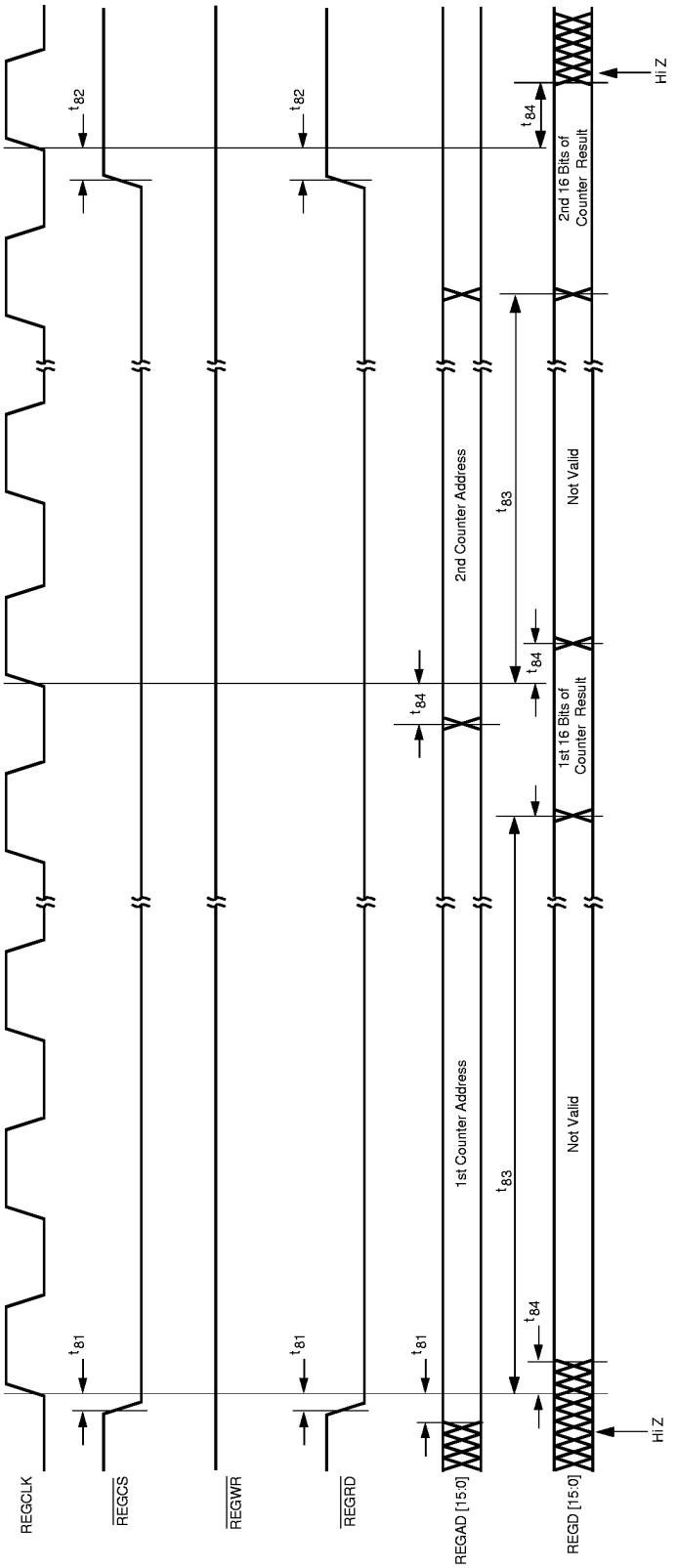
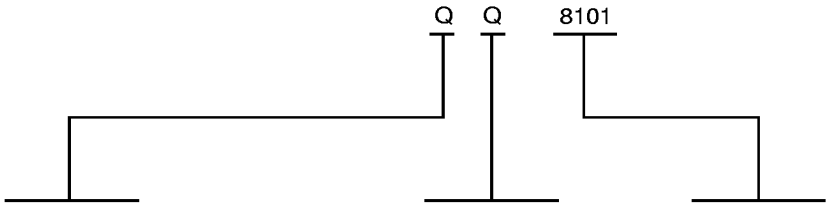


Figure 19. Register Interface Timing, Counter Read Cycle

Ordering Information



Revision History

3/17/98: Initail release, Document Number MD400176/–

4/27/98

- 4/27/98 Document Reveision Changed to MD400176/A

Page 5: 1.0 Pin Description
- Reference to +5V has been changed to +3.3V.

Page 6: 1.0 Pin Description
- PIN #149 Description copy change; ...SCLK clock frequency is 33-66 MHZ.... has been changed to...SCLK clock frequency must be between 33-66 MHZ.

- Pin #137 Description; reference to Data < Transmit has been changed to Data ≤ Transmit.

Page 7: 1.0 Pin Description
- Pin #136 Description; reference to Data < Transmit has been changed to Data ≤ Transmit.

Page 8: 1.0 Pin Description
- Pin #156 Description; reference to Data ≥ Receive has been changed to Data > Receive and reference to Below Threshold, has been changed to Equal to or Below Threshold
- Pin #155 Description; reference to Data ≥ Receive has been changed to Data > Receiveand reference to Below Threshold, has been changed to Equal to or Below Threshold

Page 9: 1.0 Pin Description
- Pin # 68 copy change; frequency can be between 5-40 MHz... has been changed to frequency must be between 5-40 MHz.

Page 19: 3.5.5 Multicast Address Filter
- Copy change ... Address Filter registers... has been changed to ...Address Filter 1-4 registers...

Page 21: Section 3.6.6 Link Down FIFO Flush
- Copy change paragraph one; ...transmit FIFO while the device... has been changed ... totransmit FIFO from the System Interface while the device...
- Section 3.6.2 Watermarks; Paragraph two copy change, ...of the FIFO. Once the end of packet has been read... has been changed to ...of the receive FIFO. Once the EOFs has been read...

Revision History

Page 24: Section PHY Loopback
- Copy change paragraph one; ...The EWRAP output is controlled... has been changed to ...The EWRAP output pin is controlled...
- Copy change paragraph two; ...When the EWRAP pin/bit is asserted,...has been changed to ...When the EWRAP pin is asserted,...

Page 26: 3.9.3 Receive Discards
- Copy change paragraph four; Reference to Table 8 has been changed to Table 10.
- Table 10 Receive Discard Conditions; RXABORT pin Description copy change, ...packet length in bytes/8 + 6.... has been chnaged to ... [(packet length in bytes)/8 + 6].

Page 27: 3.11.1 General
- Copy change paragraph one, ...8101 is compatible with the AutoNegotiation algorithm defined in IEEE 802.3z. has been changed to ...8101 meets all specifications defined in IEEE 802.3z.

Page 30: 3.13.6 MAC Control Frame AutoSend
- Copy change paragraph one,...Pause frame generated mechanism is described ... has been changed to ...Pause frame generation mechanism is described ...

Page 32: Section 3.15.1
- Paragraph 2 has been completely changed.
- New Paragraph 3.
- Current paragraph 4 has been changed.

Page 40: Section 3.18.1General
- Copy change paragraph one; ...The clock, REGCLK, can operate between 5-40 Mhz. ... has been changed to ... The REGCLK, clock Frequency must be between 5-40 Mhz....
- Section 3.16 Loopback; Copy change, ...and stored in the transmit FIFO is internally looped back into the receive FIFO and is available... has been changed to...and output from the 8BIOB Encoder is internally looped back into the receive 8B10B Decoder and is available ...
- Section 3.18.1 General; Paragraph 3 has been added.

Page 41: Section 3.18.3 Interrupt
- Copy change paragraph one, Reference to Status have been changed to Status 1.

Page 46: Table 18 Register Bit Map (cont'd)
- 32 Device ID Part0, 0 has been changed to 1.
- 32 Device ID, HREV3, HREV2, HREV1, HREV0, R 0 has been changed to R X.
- 32 Device ID, SREV3, SREV2, SREV1, SREV0, R 0 has been changed to R X.

Page 56: Table 28 Register 9
- Bit 9.5, 9.4, Definition Has been changed.

Page 60; Table 32 Register 17
- Definitions have been changed.

Revision History

Page 61; Table 33 Register 18
- Definitions have been changed.

Page 68; Table 40 Register 32
- Bit, 32.11, 32.10, 32.9, 32.8, 0 has been changed toX.
- Bit, 32.3, 32.2, 32.1, 32.0, 0 has been changed toX.

Page 78: 6.2 DC Electricval Characteristics
- VIH Max is now 5.5
- 6.1 Absolute Maximum Ratings; VCC Supply Voltage is now -3V to 4.0V, and All Inputs and Outputs is now -.3V to 5.5V.

Page 87: System Interface TXDC/RXDC Timing Characteristics
- t_{55} (MIN) isa now blank and (MAX) is now 5.5.

Page 91: Register Interface Timing Characteristics
- Section t_{83} has been completely changed

Page 92: Figure 17 Title has been changed to; Register Interface Timing (Excluding Counter Read Cycle)

Page 93: New Figure 18. Register Interface Timing, Counter Real Cycle

4/27/99

4/27/99 Document Revision changed to MD400176/B

Page 2, 1.0 Pin Configuration
- Pins Numbered 4, 5, 6, 8, 9, and 151 have been changed from Reserved to VCC.

Page 3, Table of Contents
- Heading, 3.8.8 TBC Disable, has been added to TOC

Page 4, Table of Contents
- Headings 5.4 Management Counters has been changed to 5.4 RESET, 5.5 Power Supply Decoupling has been changed to 5.5 LOOPBACK, and Headings 5.6, 5.7, 5.8 are now AutoNegotiation, Management Counters and Power Supply Decouplings.

Page 5, 1.0 Pin Description
- Pin # 4, 5, 6 , 8, 9, 151 have been added to Power Supplies, Pin Name [22:0]
- Pin Name, VCC[16:0] has been changed to VCC[22:0]
- 10-Bit PHY Interface, Pin #32, Description copy change; ...output clocks transmit data out on TX[0:9] on falling edges. has been changed to ...output clocks transmit data out on TX[0:9] on rising edges.
- Pin Name TX[0:9] Description copy change; ... outputs contain transmit data which are clocked out on falling edges of TBC. has been changed to ...outputs contain transmit data which are clocked out on rising edges of TBC.

Page 10, 1.0 Pin Description
- Miscellaneous, Pin #10 Description, copy change; 1 = All Pins Placed in High Impedance State has been changed to 1 = All Output and Bidirectional Pins Placed in High Impedance State
- Miscellaneous, Reserved Description, Pin # 4, 5, 6, 8, 9, 151 have been changed to VCC
- Pin Name, NC has been changed to Reserve
- Description copy change; Reserved. These pins must be left floating. has been changed to Reserved. These pins are reserved and must be left floating.

Revision History

Page 21, Section 3.6.2 AutoSend
- Paragraph 2 copy addition; ...A packet will also be automatically transmitted if an EOF is written into the transmit FIFO... has been added to the paragraph
- Paragraph #3, has been added to section; All of the bit settings for the transmit autosend threshold are evenly distributed over the lower...

Page 25, Section 3.8.8 TBC Disable
- Section 3.8.8 TBC Disable, has been added.

Page 32, Tab le 13. Reset Desription
- Reset TX Counters to 0, has been added to Transmit Reset, Reset Action.
- Reset RX Counters to 0, has been added to Receive Reset, Reset Action.

Page 34, Table 15. Counter Definition (cont'd)
- Ctr.#9, Counter Description Definition, copy change; ...will only count CRC errors or length < 64. has been changed to ...will only count CRC errors with length < 64.
- Ctr.#10, Counter Description Definition, copy change; There is no jabber function in Gigabit Ethernet, so this counter will be 0's. ...has been changed to... There is no jabber function in Gigabit Ethernet, so this counter is undefined.
- Ctr.#11, Counter Description Definition, copy change; This counter will be all 0's in Full Duplex. ...has been changed to... Since device is Full Duplex only, this counter is undefined.

Page 36, Table 15. Counter Definition (cont'd)
- Ctr#37; Ctr#37 is now blank; Counter Description Definition; Equivalent to "etherStatsCRCAlignErrors" has been added; Size bits is now blank; Register Address REGAD[7:0] (Lo/Hi) has been changed to, Use Ctr.#6.
- Ctr.#36, 38, 39, 41, 42, Counter Description Definition, copy change; This counter will be all 0's in Full Duplex. ...has been changed to... Since device is Full Duplex only, this counter is undefined.
- Ctr.#40, Counter Description Definition, copy change; There is no SQE for Gigabit Ethernet, so this counter will be all 0's ...has been changed to... There is no SQE for Gigabit Ethernet, so this counter is undefined.

Page 37, Table 15. Counter Definition (cont'd)
- Ctr#43, Counter Description Definition, copy change; This counter will be all 0's in Full Duplex. ...has been changed to... Since device is Full Duplex only, this counter is undefined.
- Ctr#44, Counter Description Definition, copy change, There is no CRS loopback in 8B10B Ethernet, so this counter will be all 0's. ...has been changed to... There is no CRS loopback in 8B10B Ethernet, so this counter is undefined.

Page 38, Table 15. Counter Definition (cont'd)
- Ctr#47, Counter Description Definition, copy change; This counter will be all 0's in Full Duplex. ...has been changed to... Since device is Full Duplex only, this counter is undefined.

Page 40, 3.18.1 General
- Paragraph #3, copy change; ...in less than one REGCLK cycle. Data read from the Counter 1-53 registers takes approximately 6 REGCLK cycles to be available on REGD[15:0] for the first 16-bits of counter result, and at most 3 REGCLK... has been changed to ...in one REGCLK cycle. Data read from the Counter 1-53 registers takes at most 6 REGCLK cycles to be available on REGD[15:0] for the first 16-bits of counter result, and approximately 3 REGCLK...

Page 43, Table 17. Register Address Table (cont'd)
- Register# 200-201 Register Name has been changed to Reserve.

Revision History

Page 45, Table 18. Register Bit Map
- 10 Configuration 4, Bit x.10 has been changed from 0 to TBC_DIS
- 18 Receive FIFO Threshold, Bits (x.7, R/W 0), (x.6, R/W 0), (x.5, R/W 1), (x.4, R/W 1), has been changed to (x.7, R/W 1), (x.6, R/W 1), (x.5, R/W 0), (x.4, R/W 0).

Page 46, Table 18. Register Bit Map (cont'd)
- 20 Flow Control 2, Bits (x.15, R/W 0), (x.14, R/W 0), (x.13, R/W 0), (x.12, R/W 0), (x.4, R/W 1), (x.3, R/W 1), (x.2, R/W 1) (x.1, R/W 1), (x.0 R/W 1) has been changed to (x.15, R/W 1), (x.14, R/W 1), (x.13, R/W 1), (x.12, R/W 1), (x.4, R/W 0), (x.3, R/W 0), (x.2, R/W 0) (x.1, R/W 0), (x.0 R/W 0)

Page 56, Table 28. Register 9 (Configuration 3 Register) Definition
- Bit 9.12, Definition copy change, 0 = a No Abort, has been changed to, 0 = No Abort
- Bit 9.0, Definition copy change, 0 = SD Pin Disabled, i.e., Doesn't Affect Receive Word Synchronization, has been changed to, 0 = SD Pin Disabled, i.e., Internal SD always Asserted, Doesn't Affect Receive Word Synchronization

Page 57, Table 29. Register 10 (Configuration 4 Register) Definition
- Bit 10.10 has been changed from 0, to TBC_DIS
- Bit 10.10 row has been added
- Bits 10.10, 10.9, 10.8 has been changed to 10.9, 10.8
- Bit 10.8, Definition is 0

Page 60, Table 32. Register 17 (Transmit FIFO Threshold Register) Definition
- Bits [17.5:0] Definition changed from:

Range = 0-512 Words (0-2048 Bytes)
Increment = 8 Words (32 Bytes)
111111 = Transmit Starts When 512 Words In FIFO
111110 = Transmit Starts When 504 Words In FIFO
000010 = Transmit Starts When 24 Words In FIFO
000001 = Transmit Starts When 16 Words In FIFO
000000 = Reserved, Do Not Use

to

Range = 0-1024 Words (0-4096 Bytes)
Increment = 8 Words (32 Bytes)
111111 = Reserved do not use
111110 = Transmit Starts When 504 Words In FIFO
000010 = Transmit Starts When 24 Words In FIFO
000001 = Transmit Starts When 16 Words In FIFO
000000 = Transmit Starts When 992 Words In FIFO

Note 1: An EOF written into FIFO will also start transmission of that packet regardless of the autosend threshold setting.

Note 2: The 000000 setting lets the FIFO fill up before transmission starts, facilitating transmission of oversize packets.

Page 61, Table 33 Register (Receive FIFO Threshold Register) Definition
- Bits [18.7:0], Definitions have been changed to 1, 1, 0, 0, 0, 0, 0, 0, respectively.

Revision History

Page 63, Table 35. Register 20 (Flow Control 2 Register) Definition
- Bits [20.15:0], Definitions have been changed to 1, 1, 1, 1, 0, 0, 0, 0, 0, 0, 0, 0, 0, 0, 0, 0, respectively.

Page 73, Beginning on Page 73 Sections 5.4 RESET, 5.5 LOOPBACK and 5.6 AUTONEGOTIATION, have been added to data sheet
- Table 45 Bit #6 has been added, and a copy change for bit #5 Comment, is now Stop Reset Action.

Page 75, Section 5.8 POWER SUPPLY DECOUPLING
- New Section 5.8 POWER SUPPLY DECOUPLING, has replaced the old section.

Page 76, Figure 9. Decoupling Recommendations is new.

Pages 77-79, Tables Numbers 45-48 have been changed to numbers 48-51 respectively.

Page 78, Table 50 and Table 51
- dot3StatsFCSErrors, Ctr.# has been changed from 37 to 6 and Reg. Addr. (Lo/Hi) values have changed.
- Table 51, aFrameCheckSequenceErrors, Ctr.# has been changed from 37 to 6 and Reg. Addr. (Lo/Hi) values have changed.

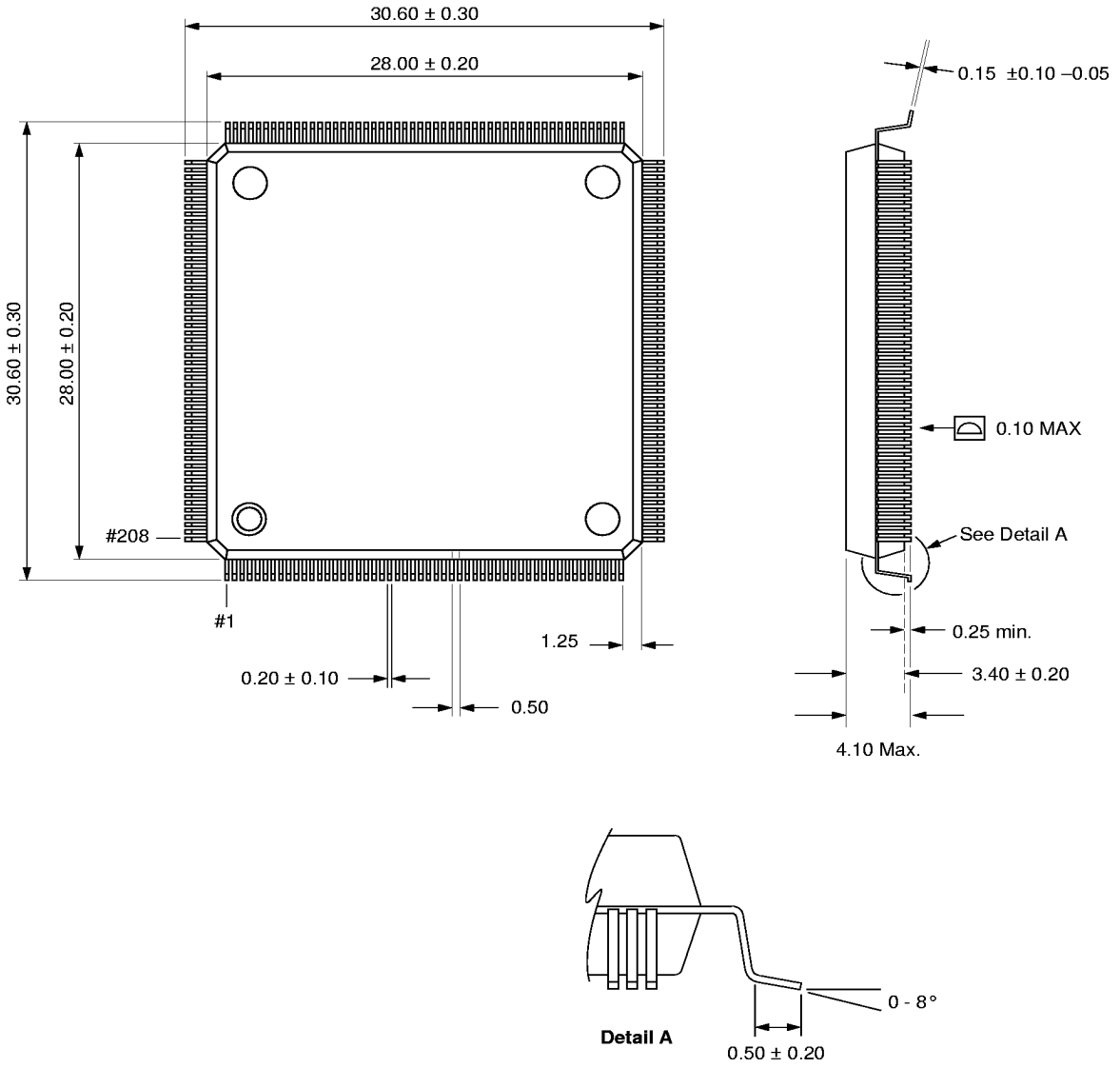
Page 80, 6.2 DC Electrical Characteristics
- Sym CIN, (MIN) 5 pF has been switched to (MAX) 5 pF.
- Sym ICC (MAX) 400 has been changed to 300mA.

Pages 81 to 95 references to Figures 9 - 18 have been changed to 10 -19 respectively.

Page 86, Figure 12. Receive System Interface Timing
- Timing RXD[31:0], and RXBE[3:0] have been changed.

Page 95, Figure 19. Register Interface Timing, Counter Read Cycle
- Timing $\overline{\text{REGWR}}$ has been changed.

208 Pin PQFP



1. All Dimensions are in (millimeters).