LSI LOGIC

Full Duplex

HURRICANE™

84301 4-Port Fast Ethernet Controller

98079

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Features

- *Low Power CMOS Technology*
- *4-Port Ethernet Controller Optimized for Switching Hub, Multiport Bridge/Router, Server Applications*
- *Supports 100Base-T4, 100 Base-TX, 100Base-FX & 10Base-T Transceivers*
- *Meets ANSI/IEEE 802.3 and ISO 8802-3 Standards for Thicknet (10Base-5), Thin Net (10Base-2) and Twisted Pair (10Base-T)*
- *Standard 10MBit/sec Serial Mode or Programmable MII Ethernet Interface for 10/100 MBit/sec Applications*
- *Preamble Generation and Removal*
- *Automatic 32-Bit FCS (CRC) Generation and Checking*
- *Collision Handling, Transmission Deferral and Retransmission with Automatic Jam and Backoff Functions*
- *Transmit Status on a Per Packet Basis Reports the Following*
  - *Occurrence of a Transmit FIFO Underflow*
  - *Transmit Collision Occurrence*
  - *16 Collision Occurrence*
  - *Carrier Sense Error During Transmission*
  - *10/100 Mbit/sec Transmit Clock Detect*
  - *Late Collision Occurrence*
  - *Transmission Successful*
  - *Transmission Deferred*
- *Single 5 V± 5% Power Supply*
- *Loopback Capability for Diagnostics*
- *The Following Additional Features can be Programmed for the 84301*
  - *64 bit Multicast Filter*
  - *Reports Status of "SQE" During Transmits*
  - *Transmit No CRC Mode*
  - *Transmit No Preamble Mode*
  - *Transmit Packet Autopadding Mode*
  - *Receive CRC Mode*
  - *Disable Self-Receive on Transmits Mode*
  - *Disable Further Transmissions when Both Transmit Status Registers are Full*
  - *Disable Loading the Transmit Status for Successfully Transmitted Packets*
  - *Disable the Receive Interrupts Independent of the Receive Command Register Setting*
- *Fifteen 32-bit Counters per Port for Network Management Statistics*
  Receive:
  - *CRC Errors*
  - *Runt Frames*
  - *Oversize Frames*
  - *Alignment Errors*
  - *Collisions*
  - *FIFO Underflow*

  Transmit:
  - *Single Retry Collisions*
  - *Multiple Retry Collisions*
  - *Sixteen Retry Collisions*
  - *FIFO Underruns*
  - *Late Collisions*
  - *Loss of Carrier*
  - *Transmit Deferred*
  - *Total Frames*
  - *Total Octets*
- *Full Duplex Operation*
  - *Provides 20/200 Mbps Bandwidth for Switched Networks*
  - *Supports AutoDUPLEX Mode for Automatic Full Duplex Operation*
- *High Bandwidth Bus Interface*
  - *32 Bits x 33 MHz*
  - *Selectable Big/Little Endianess*
- *Independent 128 Byte Transmit/Receive FIFOs/Port*
  - *Programmable Threshold Flags*
- *Full Backward Compatibility with 84C300A*
- *Error Interrupts and Status Conditions Examples:*
  - *Counter Half-Full*
  - *Rx FIFO Overflow*
  - *Tx FIFO Underflow*
- *208 Pin PQFP package*

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1.0 Pin Description

Pin	Pin Name	I/O	Description
Chip Registers' Interface			
22	$\overline{\text{ENREGIO}}$	I	**Enable Register I/O Operations** This active low input enables the chip for register operations. This input must be low before any port's registers can be written or read.
4	$\overline{\text{WR}}$	I	**Write Strobe** For a selected port within the chip, this input acts as a write strobe for one of the port's registers. The port is selected through the REGPS[1:0] inputs and the register is addressed through the A[4:0] address inputs. The data being written appears on the CDST[7:0] data lines and must be set up relative to the rising edge of the write strobe. This input is active low.
5	$\overline{\text{RD}}$	I	**Read Strobe** For a selected port within the chip, this input acts as a read strobe for one of the port's registers. The port is selected through the REGPS[1:0] inputs and the register is addressed through the A[4:0] address inputs. When the read strobe is active low, the output drivers for CDST[7:0] data bus are enabled. Valid register data appears on the data bus a specified time before the rising edge of the read strobe.
21, 20	REGPS[1:0]	I	**Register Port Select Inputs** These inputs are used to select which port's registers are read or written by asserting the RD or WR read or write strobe inputs. Binary values of 00 through 11 select channels 1 through 4 respectively with REGPS1 being the MSB of the binary value. REGPS1 / REGPS0 / Selected Port 0 / 0 / Port 1 0 / 1 / Port 2 1 / 0 / Port 3 1 / 1 / Port 4
206, 153, 6, 7, 8	A[4:0]	I	**Register Select Address** These inputs are the address lines used to select which register within a port is being read or written. A3 (153) and A4 (206) each has an internal pull down to ensure backward compatibility with the 84C300A.
9-12 15-18	CDST[7:0]	I/O	**Register Data** These bidirectional lines carry register data to or from the internal registers of each port in the chip. These lines are nominally high impedance until their output drivers are enabled by the $\overline{\text{RD}}$ and $\overline{\text{ENREGIO}}$ input pins being driven low.
47, 61, 68, 77	INT_[1:4]	O	**Interrupts** These outputs are driven by a variety of Transmit and Receive interrupt conditions of a particular port. If remains HIGH until the corresponding port's Status Register containing the reason for the interrupt is read.
49	$\overline{\text{RESET}}$	I	**Hardware Reset** This input is an active low asynchronous chip reset. After reset, all registers except the Hash and Station Address registers are reset to zero, all FIFOs are cleared, all counters are reset to zero.

Pin Description (cont.)

Pin	Pin Name	I/O	Description
Receive and Transmit FIFO Interface			
31	RXINTEN	I	**Receive Interface Enable** This is an active low input that acts as a chip enable to enable the receiver interface. Driving this pin active enables the output drivers for the RXDC[1:4] and RXRDY[1:4], pins. Also, this pin must be driven active before receive FIFO reads can be performed.
32	TXINTEN	I	**Transmit Interface Enable** This is an active low input that acts as a chip enable to enable the transmitter interface. Driving this pin active enables the output drivers for the TXRET[1:4], TXRDY[1:4] pins. Also, this pin must be driven active before transmit FIFO writes can be and performed.
36	RXRDEN	I	**Receive Read Enable** This is an active low input that, when driven active with the RXINTEN pin, enables read operations from one of the four receive FIFOs within the chip.
37	TXWREN	I	**Transmit Write Enable** This is an active low input that, when driven active with the TXINTEN pin, enables write operations to one of the four transmit FIFOs within the chip.
35	RXRD_TXWR	I	**Receive Read Transmit Write Clock** This clock input is also the chip's read/write strobe to the chip's eight receive/transmit FIFOs. With the TXINTEN and TXWREN inputs active low, this input becomes the write strobe for writing transmit data to one of the chip's transmit FIFOs. Similarly, with the RXINTEN and RXRDEN inputs active low, this input becomes the read strobe for reading receive data from one of the chip's receive FIFOs. This input must be connected to a continuous clock whose maximum frequency can be 33 MHz.
30, 29	RXTXPS[1:0]	I	**Port Select** These inputs are used to select and identify which port will be accessed for the following operations. 1. Receive FIFO Reads 2. Transmit FIFO Writes 3. Clearing a TXRET Condition 4. Clearing a RXDC Condition 5. Aborting a Receive Packet RXTXPS[1:0] RXTXPS1 / RXTXPS0 / Selected Port 0 0 Port 1 0 1 Port 2 1 0 Port 3 1 1 Port 4
23, 24 25, 26	RXTXBE[3:0]	I/O	**Receive Transmit Byte Enable** These are active low bidirectional signals that determine which bytes of the double word for a receive FIFO read are driven with valid data or which bytes of a double word being written to a transmit FIFO contain valid data.

Pin Description (cont.)

Pin	Pin Name	I/O	Description
44, 57 64, 73	TXRDY_[1:4]	O	**Transmit Ready** These are active high three state outputs. When enabled, these outputs function as a flag that indicates whether the associated port's transmit FIFO has enough space available to meet the threshold value programmed in the FIFO threshold register. When enabled, a high value on any of these outputs indicates that the associated port's transmit FIFO has greater than or equal to the threshold number of double word spaces available in the FIFO and a low value indicates it does not. The tristate drivers for all these outputs are enabled by a low value on the TXINTEN input pin.
42, 56 63, 72	RXRDY_[1:4]	O	**Receive Ready** These are active high three state outputs. When enabled, these outputs function as a flag that indicates whether the associated port's receive FIFO has enough data available to meet the threshold value programmed in the FIFO threshold register. When enabled, a high value on any of these outputs indicates that the associated port's receive FIFO has greater than or equal to the threshold number of double words available in the FIFO or has a completed receive packet in the FIFO as indicated by the packets status double word being in the FIFO. The tristate drivers for all these outputs are enabled by a low value on the RXINTEN input pin.
39	SPDTAVL	O	**Space Data Available** This is an active high output that can be used for validating reads from the receive FIFO during a read operation and preventing over writes to the transmit FIFO during a write operation. For further details, please refer to the Transmit Data Write Timing and the Receive Data Read Timing diagrams.
40	RXTXEOF	I/O	**Receive Transmit End of Frame** This is a bidirectional pin that is used to signal the last double word of a transmit or receive packet. During receive FIFO reads this pin is enabled as an output and when detected high indicates that the last double word of a receive packet has been read from the receive FIFO. During transmit FIFO writes this pin is an input and when asserted high during a write it indicates that this is the final double word of a transmit packet. In the transmit FIFO write case the value of this signal is stored as the 33rd bit in the FIFO. In the receive FIFO read case the value of this signal is read out as the 33rd bit of the receive FIFO.
41	TXNOCRC	I	**Transmit No CRC** This active high input is used to control appending of a CRC to a transmit packet. A transmit packet can be made to exclude appending a CRC value if this input is held high any time during a packet write to the transmit FIFO. Transmission of all packets without CRC can be done by setting bit #4 of configuration register #1. It should be noted that TXNOCRC pin can be used to control CRC encapsulation only on a per packet basis.
80-84 86-89 91-94 96-101 107-112 115-121	RXTXDATA[31:0]	I/O	**Receive/Transmit Data** This is the bidirectional data bus for reads from the receive FIFO or writes to the transmit FIFO of the chip. Bus direction is controlled via RXINTEN and RXDEN for reads; TXINTEN and TXWREN are used for writes. Data is clocked with the RXRD_TXWR strobe input.

Pin Description (cont.)

Pin	Pin Name	I/O	Description
Transmit and Receive Exception Indicators			
48, 62 71, 79	TXRET_[1:4]	O	**Transmit Retry** These are active high tristate outputs. All four of these output pins are driven by tristate drivers enabled by an active low being driven onto the TXINTEN input pin. Once enabled, a high value on any of these inputs indicates that the associated port could not complete transmission of a packet due to one of the following conditions and that a retransmission of the packet is requested: 1. A late collision occurred during transmission. 2. Carrier sense never went high or dropped out during transmission. 3. During a transmission attempt a transmit FIFO underflow error occurred. 4. 16 attempts to transmit the packet all resulting in transmit collisions. Internally, the TXRET signal will remain high until it is cleared by the CLRTXERR pin, (See the text on clearing error conditions). As long as the internal TXRET signal for a port remains high, that port's transmit FIFO will remain cleared and no new transmissions can occur.
45, 58 65, 74	RXDC_[1:4]	O	**Receive Discard** These are active high tristate outputs. All four of these outputs pins are driven by tristate drivers enabled by a low value being driven onto the RXINTEN input pin. Once enabled, a high value on any of these inputs indicates that the associated port discarded reception of a packet due to one of the possible receive discard conditions. Internally, a port's RXDC signal will remain high until it is cleared by the CLRRXERR pin, (See the text on "Receive Discard Conditions"). As long as the internal RXDC signal for a port remains high, that port's receive FIFO will remain cleared and no new packets will be received.
Special Purpose Pins			
38	CLRTXERR	I	**Clear Transmit Error** This active high input is used to clear transmit retry flags within the chip. See the "Receive Discard Conditions" section for how this input is used.
50	CLRRXERR	I	**Clear Receive Error** This active high input is used to clear Receive Discard flags within the chip. See the "Receive Discard Conditions" section for how this input is used.
46, 59 67, 75	RXABORT_[1:4]	I	**Receive Abort** These inputs, when pulse high concedes the corresponding port to abort reception of a frame.
127,125 124,123	$\overline{\text{FDUPLX}}$_[1:4]	I	**Full Duplex Mode** These active low inputs are used to set the corresponding port into Full Duplex mode. In this mode, the corresponding transmitter will not defer to an active carrier sense signal.
152	ONETRYMODE	I	This input when tied high will cause any of the 84301 ports to drive it's corresponding TXRET to a HIGH state for a particular port if during transmission it encounters a collision contention. The controller will not automatically attempt to retransmit a packet/frame when this input pin is high. Transmit FIFO is flushed of data and the new packet/frame needs to be reloaded to the FIFO for transmission. ONETRYMODE has an internal pull-down.

Pin Description (cont.)

Pin	Pin Name	I/O	Description
Media Independent Interface			
138	TXC_1	I	**Transmit Clock Port 1** This is the transmit clock input for port #1. In standard 10 Mbit/sec Serial Mode, this is a 10 Mhz, 50% duty cycle transmit clock used to synchronize the transmit data from port #1 to the encoder. In this mode, transmit data appears serially on the TXD0_1 output and all transitions of transmit data and the TXEN_1 output occur from the falling edge of the clock. In MII mode, this is a 2.5/25 Mhz, 50% duty cycle clock, and the transmit data appears on the TXD0_1 through TXD3_1 outputs. In this mode transitions of transmit data and the TXEN_1 output occur from the rising edge of the clock.
161	TXC_2	I	**Transmit Clock Port 2** This is the transmit clock input for port #2. In standard 10 Mbit/sec Serial Mode, this is a 10 Mhz, 50% duty cycle transmit clock used to synchronize the transmit data from port #2 to the encoder. In this mode, transmit data appears serially on the TXD0_2 output and all transitions of transmit data and the TXEN_2 output occur from the falling edge of the clock. In MII mode, this is a 2.5/25 Mhz, 50% duty cycle clock, and the transmit data appears on the TXD0_2 through TXD3_2 outputs. In this mode transitions of transmit data and the TXEN_2 output occur from the rising edge of the clock.
177	TXC_3	I	**Transmit Clock Port 3** This is the transmit clock input for port #3. In standard 10 Mbit/sec Serial Mode, this is a 10 Mhz, 50% duty cycle transmit clock used to synchronize the transmit data from port #3 to the encoder. In this mode, transmit data appears serially on the TXD0_3 output and all transitions of transmit data and the TXEN_3 output occur from the falling edge of the clock. In MII mode, this is a 2.5/25 Mhz, 50% duty cycle clock, and the transmit data appears on the TXD0_3 through TXD3_3 outputs. In this mode transitions of transmit data and the TXEN_3 output occur from the rising edge of the clock.
197	TXC_4	I	**Transmit Clock Port 4** This is the transmit clock input for port #4. In standard 10 Mbit/sec Serial Mode, this is a 10 Mhz, 50% duty cycle transmit clock used to synchronize the transmit data from port #1 to the encoder. In this mode, transmit data appears serially on the TXD0_4 output and all transitions of transmit data and the TXEN_4 output occur from the falling edge of the clock. In MII mode, this is a 2.5/25 Mhz, 50% duty cycle clock, and the transmit data appears on the TXD0_4 through TXD3_4 outputs. In this mode transitions of transmit data and the TXEN_4 output occur from the rising edge of the clock.
139-142	TXD[3:0]_1	O	**Transmit Data Port 1** In standard 10 Mbit/sec Serial Mode, TXD0_1 is the serial transmit data output from port #1 to the encoder. In MII mode, these outputs drive a nibble of transmit data every leading edge of the TXC_1 clock from port #1 to the encoder.
162, 163 164, 166	TXD[3:0]_2	O	**Transmit Data Port 2** In standard 10 Mbit/sec Serial Mode, TXD0_2 is the serial transmit data output from port #2 to the encoder. In MII mode, these outputs drive a nibble of transmit data every leading edge of the TXC_2 clock from port #2 to the encoder.
180, 181 182, 185	TXD[3:0]_3	O	**Transmit Data Port 3** In standard 10 Mbit/sec Serial Mode, TXD0_3 is the serial transmit data output from port #3 to the encoder. In MII mode, these outputs drive a nibble of transmit data every leading edge of the TXC_3 clock from port #3 to the encoder.

Pin Description (cont.)

Pin	Pin Name	I/O	Description
198, 199 201, 202	TXD[3:0]_4	O	**Transmit Data Port 4** In standard 10 Mbit/sec Serial Mode, TXD0_4 is the serial transmit data output from port #4 to the encoder. In MII mode, these outputs drive a nibble of transmit data every leading edge of the TXC_4 clock from port #4 to the encoder.
143	TXEN_1	O	**Transmit Enable Port 1** This output from port #1 is used to activate the encoder. In standard 10 Mbit/sec Serial Mode, it becomes active when the first bit of the Preamble is transmitted and inactive when the last bit of the frame is transmitted. In MII mode, this output becomes active when the first nibble of the Preamble is transmitted and inactive when the last nibble of the frame is transmitted. This output is active high.
167	TXEN_2	O	**Transmit Enable Port 2** This output from port #2 is used to activate the encoder. In standard 10 Mbit/sec Serial Mode, it becomes active when the first bit of the Preamble is transmitted and inactive when the last bit of the frame is transmitted. In MII mode, this output becomes active when the first nibble of the Preamble is transmitted and inactive when the last nibble of the frame is transmitted. This output is active high.
186	TXEN_3	O	**Transmit Enable Port 3** This output from port #3 is used to activate the encoder. In standard 10 Mbit/sec Serial Mode, it becomes active when the first bit of the Preamble is transmitted and inactive when the last bit of the frame is transmitted. In MII mode, this output becomes active when the first nibble of the Preamble is transmitted and inactive when the last nibble of the frame is transmitted. This output is active high.
203	TXEN_4	O	**Transmit Enable Port 4** This output from port #4 is used to activate the encoder. In standard 10 Mbit/sec Serial Mode, it becomes active when the first bit of the Preamble is transmitted and inactive when the last bit of the frame is transmitted. In MII mode, this output becomes active when the first nibble of the Preamble is transmitted and inactive when the last nibble of the frame is transmitted. This output is active high.
128	RXC_1	I	**Receive Clock Port 1** In standard 10Mbit/sec Serial Mode, this input is a 10Mhz, 50% duty cycle nominal receive clock which is used to synchronize incoming data from the decoder to port #1. In 10Mbit/sec Serial Mode CSN and RXD0_1 are assumed to transition from the leading edge of this clock. In MII mode this clock is a 2.5/25 Mhz, 50% duty cycle receive clock that synchronizes incoming nibble wide data from the decoder to port #1. In MII mode data and the RXDV signal are assumed to transition from the falling edge of the clock.
146	RXC_2	I	**Receive Clock Port 2** In standard 10Mbit/sec Serial Mode, this input is a 10Mhz, 50% duty cycle nominal receive clock which is used to synchronize incoming data from the decoder to port #2. In 10Mbit/sec Serial Mode CSN and RXD0_2 are assumed to transition from the leading edge of this clock. In MII mode this clock is a 2.5/25 Mhz, 50% duty cycle receive clock that synchronizes incoming nibble wide data from the decoder to port #2. In MII mode data and the RXDV signal are assumed to transition from the falling edge of the clock.

Pin Description (cont.)

Pin	Pin Name	I/O	Description
169	RXC_3	I	**Receive Clock Port 3** In standard 10Mbit/sec Serial Mode, this input is a 10Mhz, 50% duty cycle nominal receive clock which is used to synchronize incoming data from the decoder to port #3. In 10Mbit/sec Serial Mode CSN and RXD0_3 are assumed to transition from the leading edge of this clock. In MII mode this clock is a 2.5/25 Mhz, 50% duty cycle receive clock that synchronizes incoming nibble wide data from the decoder to port #3. In MII mode data and the RXDV signal are assumed to transition from the falling edge of the clock.
188	RXC_4	I	**Receive Clock Port 4** In standard 10Mbit/sec Serial Mode, this input is a 10Mhz, 50% duty cycle nominal receive clock which is used to synchronize incoming data from the decoder to port #4. In 10Mbit/sec Serial Mode CSN and RXD0_4 are assumed to transition from the leading edge of this clock. In MII mode this clock is a 2.5/25 Mhz, 50% duty cycle receive clock that synchronizes incoming nibble wide data from the decoder to port #4. In MII mode data and the RXDV signal are assumed to transition from the falling edge of the clock.
131, 133 136, 137	RXD[3:0]_1	I	**Receive Data Port 1** In standard 10 Mbit/sec Serial Mode, RXD0_1 is the serial input data to port #1 from the decoder. In MII mode, these inputs are driven with a nibble of receive data every falling edge of the RXC_1 clock from the encoder to port #1.
149, 150 151, 160	RXD[3:0]_2	I	**Receive Data Port 2** In standard 10 Mbit/sec Serial Mode, RXD0_2 is the serial input data to port #2 from the decoder. In MII mode, these inputs are driven with a nibble of receive data every falling edge of the RXC_2 clock from the encoder to port #2.
172-175	RXD[3:0]_3	I	**Receive Data Port 3** In standard 10 Mbit/sec Serial Mode, RXD0_3 is the serial input data to port #3 from the decoder. In MII mode, these inputs are driven with a nibble of receive data every falling edge of the RXC_3 clock from the encoder to port #3.
192 194-196	RXD[3:0]_4	I	**Receive Data Port 4** In standard 10 Mbit/sec Serial Mode, RXD0_4 is the serial input data to port #4 from the decoder. In MII mode, these inputs are driven with a nibble of receive data every falling edge of the RXC_4 clock from the encoder to port #4.
130	CSN_1	I	**Carrier Sense Port 1** This is port #1's carrier sense input which indicates there is traffic on the transmission medium connected to port #1. Carrier sense becomes active with the first bit of the Preamble received, and inactive one bit time after the last bit of the frame is received. This is an active high input.
129	RX_DV_1	I	**Receive Data Valid Port 1** In MII mode this input is receive data valid. Receive data valid becomes active with the first nibble of synchronized and decoded Preamble or SFD appearing on the RXD[3:0]_1 lines and goes inactive one clock time after the last nibble of the frame is received. This is an active high input.
148	CSN_2	I	**Carrier Sense Port 2** This is port #2's carrier sense input which indicates there is traffic on the transmission medium connected to port #2. Carrier sense becomes active with the first bit of the Preamble received, and inactive one bit time after the last bit of the frame is received. This is an active high input.

Pin Description (cont.)

Pin	Pin Name	I/O	Description
147	RX_DV_2	I	**Receive Data Valid Port 2** In MII mode this input is receive data valid. Receive data valid becomes active with the first nibble of synchronized and decoded Preamble or SFD appearing on the RXD[3:0]_2 lines and goes inactive one clock time after the last nibble of the frame is received. This is an active high input.
171	CSN_3	I	**Carrier Sense Port 3** This is port #3's carrier sense input which indicates there is traffic on the transmission medium connected to port #3. Carrier sense becomes active with the first bit of the Preamble received, and inactive one bit time after the last bit of the frame is received. This is an active high input.
170	RX_DV_3	I	**Receive Data Valid Port 3** In MII mode this input is receive data valid. Receive data valid becomes active with the first nibble of synchronized and decoded Preamble or SFD appearing on the RXD[3:0]_3 lines and goes inactive one clock time after the last nibble of the frame is received. This is an active high input.
191	CSN_4	I	**Carrier Sense Port 4** This is port #4's carrier sense input which indicates there is traffic on the transmission medium connected to port #4. Carrier sense becomes active with the first bit of the Preamble received, and inactive one bit time after the last bit of the frame is received. This is an active high input.
190	RX_DV_4	I	**Receive Data Valid Port 4** In MII mode this input is receive data valid. Receive data valid becomes active with the first nibble of synchronized and decoded Preamble or SFD appearing on the RXD[3:0]_4 lines and goes inactive one clock time after the last nibble of the frame is received. This is an active high input.
145	COLL_1	I	**Collision Port 1** This input indicates that a transmission contention has occurred on the transmission medium connected to port #1. The collision input is latched internally. Sampled during transmission, Collision is set by an active high pulse on the COLL input and automatically reset at the end of transmission of the JAM sequence.
168	COLL_2	I	**Collision Port 2** This input indicates that a transmission contention has occurred on the transmission medium connected to port #2. The collision input is latched internally. Sampled during transmission, Collision is set by an active high pulse on the COLL input and automatically reset at the end of transmission of the JAM sequence.
187	COLL_3	I	**Collision Port 3** This input indicates that a transmission contention has occurred on the transmission medium connected to port #3. The collision input is latched internally. Sampled during transmission, Collision is set by an active high pulse on the COLL input and automatically reset at the end of transmission of the JAM sequence.
204	COLL_4	I	**Collision Port 4** This input indicates that a transmission contention has occurred on the transmission medium connected to port #4. The collision input is latched internally. Sampled during transmission, Collision is set by an active high pulse on the COLL input and automatically reset at the end of transmission of the JAM sequence.

Pin Description (cont.)

Pin	Pin Name	I/O	Description
205	DAISY_OUT	O	**Test Mode** This output is used for parametric test of the I/O's only. **It should not be externally connected.**
2, 14, 28, 33, 52, 53, 70, 78, 102, 104, 114, 126, 132, 135, 154, 157, 158, 178, 183, 189, 193	V_{DD}	—	Power Supply 5V +/– 5%
1, 3, 13 19, 27, 34, 43, 51, 54, 55, 60, 66, 69, 76, 85, 90, 95, 103, 105, 106, 113, 122, 134, 144, 155, 156, 159, 165, 176, 179, 184, 200, 207, 208	GND	—	Ground 0 Volts

Note: All inputs must never be left floating even if they are not in use. For example the RX_DV pins must be driven either HIGH or LOW even if the corresponding channel is not in MII mode. Exceptions to this rule are the pins onetrymode (152), A4 (206) and A3 (153) which have internal pull downs.

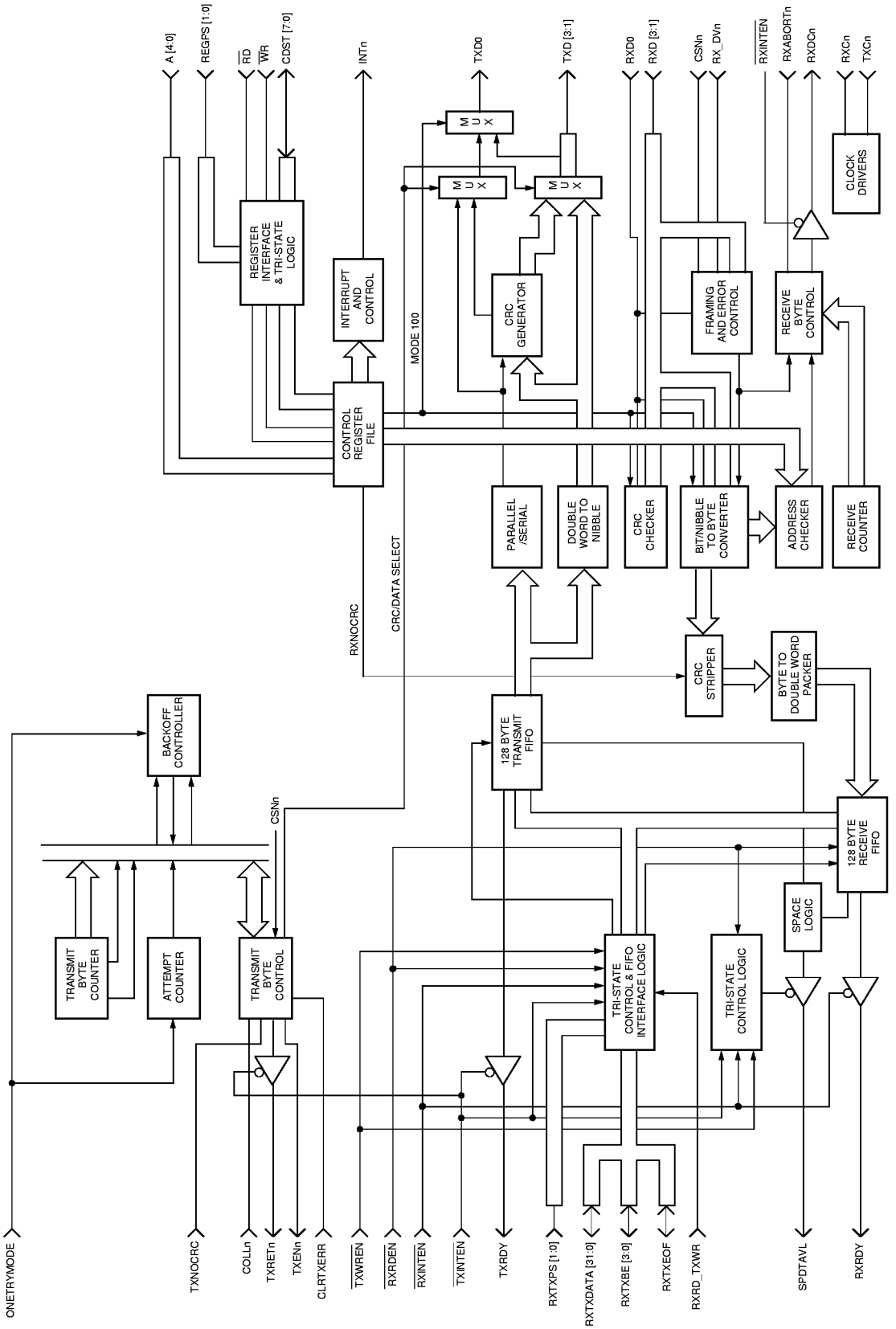


Figure 1. Individual Functional Block Diagram

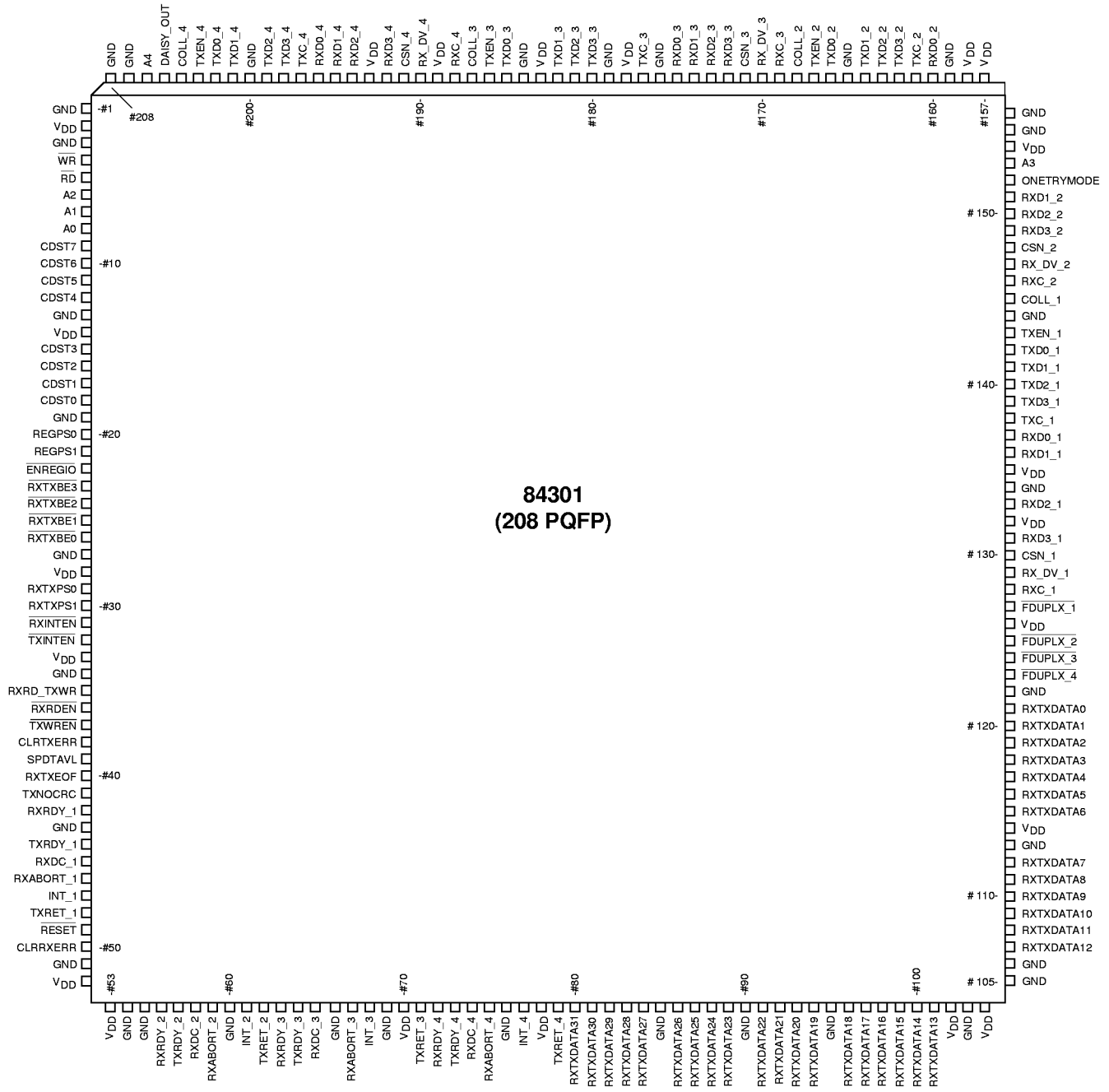


Figure 2. 84301 Pin Configuration

2.0 Introduction

The 84301 is a 4-Port Ethernet Media Access Controller (MAC) with a rich set of operating modes and features. It is manufactured as a single-chip VLSI device to simplify and enhance the development of multi-port Ethernet embedded systems such as bridges, switches, and routers.

Two input/output paths are provided for interfacing to physical layer devices. In IEEE-standard MII mode, the 84301 provides an industry standard interface supporting both 10Mbit/sec and 100Mbit/sec data rates. This interface will directly connect with physical layer devices such as SEEQ's 80C240 100Base-T4 PHY without additional glue logic. In Serial mode, the chip supports the standard Ethernet CSMA/CD protocol via a serial interface for transmit and receive data. All ports, in all interface modes, support both Half and Full Duplex operation.

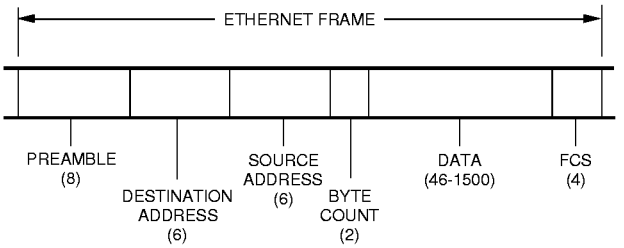
Each port of the 84301 is feature compatible with SEEQ's 80C300 Ethernet Media Access Controller. These features include: 64 bit Multicast filter, Transmit no CRC, Transmit no Preamble, Transmit Packet Autopadding, Receive CRC, Receive Own Transmit Disable, Receive Group Address Mode, Fast Receive Discard Mode, and Full Duplex Mode. Additionally, each port supports: programmable defer time between transmit packets, appending value of FCS on a packet-by-packet basis, and pin-controllable per-port receive packet abort.

A high-bandwidth universal system interface is provided which is compatible with many microprocessor or system busses, easing the integration of the 84301 into many system architectures. Its 32-bit data path width is provided to provide the bandwidth necessary to maintain full duplex wire speed communications simultaneously through all four ports. Each port is provided with dual 128 byte FIFOs to ease bus multiplexing and interfacing to different clock domains.

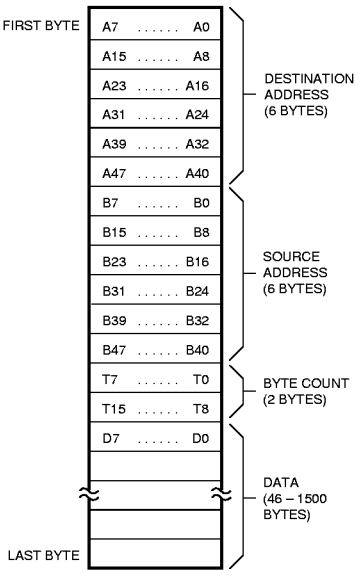
3.0 Functional Description

On an Ethernet communication network, information is transmitted and received in packets or frames. An Ethernet frame consists of a preamble, two address fields, a byte-count field, a data field and a frame check sequence (FCS). Each field has a specific format which is described in detail below. An Ethernet frame has a minimum length of 64 bytes and a maximum length of 1518 bytes exclusive of the preamble. The Ethernet frame format is shown in the figure below.

3.1 FRAME FORMAT



NOTE:
Field length bytes, in parentheses.



Typical Frame Buffer Format for Byte-Organized Memory

Preamble: *The preamble is a 64-bit field consisting of 62 alternating "1"s and "0"s followed by a "11" End-of-Preamble indicator.*

Destination Address: *The Destination Address is a 6-byte field containing either a specific Station Address, a Broadcast Address, or a Multicast Address to which this frame is directed.*

Source Address: *The Source Address is a 6-byte field containing the specific Station Address from which this frame originated.*

Byte-Count Field: *The Byte-Count Field consists of two bytes providing the number of valid data bytes in the Data Field, 46 to 1500. This field is uninterpreted at the Data Link Layer, and is passed through the EDLC chip to be handled at the Client Layer.*

Data Field: *The Data Field consists of 46 to 1500 bytes of information which are fully transparent in the sense that any arbitrary sequence of bytes may occur.*

Frame Check Sequence: *The Frame Check Sequence (FCS) field is a 32-bit cyclic redundancy check (CRC) value computed as a function of the Destination Address Field, Source Address Field, Type Field and Data Field. The FCS is appended to each transmitted frame, and used at reception to determine if the received frame is valid.*

3.2 PACKET TRANSMISSION PER PORT

The transmit data stream consists of the Preamble, four information fields, and the FCS which is computed in real time by the port and automatically appended to the frame at the end of the data. The Preamble is also generated by the port and transmitted immediately prior to the Destination Address. Destination Address, Source Address, Type Field and Data Field are prepared in the buffer memory prior to initiating transmission. The port encapsulates these fields into an Ethernet frame by inserting a preamble prior to these information fields and appending a CRC after the information fields. A port can be programmed to exclude inclusion of the preamble and/or the FCS from the transmit data stream. In this case, it is assumed that the preamble and FCS are provided as part of the data written to the port.

3.2.1 Controlling Transmit Packet Encapsulation

As was mentioned in the previous paragraph, a port can be programmed for exclusion of the FCS and/or the preamble when transmitting a packet. To program a port for transmitting a packet without creating a preamble, bit #2 of the port's Configuration Register #1 can be written high. Once this bit is set, all packets transmitted by the port will not include a preamble pattern unless it is part of the data written to the port's transmit FIFO by the system. Similarly, a port can be prevented from appending an FCS value to a packet by setting bit #4 HIGH in the Configuration Register #1. As long as this bit is high, any packet transmitted by the port will not include an FCS value unless it is written as part of the transmit data written to the port's transmit FIFO. Appending of a FCS value can be controlled on a packet per packet basis by using the TXNOCRC pin as long as the TXNOCRC Tx-Rx Configuration register bit has not been set high. If the TXNOCRC pin is held high (or) if the TXNOCRC bit is set anytime during the duration of a packet write to the transmit FIFO, that particular packet will not be appended with a CRC value.

Transmit No CRC		CRC Appendage
H/W Pin 41	S/W Bit 4 of Config 1	To the Packet
0	0	Yes
0	1	No
1	0	No
1	1	No

Please note that both the H/W pin and the software bit should be kept deasserted during the entire duration of the packet write to the transmit FIFO in order to transmit a packet with CRC.

3.2.2 Transmission Initiation in Full Duplex and CSMA/CD Networks

Packet transmission begins when data in the transmit FIFO meets or exceeds a user-defined threshold value.

The transmit threshold value is controlled by programming bits 7 through 4 of the Transmit Control/Product ID register. The default value is 0 (zero), which enables the MAC to begin packet transmission with as little as one double word in the FIFO. The threshold, measured in double words, is equal to the number programmed into Transmit Control Register times 2. Thus, if the register contains the value 3H, transmission is deferred until there are at least 6 double words of data in the FIFO.

Packet transmission initiation is also dependent upon whether the 84301 is in Full Duplex or CSMA/CD mode. If the Chip is in CSMA/CD mode, transmission may also be prevented or delayed due to activity on the shared network medium. If the network is not busy due to other data traffic, transmission will begin after the appropriate defer time (from end of previous traffic) has expired. Otherwise,

transmission is delayed until after current data transfers are complete, and the defer time requirements have been satisfied. Following the IEEE 802.3 specifications, the minimum defer time is split into two periods. The beginning of the defer time occurs upon the transmitter sensing carrier sense going LOW. Once this case occurs then if carrier sense is reasserted during the 1st period of the defer time, the transmitter will reset its defer time counter and restart the total defer timeout period from 0. If carrier sense is reasserted during the 2nd period of the total defer time interval, the transmitter will ignore carrier sense and start transmission as soon as the defer time is met. The 1st period of the total defer time is programmable through use of the transmit defer register. The second period of the defer time interval is either 3.2 µs or 0.32 µs depending on whether the chip is in 10Mbit/sec or 100Mbit/sec mode. The total default defer time for 10Mbit/sec serial mode is 9.6 µs as measured from TXEN going LOW to TXEN going High assuming the transmit defer register is at 00 hex and assuming that the TXEN going LOW to CSN going LOW delay of the physical device is less than 5 TXC clock periods. When the chip is in Full Duplex mode, transmission of data onto the network occurs independent of whether carrier sense indicates a busy network condition or not.

Because of the variability in delays given for TXEN going LOW to CSN going LOW for different 100Mbit/sec physical devices, the default defer time in 100 Mbit/sec MII mode has been set assuming full duplex conditions where carrier sense is not monitored by the transmitter. In this case the default is 0.96 µs from TXEN going LOW to TXEN going HIGH. To adjust the defer time to some other value, the programmable defer register can be set using the formulas given in the section describing the defer register. When transmission begins, the chip activates the transmit enable (TXEN) line concurrently with the transmission of the first bit, or first nibble in the MII case, of the Preamble and keeps it active for the duration of the transmission.

3.2.3 Collision on Transmit

On the occurrence of a transmit collision condition that does not represent the 16th transmission attempt for the packet or does not occur after 64 byte times into the transmission, the controller will automatically attempt to retransmit the packet. First, the controller will halt the transmission of data from the FIFO and begin transmitting a Jam pattern consisting of 55555555 hex. The controller will also reset the Transmit FIFO read address pointer back to the beginning of the transmit packet within the FIFO. At the end of transmitting the Jam pattern the controller will then begin the Backoff wait period. Once the backoff period is finished the controller will automatically retransmit the packet. If a packet reaches 16 retransmission attempts without success due to collisions, or if a collision occurs later than 64 Byte times after the beginning of a transmission, this is considered to represent a serious network error. Upon any one of these two error conditions occurring, the selected port's Transmit FIFO will be cleared and the corresponding TXRET output will be driven HIGH. If the TXRET signal was driven HIGH due to 16 transmission attempts, Bit '2' of the transmit status register gets set indicating the occurrence of 16 collisions. When either of the two above error conditions occurs, retransmission of any packets that were in the transmit FIFO requires first clearing the TXRET error condition and then reloading the packet or packets in the Transmit FIFO.

Scheduling of retransmission is determined by a controlled randomization process called Truncated Binary Exponential Backoff. The chip waits a random interval between 0 and 2^K slot times (51.2 µs per slot time for 10 Mbit Ethernet or 5.12 µs per slot time for 100 Mbit Ethernet) before attempting retransmission, where "K" is the current transmission attempt number (not to exceed 10).

3.2.4 Transmit Termination Conditions

A port will terminate transmission under the following conditions.

***Normal:** The frame has been transmitted success fully without contention. Loading of the last data byte into a port's Transmit FIFO is signaled to the port by activation of its RxTxEOF signal concurrently with the last double word of data loaded into the Transmit FIFO. This line acts as a thirty-third bit in the Transmit FIFO. When the last valid byte of the last double word has been transmitted, if the port is not in Transmit No CRC mode, then the CRC is appended and transmitted concluding frame transmission. The Transmission Successful bit of the Transmit Status Register will be set by a normal termination.*

***Collision:** Transmission attempted by two or more Ethernet nodes. The Jam sequence is transmitted, the Collision status bit is set, transmit Collision Counter is updated, the Backoff interval begun, and the Transmit FIFO address is set to point to the beginning of the packet for retransmission.*

***Underflow:** Transmit data is not ready when needed for transmission. Once transmission has begun, a port on average requires one transmit double word every 3200 ns for 10 Mbit Ethernet or 320 ns for 100 Mbit Ethernet in order to avoid Transmit FIFO under flow (starvation). If this condition occurs, the port terminates the transmission, issues a TXRET signal, and sets the Transmit-Underflow status bit.*

***16 Transmission Attempts:** If a Collision occurs for the sixteenth consecutive time, the 16-Transmission-Attempts status bit is set, the Collision status bit is set, the TXRET signal is generated, and the Backoff*

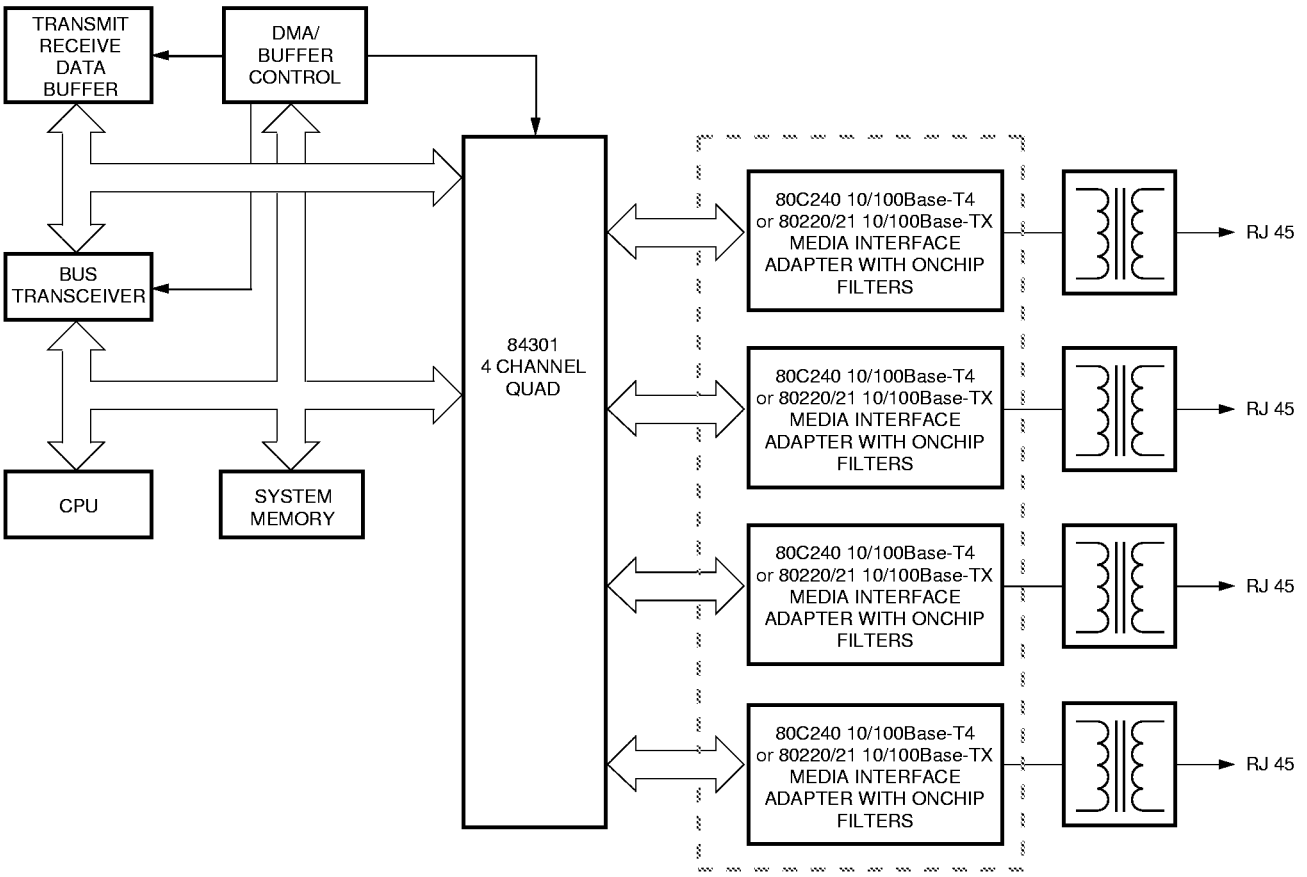


Figure 3. Typical Application Example

interval begun. The counter that keeps track of the number of collisions is modulo 16 and therefore rolls over on the 17th collision. Bits 15 to 11 of a port's transmit collision counter allow a user to determine how many transmission attempts were necessary to successfully transmit the packet.

***Late Collision:** If a Collision occurs greater than 64 byte times after the transmission begins this is considered a late collision error. Upon this condition the transmission is terminated, the TXRET output is driven HIGH, and the late collision status bit is set.*

At the completion of every transmission or retransmission, new status information is loaded into the Transmit Status Register. Dependent upon the bits enabled in the Transmit Command Register, an interrupt will be generated for the just completed transmission.

3.2.5 Conditions That Will Cause a Port's TXRET Pin to go High

Detection of a HIGH value on one of the chips 4 TXRET pins indicates that the associated port could not complete transmission of a packet due to one or more of the following conditions:

1. *A transmit FIFO underflow occurred while transmitting the packet.*
2. *A late collision occurred while transmitting the packet.*
3. *Carrier sense never went active during transmission or went from an active to inactive state during transmission.*
4. *16 attempts to transmit the packet all resulted in transmit collisions.*
5. *The ONETRYMODE pin is HIGH and a collision occurs.*

Any of the above conditions will cause the port to flush the transmit FIFO and initiate a transmit retry request. With initiation of a transmit Retry Request the port's TXRDY output will go low and stay low until the TXRET flag is cleared. Similar to a port's receive discard signal, a transmit retry signal going to the external TXRET pin is latched upon a transmit retry condition and held high until

cleared. Until a port's transmit retry signal is cleared, no new transmit packets can be written to the transmit FIFO.

3.2.6 Detecting and Clearing a Transmit Retry Condition

To enable the output drivers for the four TXRET pins, the the TXINTEN input is driven low. Once a Tx retry condition is detected, that port's internal Tx retry signal can be cleared by first setting the RXTXPS[1:0] inputs to point to that port. Then by driving the TXINTEN input low and then pulsing the CLRTXERR input high for a minimum of one RXRD_TXWR clock cycle, this will clear that port's TXRET signal. The RXTXPS [1:0] and TXINTEN inputs must not change during the high time of the CLRTXERR input.

3.3 PACKET RECEPTION PER PORT

Each port within the chip continuously monitors the network. When activity is recognized via the Carrier Sense (CSN) signal in 10 Mbit/sec Serial Mode, or through the Receive Data Valid (RX_DV) signal in MII mode, the port will then synchronize itself to the incoming data stream through recognition of the Start Frame Delimiter (SFD) at the end of Preamble. The destination address field of the frame is then examined. Depending on the Address Match Mode specified, the port will either recognize the frame as being addressed to itself in a general or specific fashion or abort the frame reception. The port can also be programmed to count all collisions on the network it's connected to.

3.3.1 Preamble Processing

A port recognizes activity on the Ethernet via its Carrier Sense line in 10 Mbit/sec Serial Mode or through its Receive Data Valid line in MII mode. In 10 MBit/sec Serial Mode the end of preamble is detected by a double 1 serial receive data pattern preceded by 6 bits of alternating 1's and 0's. In MII mode the end of preamble is recognized by the following nibble pattern:

	Logic Values
RXD3	0 1
RXD2	1 1
RXD1	0 0
RXD0	1 1

In 10 MBit/sec Serial Mode, detection of a double 0 pattern 16 bit times after CSN goes high and before a proper Start Frame Delimiter pattern is received will prevent reception of the packet by the receiver. In MII mode, when RX_DV goes high the RXD[3:0] lines must be driven with at least 1 byte of proper SFD pattern.

3.3.2 Address Matching

Ethernet addresses consist of two 6-byte fields. The first bit of the address signifies whether it is a Station Address or a Multicast/Broadcast Address.

First Bit	Address
0	Station Address (Physical)
1	Multicast/Broadcast Address (logical)

Address matching occurs as follows:

Station Address: *All destination address bytes must match the corresponding bytes found in the Station Address Register. If Group Address mode is enabled, the last 4 bits of the station address are masked out during address matching.*

After computing the FCS on the first six bytes of the address field (Destination address), a port uses bits 0 thru 5 as an address to its Multi-cast address filter register. Bit 0 of the FCS is assumed to be where receive data enters the FCS generation circuitry. If the corresponding bit addressed in the Multicast address filter register is a '1' the port will receive the frame, otherwise it will discard the frame. Addressing of the Multicast address filter register occurs using bits 0 thru 2 to determine which byte is selected and bits 3 thru 5 to determine which bit according to the following tables:

FCS Bits 0 1 2	Byte Selected	FCS Bits 3 4 5	Bit Selected
0 0 0	Byte 0	0 0 0	Bit 0
0 0 1	Byte 1	0 0 1	Bit 1
0 1 0	Byte 2	0 1 0	Bit 2
0 1 1	Byte 3	0 1 1	Bit 3
1 0 0	Byte 4	1 0 0	Bit 4
1 0 1	Byte 5	1 0 1	Bit 5
1 1 0	Byte 6	1 1 0	Bit 6
1 1 1	Byte 7	1 1 1	Bit 7

Multicast Address: *If the first bit of the incoming address is a 1 and the port is programmed to accept Multicast Addresses without using Hash filtering, the frame is received. A port also can be programmed to use the hash filter for determining acceptance of multicast addresses.*

Broadcast Address: *The six incoming destination address bytes must all be FF hex. If a port is programmed to accept Broadcast or Multicast Addresses the frame will be received.*

If the incoming frame is addressed to a port in the chip specifically (Destination Address matches the contents of the Station Address Register), or is of general or group interest (Broadcast or Multicast Address), the port will pass the frame exclusive of Preamble and FCS to the CPU buffer and indicate any error conditions at the end of the frame. If, however, the address does not match, as soon as the mismatch is recognized, the port will terminate reception and issue an RxDC.

A port may be programmed via the Match Mode bits of the Receive Command Register to ignore all frames (Disable Receiver), accept all frames (Promiscuous mode), accept frames with the proper Station Address or the Broadcast Address (Station/Broadcast), or accept all frames with the proper Station Address, the Broadcast Address, or all Multicast Addresses (Station/Broadcast/Multicast).

3.3.3 Terminating Reception

Reception is terminated when either of the following conditions occur:

Carrier Sense or Receive Data Valid Inactive: *Indicates that traffic is no longer present on the Ethernet cable.*

Overflow: *The host node for some reason is not able to empty a port Receive FIFO as rapidly as it is filled, and an error occurs as frame data is lost. On average a port's Receive FIFO must be serviced every 3200 ns for 10 Mbit Ethernet or 320 ns for 100 Mbit Ethernet to avoid this condition.*

3.3.4 Using the RXABORT Pins to Terminate Reception of a Packet

By pulsing the corresponding RXABORT pin high for a minimum of 1 RXC cycle any time during the reception of a packet, that particular port's packet reception can be terminated. When reception of a packet is terminated this way, the Receive FIFO will be cleared and will stay cleared until carrier sense in 10 MBit Serial Mode or Receive Data Valid in MII mode, transitions from high to low or from low to high indicating either the end of the packet being aborted or the beginning of a new receive packet. It is important to note that RXABORT will cause the RXDC pin to go high based on the conditions described under "Conditions that cause the RXDC pin to go high".

The RXDC signal is asserted so that an external processor will always have an indication of a packet abortion irrespective of whether it's aborted by the user or by an external PHY. However, the assertion of the RXDC signal can be avoided by setting bit 4 of configuration register #2. This will enable the reception of any packet irrespective of errors and also reduce the number of signals (RXDC1_4 and CLRRXERR) that need to be processed when the corresponding RXABORT goes high.

3.3.5 Receive Discard Conditions

Receive packets can be discarded for not meeting the minimum IEEE 802.3 requirements for a good packet, for address mismatches when the chip is not in promiscuous mode, and by either user intervention or symbol errors occurring from a 100 Mbit/sec physical device. in the case of discards due to oversized packets, address mismatches, or the assertion of the RXABORT pin during packet reception, further writing of receive packet data to the receive FIFO is halted once the mismatch, receive abort or oversized packet condition is determined.

Except for discards due to address mismatches, all packet discards occur after carrier sense, or Receive Data Valid in MII mode, deasserts. The discarding of receive packets for error conditions can be controlled through bits 0 through 3 of the receive command register, and through bit 4 of configuration register #2. Listed below are the required conditions for a receive discard to be produced:

1. *Bit 0 of the Rx command register is LOW and a receive FIFO overflow occurred during reception.*
2. *Bit 1 of the Rx command register is LOW and a packet with a CRC error was received.*
3. *Bit 4 of Configuration register 2 is LOW and the RXABORT pin is driven high while CSN is high.*
4. *Bit 3 of the Rx command register is LOW and a packet with less than 64 bytes of data was received.*
5. *Bit 4 of the Rx command register is LOW and a packet of size greater than 1518 was received.*
6. *The Receiver is not in promiscuous mode and a address mismatch occurs.*

Discarding of a receive packet by a port will cause any packet data that was written to that receive FIFO to be flushed from the FIFO. If no completely received packets are in the receive FIFO at the time a receive discard occurs, the receive FIFO will be completely flushed of data. If however, a completely received packet, as indicated by the packets status double word having been written to the FIFO, is in the receive FIFO at the time of a

receive discard, the FIFO will be flushed only up to the last completely received packet. To prevent a receive packet from being discarded due to an error condition, you can selectively enable the reception of errored packets as described in the section describing bit settings on configuration register #2.

Conditions that Cause the RXDC Pin to go HIGH

As packets are discarded due to the receive packet error conditions given in section "3.3.5 Receive Discard Conditions", the corresponding port's RXDC pin may or may not assert. If a receive packet's status has been written to the receive FIFO and the packet's status has not yet been read from the FIFO, discards caused by following packets with errors are handled within the chip and the RXDC pin will not go HIGH. If all status double words for all packets written to the FIFO have been read out then the RXDC pin will go HIGH under the following condition:

1. *Enough of a receive packet has been written to the FIFO to cause RXRDY to go HIGH before the packet is discarded due to an error condition.*

2. *If there are no status double words in the receive FIFO and if RXRDY goes HIGH just before a discard condition occurs, RXRDY may go LOW again before any FIFO reads have occurred. This is due to the receive discard clearing the FIFO of any receive bytes already written to the FIFO. In this case, RXRDY is guaranteed to remain HIGH for at least one RXRD_TXWR clock cycle.*

Detecting and Clearing a Receive Discard Condition

To enable the output driver for the RXDC pins, the RXINTEN input must be driven low. Once a discard condition is detected, the receive discard can be cleared by driving the RXINTEN input low and then pulsing the CLRRXERR input high for a minimum of one RXRD_TXWR clock cycle. The RXINTEN input must not change state for the duration of the time that the CLRRXERR input is high.

Clearing Interrupts

Within one port, both receive and transmit interrupts are combined into a single interrupt signal which then goes to the INT output pin. The interrupt signal in the chip is actually the result of the receive/transmit status register outputs and the receive/transmit command register interrupt enable bits that are set. To clear an interrupt, the status that caused the interrupt needs to be cleared. This can be accomplished by reading the transmit status register and/or the receive status register.

3.4 SYSTEM INTERFACE

The chip system interface consists of one receive/transmit 32-bit bidirectional data bus, one 8-bit bidirectional command/status data bus, and each busses respective control signals. Receive FIFO data is read and Transmit FIFO data is written over the RXTXDATA[31:0] bus, and Command/Status data is written or read over the bidirectional CDST[7:0] data bus.

3.5 FIFO INTERFACE

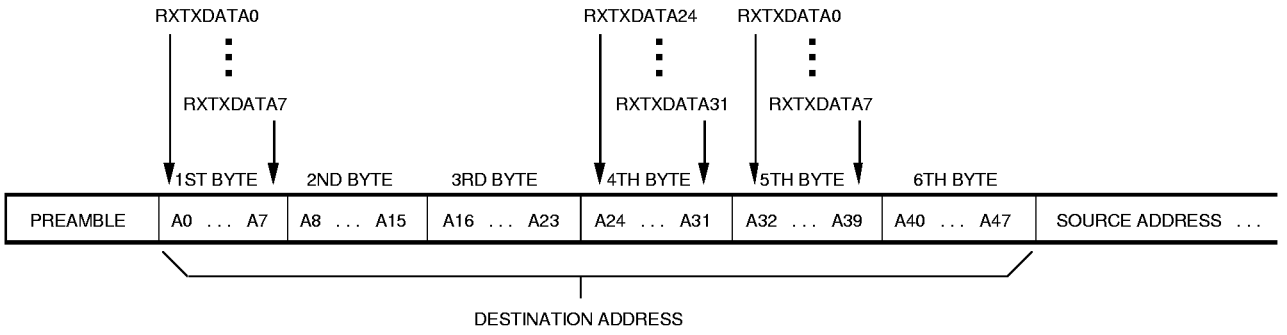
3.5.1 Little Endian and Big Endian Format

The FIFO interface control includes the BUSMODE bit 7 in configuration register #2, which sets the 84301 FIFO interface to Big Endian or Little Endian byte transmit/ receive data order. In Big Endian mode, data written to the transmit FIFO is transmitted most significant byte of the RXTXDATA bus first and least significant byte of the RXTXDATA bus last. In Little Endian mode, the least significant byte of each double word is transmitted first and the most significant byte of each double word is transmitted last. On the receive side, if Big Endian mode is in effect then the first data bytes received are assumed to be the most significant bytes of the double word and appear on the most significant portion of the RXTXDATA bus for receive FIFO reads. The receiver reverses this order if the chip is in Little Endian mode. The value of the BUSMODE bit has no effect on the operation of the 84301 register interface. It is important to note that the operation of the byte enables remain the same for both modes.

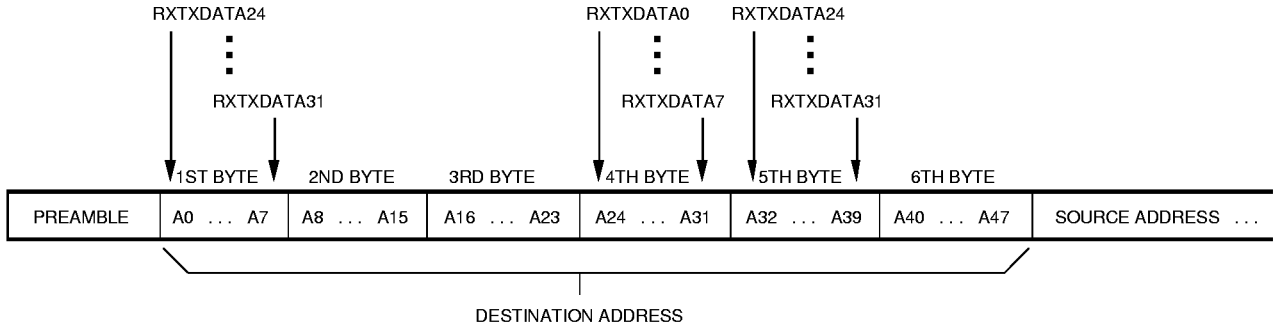
3.5.2 Transmit FIFO Interface

To determine if the transmit FIFO for any of the chips ports has reached its threshold number of double words of space available, all four TXRDY outputs can be enabled by driving the TXINTEN input low. The TXRDY output for a port will be high if there is enough space available in the port's transmit FIFO to meet or exceed the programmed threshold value.

Once one of the TXRDY outputs is determined to be high, that port's Transmit FIFO can be written. To write to a port's Transmit FIFO, the TXWREN and TXINTEN inputs must be asserted low and at least one of the RXTXBE byte enables must be low for each write cycle. The value of the RXTXPS inputs determines which port is being written. All of the above inputs are clocked into the chip on the high going edge of the RXRD_TXWR clock input which also acts as the FIFO write strobe. Because of this pipe lining the actual FIFO write will occur one RXRD_TXWR cycle after the assertion of the Transmit FIFO interface control



Bit Serialization/Deserialization for Little Endian Format



Bit Serialization/Deserialization for Big Endian Format

signals. Valid combinations of the $\overline{RXTXBE}$ inputs for transmit FIFO writes are given below:

$\overline{RXTXBE3}$	$\overline{RXTXBE2}$	$\overline{RXTXBE1}$	$\overline{RXTXBE0}$
0	0	0	0
1	0	0	0
0	0	0	1
1	1	0	0
1	0	0	1
0	0	1	1
1	1	1	0
1	1	0	1
1	0	1	1
0	1	1	1

The TXRDY output for the port being read will remain high until the port's transmit FIFO no longer has enough double word space to meet the programmed threshold value.

The transmit and the receive FIFO are 128 bytes deep organized as double word (32 bits) rows. During writes to the transmit FIFO, the FIFO pointer gets incremented on every write to the FIFO, irrespective of whether all the four byte enables are asserted or not. Hence, during non double word writes to the FIFO, one entire row of the FIFO gets filled irrespective of whether all the bytes are valid or not. The 84301 automatically ignores the invalid bytes when the data gets transmitted from the FIFO.

While transmit FIFO writes are occurring the SPDTAVL output will remain high until the highgoing edge of the write to the second to the last remaining double word space in the FIFO. Because transmit FIFO writes are pipelined, there will always be one more internal FIFO write after $\overline{TXWREN}$ is deasserted.

Effect of Auto Retransmission Upon TXRDY Behavior

As a packet is read out of a port's Transmit FIFO by the transmitter for transmission onto the network, the corresponding TXRDY signal will not reflect any reads that have occurred to the FIFO until enough bytes of data have been transmitted to get past the normal collision window of less than 64 byte times. This means that if a port's TXRDY goes low during the writing of a packet to the Transmit FIFO, it will not go HIGH again until both of the following conditions are true:

1. The packet has been completely transmitted or to a point 64 byte times from the beginning of the transmission has been reached.
2. The number of bytes taken out of the transmit FIFO for transmission subtracted from the number of bytes written to the FIFO leaves the FIFO with enough double word space avail able to meet the threshold setting.

It is important to note that until the packet is completely transmitted or until enough of the packet is transmitted to get past the normal collision window, the TXRDY output will only reflect how many writes have occurred and will not reflect how much of the FIFO data has been read out for transmission. Because of this, it is important to insure enough packet data has been written to prevent FIFO underflows if there exists a large latency between the TXRDY output being determined HIGH and the writing of more data to the FIFO.

3.5.3 Receive FIFO Interface

To determine if the receive FIFO has reached its threshold number of double words of data, the RXRDY output can be enabled by driving the $\overline{RXINTEN}$ input low. The RXRDY output for the chip will be high under one of the following conditions:

1. There are enough double words of data in the channel's receive FIFO to meet or exceed the programmed threshold value.
2. The status double word for a receive packet with an end of frame value of HIGH is in the receive FIFO.

Once the RXRDY output is determined to be high, the receive FIFO can be read. To read from the Receive FIFO, the $\overline{RXRDEN}$ and $\overline{RXINTEN}$ inputs must be asserted low and the $\overline{RXTXBE}$ byte enables must be low for each read cycle. Similar to the Transmit FIFO interface, all of the above Receive FIFO interface control signals are clocked into the chip on the high going edge of the RXRD_TXWR clock input which also acts as the FIFO read strobe. Because of this pipe lining the actual FIFO read will occur one RXRD_TXWR cycle after the assertion of the Receive FIFO interface control signals.

Depending on the way RXRDEN is used, two different modes are possible, when the chip is used in the non-bidirectional byte enable mode.

On burst reads (RXRDEN being asserted for multiple clock cycles), if the first read is not a double word read, the second read will always increment the FIFO pointer irrespective of whether all the byte enables are enabled or not. In this mode, 16 bit reads are possible by muxing the LSB and the MSB of the data bus. 8 bit reads are not possible.

On single reads (RXRDEN being asserted for only one clock cycle), the FIFO pointer will get incremented only on a double word read. In this mode, the different bytes of the data bus can be muxed to perform multiple 8 bit or 16 bit reads. But, all the reads of the bytes belonging to one row should be terminated with a double word read to increment the FIFO pointer.

When the chip is used in the bidirectional byte enable mode, all reads will have all four byte enable bits asserted except for the last data double word which could have all or partial byte enable bits asserted depending on the received data byte count.

When the chip is being read, the RXRDY output will remain high until the high going edge of the read that results in one of the following conditions:

1. *The FIFO no longer has enough data to meet the threshold setting.*
2. *A packet's status double word with its associated HIGH end of frame value is read out.*

In the case of RXRDY being driven LOW upon condition two given above, it will remain LOW for 8 RXRD_TXWR clock cycles and then goes back HIGH if one of the conditions for RXRDY being HIGH is met.

During reads from the FIFO, the SPDTAVL output will remain high until the high going edge of the RXRD_TXWR of the read that causes one of the following conditions to occur:

1. *The read that empties the FIFO completely.*
2. *The read that reads a packets status double word from the FIFO.*

When one of the above conditions is met and SPDTAVL is driven low upon the high going edge of the RXRD_TXWR, the SPDTAVL output will remain low for a period of 8 RXRD_TXWR clock cycles. For the time that SPDTAVL remains low, further reads are blocked within the chip even if external reads continue. This allows overreading the receive FIFO by a few cycles without, internal to the chip, reading an empty FIFO or reading new packet data before the present packet is processed. It is up to the processor doing the FIFO reads to determine on which read cycle the SPDTAVL went low and thereby which read cycles are over reads containing invalid data.

3.5.4 Special Conditions on the RXRD_TXWR input

This input is required to be tied to a continuous clock signal whose maximum clock frequency can be 33Mhz. The number of read or write cycles occurring to the chip is controlled through the TXWREN and RXRDEN inputs. All transitions of the TXRDY, RXRDY, RXTXEOF, SPDTAVL, RXDC, RXTXDATA[31:0], and TXRET outputs are synchronized internally to the RXRD_TXWR clock and are clocked to the output drivers on the highgoing edge of the clock.

3.6 REGISTER INTERFACE

3.6.1 Internal Port Register Addressing Table

Writing of Command, Configuration, and Station Address registers and reading of status registers is controlled by the ENREGIO, RD, WR, REGPS[1:0], and A[4:0] signals. The ENREGIO signal is used as a general register interface enable and must be active low before any register operations can occur. The REGPS signals are used to select which port's registers are to be accessed. The A[4:0] are used to address which register within a port is being accessed. Initiation of a register read is controlled by the RD signal and initiation of a register write is controlled by the WR signal. A port's registers may be accessed at any time. However, it is recommended that writing to the command register, be done only during interframe gaps.

With the exception of the two Match Mode bits in the Receive Command Register, all bits in both command registers are interrupt enable bits. Changing the interrupt enable bits during frame transmission does not affect the frame integrity. Asynchronous error events, however, e.g., overflow, underflow, etc., may cause chip operation to vary, if their corresponding enable bits are being altered at the same time.

Reading the status registers may also occur at any time during transmission or reception.

Status Registers and all management counters are read only registers. The Rx and Tx Command Registers are write only or read/write registers based on the address inputs. Please refer to the mode/port select table for details. All other registers are writable and readable. Access to these registers is via the CPU interface: Control signals ENREGIO, RD, WR, REGPS [1:0] A[4:0], and the Command/Status Data Bus CdSt [7:0].

3.6.2 Station Address Register

The Station Address Register is 6 bytes in length. The contents may be written in any order, with bit "0" of byte "0" corresponding to the first bit received in the data stream,

3.6.1 Internal Port Register Addressing Table

Transmit Command Register Bits		Register Address					Register Description	
6	5	A4	A3	A2	A1	A0	Read	Write
0	0	0	0	0	0	0	Station Address 0	Station Address 0
0	0	0	0	0	0	1	Station Address 1	Station Address 1
0	0	0	0	0	1	0	Station Address 2	Station Address 2
0	0	0	0	0	1	1	Station Address 3	Station Address 3
0	0	0	0	1	0	0	Station Address 4	Station Address 4
0	0	0	0	1	0	1	Station Address 5	Station Address 5
X	X	0	0	1	1	0	Rx Status Register	Rx Command Register
X	X	0	0	1	1	1	Tx Status Register	Tx Command Register
0	1	0	0	0	0	0	Hash Register 0	Hash Register 0
0	1	0	0	0	0	1	Hash Register 1	Hash Register 1
0	1	0	0	0	1	0	Hash Register 2	Hash Register 2
0	1	0	0	0	1	1	Hash Register 3	Hash Register 3
0	1	0	0	1	0	0	Hash Register 4	Hash Register 4
0	1	0	0	1	0	1	Hash Register 5	Hash Register 5
1	0	0	0	0	0	0	Hash Register 6	Hash Register 6
1	0	0	0	0	0	1	Hash Register 7	Hash Register 7
1	0	0	0	0	1	0	FIFO Threshold Register	FIFO Threshold Register
1	0	0	0	0	1	1	Configuration Register #2	Configuration Register #2
1	0	0	0	1	0	0	Configuration Register #1	Configuration Register #1
1	0	0	0	1	0	1	Defer Count Register	Defer Count Register
1	1	0	0	0	0	0	CRC Error Counter	—
1	1	0	0	0	0	1	Runt Frame Counter	—
1	1	0	0	0	1	0	Oversize Frame Counter	—
1	1	0	0	0	1	1	Dribble Error Counter	—
1	1	0	0	1	0	0	Tx Collision Counter	—
1	1	0	0	1	0	1	Rx Collision Counter	—
X	X	0	1	0	0	0	Transmit Control/Product I.D. Register	Transmit Control/Product I.D. Register
X	X	0	1	0	0	1	Configuration Register #3	Configuration Register #3
X	X	0	1	0	1	0	Tx Collision Single Retry Counter	—
X	X	0	1	0	1	1	Tx Collision Multiple Retries Counter	—
X	X	0	1	1	0	0	Tx Collision 16 Retries Counter	—
X	X	0	1	1	0	1	Total Successful Tx Frames Counter	—
X	X	0	1	1	1	0	Total Successful Tx Octets Counter	—
X	X	0	1	1	1	1	Transmit FIFO Underruns Counter	
X	X	1	0	0	0	0	Transmit Late Collisions Counter	—

3.6.1 Internal Port Register Addressing Table (continued)

Transmit Command Register Bits		Register Address					Register Description	
6	5	A4	A3	A2	A1	A0	Read	Write
X	X	1	0	0	0	1	Carrier Sense Error During Tx Counter	—
X	X	1	0	0	1	0	Transmit Deferred Counter	—
X	X	1	0	0	1	1	Rx FIFO Overflow Counter	—
X	X	1	0	1	0	0	Counter Interrupt Enable Register #1	Counter Interrupt Enable Register #1
X	X	1	0	1	0	1	Counter Interrupt Enable Register #2	Counter Interrupt Enable Register #2
X	X	1	0	1	1	0	Counter Interrupt Status Register #1	—
X	X	1	0	1	1	1	Counter Interrupt Status Register #2	—
X	X	1	1	0	0	0	CRC Error Counter	—
X	X	1	1	0	0	1	Short Frame Counter	—
X	X	1	1	0	1	0	Oversize Frame Counter	—
X	X	1	1	0	1	1	Dribble Error Counter	—
X	X	1	1	1	0	0	Full Duplex Status	—
X	X	1	1	1	0	1	Rx Collision Counter	—
X	X	1	1	1	1	0	Rx Command Register	Rx Command Register
X	X	1	1	1	1	1	Tx Command Register	Tx Command Register

and indicating whether the address is physical or logical. Bit 7 of station address byte 5 is compared to the last bit of the received destination address. The Station Address should be programmed prior to enabling a port's receiver.

3.6.3 Transmit Command Register

The transmit command register is an 8 bit register. Bits 0 through 3 of the Transmit Command Register function as interrupt mask bits, which provide for control of the conditions allowed to generate transmit interrupts. Each of the four bits may be individually set or cleared. When set, the occurrence of the associated condition will cause an interrupt to be generated. The four specific conditions for which interrupts may be generated are:

1. *A Transmit FIFO underflow occurred while transmitting the packet.*
2. *A collision occurred while transmitting the packet.*
3. *A transmit error condition occurred i.e, (Carrier sense never went active during transmission or went from an active to inactive state during transmission or 16 collisions occurred for a transmit packet or a late collision occurred).*
4. *The packet was transmitted successfully.*

Interrupts are cleared by following the procedure given in the section entitled "Clearing Interrupts" in section 3.3.5.

Transmit Command Register Format

7	6	5	4	3	2	1	0

Bit	Value	Definition		R/W*	Default Values After Reset
0	'1'	Generates an interrupt on the occurrence of a transmit underflow.		R/W	0
1	'1'	Generates an interrupt on the occurrence of a collision during the transmission of a packet.		R/W	0
2	'1'	Generates an interrupt on the occurrence of a transmit error condition.		R/W	0
3	'1'	Generates an interrupt on the occurrence of a successful transmission.		R/W	0
4	'1'	Sets the chip into the MII mode		R/W	0
5	'1'	Register Code Bit 0.	These two bits are used in conjunction with the A[4:0] address pins to access registers other than the Receive and Transmit command registers within a port.	R/W	0
6	'1'	Register Code Bit 1.		R/W	0
7	'0'	Test Mode. Note: This bit should not be written HIGH under normal circumstances.		R/W	0

* This register can be used as a write only register or a Read/Write register by configuring the address inputs accordingly. Please refer to "3.6.1 Internal Port Register Addressing Table" for details.

3.6.4 Transmit Status Register

Within each port's transmit section are 2 transmit status registers. These registers give the appearance of a single register to an external CPU. With each transmission attempt, whether successful or not, one of the status registers is written with the transmit status for that packet and bit 7 of that register is set to a 0 until both registers are full. When both registers are full, no new transmit status can be written until one of the registers is read. To an external CPU, both transmit status registers appear as a single register. If the CPU reads a LOW value for bit 7 of the transmit status register, this indicates that either one or both of the internal transmit registers contains new status. A delay time after the highgoing edge of the read operation that reads new transmit status, one of the internal transmit status registers will be cleared and made available for new transmit status. Following are the types of transmit status given through status register:

A port can be programmed so that if both transmit registers are full, no new transmissions will occur until at least one of the register is cleared by reading it. To program this feature, bit #1 of configuration register #2 needs to be written to a 1 value.

Also a port can be programmed so that no new transmit status is loaded if the transmission is successful.

Transmit Status Register Format

7	6	5	4	3	2	1	0

Bit	Value	Definition	R/W	Value After Reset
0	'1'	Indicates the occurrence of a Transmit FIFO underflow.	R	0
1	'1'	Indicates the occurrence of a collision during a transmission attempt.	R	0
2	'1'	Indicates that 16 collisions occurred while attempting to transmit a packet.	R	0
3	'1'	Indicates the successful completion of a packet tranmission.	R	0
4	'1'	Indicates the occurrence of a carrier sense error during a transmission attempt.	R	0
5	'1'	Indicates the occurrence of a deferred transmission due to carrier sense being detected HIGH.	R	0
6	'1'	Indicates the occurrence of a late collision. Late collision is the occurrence of a transmit collision 64 byte times after TXEN went HIGH.	R	0
7	'1'	Indicates old/new status.	R	0

3.6.5 Receive Command Register

A port's Receive Command Register has two primary functions, it specifies the Address Match Mode, and it specifies which types of receive frames will be received and if an associated interrupt will be produced. To set interrupt conditions the Receive Command Register uses bits 5 through 0 in conjunction with bit #7 of configuration register #1.

Bit 7 of configuration register #1 is a general receive interrupt disable. Setting this bit HIGH disables all receive interrupt conditions even if one of the bits 0 through 5 in the receive command register is set HIGH. This allows enabling reception of receive packets with errors without an interrupt being produced. With the general receive interrupt bit LOW, a receive interrupt can be produced on one or more of the following conditions by setting its associated interrupt enable bit in the receive command register:

Receive Command Register Format

7	6	5	4	3	2	1	0

Receive Command Register	Receive Command Register Values	Definition	R/W*	Default Values Upon Reset
Bit 0	1	Enables Reception of packets with a receive overflow error without generating an RXDC.	R/W	0
	0	Automatically discards packets with a receive overflow error generating an RXDC.	R/W	0
Bit 1	1	Enables Reception of packets with a receive CRC error without generating an RXDC.	R/W	0
	0	Automatically discards packets with a receive CRC error generating an RXDC.	R/W	0
Bit 2	1	Enables Reception of oversized packets without generating an RXDC.	R/W	0
	0	Automatically discards oversized packets generating an RXDC.	R/W	0
Bit 3	1	Enables Reception of undersized packets without generating an RXDC.	R/W	0
	0	Automatically discards undersized packets generating an RXDC.	R/W	0
Bit 4	1	Depending on the value of Bit #7 of Configuration Register #3, this bit can be used as an indication of the first 12 bytes received.	R/W	0
Bit 5	1	Depending on the value of Bit #7 of Configuration Register #3, this bit can be used as an indication of the reception of a good packet for debugging purposes.	R/W	0
Bit 6	Please Refer to the following table for match mode definitions			
Bit 7				

Note: Bit 7 of configuration register #1 is a general receive interrupt disable mode. Setting this bit HIGH will prevent a interrupt from being generated even if one of the bits 0 through 5 in the receive command register is set HIGH. This enables the reception of receive packets with errors without generating an interrupt.

*This register can be used as a write only or a Read/Write register by configuring the address input accordingly. Please refer to "3.6.1 Internal Port Register Addressing Table" for details.

	Match Mode 1	Match Mode 0	Function
0	0	0	Receiver Disable
1	0	1	Receive All Frames
2	1	0	Receive Station or Broadcast Frames
3	1	1	Receive Station, Broadcast/Multicast Frames

NOTE
Changing the receive Match Mode bits during frame reception may change chip operation and give unpredictable results.

3.6.6 Receive Status Register

Within each port's receive section there is a receive status register that is written with the status of each receive packet whether it is discarded or not. Once the receive status register is written, bit 7 of the register is set to a 0 and the register is write protected from being overwritten with new status until it is read. Reading the receive status register clears the register and enables it to be written with new status. The following packet status is reported in the receive status register:

Receive Status Register Format

7	6	5	4	3	2	1	0

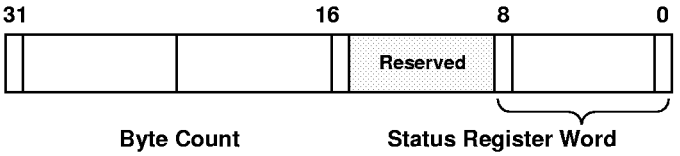
Bit	Value	Definition	R/W	Default
0	'1'	Indicates that a frame with an overflow error has been received.	R	0
1	'1'	Indicates that a frame with a CRC error has been received.	R	0
2	'1'	Indicates that a frame with dribble bits or nibbles has been received.	R	0
3	'1'	Indicates that a short frame has been received.	R	0
4	'1'	Indicates that an oversized frame has been received.	R	0
5	'1'	Indicates that a good frame has been received.	R	0
6	'1'	Indicates that the first 12 bytes of a frame has been received.	R	0
7	'1/0'	Indicates old (1) /new (0) status	R	0

Receive packet status is also included as part of the final double word of receive data for a packet that is not discarded. The final double word of a packet as read from the receive FIFO contains the status and the byte count for that packet with the status appearing as the least significant word of the double word and the byte count appearing in the two most significant bytes of the double word. The status read through the FIFO has the same bit values as the receive status register except for the following:

Bit 7: RXABORT During Reception
Bit 8: Read Error Condition

Bit 7 is an indication that the RXABORT pin was pulsed HIGH while CSN was HIGH for the packet. Bit 8 Indicates that some type of error has occurred in the receive FIFO control circuitry with a result that the number of double words written to the FIFO as indicated by the byte count portion of the status double word does not equal the number of double words read from the FIFO for the packet.

The Status Double Word Format



Note: This status double word gets appended to the packet in the same format for both Little and Big Endian modes.

This type of error can only be caused by some type of noise glitch or other unusual occurrence within the receive section. Any packet read from the FIFO with Bit 8 of the status set HIGH should be considered to have bad data. This condition should never occur in a properly designed application. If status is ever read with Bit 8 being HIGH, the receive section will automatically reset itself to provide a clean starting point for further packet reception.

Clearing Interrupts

Both receive and transmit interrupts for a port are combined into a single interrupt signal which then goes to that port's INT output pin. The interrupt signal within a port in the chip is actually the result of the receive/transmit status register outputs and the receive/transmit command register interrupt enable bits that are set. To clear an interrupt the status that caused the interrupt needs to be cleared. This can be accomplished by reading the transmit status register and/or the receive status register.

3.6.7 Configuration Registers

Configuration Register #1

Allows for control of a port's various transmit and receive features. Set to all 0's after reset.

Mode A: Group Address Mode

In this mode the last 4 bits of the serial receive data stream for the destination address are masked out in address comparison. This means that when the destination address is compared against the value

Configuration Register #1

7	6	5	4	3	2	1	0

Bit	Value		Definition	R/W	Default	Mode
0	W	'1'	Enables Group Address Mode.	R/W	0	A
		'0'	Disables Group Address Mode.			
	R	'1'	Detection of a 25 MHz TXCLK from the Transceiver.			
		'0'	Detection of a 25 MHz TxCLK from the Transceiver			
1	'1'		Enables Transmit packet Autopad Mode.	R/W	0	B
2	'1'		Enables transmit no preamble mode.	R/W	0	C
3	'1'		Refer to TABLE A	R/W	0	D
4	'1'		Enables transmit no CRC mode.	R/W	0	E
5	'1'		Refer to TABLE A	R/W	0	F
6	'1'		Enables Receive CRC Mode.	R/W	0	G
7	'1'		Disables Receive Interrupts	R/W	0	H

programmed in the station address register that the packet will not be rejected due to incorrect address even its last 4 bits did not match.

Mode B: Transmit Packet Autopad Mode
This feature automatically pads packets to be transmitted with less than 60 bytes of data out to a minimum IEEE 802.3 standard packet length of 60 bytes excluding FCS. Padding is done with bytes of 00 hex in 10 Mbit/sec Serial Mode and 55 hex in MII mode.

Mode C: Transmit No Preamble Mode
This mode prevents the transmitter from adding a preamble pattern at the beginning of data to be transmitted.

Mode D: Receive Own Transmit Disable Mode
This mode prevents a port from receiving a packet if it is also transmitting a packet. Please refer to Table A for details.

Mode E: Transmit No CRC Mode
This mode prevents a port's transmitter from appending transmit data with an FCS.

Mode F: Full Duplex Mode
In this mode a ports transmitter will ignore carrier sense and will not defer to it if it is ready to transmit a packet.

The software bit setting and the hardware setting (pin #123, 124, 125 or 127) have an OR relationship. This means that either the hardware or software setting will enable Full Duplex.

Note: *Bit 3 setting will vary according to the Full Duplex or Half Duplex setting. Please refer to Table A for details.*

Mode G: Receive CRC Mode
In this mode a ports receiver loads the 4 bytes of FCS into the receive FIFO along with the data allowing the FCS value to be read out.

Mode H: Disable Receive Interrupts
With this bit set a ports receiver is disabled from producing receive interrupts.

Full Duplex/Half Duplex Modes
Operation with Receive Own Transmit Disable. TABLE A

The following description assumes that a transceiver is connected to the MAC.

Bit 3	Bit 5	Mode	Functional Description
1	0 (Default)	Half Duplex	In this mode the transmit data looped back from the transceiver is ignored by the controller. The data does not get written into the receive FIFO and the Rxrdy does not reflect the incoming data.
0 (Default)	1	Full Duplex	In this mode the transceiver (In Full Duplex mode) will not loopback the transmitted data. However, since data reception is possible during transmission, bit 3 should be written with '0' so that the data gets written to the Receive FIFO.
0 (Default)	0 (Default)	Loopback Mode	In normal Half Duplex operation the PHY loops back the transmitted data back to the MAC. In other words, the PHY always loops back the transmitted data in half duplex mode. As far as the controller is concerned, it knows that the data coming back is it's own transmitted packet and since bit 3 is not set, the transmitted packet gets written into the receive FIFO.
1	1		Reserved

Note: There is no internal loopback within the MAC. Loopback is dependent on a PHY connected to the MAC.

Configuration Register #2

Allows for control of a port's transmission of one packet at a time, Busmode, Multi-cast hash filter, reception of runt frames, and halting new transmissions until one of the port's transmit status registers is cleared.

Mode A: Don't Load Tx Status Upon Successful Transmit Mode

If bit #0 of configuration register #2 is set, then a packet that has been transmitted successfully will not have it's status loaded into either of the two internal transmit status registers.

Mode B: Disable Further Transmission Upon Full Tx Status Register Mode

If bit #1 of configuration register #2 is set, whenever both Tx Status Registers have been filled, no new transmissions will occur until one of the Tx Status Registers is cleared, even if the transmit FIFO has transmit data.

Mode C: EOF on Data

This function puts a HIGH EOF value on both the last double word of data and the status double word.

Mode D: Multicast Mode

Each port has a 64 bit multicast address filter register which can be accessed as shown in the Internal Port Register Addressing Table (page 18). When a port is programmed to receive multicast frames (match mode 3), after computing the CRC on the address field of the receiving frame (first 6 bytes), it will index

Configuration Register #2

7	6	5	4	3	2	1	0

Bit	Value	Definition	R/W	Default	Mode
0	'1'	Disables loads to the transmit status register upon a successful transmission.	R/W	0	A
1	'1'	Disables new transmissions upon a full transmit status register condition.	R/W	0	B
2	'1'	Generates an EOF on both the last double word of data and also the status double word.	R/W	0	C
3	'1'	Enables the hash filter for multicast operation.	R/W	0	D
4	'1'	Enables the reception of packets without a discard even if the RXABORTgoes high during the reception of a packet.	R/W	0	E
5[3]	'1'	Packs only two bytes into the first double word written to the Receive FIFO.[1]	W only	0	F1
	'0'	Normal mode.[2]			
	'1'	SQE Test Pass	R only	0	F2
	'0'	SQE Test Fail[4]			
6	'1'	When this bit is SET, the TXRDY is driven low after an EOF is written into the transmit FIFO and stays low until the packet is successfully transmitted.	R/W	0	G
7	'1'	Sets the chip into Big Endian Mode	R/W	0	H

Notes: 1. Non-Bidirectional Byte Enable Mode only.
2. Must be used for Bidirectional Byte Enable Mode.
3. This bit address is shared for two functions.
4. Read will clear this bit to '0'.

to the multicast address filter register depending on bits 0 to 5 of the CRC. If the corresponding bit is a '1' it will receive the frame, otherwise it will discard the frame.

Mode E: Receive Without Discard Mode
When this bit is written "High", packets will be received without discarding even if the RXABORT goes high during reception.

Mode F1/F2: Pack Only Two Valid Bytes in First Receive Double Word/SQE Status, Bit 5
Mode F1: When this bit is written HIGH, the first double word of data written to the receive FIFO for a receive packet will have only two valid bytes. When this first double word is read out of the receive FIFO, which two bytes are valid depends on whether the port has been programmed for Big Endian or Little Endian data formats. Thus, if bit 7 of Configuration Register #2 (Endianess selection) is set HIGH (Big Endian), RXTXDATA[15:0] will be valid for the first double word read; if bit 7 is set LOW (Little Endian), RXTXDATA[31:16] will be valid. All subsequent double words of data read from the receive FIFO will contain 4 valid bytes except for the last double word which may not have all 4 bytes valid.

***Note**: This mode is available only if the chip is used in non-bidirectional byte enable operating mode.*

Mode F2: Reading this bit provides SQE test result. The SQE function is always on; reading this register causes an automatic reset of this bit value to "zero".

Mode G: Successful Packet Transmission Complete Feature
This feature is programmable by setting bit 7 of configuration register #2 to a '1' value. If this bit is set, then, independent of the FIFO threshold setting, the corresponding port's TXRDY pin will go LOW once the final double word of data for a transmit packet is written to the transmit FIFO. Once a port's TXRDY has been driven LOW due to this condition, it will remain LOW until the packet has completed transmission without error or until a transmission exception condition causing the TXRET pin to go HIGH is cleared. This allows the user to determine when a packet has completed successful transmission by detecting when the corresponding port's TXRDY goes HIGH after the final double word of the packet has been written. After TXRDY goes LOW due to a double word write with the RXTXEOF pin HIGH, further writes to the transmit FIFO are allowed as long as the SPDTAVL pin indicates that there is still space available within the transmit FIFO.

Mode H: Big Endian Mode
Writing this bit HIGH programs the port to Big Endian mode.

Configuration Register #3

Mode A:

Bit 0 - When written to a 1 this bit programs the 84301 into bidirectional byte enable mode. In this mode the RXTXBE [3:0] pins act as inputs during Transmit FIFO write operations and as outputs during Receive FIFO read operations. When this bit is 0 the RXTXBE [3:0] pins are input only. The value of this bit after reset is 0.

Mode B: Status Non-Appendage Mode

Bit 1 - When written to a 1 this bit stops the 84301 from including a status double word in the Receive FIFO at the end of receive packet data. When this bit is 0 any packet received without discard will include a status double word in the FIFO. The value of this bit after reset is 0.

Note: *If both this bit and bit 2 of configuration register #2 have been written to a 1, the chip will behave as if bit 2 of configuration register #2 were a 0. In other words only one EOF, occurring on the last double word of data, will be read out and no status double word will occur during reading of the receive packet data.*

Mode C: 32 Bit-Mode for Some Counters

Bit 2 - When written to a 1 this bit enables the full 32-bit size of the following counters.

CRC Error Counters
Short Frame Counter
Oversize Frame Counter
Dribble Error Counter
Receive Collision Counter

When this bit is 0 the above counters behave as 16-bit counters. The value of this bit after reset is 0.

Note: *This bit must be written to 1 before interrupts for these counters can be enabled using bits 6 through 2 of the Counter Interrupt Mask Register #2. Otherwise, these counters will never cause an interrupt condition or set any of the interrupt status bits in the Interrupt Status Register #2.*

Mode D: Counter Operations

Bit 3 - This bit controls the effect that completion of a read operation to a management counter has upon that counters next value in the following ways:

Counter Reset Mode

When written to a 1 - Upon reading the least significant byte of a management counter, the counter value will either be reset to 00000000 hex or preloaded to a value other than 00000000 hex if there was an attempt to update the counter during the time the counter value was frozen due to a read operation in progress. (Please see counter description section).

Counter Incrementing Mode

When written to a 0 - Upon reading the least significant byte of a management counter, the counter will either maintain its present value, or be incremented if there was an attempt to update the counter during the time the counter value was frozen due to a read operation in progress.

Configuration Register #3

7	6	5	4	3	2	1	0

Bit	Value	Definition	R/W	Default	Mode
0	'1'	Sets the Chip into Bidirectional Byte Enable Mode.	R/W	0	A
1	'1'	When this bit is set, the status double word will be prevented from being appended to the end of a packet received.	R/W	0	B
2	'1'	Enables 32 bit mode for some counters.	R/W	0	C
3	'1'	Counter Reset Mode	R/W	0	D
	'0'	Counter Incrementing Mode			
4	–	Unused	R	0	–
5	–	Unused	R	0	–
6	–	Unused	R	0	–
7	–	Unused	R	0	–

Bits 4 thru 7 - Unused. These bits when read will have a 0 value.

3.6.8 FIFO Threshold Register

This register allows programming of the threshold of Space Available and/or Data Available double word counts that cause assertion of the TxRDY and/or RxRDY signals respectively. Bits 4 through 7, when written with a binary value, indicates the minimum number of double words necessary in the receive FIFO before RxRDY is asserted. Similarly, bits 0 through 3, when written with a binary value, indicate the minimum number of double word wide spaces necessary in the transmit FIFO for TxRDY to be asserted. Table 3.6.8.1 shows how many double words of space/data are required to cause the TXRDY/ RXRDY signals to go high for each threshold setting.

3.6.9 Defer Register Calculations for the 84301

Defer Time Definitions

In the standard Half Duplex Mode, Defer time is defined as the time from the falling edge of carrier sense to the rising edge of TXEN. In full duplex mode, the defer time is measured as the time from the falling edge of TXEN to the next rising edge of TXEN. The binary value programmed into the defer count register is used to determine how many byte times the defer time will be set to. The algorithms below illustrates how the defer time is calculated.

The defer time is split into two periods. The first period is the first 2/3 and the second period is the second 1/3 of the defer time. The defer time calculated by the following algorithms are for the first 2/3 of the defer period only. For further details, please refer to the section 3.2.2.

Algorithm for Defer Time Calculations for MII

Defer Time = Int{{Int (Delay /40) + 5 + DefRegSet}/2}+2

Defer Time = The transmit defer time in byte times

Delay = Delay from the falling edge of TXEN to the falling edge of CSN. (Half Duplex)
= 0 (Full Duplex)

DefRegSet = The transmit defer register setting

Int = Using the Whole Number Portion

Example Calculations

To find out the value that needs to be programmed into the defer register for a defer time of 960 ns, the following steps need to be taken

Assume Delay = 340 ns
Desired Defer Time = 960 ns = 12 byte times
Note: The desired defer time should be a multiple of 80

3.6.8.1 FIFO Threshold Register Settings Table

Fifo Threshold Register Bits								Minimum # of Double Words of Data for RXRDY High	Minimum # of Double Word Spaces for TXRDY High
7	6	5	4	3	2	1	0		
0	0	0	0	0	0	0	0	1	1
0	0	0	1	0	0	0	1	2	2
0	0	1	0	0	0	1	0	3	3
0	0	1	1	0	0	1	1	4	4
0	1	0	0	0	1	0	0	5	5
0	1	0	1	0	1	0	1	6	6
0	1	1	0	0	1	1	0	7	7
0	1	1	1	0	1	1	1	8	8
1	0	0	0	1	0	0	0	9	9
1	0	0	1	1	0	0	1	10	10
1	0	1	0	1	0	1	0	11	11
1	0	1	1	1	0	1	1	12	12
1	1	0	0	1	1	0	0	13	13
1	1	0	1	1	1	0	1	14	14
1	1	1	0	1	1	1	0	15	15
1	1	1	1	1	1	1	1	16	16

Step 1: Calculation of the Actual Defer Time

Let's assume a Defer Register Setting Value of 10

Defer Time = Int{ {Int (Delay / 40) + 5 + DefRegSet} /2} + 2

= Int { { Int (8.5) + 5 + 10 }/2} + 2

= Int { 11.5 } + 2

= 11 + 2 = 13 byte times

Step 2: Calculation of the Actual Defer Register Setting

Since we know that the value derived from the previous step is 1 byte time greater than what is desired we will decrement the assumed defer register setting by 3 and do the calculations again.

Let's assume a Defer Register Setting Value of 7

Defer Time = Int { {Int(Delay/40) + 5 + DefRegSet} /2} + 2

= Int { { Int(8.5) + 5 + 7 } /2 } + 2

= Int { 10 } + 2

= 12 byte times

Note: Please note that you might have to do this process several times before you can get the actual defer register setting for a desired defer time based on your delays.

Algorithm for Defer Time Calculations for 10 Mbit Serial Mode

Defer Time = Int {{Int (Delay/100)+17+DefRegSet}/8}+2

Defer Time = The transmit defer time in byte times

Delay = Delay from the down going edge of TXEN to the down going edge of CSN. (Half Duplex)
= 0 (Full Duplex)

DefRegSet = The transmit defer register setting

Int = Using the Whole Number Portion

Example Calculations

To find out the value that needs to be programmed into the defer register for a defer time of 9600 ns, the following steps need to be taken

Assume Delay = 3400 ns
Desired Defer Time = 9600 ns = 12 byte times
The desired byte times should be a multiple of 800

Step 1: Calculation of the Actual Defer Time

Let's assume a Defer Register Setting Value of 21

Defer Time = Int { { Int (Delay / 100) + 17 + DefRegSet} /8} + 2

= Int { { Int (34) + 17 + 21}/8} + 2

= Int {9} + 2

= 9 + 2 = 11 byte times

Step 2: Calculation of the Actual Defer Register Setting

Since we know that the value derived from the previous step is 1 byte time lower than what is desired we will increment the assumed defer register setting by 8 and do the calculations again.

Let's assume a Defer Register Setting Value of 29

Defer Time = Int {{Int (Delay / 100)+17+DefRegSet} /8} + 2

= Int { { Int (34) + 17 + 29 } /8} + 2

= Int { 10 } + 2

= 10 + 2 = 12 byte times

Please note that you might have to do this process several times before you can get the actual defer register setting for a desired defer time based on your delays.

3.6.10 Transmit Control/Product I.D. Register

The lower four bits can be used to set a threshold value on the transmit FIFO that can be used to control the packet transmission and the upper four bits of this register contains the product I.D. When the lower four bits are written with a decimal value ranging from 1 to 15, packet transmission from the FIFO will begin only when the count of the double words of data written into the transmit FIFO equals or exceeds twice the register value. For example, when the lower four bits are written with a decimal value of 15, data transmission will begin only after the FIFO is written with 30 or more double words of data. This threshold value is valid only at the beginning of frame transmission and it will take effect again when the user starts to load the beginning of the next frame. The default decimal value of the lower four bits is '0' and packet transmission will begin automatically when the FIFO is loaded with a minimum of one double word of data. The upper four bits are read only and contain a value of 'C'.

3.6.11 Full Duplex Status Register

A port's Full Duplex status can be read from bit 0 of this register. A read back value of '1' indicates that the port is in Full Duplex mode which is enabled by either the software bit setting (configuration register #1 bit 3 and 5) or the hardware setting (pin # 123, 124, 125 or127).

3.7 COUNTERS

Each 84301 port supports fifteen 32-bit receive/transmit statistics counters, as described below:

CRC Error Counter [1] - This counter is incremented by 1 any time a frame is received with a proper preamble and start frame delimiter that has greater than or equal to 64 bytes of data, excluding preamble and including CRC, and also has a CRC error.

Runt Frame Counter [1] - This counter is incremented by 1 any time a frame is received with a proper preamble and Start Frame delimiter that has less than 64 bytes of data, excluding preamble and including CRC.

Oversize Frame Counter [1] - This counter is incremented by 1 any time a frame is received with a proper preamble and start frame delimiter that has greater than 1518 bytes of data excluding preamble bytes and including CRC.

Alignment Error Counter [1] - This counter is incremented by 1 any time a frame is received with a proper preamble and start frame delimiter that has greater than 64 bytes of data, excluding preamble and including CRC, and also has a CRC error and a non-integral number of octets of data.

Transmit Collisions Single Retry - This counter is incremented by 1 any time a frame requires 1 and only 1 retransmission due to a collision before it is successfully transmitted. Late transmit collision occurrences will never cause this counter to be incremented. This counter will never be incremented if the port is in full-duplex mode since in this mode a port's COLL pin should never be driven HIGH.

Transmit Collisions Multiple Retries - This counter is incremented by 1 any time a frame requires greater than 1 but less than 16 retransmission attempts before it is successfully transmitted. Late transmit collision occurrences will never cause this counter to be incremented. This counter will never be incremented if the port is in full-duplex mode since in this mode a port's COLL pin should never be driven HIGH.

Transmit Collision Sixteen Retries - This counter is incremented by 1 any time a frame fails to be transmitted due to 16 collision occurrences. If the 16th collision is also a late collision then both this counter and the Late Collision Counter will be incremented. This counter will never be incremented if the port is in full-duplex mode since in this mode a port's COLL pin should never be driven HIGH.

Receive Collisions - This counter is incremented by 1 any time the chip is not transmitting, the TXEN output is LOW, and the COLL pin goes HIGH for greater than 2 receive clock cycles 6.4 µs after TXEN has gone LOW if this is in 10 MBit/sec serial mode.

Transmit FIFO Underruns - This counter is incremented by 1 any time a Transmit FIFO Underrun error occurs. A transmit FIFO Underrun Error occurs any time the transmitter empties the transmit FIFO before seeing an end of frame indication in the FIFO.

Late Collisions - This counter is incremented by 1 any time a collision occurs greater than 64 byte times after TXEN has gone high during the transmission of a frame. This counter will never be incremented if the port is in full-duplex mode since in this mode a port's COLL pin should never be driven HIGH.

Loss of Carrier - This counter is incremented by 1 any time when during the transmission of a frame as indicated by TXEN being HIGH, carrier sense never goes HIGH or carrier goes from HIGH to a LOW.

Transmit Deferred - This counter is incremented by 1 any time that the transmit FIFO has data and the transmitter is ready to start transmission but the transmitter has to defer transmission due to carrier sense being HIGH. This counter will never be incremented if the port is in full-duplex mode.

Receive FIFO Overflow - This counter is incremented by 1 any time an incoming receive packet causes the receiver to attempt to write to a full Receive FIFO.

Transmit Frames - This counter is incremented by 1 any time a frame is transmitted successfully by the port.

Transmit Octets - This counter is incremented by the total number of octets of data excluding preamble but including CRC of a transmit frame if that frame was successfully transmitted.

3.7.1 Accessing the Counters

The counters will be accessed through the 8-bit Register Interface Bus. Write operations to the counters will have no effect. Read operations will be conducted through multiple 8-bit accesses. Accesses to register space which are interleaved with those to read the counters shall not disturb the counter accesses. The contents of all counters

Note1: Whether these counters are 16-bit or 32-bit depends on the value of bit 2 of Configuration Register #3. (See Section 3.6.7)

will be provided to the 8-Bit Register Interface with Big Endian Byte Ordering. For most of the counters 4 read operations are required to completely read the counter value. The only exception to this is if bit 2 of Configuration Register #3 is 0, then the counters mentioned in the description of that bit's function will require only 2 reads to completely read them. The value of the counter being read will be held upon detection of the first byte read operation. The counter value will be held until completion of the read that reads out the least significant byte of the counter. Once all bytes of a counter have been read, what happens to the counter value depends upon the value of the bit 3 of Configuration Register #3 and is described in the section below.

3.7.2 Counter Value After Read Operation Completion

Depending on the value written to bit 3 of Configuration Register #2 the value of a counter after the least significant byte has been read will either be preset to a value or reset to 00000000 hex dependent upon the following:

1. *If bit 3 is set in Configuration Register #3, then after the last byte of the counter is read, the counter will be cleared to zero if no attempts were made to increment the counter while its value was being held. If a port tries to update a counter when it's value was being held due to a read operation in progress, then once the least significant byte of the counter has been read, the counter will be preset to the count value it would have if the counter had started from zero and been incremented once.*

2. *If bit 3 is not set in Configuration Register #3 then after the last byte of the counter is read the counter will simply maintain its present value or, be incre mented after the least significant byte is read if a port attempted to increment the counter while the counter value was being held due to a read operation in progress.*

3.7.3 Counter Behavior Upon Reaching Maximum Count

When a counter reaches its maximum count (all bits are 1), the counter will not be allowed to increment further. The counter will be held at the maximum count until completion of a read operation to the counter causes its value to change according to the description given in item 1 of section 3.7.2, with the exception that in this case the actual value of bit 3 in Configuration Register #3 is ignored. Because the counter has overflowed, only those attempts to increment the counter while it was frozen for reading will be reflected in the new preset value. Any counter events that occurred while the counter was frozen prior to the beginning of being read are lost.

3.7.4 Counter Interrupt Conditions

3.7.4.1 Enabling Counter Interrupts

Writing any of the bits of either of the Counter Interrupt Enable Registers #1 or #2 will enable the assertion of an interrupt on the interrupt pin INT [4:1] for that port, should the associated counter reach a condition described in the next section. To determine if one or more counters have caused an interrupt condition, the Counter Interrupt Status Registers can be read. Once a counter has reached a condition described in section 3.7.4.2 its associated bit in the Counter Interrupt Status Register will be set independent of the setting of its associated Counter Interrupt Enable Register bit. To clear an interrupt condition either one or both the counters interrupt status registers has to be read.

3.7.4.2 Counter Attention Conditions

Each N-bit counter has a unique "Counter Attention Condition" bit which is automatically set when the count for the N-bit counter reaches a count of 80000000 hex which is half full of its terminal count of FFFFFFFF hex. The half full condition is specified to occur when the most significant bit of the counter transitions from a 0 to a 1.

These "attention bits" are stored in the Counter Interrupt Status Register #1 and #2. These registers are 8-bits wide. Writes to these registers will have no effect. Note that the contents of the Counter Interrupt Status Registers will be cleared after it is read.

Counter Interrupt Enable Register #1

7	6	5	4	3	2	1	0

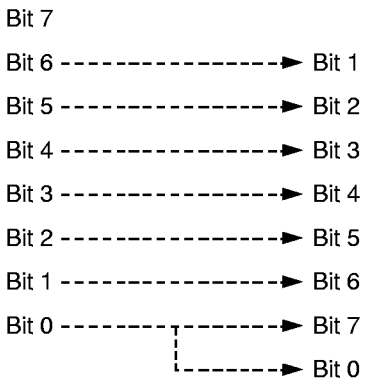
Bit	Value	Definition	R/W	Value After Reset
0	'1'	Enables an interrupt upon the Tx Collision Single Retry Counter reaching 80000000 hex.	R/W	0
1	'1'	Enables an interrupt upon the Tx Collision Multiple Retries Counter reaching 80000000 hex.	R/W	0
2	'1'	Enables an interrupt upon the Tx Collision 16 Retries Counter reaching 80000000 hex.	R/W	0
3	'1'	Enables an interrupt upon the Total Successful Tx Frames Counter reaching 80000000 hex.	R/W	0
4	'1'	Enables an interrupt upon the Total successful Tx octets Counter reaching 80000000 hex.	R/W	0
5	'1'	Enables an interrupt upon the Transmit FIFO Underruns Counter reaching 80000000 hex.	R/W	0
6	'1'	Enables an interrupt upon the Transmit Late Collisions Counter reaching 80000000 hex.	R/W	0
7	'x'	Unused	R/W	0

Counter Interrupt Enable Register #2

7	6	5	4	3	2	1	0

Bit	Value	Definition	R/W	Value After Reset
0	'1'	Enables an interrupt upon the transmit deferred counter reaching 80000000 hex.	R/W	0
1	'1'	Enables an interrupt upon the Receive FIFO Overflow Counter reaching 80000000 hex.	R/W	0
2	'1'	Enables an interrupt upon the CRC Error Counter reaching 80000000 hex.	R/W	0
3	'1'	Enables an interrupt upon the Short Frame Counter reaching 80000000 hex.	R/W	0
4	'1'	Enables an interrupt upon the Dribble Error Counter reaching 80000000 hex.	R/W	0
5	'1'	Enables an interrupt upon the Oversize Frame Counter reaching 80000000 hex.	R/W	0
6	'1'	Enables an interrupt upon the Receive Collision Counter reaching 80000000 hex.	R/W	0
7	'x'	Unused	R/W	0

Note: During read operations the bit order is changed to read in the following manner.



Hence for example; If a value "E2" is written, when read, the register will return a value of "46".

Counter Interrupt Status Register #1

7	6	5	4	3	2	1	0

Bit	Value	Definition	R/W	Value After Reset
0	'1'	Indicates that the Tx Collision Single Retry Counter has reached 80000000 hex.	R	0
1	'1'	Indicates that the Tx Collision Multiple Retries Counter has reached 80000000 hex.	R	0
2	'1'	Indicates that the Tx Collision 16 Retries Counter has reached 80000000 hex.	R	0
3	'1'	Indicates that the Total successful Tx Frames Counter has reached 80000000 hex.	R	0
4	'1'	Indicates that the Total Successful Tx Octets Counter has reached 80000000 hex.	R	0
5	'1'	Indicates that the Tx FIFO Underruns Counter has reached 80000000 hex.	R	0
6	'1'	Indicates that the TX Late Collisions Counter has reached 80000000 hex.	R	0
7	'1'	Indicates that the Carrier Sense Dropout Counter has reached 80000000 hex.	R	0

Note: If any of the above bit values are set to a '1', then reading of this register will clear this bit and the associated interrupt if bit 1 of the Counter Interrupt Enable Register #1 is programmed to a one.

Counter Interrupt Status Register #2

7	6	5	4	3	2	1	0

Bit	Value	Definition	R/W	Value After Reset
0	'1'	Indicates that the Tx Deferred Counter has reached 80000000 hex.	R	0
1	'1'	Indicates that the Receive FIFO Overflow Counter has reached 80000000 hex.	R	0
2	'1'	Indicates that the CRC Error Counter has reached 80000000 hex.	R	0
3	'1'	Indicates that the Short Frame Counter has reached 80000000 hex.	R	0
4	'1'	Indicates that the Dribble Error Counter has reached 80000000 hex.	R	0
5	'1'	Indicates that the Oversize Frame Counter has reached 80000000 hex.	R	0
6	'1'	Indicates that the Receive Collisions Counter has reached 80000000 hex.	R	0
7	'x'	Unused	R	0

Note: If any of the above bit values are set to a '1', then reading of this register will clear this bit and the associated interrupt if bit 1 of the Counter Interrupt Enable Register #2 is programmed to a one.

ABSOLUTE MAXIMUM RATINGS

Absolute maximum ratings are limits beyond which may cause permanent damage to the device or affect device reliability. All voltages are specified with respect to GND, unless otherwise specified.

VCC Supply Voltage .....-.3V to 6.0V

All Inputs and Outputs with Respect to GND .....-.3V to VCC+.3V

Package Power Dissipation ..... 2.2 Watt @ 70 °C
Storage Temperature .....-65 to +150°C
Temperature Under Bias..... -10 to +80°C
Lead Temperature (Soldering, 10 Sec) ..... 260°C
Body Temperature (Soldering, 30 Sec) .....220°C

4.0 DC Characteristics T_A = 0° C to 70°C, V_{CC} = 5 V ± 5%

Symbol	Parameter	Limits[1]			Units	Condition
		Min.	Typ.	Max.		
I_{IN}	Input Leakage Current			10	µA	V_{IN} = 0.45 V to 5.25 V
I_O	Output Leakage Current			10	µA	V_{OUT} = 0.45 V to 5.25 V
I_{CC}	V_{CC} Current		250	300	mA	
V_{CH}	Clock Input High Voltage	2.4			V	
V_{CL}	Clock Input Low Voltage			0.6	V	
V_{IL}	Input Low Voltage			0.8	V	
V_{IH_1}	Input High Voltage	2.0			V	
V_{OL}	Output Low Voltage RXTXDATA [31:0], RXTXEOF, SPDTAVL, TXRDY_[1:4], RXRDY_[1:4], TXRET_[1:4], RXDC_[1:4]			0.4	V	I_{OL} = 8 mA
V_{OH}	Output High Voltage RXTXDATA [31:0], RXTXEOF, SPDTAVL, TXRDY_[1:4], RXRDY_[1:4], TXRET_[1:4], RXDC_[1:4]	2.4			V	I_{OH} = 8 mA
V_{OL}	Output Low Voltage TXD [0:3]_[1:4], TXEN_[1:4]			0.4	V	I_{OL} = 4 mA
V_{OH}	Output High Voltage TXD [0:3]_[1:4], TXEN_[1:4]	2.4			V	I_{OH} = 4 mA
V_{OL}	Output Low Voltage All Other Outputs			0.4	V	I_{OL} = 2 mA
V_{OH}	Output High Voltage All Other Outputs	2.4			V	I_{OH} = 2 mA

NOTE:
1. Typical values are for T_A = 25°C and nominal supply voltages.

AC Test Conditions

Output Load: 1 Schottky TTL Gate + CL = 100 pF except where specifically given otherwise in the condition column.
Input Pulse Level:0.4 V to 2.4 V
Timing Reference Level:1.5 V

Capacitance $T_A = 25°C, F_C = 1\ MHz$

Symbol	Parameter	Maximum	Condition
C_{IN}	Input Capacitance	15 pF	$V_{IN} = 0$ V
$C_{I/O}$	I/O Capacitance	15 pF	$V_{I/O} = 0$ V

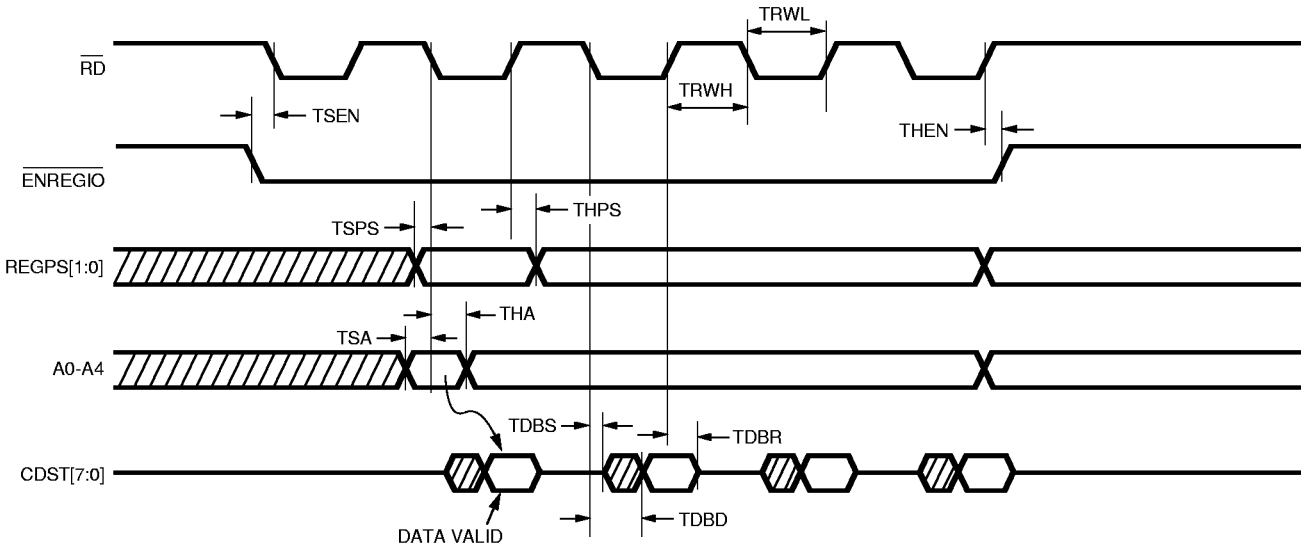
5.0 COMMAND/STATUS INTERFACE TIMING

AC Characteristics $T_A = 0°C$ to $70°C, V_{CC} = 5\ V \pm 5\%$

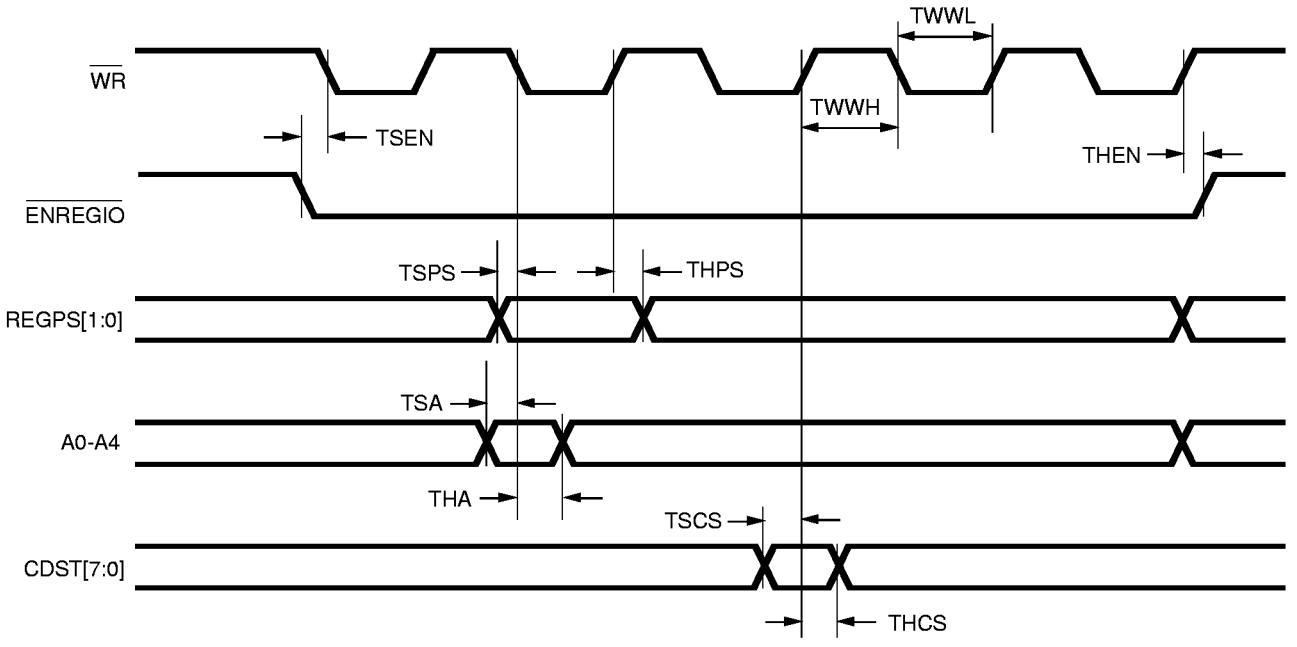
Sym	Parameter	Limits Min.	Limits Typ.	Limits Max.	Units (ns)	Condition
TDBD	Receive/Transmit Status Command Status, and Management Counters Delay	0.5RXC/TXC Cycles+10ns		1.5RXC/TXC Cycles[1] Plus50ns	ns	
	All Other Registers	10		40	ns	
TDBR	CDST [7:0] Bus Release Delay	1		10	ns	
TDBS	CDST [7:0] Bus Siezure Delay	7		35	ns	
THA	A[4:0] Hold	10			ns	
THPS	REGPS[1:0] Hold	10			ns	
THEN	$\overline{\text{ENREGIO}}$ Hold	10			ns	
THCS	CdSt Bus Hold	0			ns	
TSA	A[4:0] Setup	0			ns	
TSPS	REGPS[1:0] Setup	5			ns	
TSEN	$\overline{\text{ENREGIO}}$ Setup	5			ns	
TSCS	CdSt Bus Setup	10			ns	
TRWH	$\overline{\text{RD}}$ High Width for RX/TX Status, & Management Counters	1RXC/TXC Cycle+10ns				
	All Others	50			ns	
TRWL	$\overline{\text{RD}}$ Low Width for RX/TX Status, & Management Counters	1.5RXC/TXC Cycles[1] +60ns[2] for $\overline{\text{RD}}$ or +50ns for $\overline{\text{WR}}$			ns	
	All Others	50			ns	
TWWH	$\overline{\text{WR}}$ High Width	30			ns	
TWWL	$\overline{\text{WR}}$ Low Width	30			ns	

NOTES:
1. 2 TXC for TX Octect Counter.
2. Assuming 10 ns setup time before $\overline{\text{RD}}$ goes high.

5.01 Command/Status Interface Read Timing



5.02 Command/Status Interface Write Timing

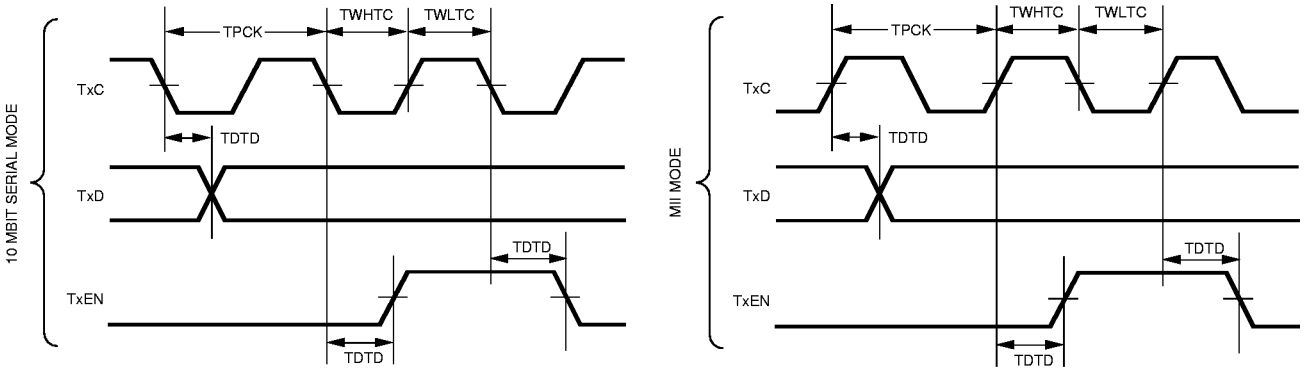


6.0 Ethernet Transmit and Receive Interface Timing

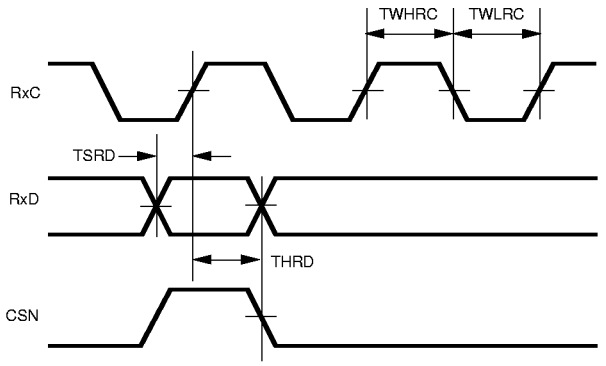
AC Characteristics T_A = 0° C to 70°C, V_{CC} = 5 V ± 5%

ETHERNET TRANSMIT INTERFACE TIMING					
		Limits			
Symbol	Parameter	Min.	Typ.	Max.	Condition
TDTD	TXD/TXEN Delay	5 ns		22 ns	
TWHTC	TXC High Width	1 TXC Cycle/2 – 5			
TWLTC	TXC Low Width	1 TXC Cycle/2 – 5			
ETHERNET RECEIVE INTERFACE TIMING					
THRD	RxD Hold	5 ns			
TSRD	RxD Setup	5 ns			
TWHRC	RxC High Width	1 RXC Cycle/2 – 5			
TWLRC	RxC Low Width	1 RXC Cycle/2 – 5			

6.01 Ethernet Transmit Interface Timing



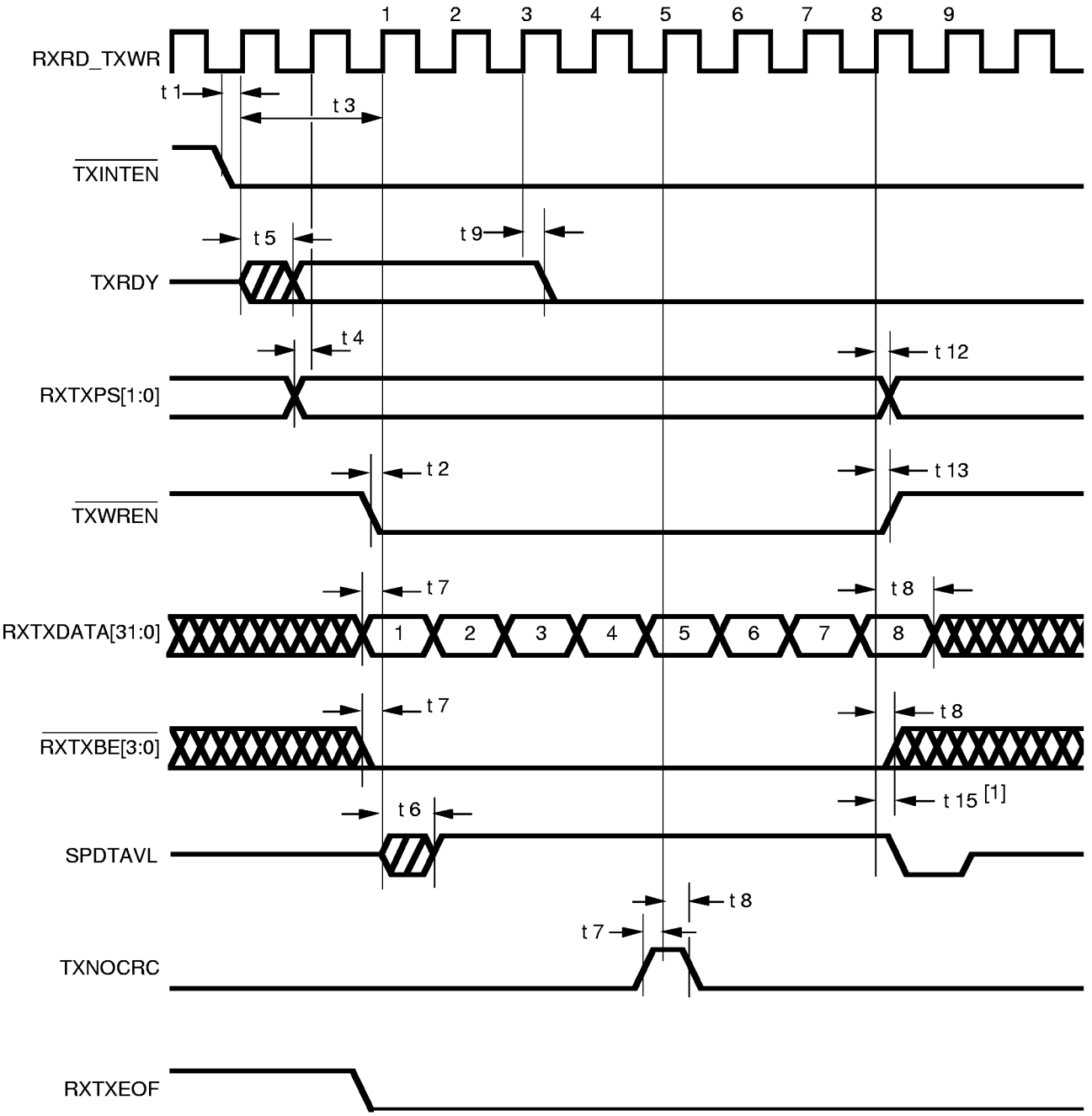
6.02 Ethernet Receive Interface Timing



7.0 Transmit Data Interface Write Timing

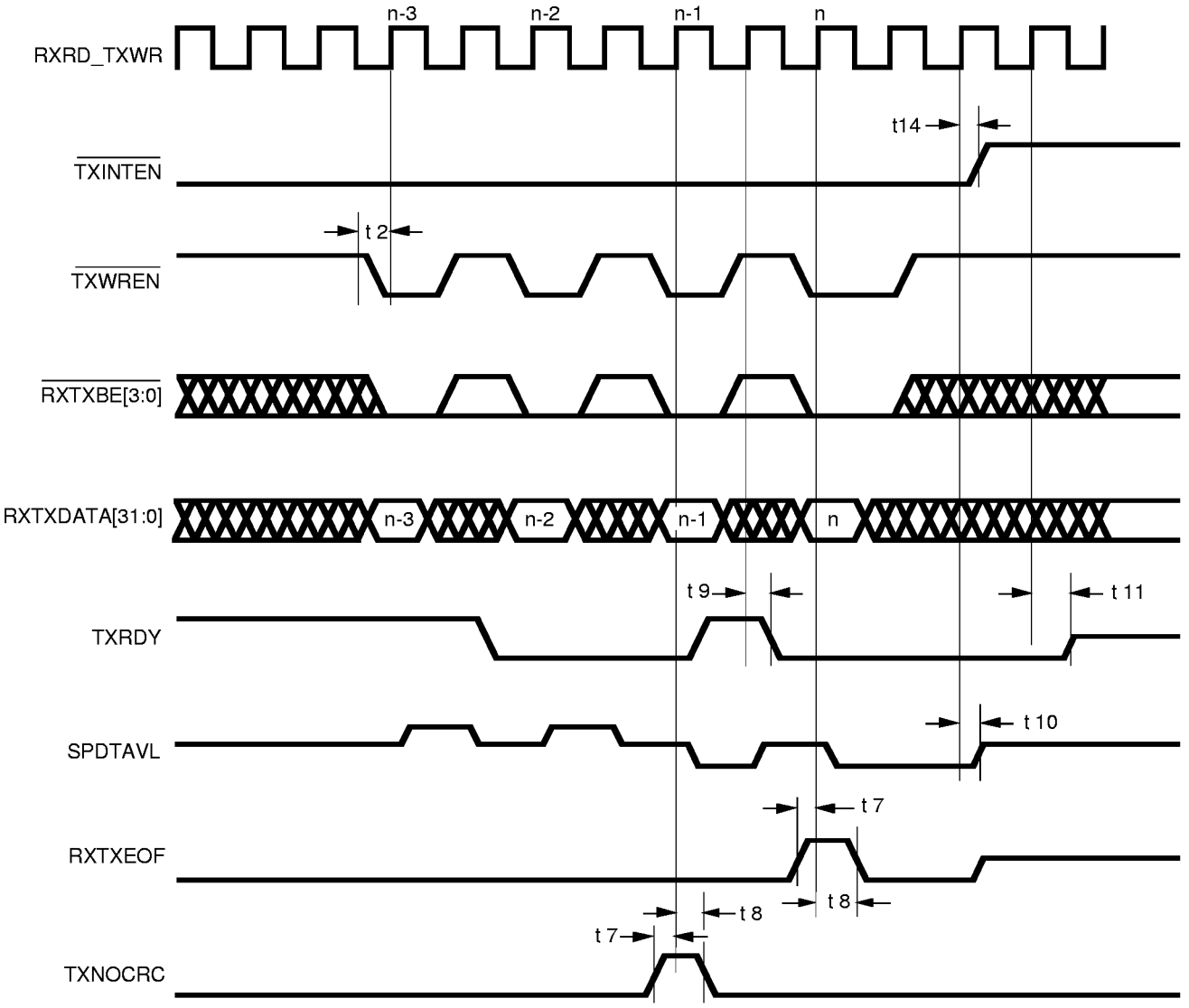
Symbol	Parameter	Min.	Typ.	Max.
t_1	Transmit Interface Enable to Clock Setup Time	5ns		
t_2	Transmit Write Enable to Clock Setup Time	5 ns		
t_3	Transmit Interface Enable to Transmit Write Enable Timing Skew	0 ns		
t_4	Port Select Inputs to Clock Setup Time	5 ns		
t_5	TXRDY Output Enabled to Output Valid Delay	3 ns		20 ns
t_6	SPDTAVL Output Enable to Output Valid Delay	3 ns		20 ns
t_7	Transmit Data, Byte Enables, TXEOF, TXNOCRC to Clock Setup Time	5 ns		
t_8	Transmit Data, Byte Enables, TXEOF, TXNOCRC Hold Time	0.5 ns		
t_9	TXRDY Deassert Due to Space Available Lower than Threshold	4 ns		22 ns
t_{10}	SPDTAVL Output Disabled to Hi-Z Delay	4 ns		20 ns
t_{11}	TXRDY Output Disabled to Hi-Z Delay	4 ns		20 ns
t_{12}	Port Select Inputs Hold Time	0 ns		
t_{13}	Transmit Write Enable Hold Time	0 ns		
t_{14}	Transmit Interface Enable Hold Time	0 ns		
t_{15}	SPDTAVL Deassert Due to Transmit FIFO Reading, an almost Empty Condition	4 ns		22 ns

7.01 Transmit Data Interface Write Timing 1



Notes: 1. SPDTAVL gets deasserted because of the 7th double word write to the transmit FIFO indicating that the 8th double word write will fill the FIFO completely. It is important to note that the data gets pipelined internally, hence the 7th external double word write (The 7th Clock Edge that latches in the active low TXWREN) actually happens on the 8th clock cycle internally.

7.02 Transmit Data Interface Write Timing 2



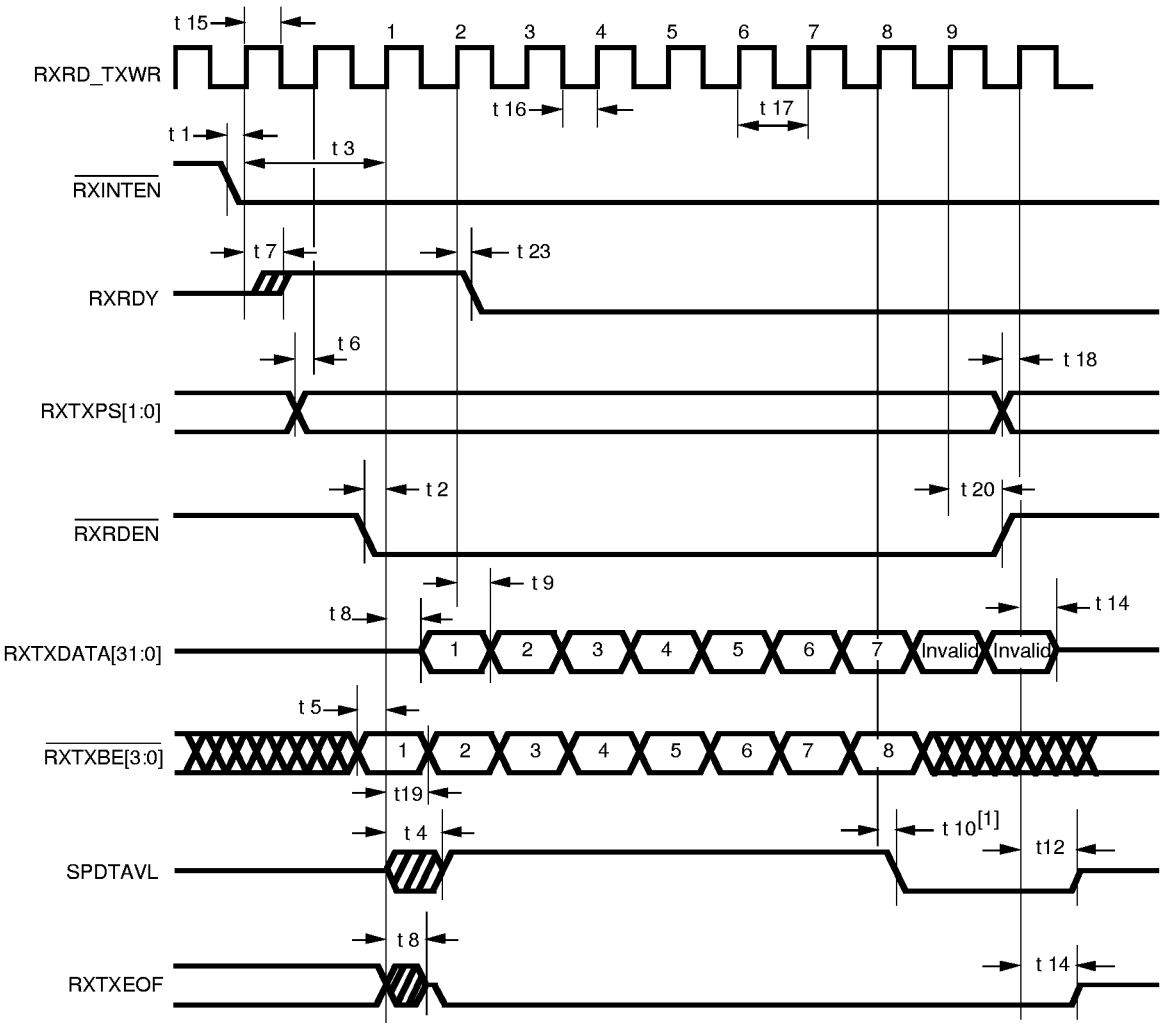
8.0 Receive Data Interface Read Timing

Symbol	Parameter	Min.	Typ.	Max.	Condition
t_1	Receive Interface Enable to Clock Setup Time	5ns			
t_2	Receive Read Enable to Clock Setup Time	5 ns			
t_3	Receive Interface Enable to Receive Read Enable Timing Skew	0 ns			
t_4	SPDTAVL Output Enabled to Output Valid Delay	5 ns		20 ns	
t_5	Receive Byte Enables to Clock Setup Time	5 ns			
t_6	Port Select Inputs to Clock Setup Time	5 ns			
t_7	RXRDY Output Enabled to Output Valid Delay	5 ns		20 ns	
t_8	RXTXDATA [31:0], RXTXEOF Outputs Enabled to Outputs Valid Delay	5 ns		24 ns	
t_9	FIFO Read Strobe High to RXTXEOF, RXTXDATA[31:0] FIFO Data Out Delay	5 ns		20 ns	
t_{10}	Clock to SPDTAVL Low Delay			22 ns	
	SPDTAVL Deassert to Assert Minimum Low Time	8 RXRD_TXWR Cycles			If Both $\overline{\text{RXDEN}}$ and $\overline{\text{RXINTEN}}$ are Asserted
t_{12}	SPDTAVL Output Disabled to Hi-Z Delay	5 ns		20 ns	
t_{13}	RXRDY Output Disabled to Hi-Z Delay	5 ns		20 ns	
t_{14}	Receive Data and RXTXEOF Outputs Disabled to Hi-Z Delay	5 ns		20 ns	
t_{15}	RXRD_TXWR Clock Pulse Width High	12 ns			
t_{16}	RXRD_TXWR Clock Pulse Width Low	12 ns			
t_{17}	RXRD_TXWR Clock Period	30 ns		125 ns	TXC/RXC = 10 MHz
		30 ns		50 ns	TXC/RXC = 25 MHz
		30 ns		500 ns	TXC/RXC = 2.5 MHz
t_{18}	Port Select Inputs Hold Time	0 ns			
t_{19}	Byte Enables Hold Time	0 ns			
t_{20}	Receive Read Enable Hold Time	0 ns			
t_{21}	Receive Interface Enable Hold Time	0 ns			

Receive Data Interface Read Timing (cont'd)

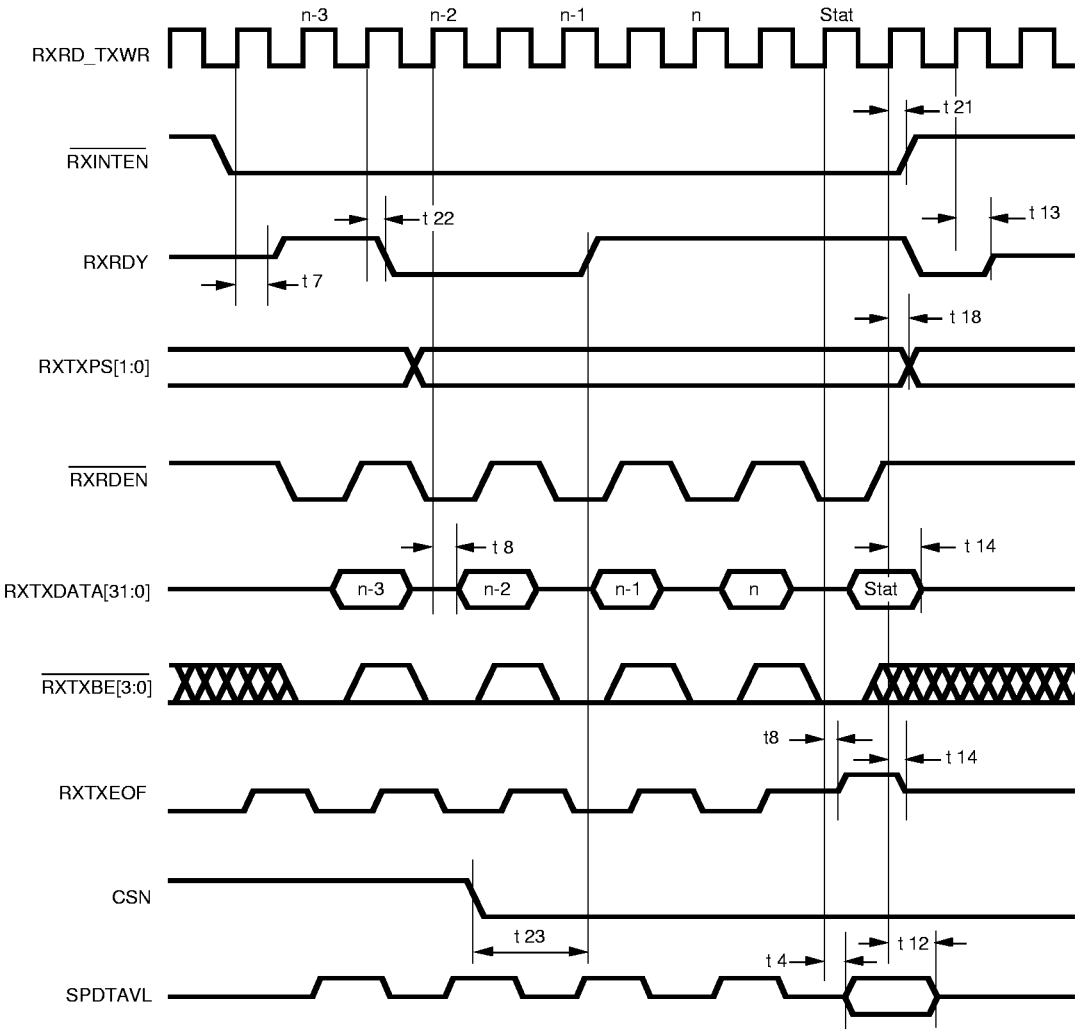
Symbol	Parameter	Min.	Typ.	Max.	Condition
t_{22}	RXRDY Deassert Due to Emptying RX FIFO Below Threshold	5 ns		20 ns	
t_{23}	RXRDY Assert from CSN Going Low Due to Status Write	9 RXC Cycles + 2.5 RXRD_TXWR Cycles + 5 ns (10MBit/secSerialMode)		17 RXC Cycles + 3.5 RXRD_TXWR Cycles + 20 ns (10MBit/secSerialMode)	
		3 RXC Cycles + 2.5 RXRD_TXWR Cycles + 5 ns (MII Mode)		5 RXC Cycles +3.5 RXRD_TXWR Cycles + 20 ns (MII Mode)	

8.01 Receive Data Interface Read Timing 1



Notes: 1. SPDTAVL gets deasserted because of the 7th double word read from the receive FIFO indicating that there is no more data available in the receive FIFO and further reads will cause invalid reads. Here, it is important to note that the 7th read is referred to the 7th clock edge that latches in the active low RXRDEN and the resultant data can be latched out on the 8th clock edge because of the pipelining effect.

8.02 Receive Data Interface Read Timing 2



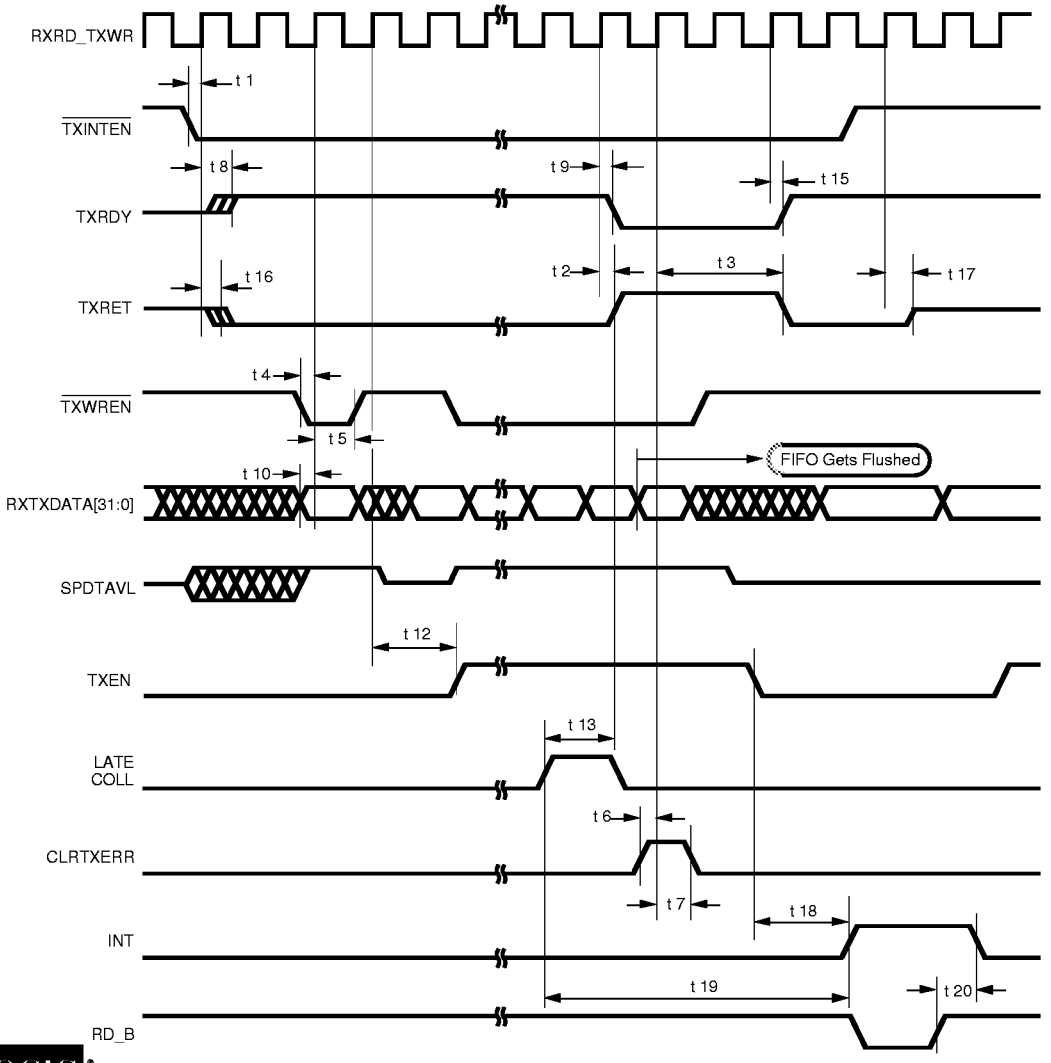
9.0 Transmit Data Interface Timing on Exception Conditions

Symbol	Parameter	Min.	Typ.	Max.
t_1	TXINTEN Setup Time	5 ns		
t_2	RXRD_TXWR to TXRET Delay	5 ns		22 ns
t_3	TXRET Deassert from CLRTXERR	1 TXC Cycle + 1 RXRD_TXWR Cycle + 5 ns		2 TXC Cycles + 2 RXRD_TXWR Cycles + 25 ns
t_4	TXWREN Setup Time	5 ns		
t_5	TXWREN Hold Time	0 ns		
t_6	CLRTXERR Setup Time	5 ns		
t_7	CLRTXERR Hold Time	0 ns		
t_8	TXRDY Output Enabled to Output Valid Delay	3 ns		20 ns
t_9	TXRDY Deassert Due to TXRET Going HIGH Because of an Exception Condition	3 ns		1 RXRD_TXWR Cycle + 22 ns
t_{10}	RXTXDATA Setup Time	5 ns		
t_{12}	TXEN Assert from First Data Write to the Transmit FIFO (Assuming Defer Time Has Been Met)	0.75 RXRD_TXWR Cycles + 18.5 TXC Cycles + 5 ns (10 Mbit/sec Serial Mode)		0.75 RXRD_TXWR Cycles + 26.5 TXC Cycles + 22 ns (10 Mbit/sec Serial Mode)
		0.75 RXRD_TXWR Cycles + 6.5 TXC Cycles + 5 ns (MII Mode)		0.75 RXRD_TXWR Cycles + 8.5 TXC Cycles + 22 ns (MII Mode)
t_{13}	TXRET Set Delay Due to Late Collision or 16 Collisions	25 TXC Cycles + 1 RXRD_TXWR Cycle + 5 ns (10 Mbit/sec Serial Mode)		34 TXC Cycles +2 RXRD_TXWR Cycles + 22 ns (10Mbit/sec Serial Mode)
		7 TXC Cycles + 1 RXRD_TXWR Cycle + 5 ns (MII Mode)		10 TXC Cycles + 2 RXRD_TXWR Cycles + 22 ns (MII Mode)
	TXRET Set Due to Underflow	8 TXC Cycles + 1 RXRD_TXWR Cycle + 5 ns (10 Mbit/sec Serial Mode)		8 TXC Cycles + 2 RXRD_TXWR Cycles + 22 ns (10 Mbit/sec Serial Mode)
		2 TXC Cycles + 1 RXRD_TXWR Cycle + 5 ns (MII Mode)		2 TXC Cycles + 2 RXRD_TXWR Cycles + 22 ns (MII Mode)
t_{15}	TXRDY Going HIGH Due to TXRET Going Low	5 ns		22 ns
t_{16}	TXRET Output Enabled to Output Valid Delay	5 ns		22 ns
t_{17}	TXRET Output Disabled to Hi-Z Delay	3 ns		12 ns

9.0 Transmit Data Interface Timing on Exception Conditions (continued)

Symbol	Parameter	Min.	Typ.	Max.
t_{18}	INT High to TXEN Low Delay Due to Underflow	1 TXC Cycle + 8 ns		1 TXC Cycle + 32 ns
	TXEN Low to INT HIGH Delay Due to Carrier Sense Dropout	3 TXC Cycles + 8 ns		3 TXC Cycles + 32 ns
	TXEN Low to INT High Delay Due to Successful Transmission	1 TXC Cycle + 8 ns		1 TXC Cycle + 32 ns
t_{19}	COLL High to INT High Delay	20 TXC Cycles + 8 ns (10 Mbit/sec Serial Mode)		27 TXC Cycles + 32 ns (10 MBit/sec Serial Mode)
		8 TXC Cycles + 8 ns (MII Mode)		9 TXC Cycles + 32 ns (MII Mode)
t_{20}	INT Clear Delay	1.5 TXC Cycles + 10 ns		2.5 TXC Cylces + 40 ns

9.01 Transmit Data Interface Timing on Exception Conditions

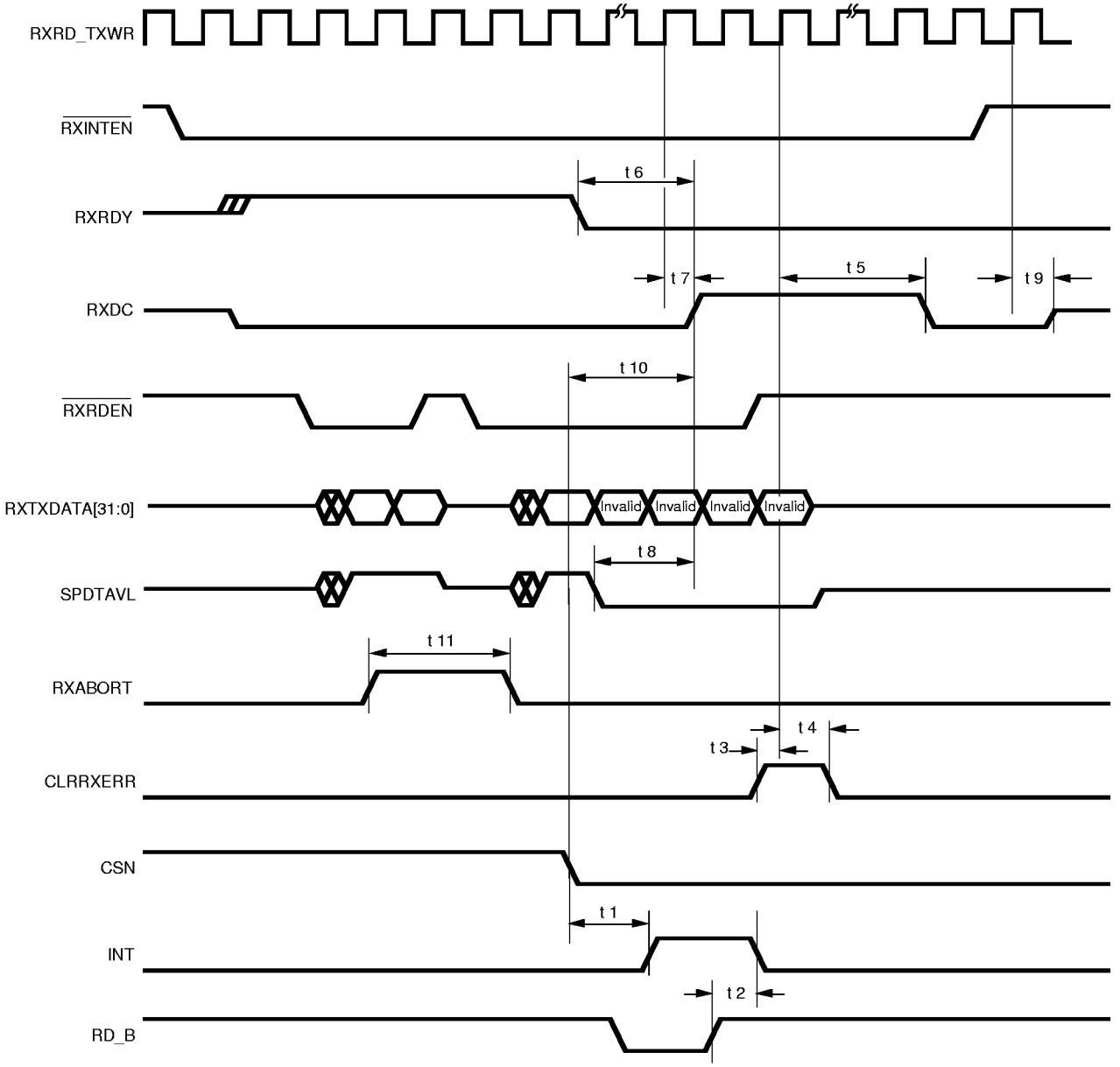


10.0 Receive Data Interface Timing on Exception Conditions

Symbol	Parameter	Min.	Typ.	Max.	Condition
t_1	Receive INT Delay Due to Shortframe, CRC, Good Frame, or Oversized Packet	2 RXC Cycles + 5 ns		2 RXC Cycles + 32 ns	
	Receive INT Delay Due to Overflowed Packet	2 RXC Cycles + 5 ns		18 RXC Cycles + 32 ns	
t_2	INT Clear Delay	1.5 RXC Cycles + 10 ns		2.5 RXC Cycles + 40 ns	
t_3	CLRRXERR Setup Time to RXRD_TXWR	4 ns			
t_4	CLRRXERR to RXRD_TXWR Hold Time	1 ns			
t_5	CLRRXERR High to RXDC Low Delay	1 RXC Cycle + 3 RXRD_TXWR Cycles + 5 ns		2 RXC Cycles + 4 RXRD_TXWR Cycles + 25 ns	
t_6	RXRDY Deassert Due to Discard to RXDC High Delay	5 ns		1 RXRD_TXWR Cycle + 11 ns	
t_7	RXRD_TXWR to RXDC Delay	5 ns		30 ns	
t_8	SPDTAVL Deassert Due to Discard to RXDC High Delay	5 ns		1 RXRD_TXWR Cycle + 13 ns	
t_9	RXRD_TXWR to RXDC Hi-Z	5 ns		25 ns	
t_{10}	CSN Deassert to RXDC High Due to Receive Overflow Condition	2 RXC Cycles + 3 RXRD_TXWR Cycles + 5 ns (10MBit/sec Serial Mode)		18 RXC Cycles + 4 RXRD_TXWR Cycles + 30 ns (10MBit/sec Serial Mode)	
		2 RXC Cycles + 3 RXRD_TXWR Cycles + 5 ns (MII Mode)		6 RXC Cycles + 4 RXRD_TXWR Cycles + 30 ns (MII Mode)	
t_{10a}*	RXDC High From Point of Detection of Receive Packet with Greater than 1518 Bytes	2 RXC Cycles + 3 RXRD_TXWR Cycles + 5 ns		2 RXC Cycles + 4 RXRD_TXWR Cycles + 30 ns	
t_{11}	RXABORT Pulse Width	1.5 RXC			RXABORT is Asynchronously Asserted with Respect to RXC
	RXABORT to RXC Setup Time	5 ns			RXABORT is Synchronously Asserted with Respect to RXC
	RXC to RXABORT Hold Time	5 ns			

* Not shown on the timing diagram.

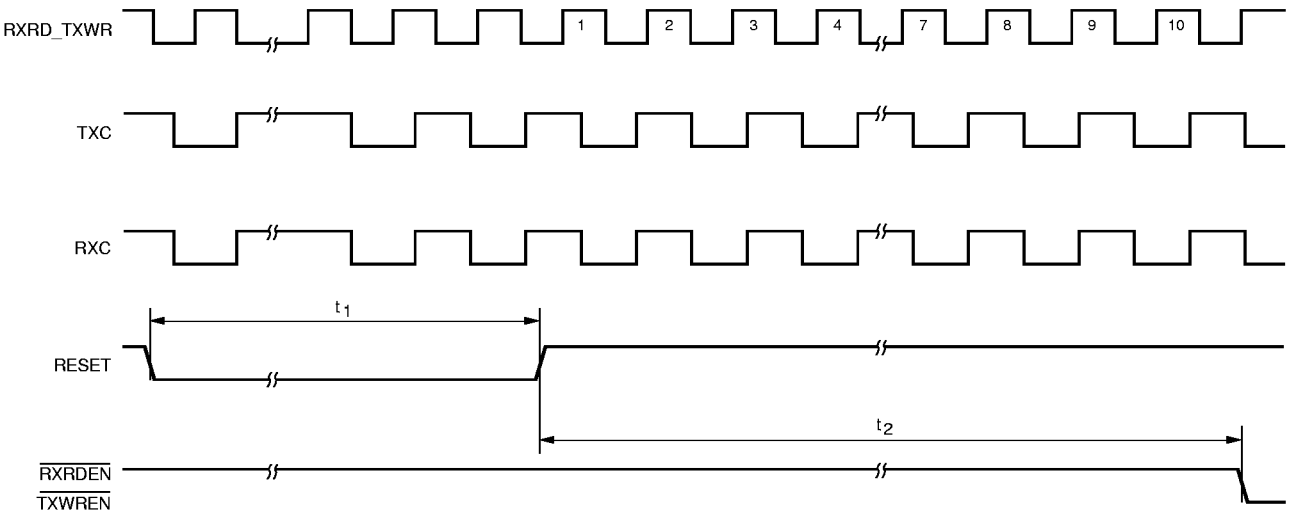
10.01 Receive Data Timing Diagram on Exception Conditions



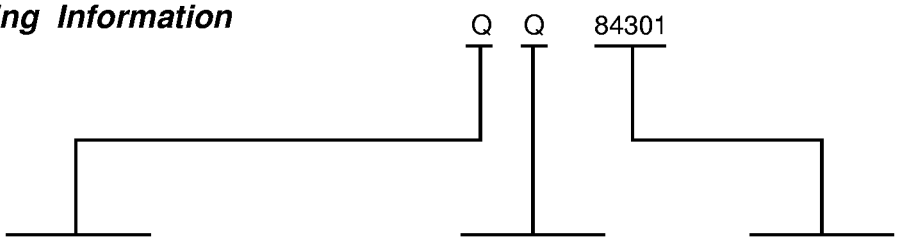
11.0 Reset Timing

Symbol	Parameter	Min.	Typ.	Max.	Condition
t_1	Asynchronous Reset Pulse Width	10 µs			All clocks must be active during this peroid of time
t_2	Reset Completion to Normal Operation Delay	10 RXDR_TXWR Cycles			

11.0 Reset Timing

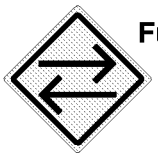


Ordering Information



SEEQ Hurricane, Full Duplex Designation

SEEQ's Hurricane family of products offer 100MBit Fast Ethernet Solutions. Symbol indentifies product as a part of SEEQ's Hurricane family.



Full Duplex

Symbol indentifies product as Full Duplex device.

Revision History

9/3/96: Initial release.

9/3/96

Page 53: The dimension diagram on this page has changed, for complete details call SEEQ Technology, (510) 226-7400 ext. 3051.

2/14/97

- 2/14/97 Document revision changed to MD400158/B

Page 2: Table of Contents

- 3.6.1 Internal Channel Register Addressing Table has been changed to Internal Port Register Addressing Table.
- 3.6.11 Full Duplex Status Register has been added.
- 5.01 and 5.02 Command/Status Interface Read and Write Timing have been added.
- 6.01 and 6.02 Ethernet Transmit and Receive Interface Timing have been added.
- 7.0 Receive Interface Timing has been changed to Transmit Data Interface Timing.
- 7.01 and 7.02 Transmit Data Interface Write Timing 1 and 2 have been added.
- 8.0 Transmit Data Interface Timing has been changed to Receive Data Interface Timing.
- 8.01 and 8.02 Receive Data Interface Read Timing 1 and 2 have been added.
- 9.0 Receive Data Interface Timing has been changed to Transmit Data Interface Timing on Exception Conditions.
- 10.0 Receive Data Interface Timing on Exception Conditions has been added.

Revision History

Page 3: 1.0 Pin Description
- Description, Register Select Address, ...A4 (206) has an internal ... has been changed to ...A3 (153) and A4 (206) each has an internal pull down...

Page 5: 1.0 Pin Description (cont.)
- Description, Receive/Transmit Data, Pins 96-101, 107-112 have been added.
- Description, Receive/Transmit Data, ...This is the bidirectional data bus for reads or writes to the chip's receive and transmit FIFO's... has been changed to ...This is the bidirectional data bus for reads from the receive FIFO or writes to, the transmit FIFO of the chip...

Page 11: Figure 1. Individual Functional Block Diagram
- Reference to RXINTEN has been changed to $\overline{\text{RXINTEN}}$, reference to TXINTEN has been changed to $\overline{\text{TXINTEN}}$, reference to $\overline{\text{RXRD}}$ has been changed to $\overline{\text{RXRD\_TXWR}}$.

Page 14: Section 3.2.2 Transmission Initiation/Deferral has been changed to 3.2.2 Transmission Initiation in Full Duplex and CSMA/CA Networks and this section 3.2.2 has been replace with new copy.

Page 18: Beginning on page 18 a pagination change has occurred, from pages 18 to the rest of the document.

Page 18: Conditions that cause the RXDC pin to go HIGH
- "Description of How Receive Packets are Discarded", has been changed to "3.3.5 Receive Discard Conditions".

Page 21: 3.5.2 Transmit FIFO Interface
- Paragraph 5, ... one more write after... has been changed to ...one more internal FIFO write after...

Page 22: 3.5.3 Receive FIFO Interface
- Paragraph 6, When the chip is used ... has been added.
- Paragraph 9, ...high going edge of the read... has been changed to ...high going edge of the $\overline{\text{RXRD\_TXWR}}$ of the read...
- Paragraph 10, ...In the case of SPDTAVL being driven low upon the high going edge of the read that meets one of the above conditions, the SPDTAVL... has been changed to ...When one of the above conditions is met and SPDTAVL is driven low upon the high going edge of the $\overline{\text{RXRD\_TXWR}}$, the SPDTAVL...
- 3.6.1 Internal Channel Register Addressing Table has been changed to Internal Port Register Addressing Table.

Page 23: 2.0 Port Register Addressing Table, has been changed to 3.6.1 Internal Port Addressing Table.

Page 24: 2.0 Port Register Addressing Table (continued), has been changed to 3.6.1 Internal Port Addressing Table (continued).

Page 25: 3.6.3 Transmit Command Register
- Paragraph 2, "Clearing Interrupts" has been changed to "Clearing Interrupts" in section 3.3.5.
- Transmit Command Register Format
  - Note ...Please refer to the mode port/select table for details... has been changed to ...Please refer to "3.6.1 Internal Port Register Addressing Table" for details...

Page 27: Receive Command Register Format
- Note, ...*This register can be used as a write only or a Read/Write register by configuring the address input accordingly. Please refer to "3.6.1 Internal Port Register Addressing Table" for details... has been added.

Page 30: Full Duplex/Half Duplex Modes Operation with Receive Own Transmit Disable. TABLE A
- Loopback Mode, and Reserved Functional Description have been added to this table.
- Note: There is no internal loopback within the MAC . Loopback is dependent on a PHY connected to the MAC, has been added.
- Mode F: Full Duplex Mode, ...(pin #108)... has been changed to ...(pin #123, 124, 125, or 127)...
- Mode F, Note: ...Please refer to Mode D for details... has been changed to ...Please refer to Table A for details...

Page 31: - Mode C: EOF on Data Bit 2 has changed to Mode C: EOF on Data.
- Configuration Register #2, Bit 5 row has changed.
- Note 3. This bit address is shared for two functions, and Note 4. Read will clear this bit to '0', have been added.

Revision History

Page 32: - Mode E: Receive Without Discard Mode has been added.
- Mode F1/F2, Last paragraph, ...Mode F2: Reading this bit provides SQE status. The SQE function is always on; reading this register causes an automatic reset of this bit value... has been changed to ...Mode F2: Reading this bit provides SQE test result. The SQE function is always on; reading this register causes an automatic reset of this bit value to "zero".

Page 34: - 3.6.6.1 FIFO Threshold Register Setting Table has been changed to 3.6.8.1 FIFO Threshold Register Setting Table.

Page 36: - 3.6.11 Full Duplex Status Register has been added.
- Note 1. ...(See Section 3.1) has been changed to (See Section 3.6.7).

Page 42: - Absolute Maximum Ratings
- A new Absolute Maximum Ratings has been added, and Operating Conditions has been deleted.
- 4.0 DC Characteristics
- V_{CH} Limits (Min) has been changed from 4.0 to 2.4.
- V_{CH} Limits (Max) has been deleted.
- V_{CL} Limits (Max) has been changed from 1.0 to 0.6.
- V_{IH1} Limits (Max) has been deleted.

Page 43: AC Characteristics
- Symbol, THAR has changed to THA, THRS has changed to THPS, THDA has changed to THCS, TSAR has changed to TSA, TSRS has changed to TSPS, TWCH has changed to TRWH, TWCL has changed to TRWL.
- All Conditions have been deleted.
- Symbols, THEN, TSEN, TWWH and TWWL have been added.
- THPS, Parameter REGPS[1:0]/ENREGIO Hold has been changed to REGPS[1:0] Hold.
- TSPS, Parameter REGPS[1:0]/ENREGIO Setup has been changed to REGPS[1:0] Setup.
- TRWH, Parameter reference to $\overline{RD}/\overline{WR}$ has been changed $\overline{RD}$.
- TRWL, Parameter reference to $\overline{RD}/\overline{WR}$ has been changed $\overline{RD}$.

Page 44: - Figures 5.01 Command/Status Interface Read Timing, and 5.02 Command/Status Interface Write Timing have replaced Figure 5.0 Command Status Interface Timing.

Page 45: - Figures 6.01 Ethernet Transmit Interface Timing and 6.02 Ethernet Receive Interface Timing have replaced Figures 6.0 Ethernet Transmit Interface Timing, and 7.0 Receive Interface Timing.
- 6.0 Ethernet Transmit and Receive Interface Timing has replaced AC Characteristics Ethernet Transmit Interface Timing, and AC Characteristics Receive Interface Timing.

Page 46: - 7.0 Transmit Data Interface Timing Table has replaced Transmit Data Interface Timing Table.

Page 47: - Figure, 7.01 Transmit Data Interface Write Timing 1 has been added, and replaces Figure 8.0 Transmit Data Interface Timing.

Page 48: - Figure, 7.02 Transmit Data Interface Write Timing 2 has been added, and replaces Figure 8.0 Transmit Data Interface Timing.

Page 49: - 8.0 Receive Data Interface Timing has been added and replaces Receive Data Interface Timing.

Page 50: - Figure 8.01 Receive Data Interface Timing 1, has been added, and replaces Figure 9.0 Receive Data Interface Timing.

Page 51: - Figure 8.02 Receive Data Interface Timing 2, has been added, and replaces Figure 9.0 Receive Data Interface Timing.

Page 52: - 9.0 Transmit Data Interface Timing on Exception Conditions has been added.

Page 53: - Figure 9.01 Transmit Data Interface Timing on Exception Conditions has been added.

Page 54: - 10.0 receive Data Interface Timing on Exception Conditions has been added.

Page 55: - Receive Data Timing Diagram on Exception Conditions has been added.

Revision History

Page 57: 208 Pin PQFP Dimension Diagram
- Reference to 4.25 Max. has changed to 4.10 Max.
- Reference to 3.75 ± 0.10 has changed to 3.40 ± 0.20.
- Reference to 0.25 - 0.40 has changed to 0.25 Min.

4/9/97:

- Latest version MD400158/C

- All references to $\overline{\text{RXRD\_TXWR}}$, have been changed to RXRD_TXWR.

Page 3: - Pin 4, Description, reference to A[2:0] has been changed to A[4:0], reference to $\overline{\text{REGPS[1:0]}}$ has been changed to REGPS[1:0].
- Pin 5, Description, reference to A[2:0] has been changed to A[4:0], reference to $\overline{\text{REGPS[1:0]}}$ has been changed to REGPS[1:0].
- Pin 21,20, Pin Name, $\overline{\text{REGPS[1:0]}}$ has been changed to REGPS[1:0].
- Pin 21,20, Description, $\overline{\text{REGPS1}}$ has been changed to REGPS1, also REGPS1, REGPS0 , Selected Port, Table has been added.
- Pin 49, Description, This input is an... copy has been changed to... This input is an active low asynchronous chip reset. After reset, all registers except the Hash and Station Address registers are reset to zero, all FIFOs are cleared, all counters are reset to zero.

Page 4: - Pin 30,29, Description, Table RXTXPS[1:0] has been added.

Page 12: - Pagination change has occurred.

Page 15: - End of Section 3.2.1 Controlling Transmit Packet Encapsulation, Table Transmit No CRC has been added, also paragraph Please note that both ... has been added.

Page 19: - Section 3.3.4 Using the RXABORT Pins to Terminate Reception of a Packet, paragraph one, By pulsing the corresponding... copy has changed to ...By pulsing the corresponding RXABORT pin high for a minimum of 1 RXC cycle any time during the reception of a packet, that particular port's packet reception can be terminated.

Page 24: - 3.6.1 Internal Port Register Addressing Table, Reference to Short Frame Counter, has been changed to Runt Frame Counter.

Page 35: - Section 3.6.9 Defer Register Calculations for the 84301, last paragraph The defer time is split... has been added.

Page 45: - 5.01 Command/Status Interface Read Timing, Reference to A0-A3 has been changed to A0-A4.
- 5.02 Command/Status Interface Write Timing, Reference to A0-A3 has been changed to A0-A4.

Page 47: - 7.0 Transmit Data Interface Write Timing
- t_8 (min) 0 ns has been changed to 0.5 ns.

Page 48: - 7.01 Transmit Data Interface Write Timing 1
- Timing TXNOCRC, has been changed.

Page 49: - 7.01 Transmit Data Interface Write Timing 2
- Timing TXNOCRC, has been changed.

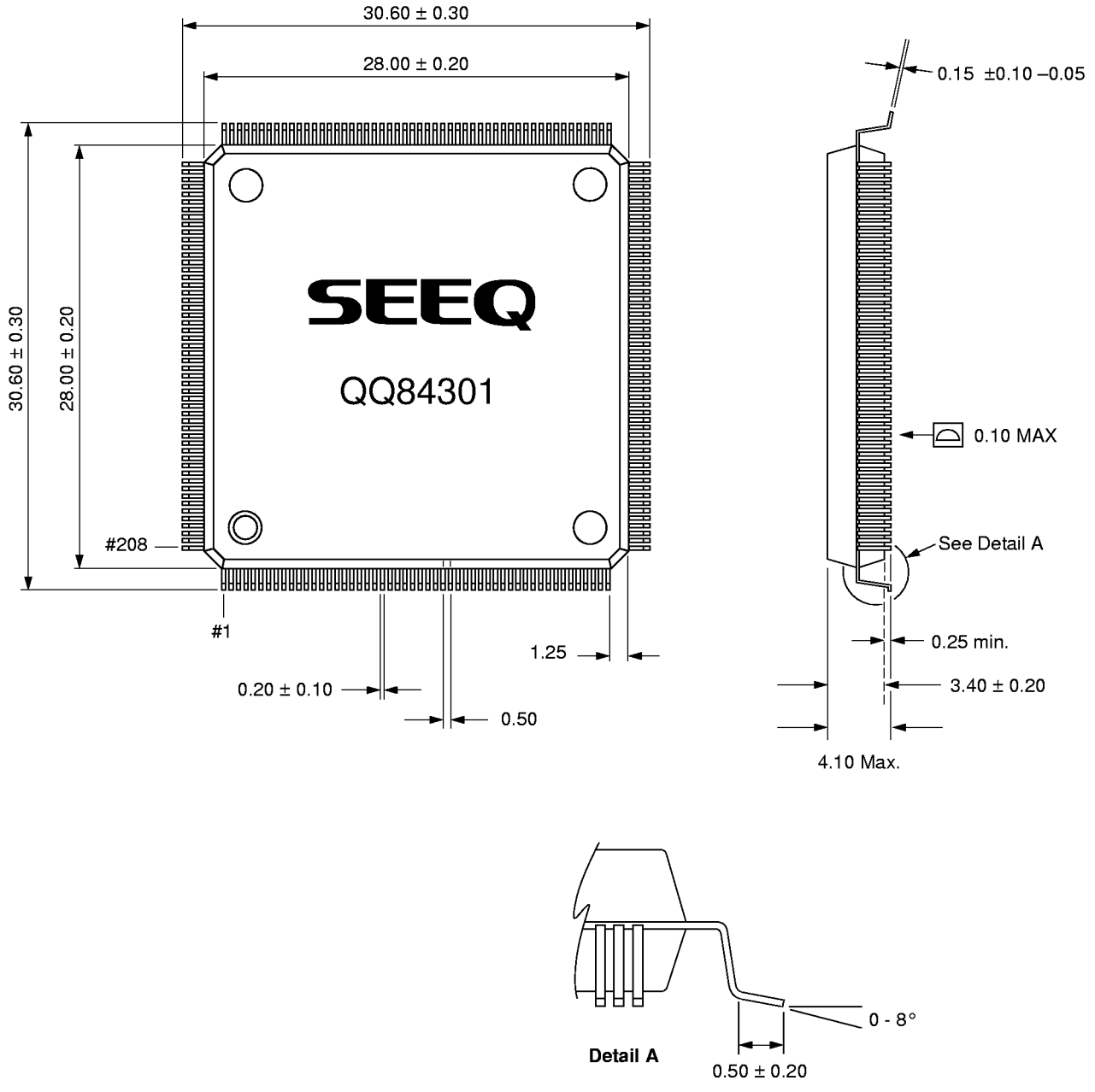
3/20/98:

- Latest version MD400158/D

Page 2 - Table of Contents Reference to 11.0 Reset Timing added.

Page 57 - 11.0 Reset Timing Table and Timing Diagram added.

208 Pin PQFP



1. **All dimensions are in (millimeters).**