XILINX

XC4000
Logic Cell™ Array Family

Product Description, December 1991

FEATURES

- Third Generation Field-Programmable Gate Array
  - Abundant flip-flops
  - Flexible function generators
  - On-chip ultra-fast RAM
  - Dedicated high-speed carry propagation circuit
  - Fast, wide decoders
  - Efficient implementation of multi-level logic
  - Hierarchy of interconnect lines
  - Internal 3-state bus capability
- Flexible Array Architecture
  - Programmable logic blocks and I/O blocks
  - Programmable interconnects and wide decoders
- Sub-micron CMOS Process
  - High-speed logic and Interconnect
  - Low power consumption
- Systems-Oriented Features
  - Programmable output slew rate
  - Programmable input pull-up or pull-down resistors
  - 12-mA sink current per output
  - 24-mA sink current per output pair
- Configured by Loading Binary File
  - Unlimited re-programmability
  - Six programming modes
- XACT™ Development System runs on '386/'486-type PC and on Apollo, Sun-3/4, and DECstation 3100
  - Interfaces to popular design environments like FutureNet, Viewlogic, Mentor Graphics and OrCAD
  - Fully automatic partitioning, placement and routing
  - Interactive design editor for design optimization
  - 276 macros, 36 hard macros, RAM/ROM compiler

DESCRIPTION

The XC4000 family of Field-Programmable Gate Arrays (FPGAs) provides the benefits of custom CMOS VLSI, while avoiding the initial cost, time delay, and inherent risk of a conventional masked gate array.

The result of experience gained with two successful previous FPGA families (XC2000 and XC3000), the XC4000 family provides a regular, flexible, programmable architecture of Configurable Logic Blocks (CLBs), interconnected by a powerful hierarchy of versatile and abundant routing resources, and surrounded by a perimeter of programmable Input/Output Blocks (IOBs).

The devices are customized by loading configuration data into the internal memory cells. The FPGA can either actively read its configuration data out of external serial or byte-parallel PROM (master modes), or the configuration data can be written into the FPGA (slave and peripheral modes).

The XC4000 family is supported by powerful and sophisticated software, covering every aspect of design: from schematic entry, to simulation, to automatic block placement and routing of interconnects, and finally the creation of the configuration bit stream.

Since Xilinx FPGAs can be re-programmed an unlimited number of times, they can be used in innovative designs where hardware is changed dynamically, or where hardware must be adapted to different user applications.

FPGAs are ideal for shortening the design and development cycle, but they also offer a cost-effective solution for production rates well beyond 1000 systems per month.

Device:	XC4002	4003	4004	4005	4006	4008	4010	4013	4016	4020
Appr. Gate Count:	2,000	3,000	4,000	5,000	6,000	8,000	10,000	13,000	16,000	20,000
CLB Matrix:	8 x 8	10 x 10	12 x 12	14 x 14	16 x 16	18 x 18	20 x 20	24 x 24	26 x 26	30 x 30
Number of CLBs:	64	100	144	196	256	324	400	576	676	900
Number of Flip-Flops:	256	360	480	616	768	936	1120	1536	1768	2280
Max RAM Bits:	2,048	3,200	4,608	6,272	8,192	10,368	12,800	18,432	21,632	28,800
Number of IOBs	64	80	96	112	128	144	160	192	208	240

Table 1. The XC4000 Family of Field-Programmable Gate Arrays

XC4000 Compared to XC3000

For those readers already familiar with the XC3000 family of Xilinx Field Programmable Gate Arrays, here is a concise list of the major new features in the XC4000 family.

CLB has two **independent** 4-input function generators.
A **third** function generator combines the outputs of the two other function generators with a ninth input.
All function inputs are swappable, all have full access; none are mutually exclusive.
CLB has **very fast arithmetic carry** capability.
CLB function generator look-up table can also be used as high-speed **RAM.**
CLB flip-flops have asynchronous set **or** reset.
CLB has **four outputs**, two flip-flops, two combinatorial.
CLB connections symmetrically located on all **four** edges.

IOB has more versatile clocking polarity options.
IOB has programmable input set-up time:
long to avoid potential hold time problems,
short to improve performance.
IOB has Long Line access through its own TBUF.
Outputs are **n-channel only**, lower V_{OH} increases speed, outputs do not clamp to Vcc.
Outputs can be paired to double sink current to **24 mA.**

IEEE 1149.1- type **boundary scan** is supported in the I/O.

Wide decoders on all four edges of the LCA.

Increased **number of interconnect resources.**
All CLB inputs and outputs have **access to most interconnect lines.**
Switch Matrices are simplified to increase speed.
Eight global nets can be used for clocking or distributing logic signals.
TBUF output configuration is more versatile and 3-state control less confined.

Program is single-function input pin,overrides everything.
INIT pin also acts as Configuration Error output.

Peripheral Synchronous Mode (8 bit) has been added.
Peripheral Asynchronous Mode has improved handshake.
Start-up can be **synchronized** to any user clock (this is a configuration option).
No Powerdown, but instead a **Global 3-state input** that does not reset any flip-flops.
No on-chip **crystal oscillator** amplifier.

Configuration Bit Stream includes **CRC error checking.**
Configuration Clock can be increased to **>8 MHz.**
Configuration Clock is **fully static**, no constraint on the maximum Low time.

Readback either ignores flip-flop content (avoids need for masking) or it takes a **snapshot** of all flip-flops at the start of Readback.
Readback has same **polarity** as Configuration and can be **aborted.**

Parameter	XC4000	XC3000	XC2000
Max number of flip-flops	2280	928	174
Max number of user I/O	240	144	74
Max number of RAM bits	28,800	0	0
Function generators per CLB	3	2	2
Number of logic inputs per CLB	9	5	4
Number of logic outputs per CLB	4	2	2
Number of low-skew global nets	8	2	2
Dedicated decoders	yes	no	no
Fast carry logic	yes	no	no
Internal 3-state drivers	yes	yes	no
Output slew-rate control	yes	yes	no
Power-down option	no	yes	yes
Crystal oscillator circuit	no	yes	yes

Table 2. Three Generations of Xilinx Field-Programmable Gate Array Families

ARCHITECTURAL OVERVIEW

The XC4000 family achieves high speed through advanced semiconductor technology and through improved architecture, and supports system clock rates of 60 to 70 MHz. Compared to older Xilinx FPGA families, the new family is more powerful, offering on-chip RAM and wide-input decoders. It is more versatile in its applications, and design cycles are faster due to a combination of increased routing resources and more sophisticated software. And last, but not least, it more than doubles the available complexity, up to the 20,000-gate level.

The family will have 10 members, ranging in complexity from 2,000 to 20,000 gates.

Logic Cell Array Families

Xilinx high-density user-programmable gate arrays comprise three major configurable elements: configurable logic blocks (CLBs), input/output blocks (IOBs), and interconnections. The CLBs provide the functional elements for constructing the user's logic. The IOBs provide the interface between the package pins and internal signal lines. The programmable interconnect resources provide routing paths to connect the inputs and outputs of the CLBs and IOBs onto the appropriate networks. Customized configuration is established by programming internal static memory cells that determine the logic functions and interconnections implemented in the LCA device.

The first generation of LCA devices, introduced in 1985, features logic blocks consisting of a combinatorial function generator capable of implementing 4-input Boolean functions and a single storage element. The XC2000 family has two members ranging in complexity from 1200 to 1800 gates.

In the second-generation LCA devices, introduced in 1987, the logic block was expanded to implement wider Boolean functions and to incorporate a second flip-flop in each logic block. The XC3000 family has five members, ranging in complexity from 1200 to 5000 usable gates. The XC3000 family has a maximum guaranteed toggle frequency of up to 125 MHz, equivalent to maximum system clock frequencies of 30 to 40 MHz.

The third generation of LCA devices further extends this architecture with a yet more powerful and flexible logic block. I/O block functions and interconnection options have also been enhanced with each successive generation, further extending the range of applications that can be implemented with an LCA device.

This third-generation architecture forms the basis of the XC4000 family of devices that features logic densities up to 20,000 usable gates and supports system clock rates of up to 60 to 70 MHz, about twice the system speed and density of previous FPGA generations. The use of an advanced, sub-micron CMOS process technology as well as architectural improvements contribute to this increase in FPGA capabilities. However, achieving these high logic-density and performance levels also requires new and more powerful automated design tools. IC and software engineers collaborated during the definition of the third-generation LCA architecture to meet an important performance goal — an FPGA architecture and companion design tools for completely automatic placement and routing of 95% of all designs, plus a convenient way to complete the remaining few designs.

Configurable Logic Blocks

A number of architectural improvements contribute to the XC4000 family's increased logic density and performance levels. The most important one is a more powerful and flexible CLB surrounded by a versatile set of routing resources, resulting in more "effective gates per CLB." The principal CLB elements are shown in Figure 1. Each new CLB also packs a pair of flip-flops and two independent 4-input function generators. The two function generators offer designers plenty of flexibility because most combinatorial logic functions need less than four inputs. Consequently, the design-software tools can deal with each function generator independently, thus improving cell usage.

Thirteen CLB inputs and four CLB outputs provide access to the function generators and flip-flops. More than double the number available on the XC3000 family, these inputs and outputs connect to the programmable interconnect resources outside the block. Four independent inputs are provided to each of two function generators (F1 - F4 and G1 - G4). These function generators, whose outputs are labeled F' and G', are each capable of implementing any arbitrarily defined Boolean function of their four inputs. The function generators are implemented as memory look-up tables; therefore, the propagation delay is independent of the function being implemented. A third function generator, labeled H', can implement any Boolean function of its three inputs: F' and G' and a third input from outside the block (H1). Signals from the function generators can exit the CLB on two outputs; F' or H' can be connected to the X output, and G' or H' can be connected to the Y output. Thus, a CLB can be used to implement any two independent functions of up-to-four variables, or any single function of five variables, or any function of four variables together with some functions of five variables , or it can implement even some functions of up to nine variables. Implementing wide functions in a single block reduces both the number of blocks required and the delay in the signal path, achieving both increased density and speed.

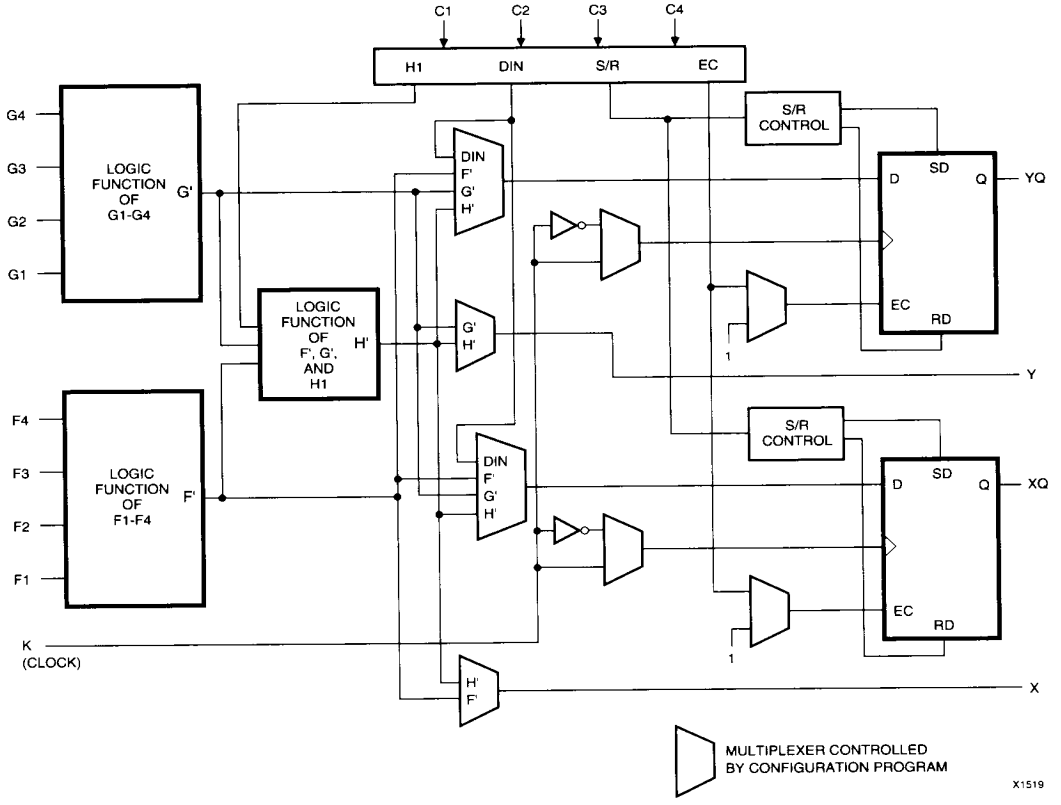


Figure 1. Simplified Block Diagram of XC4000 Configurable Logic Block

The two storage elements in the CLB are edge-triggered D-type flip-flops with common clock (K) and clock enable (EC) inputs. A third common input (S/R) can be programmed as either an asynchronous set or reset signal independently for each of the two registers; this input also can be disabled for either flip-flop. A separate global Set/Reset line (not shown in Figure 1) sets or clears each register during power-up, reconfiguration, or when a dedicated Reset net is driven active. This Reset net does not compete with other routing resources; it can be connected to any package pin as a global reset input.

Each flip-flop can be triggered on either the rising or falling clock edge. The source of a flip-flop data input is programmable: it is driven either by the functions F', G', and H', or the Direct In (DIN) block input . The flip-flops drive the XQ and YQ CLB outputs.

In addition, each CLB F' and G' function generator contains dedicated arithmetic logic for the fast generation of carry and borrow signals, greatly increasing the efficiency and performance of adders, subtracters, accumulators, comparators and even counters.

Multiplexers in the CLB map the four control inputs, labeled C1 through C4 in Figure 1, into the four internal control signals (H1, DIN, S/R, and EC) in any arbitrary manner.

The flexibility and symmetry of the CLB architecture facilitates the placement and routing of a given application. Since the function generators and flip-flops have independent inputs and outputs, each can be treated as a separate entity during placement to achieve high packing density. Inputs, outputs, and the functions themselves can freely swap positions within a CLB to avoid routing congestion during the placement and routing operation.

Speed Is Enhanced Three Ways

Delays in LCA-based designs are layout dependent. While this makes it hard to predict a worst-case guaranteed performance, there is a rule of thumb designers can consider — the system clock rate should not exceed one third to one half of the specified toggle rate. Critical portions of a design, shift registers and simple counters, can run faster — approximately two thirds of the specified toggle rate. For example, a -125 version of the XC3000 family with a simple synchronous design, like a shift register, will work reliably (worst-case) with a maximum clock frequency of up to 80 MHz. Synchronous counters can be clocked at up to 60 MHz, and more complex synchronous designs can typically be clocked at 30 MHz

The new XC4000 family can run at synchronous system clock rates of up to 50 MHz. This increase in performance over the previous families stems from three basic improvements: more advanced processing, improved architecture, and more abundant routing resources.

Advanced Processing

The XC4000 family is manufactured using a sub-micron process. Compared to the older 1.2 μ process, all logic and interconnect delays shrink about 20%. This results in a 25% increase in maximum clock and data rate even before any architectural improvements are taken into account.

Improved Architecture

More Inputs: The versatility of the CLB function generators improves system speed significantly. Table 3 shows how XC4000 implements many functions more efficiently and faster than is possible with XC3000. A 9-bit parity checker, for example, can be implemented in one CLB with a propagation delay of 6 ns. In the XC3000 family, the same function requires two CLBs with a propagation delay of 2 x 5.5 ns = 11 ns. One XC4000 CLB can determine whether two 4-bit words are identical, again with a 6-ns propagation delay. The ninth input can be used for simple ripple expansion of this identity comparator (25.5 ns over 16 bits, 51.5 ns over 32 bits), or a 2-layer identity comparator can generate the result of a 32-bit comparison in 15 ns, at the cost of a single extra CLB. Simpler functions like multiplexers also benefit from the greater flexibility of the XC4000 family CLB. A 16-input multiplexer uses 5 CLBs and has a delay of only 13.5 ns.

More Outputs: The CLB can pass the combinatorial output(s) to the interconnect network, but can also store the combinatorial result(s) or other incoming data in one or two flip-flops, and connect their outputs to the interconnect network as well. With XC3000 CLBs the designer has to make a choice, either output the combinatorial function or the stored value. In the XC4000 family, the flip flops can be used as registers or shift registers without blocking the function generators from performing a different, perhaps unrelated task. This increases the functional density of the device.

When a function generator drives a flip-flop in a CLB, the combinatorial propagation delay *overlaps completely* with the set-up time of the flip-flop. The set-up time is specified between the function generator inputs and the clock input. This represents a performance advantage over competing technologies where combinatorial delays must be added to the flip-flop set-up time.

Fast Carry: As described earlier, each CLB includes high-speed carry logic that can be activated by configuration. The two 4-input function generators can be configured as a 2-bit adder with built-in hidden carry that can be expanded to any length. This dedicated carry circuitry is so fast and efficient that conventional speed-up methods like carry generate/propagate are meaningless even at the 16-bit level, and of marginal benefit at the 32-bit level.

A 16-bit adder requires nine CLBs and has a combinatorial delay of 20.5 ns. Compare that to the 30 CLBs and 50 ns, or 41 CLBs and 30 ns in the XC3000 family.

The fast-carry logic opens the door to many new applications involving arithmetic operation, where the previous generations of FPGAs were not fast and/or not efficient enough. High-speed address offset calculations in microprocessor or graphics systems, and high-speed addition in digital signal processing are two typical applications.

Function		XC3000-125 Family	XC4000-5 Family
8/9- bit Parity Generate/Check		11 ns / 2 CLBs	6 ns / 1 CLB
25-bit Input Decode		15 ns / 6 CLBs	10 ns / 0 CLBs
32:32-bit Identity Comparator		16 ns / 16 CLBs + 1 Longline	15 ns / 9 CLBs
16:1 Multiplexer		28 ns / 15 CLBs	14 ns / 5 CLBs
16-bit Loadable Counter	(Maximum Density)	57 ns / 16 CLBs	24 ns / 8 CLBs
	(Maximum Speed)	33 ns / 23 CLBs	24 ns / 8 CLBs
16-bit Up/Down Counter	(Maximum Density)	57 ns / 16 CLBs	24 ns / 8 CLBs
	(Maximum Speed)	40 ns / 23 CLBs	24 ns / 8 CLBs

Table 3. Density and Performance for Several Common Circuit Functions

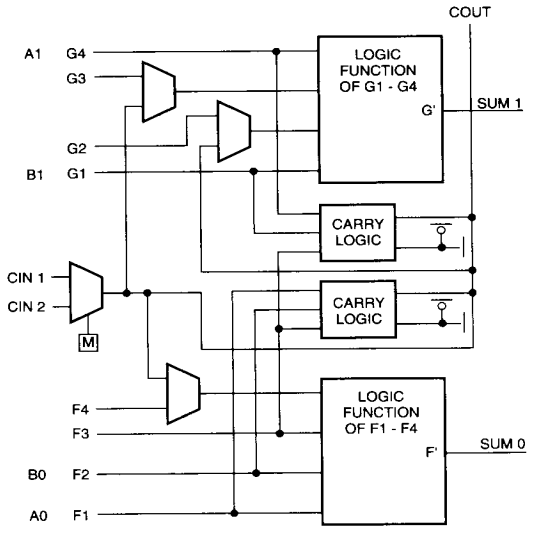


Figure 2. Fast Carry Logic in Each CLB

Faster and More Efficient Counters: The XC4000 fast-carry logic puts two counter bits into each CLB and runs them at a clock rate of up to 42 MHz for 16 bits, whether the counters are loadable or not. For a 16-bit up/down counter, this means twice the speed in half the number of CLBs, compared with the XC3000 family.

Pipelining Speeds Up The System: The abundance of flip-flops in the CLBs invites pipelined designs. This is a powerful way of increasing performance by breaking the function into smaller subfunctions and executing them in parallel, passing on the results through pipeline flip-flops. This method should be seriously considered wherever total performance is more important than simple through-delay.

Wide Decoding is Fast: For years, FPGAs have suffered from the lack of fast and wide decoding circuitry. When the address or data field is wider than the function generator inputs(five bits in the XC3000 family), FPGAs need multi-level decoding and are thus slower than PALs. The XC4000-family CLBs have nine inputs; any decoder of up to nine inputs is, therefore, compact and fast. But, there is also a need for much wider fast decoders, especially for address decoding in large microprocessor systems.The XC4000 family has 16 very fast programmable decoders, each with up to 42 inputs in the XC4005, 90 inputs in the XC4020. These dedicated decoders are located at the chip periphery, four decoders on each chip edge. They accept I/O signals and internal signals as input and generate a decoded output in 10 ns. Each decoder AND gate can also be split in two, when a larger number of narrower decoders is required. Very large PALs can be emulated by ORing the decoder outputs in a CLB. This fast decoding feature covers what has long been considered a weakness of FPGAs. Users often resorted to external PALs for simple but fast decoding functions. Now, the dedicated decoders in the XC4000 can implement these functions efficiently and fast.

Higher Output Current: The 4-mA maximum output current specification of today's FPGAs often forces the user to add external buffers, cumbersome especially on bidirectional I/O lines. The XC4000 solves many of these problems by increasing the maximum output sink current to 12 mA. Two adjacent outputs may be interconnected to increase the output sink current to 24 mA. The FPGA can thus drive short buses on a pc board.

While the XC2000 and XC3000 families used complementary output transistors, the XC4000 outputs are n-channel for both pull-down and pull-up, somewhat analogous to the classical totem pole used in TTL. The reduced output High level (V_{OH}) makes circuit delays more symmetrical for TTL-threshold systems. N-channel pull-ups have one additional advantage: the output can be pulled higher than V_{CC}, whereas a true CMOS output structure clamps against V_{CC}, causing problems when a system is partially powered-down. When high-current drivers, like LS240s, are powered-up, but CMOS outputs on the same bus are not yet or no longer powered-up, there can be uncontrolled input currents in excess of 100 mA forced into the clamping diodes, leading to potential latch-up or other reliability problems. The n-channel output pull-up transistors of the XC4000 family avoid that problem completely.

Abundant Routing Resources

Connections between blocks are made by metal lines with programmable switching points and switching matrices. Compared to the previous LCA families, these routing resources have been increased dramatically.The number of globally distributed signals has been increased from two to eight, and these lines have access to any clock or logic input. The designer of synchronous systems can now distribute not only several clocks, but also control signals, all over the chip, without having to worry about any skew.

There are more than twice as many horizontal and vertical Longlines that can carry signals across the length or width of the chip with minimal delay and negligible skew.The horizontal Longlines can be driven by 3-state buffers, and can thus be used as unidirectional or bidirectional data buses; or they can implement wide multiplexers or wired-AND functions.

Single-length lines connect the switching matrices that are located at every intersection of a row and a column of CLBs. These lines provide the greatest interconnect flexibility, but cause a delay whenever they go through a switching matrix. Double-length lines bypass every other matrix, and provide faster signal routing over intermediate distances.

Compared to the XC3000 family, the XC4000 family has more than double the routing resources, and they are arranged in a far more regular fashion. In older devices, inputs could not be driven by all adjacent routing lines. In the XC4000 family, these constraints have been largely eliminated. This makes it easier for the software to complete the routing of complex interconnect patterns.

Chip architects and software designers worked closely together to achieve a solution that is not only inherently powerful, but also easy to utilize by the software-driven design tools for Partitioning, Placement and Routing. The goal was to provide automated push-button software tools that complete almost all designs, even large and dense ones, automatically, without operator assistance. But these tools will still give the designer the option to get involved in the partitioning, placement and, to a lesser extent, even the routing of critical parts of the design, if that is needed to optimize the performance.

On-Chip Memory

The XC4000 family LCAs are the first programmable logic devices to include on-chip static memory resources, further increasing system integration levels.

An optional mode for each CLB makes the memory look-up tables in the F' and G' function generators usable as either a 16 x 2 or 32 x 1 bit array of Read/Write memory cells (Figure 3). The F1-F4 and G1-G4 inputs to the function generators act as address lines, selecting a particular memory cell in each look-up table. The functionality of the CLB control signals change in this configuration; the H1, DIN, and S/R lines become the two data inputs and the Write Enable (WE) input for the 16 x 2 memory. When the 32 x 1 configuration is selected, D1 acts as the fifth address bit and D0 is the data input. The contents of the memory cell(s) being addressed are available at the F' and G' function-generator outputs, and can exit the CLB through its X and Y outputs, or can be pipelined using the CLB flip-flop(s).

Configuring the CLB function generators as Read/Write memory does not affect the functionality of the other portions of the CLB, with the exception of the redefinition of the control signals. The H' function generator can be used to implement Boolean functions of F', G', and D1, and the D flip-flops can latch the F', G', H', or D0 signals.

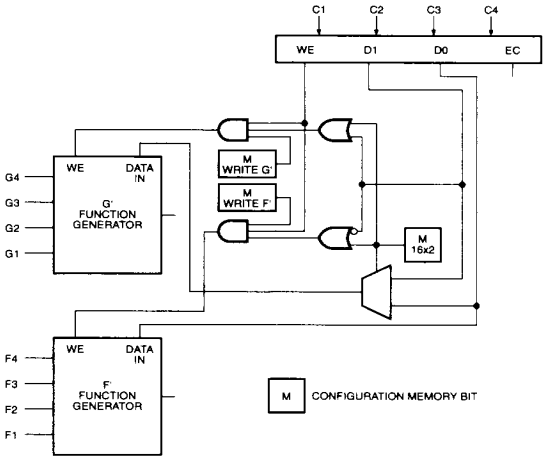


Figure 3. CLB Function Generators Can Be Used as Read/Write Memory Cells

The RAMs are very fast; read access is the same as logic delay, about 5 ns; write time is about 6 ns; both are several times faster than any off-chip solution. Such distributed RAM is a novel concept, creating new possibilities in system design: registered arrays of multiple accumulators, status registers, index registers, DMA counters, distributed shift registers, LIFO stacks, and FIFO buffers. A 16-byte FIFO uses four CLBs for storage, six CLBs for address counting and multiplexing, and two for arbitration and handshake (Figure 4). With 32 storage locations per CLB, compared to two flip-flops per CLB, the cost of intelligent distributed memory has been reduced by a factor of 16.

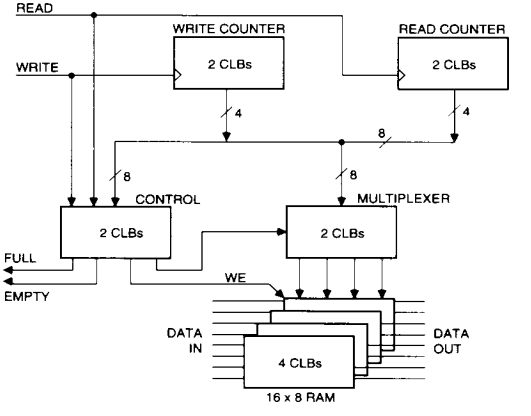


Figure 4. 16-byte FIFO

Input/Output Blocks (IOBs)

User-configurable IOBs provide the interface between external package pins and the internal logic (Figure 5). Each IOB controls one package pin and can be defined for input, output, or bidirectional signals.

Two paths, labeled I_1 and I_2, bring input signals into the array. Inputs are routed to an input register that can be programmed as either an edge-triggered flip-flop or a level-sensitive transparent latch. Optionally, the data input to the register can be delayed by several nanoseconds to compensate for the delay on the clock signal, that first must pass through a global buffer before arriving at the IOB. This eliminates the possibility of a data hold-time requirement at the external pin. The I_1 and I_2 signals that exit the block can each carry either the direct or registered input signal.

Output signals can be inverted or not inverted, and can pass directly to the pad or be stored in an edge-triggered flip-flop. Optionally, an output enable signal can be used to place the output buffer in a high-impedance state, implementing 3-state outputs or bidirectional I/O. Under configuration control, the output (OUT) and output enable (OE) signals can be inverted, and the slew rate of the output buffer can be reduced to minimize power bus transients when switching non-critical signals. Each output buffer is capable of sinking 12 mA; two adjacent output buffers can be wire-ANDed externally to sink up to 24 mA .

There are a number of other programmable options in the IOB. Programmable pull-up and pull-down resistors are useful for tying unused pins to V_{CC} or ground to minimize power consumption. Separate clock signals are provided for the input and output registers; these clocks can be inverted, generating either falling-edge or rising-edge triggered flip-flops. As is the case with the CLB registers, a global set/reset signal can be used to set or clear the input and output registers whenever the RESET net is active.

Embedded logic attached to the IOBs contains test structures compatible with IEEE Standard 1149.1 for boundary-scan testing, permitting easy chip and board-level testing.

Programmable Interconnect

All internal connections are composed of metal segments with programmable switching points to implement the desired routing. An abundance of different routing resources is provided to achieve efficient automated routing. The number of routing channels is scaled to the size of the array; i.e., it increases with array size.

In previous generations of LCAs, the logic-block inputs were located on the top, left, and bottom of the block; outputs exited the block on the right, favoring left-to-right data flow through the device. For the third-generation family, the CLB inputs and outputs are distributed on all four sides of the block, providing additional routing flexibility (Figure 6). In general, the entire architecture is more symmetrical and regular than that of earlier generations, and is more suited to well-established placement and routing algorithms developed for conventional mask- programmed gate-array design.

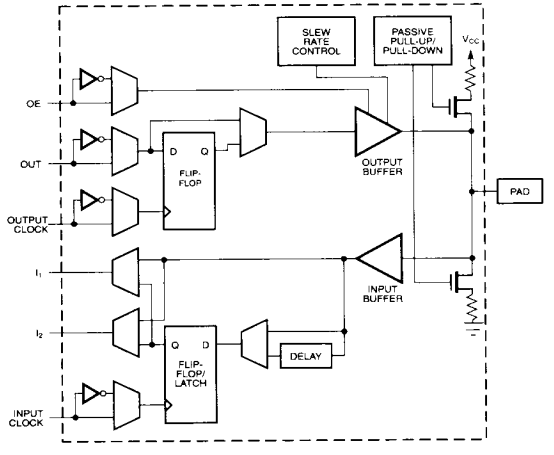


Figure 5. XC4000 Input/Output Block

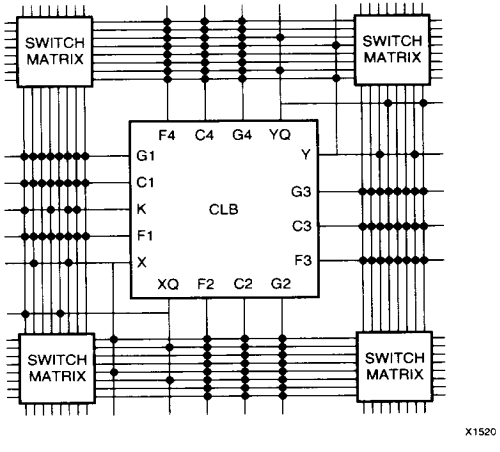


Figure 6. Typical CLB Connections to Adjacent Single-Length Lines

There are three main types of interconnect, distinguished by the relative length of their segments: single-length lines, double-length lines, and Longlines. Note: The number of routing channels shown in Figures 6 and 9 are for illustration purposes only; the actual number of routing channels varies with array size. The routing scheme was designed for minimum resistance and capacitance of the average routing path, resulting in significant performance improvements.

The single-length lines are a grid of horizontal and vertical lines that intersect at a Switch Matrix between each block. Figure 6 illustrates the single-length interconnect lines surrounding one CLB in the array. Each Switch Matrix consists of programmable n-channel pass transistors used to establish connections between the single-length lines (Figure 7). For example, a signal entering on the right side of the Switch Matrix can be routed to a single-length line on the top, left, or bottom sides, or any combination thereof, if multiple branches are required. Single-length lines are normally used to conduct signals within a localized area and to provide the branching for nets with fanout greater than one.

Compared to the previous generations of LCA architectures, the number of possible connections through the Switch Matrix has been reduced. This decreases capacitive loading and minimizes routing delays, thus increasing performance. However, a much more versatile set of connections between the single-length lines and the CLB inputs and outputs more than compensate for the reduction in Switch Matrix options, resulting in overall increased routability.

The function generator and control inputs to the CLB (F1-F4, G1-G4, and C1-C4) can be driven from any adjacent single-length line segment (Figure 6). The CLB clock (K) input can be driven from one-half of the adjacent single-length lines. Each CLB output can drive several of the single-length lines, with connections to both the horizontal and vertical Longlines.

The double-length lines (Figure 8) consist of a grid of metal segments twice as long as the single-length lines; i.e, a double-length line runs past two CLBs before entering a Switch Matrix. Double-length lines are grouped in pairs,

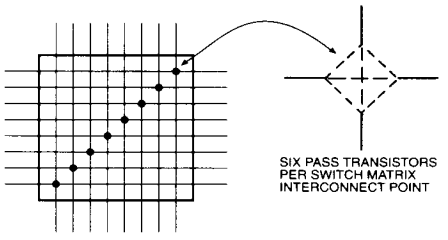


Figure 7. Switch Matrix

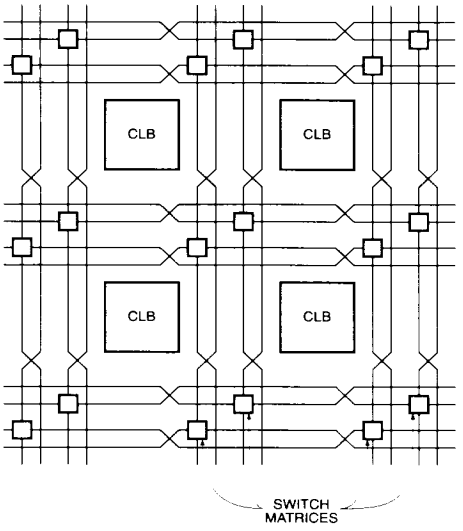


Figure 8. Double-Length Lines

with the Switch Matrices staggered so that each line goes through a Switch Matrix at every other CLB location in that row or column. As with single-length lines, all the CLB inputs except K can be driven from any adjacent double-length line, and each CLB output can drive nearby double-length lines in both the vertical and horizontal planes. Double-length lines provide the most efficient implementation of intermediate length, point-to-point interconnections.

Longlines form a grid of metal interconnect segments that run the entire length or width of the array (Figure 6). Additional vertical long lines can be driven by special

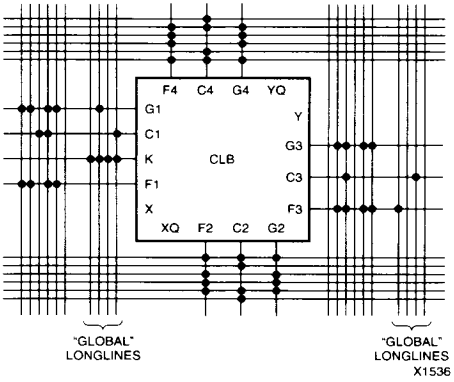


Figure 9. Longline Routing Resources with Typical CLB Connections

global buffers, designed to distribute clocks and other high fanout control signals throughout the array with minimal skew. Longlines are intended for high fan-out, time-critical signal nets. Each Longline has a programmable "splitter switch" at its center, that can separate the line into two independent routing channels, each running half the width or height of the array. CLB inputs can be driven from a subset of the adjacent Longlines; CLB outputs are routed to the Longlines via 3-state buffers or the single-length interconnect lines.

Communication between Longlines and single-length lines is controlled by programmable interconnect points at the line intersections. Double-length lines do not connect to other lines.

Three-State Buffers

A pair of 3-state buffers, associated with each CLB in the array, can be used to drive signals onto the nearest horizontal Longlines above and below the block. This feature is also available in the XC3000 generation of LCAs. The 3-state buffer input can be driven from any X, Y, XQ, or YQ output of the neighboring CLB, or from nearby single-length lines; the buffer enable can come from nearby vertical single-length or Longlines. Another 3-state buffer with similar access is located near each I/O block along the right and left edges of the array. These buffers can be used to implement multiplexed or bidirectional buses on the horizontal Longlines. Programmable pull-up resistors attached to both ends of these Longlines help to implement a wide wired-AND function.

Special Longlines running along the perimeter of the array can be used to wire-AND signals coming from nearby IOBs or from internal long lines.

Taking Advantage of Reconfiguration

All three families of LCA devices can be re-configured to change logic function while resident in the system. This gives the system designer a new degree of freedom, not available with any other type of logic. Hardware can be changed as easily as software. Design updates or modifications are easy. An LCA device can even be reconfigured dynamically to perform different functions at different times. Reconfigurable logic can be used to implement system self-diagnostics, create systems capable of being reconfigured for different environments or operations, or implement dual-purpose hardware for a given application. As an added benefit, use of reconfigurable LCAs simplifies hardware design and debugging and shortens a product's time-to-market.

DEVELOPMENT SYSTEM

The powerful features of the XC4000 device family require an equally powerful, yet easy-to-use set of development tools. Xilinx provides an enhanced version of the Xilinx Automatic CAE Tools (XACT) optimized for the XC4000 family.

The XACT Design Manager (XDM) simplifies the selection of command-line options with pull-down menus and on-line help text. Application programs ranging from schematic capture to Partitioning, Placement, and Routing (PPR) can be accessed from XDM, while the program-command sequence is generated and stored for documentation prior to execution. The XMake command in XDM automates the entire process, from design entry to the generation of configuration and report files.

Similar to that for the XC2000 and XC3000 families, the XC4000 design flow consists of three steps–Design Entry, Design Implementation, and Design Verification.

Design Entry

A design can be entered using schematic-capture software, state-machine description or Boolean-equation entry.

Xilinx and third-party vendors have developed library and interface products compatible with a wide variety of design-entry and simulation environments. A standard interface-file specification, XNF, is provided to simplify file transfers into and out of the XACT development system.

Xilinx offers XACT development-system interfaces to the following design environments.

- FutureNet DASH
- Viewlogic Viewdraw and Viewsim
- Mentor Graphics NETED and QuickSim
- Cadence Composer Schematic Entry, Verilog Simulator
- OrCAD SDT and VST

Several other environments are supported by third-party vendors. Currently, more than 100 packages are supported.

Macro Libraries

Along with the standard library of Soft Macros, like those included with the XC3000 family, the XC4000 family also includes a library of Hard Macros. The Soft Macro library contains detailed descriptions of common logic functions such as counters, adders, etc.; it does not contain any partitioning or routing information. The performance of Soft Macros depends, therefore, on how the PPR software processes the macro.

Hard Macros, on the other hand, do contain complete partitioning, placement, and routing information. These predefined and tested functions permit the user to build timing-critical designs with optimized performance. Designing with Hard Macros is as easy as designing with MSI/LSI.

276 Soft Macros
(Simplify Schematic Entry)

98	Gates
12	Flip-Flops (D, J-K, input mux)
9	Latches (including '259, '373)
15	Decoders (including '42, '48, '138, '139, '154)
19	Multiplexers (including '150...'153, '157, '257, '352)
13	Comparators (2 to 32 bits, identity or magnitude)
12	Adders/Subtactors (2 to 32 bits)
32	Registers (4 to 16 bits)
35	Counters (synchr., 2 to 32 bits, up, dwn, up/dwn, PE)
9	RAMs (16 x 2 to 128 x 8)
18	I/O Circuits
4	Priority Encoders and Parity Checkers

36 Hard Macros
(Pre-Partitioned) Predictable Performance

Adders, Comparators, Multiplexers, Decoders, Encoders, Parity Check
RAMs (4,8,16 wide, 16,32 deep)
FIFOs (4,8,16 wide, 16,32 deep)
LIFOs (4,8,16 wide, 16,32 deep)
Register Files (4,8,16 wide, 16,32 deep)
Counters (synchronous, 8 and 16 bit, up or down, Parallel Enable, utilizing Fast Carry logic)

Design Implementation

The design-implementation tools have been greatly enhanced to cope with the higher density of the XC4000 devices and to satisfy the requirement for a completely automated design process. Logic partitioning, block placement and signal routing encompass the design implementation process. The partitioner takes the logic from the schematic or other entry method, and divides the logic to fit into the blocks available on the device. The placer then determines the best locations for the blocks, depending on their connectivity and the required performance. The router finally connects the placed blocks together.

The improved PPR algorithms result in fully automatic implementation of most designs. The new algorithms also reduce execution time compared to previous software generations.

The automated implementation tools are complemented by the XACT Design Editor (XDE), an interactive graphics-based editor that displays a model of the actual logic and routing resources of the FPGA. XDE can be used to directly view the results achieved by the automated tools. Modifications can be made using XDE; XDE can also perform checks for logic connectivity and possible design-rule violations.

Interactive point-to-point timing-delay calculations provide timing analysis and help to determine critical paths. The user can, thus, identify and correct timing problems while the design is still in process.

Design Verification

The high development cost associated with common mask-programmed gate arrays necessitates extensive simulation to verify a design. Due to the custom nature of masked gate arrays, mistakes or last-minute design changes cannot be tolerated. A gate-array designer must simulate and test all logic and timing using simulation software. Simulation describes what happens in a system under worst-case situations. However, simulation is tedious and slow; somebody has to write simulation vectors. A few seconds of system time can take weeks to simulate.

Programmable-gate-array users, however, can use in-circuit debugging techniques in addition to simulation. Because Xilinx devices are reprogrammable, designs can be verified in the system in real time without the need for extensive simulation vectors.

The XACT development system supports both simulation and in-circuit debugging techniques. For simulation, the system extracts the post-layout timing information from the design database. This data can then be sent to the simulator to verify timing-critical portions of the design.

For in-circuit debugging,XACT has a serial download and readback cable (XChecker) that connects the device in the system to the PC or workstation through an RS232 serial port. The engineer can download a design or a design revision into the system for testing. The designer can also single-step the logic, read the contents of the numerous flip-flops on the device and observe the internal logic levels. Simple modifications can be downloaded into the system in a matter of minutes.

Summary

The result of five years of FPGA design experience and feedback from thousands of customers, the new XC4000 family combines architectural versatility, on-chip RAM, increased speed and gate complexity with abundant routing resources and new, sophisticated software to achieve fully automated implementation of complex, high-performance designs.

CLB Count of Selected XC4000 Soft Macros

7400 Equivalents

	# of CLBs
'42	5
'48	8
'83	4
'85	4
'138	4
'139	2
'147	4
'148	6
'150	5
'151	2
'152	2
'153	2
'154	9
'157	2
'158	2
'160	5
'161	6
'162	5
'163	7
'164	4
'165s	4
'166	5
'168	9
'174	3
'194	4
'195	3
'198	9
'199	5
'257	2
'258	2
'259	17
'278	4
'280	2
'283	4
'298	2
'352	2
'373	4
'374	4
'390	2
'518	2
'521	2
'577	4

Adders

	# of CLBs	
add8	8	(5)
add16	16	(9)
add32	32	

Barrel Shifters

brlshft4	4
brlshft8	12

4-Bit Counters

c10bcrd	2
c10cprd	4
c16bcr	2
c16bcrd	2
c16cprd	4
c16budrd	5

5,6,8-Bit Counters

c32budrd	6
c64budrd	9
c256bcr	7
c256bcrd	5
c256bcpr	8

Identity Comparators

comp4	1
comp8	2
comp16	4
comp32	9

Magnitude Comparators

compm4	3	
compm8	8	(5)
compm16	17	(9)
compm32	39	

Decoders

d2-4e	2
d3-8e	4
d4-16	8
d4-16e	16

FIFOs

	# of CLBs
fif16x4	15
fif16x8	17
fif16x16	21
fif32x4	20
fif32x8	24

LIFOs (Stacks)

lif16x4	10
lif16x8	12
lif32x4	15
lif32x8	19
lif32x16	27

Multiplexers

m2-1e	0.5
m4-1	1
m4-1e	2
m8-1e	2
m16-1e	5

Registers

rd4r	2
rd8r	4
rd16r	8

Shift Registers

rs8p	4
rsr16	2
rsr32	16

Register Files

rf16x4	2
rf16x16	8
rf32x4	4
rf32x16	16

RAMs

ram 16x4	2
ram 16x8	4
ram 32x8	8
ram 64x8	21

Explanation of counter nomenclature:
b=binary, p=synchronous parallel loadable, ud=up/down, c=count enable, r=synchronous reset, rd=asynchronous reset direct.

Note: When a device is not fully utilized, the automatic partitioner may assign a larger number of CLBs in order to improve speed and routing. Values in parentheses refer to Hard Macros.

Figure 10

FUNCTIONAL DESCRIPTION

Input/Output Blocks

The IOB forms the interface between the internal logic and the I/O pads of the LCA device. Under configuration control, the output buffer receives either the logic signal (.out) routed from the internal logic to the IOB, or the complement of this signal, or this same data after it has been clocked into the output flip-flop.

As a configuration option, each flip-flop (CLB or IOB) is initialized as either set or reset, and is also forced into this programmable initialization state whenever the global Set/Reset net is activated after configuration has been completed. The clock polarity of each IOB flip-flop can be configured individually, as can the polarity of the 3-state control for the output buffer.

Each output buffer can be configured to be either fast or slew-rate limited, which reduces noise generation and ground bounce. Each output can be configured with either an internal pull-up or pull down resistor, or with no internal resistor. Independent of this choice, each IOB has a pull-up resistor during the configuration process.

The 3-state output driver uses a totem pole n-channel output structure capable of sinking 12 mA and sourcing 4 mA. V_{OH} is one n-channel threshold lower than Vcc, which makes rising and falling delays more symmetrical. When in the high-impedance state, the output may be pulled more positive than the level on Vcc, but not higher than 7 V. This avoids problems when a system is partially powered down. Adjacent outputs can be paired for 24-mA sink capability without any danger of contention during the transition.

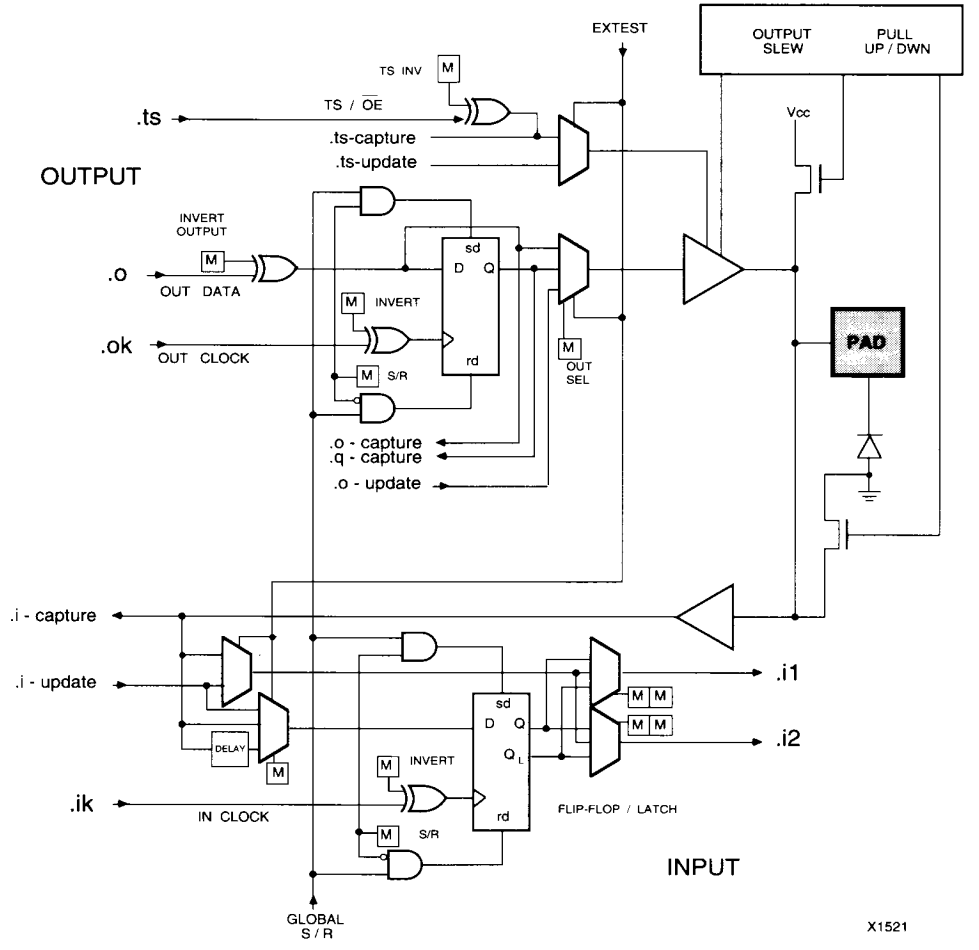


Figure 11. I/O Block

The inputs drive TTL-compatible buffers with 1.2-V input threshold and a slight hysteresis of about 300 mV. These buffers drive the internal logic as well as the D-input of the input flip-flop.

Under configuration control, the set-up time of this flip-flop can be increased so that normal clock routing does not result in a hold-time problem. Note that the input flip-flop set-up time is defined between the data measured at the device I/O pin and the clock input at the IOB. Any clock routing delay must, therefore, be subtracted from this set-up time to arrive at the real set-up time requirement on the device pins. A short specified set-up time might, therefore, result in a negative set-up time at the device pins, i.e. a hold-time requirement, which is usually undesirable. The optional long set-up time can tolerate more clock delay without causing a hold-time requirement.

The input block has two connections to the internal logic, I_1 and I_2. Each of these is driven either by the incoming data, by the master or by the slave of the input flip-flop.

Wide Fast Decoders

The periphery of the chip has four wide and fast decoder circuits at each edge. The inputs to each decoder are any of the I1 signals on that edge plus one local interconnect per CLB row or column. Each decoder generates an active High output (resistor pull-up) when the AND condition of the selected inputs, or their complements, is true. This is analogous to the AND term in typical PAL devices. Each decoder can be split at its center; therefore, the largest total number of fast decoders on any one chip is 32.

The decoder outputs can drive CLB inputs so they can be combined with other logic, or to form a PAL-like AND/OR structure. The decoder outputs can also be routed directly to the chip outputs. For fastest speed, the output should be on the same chip edge as the decoder.

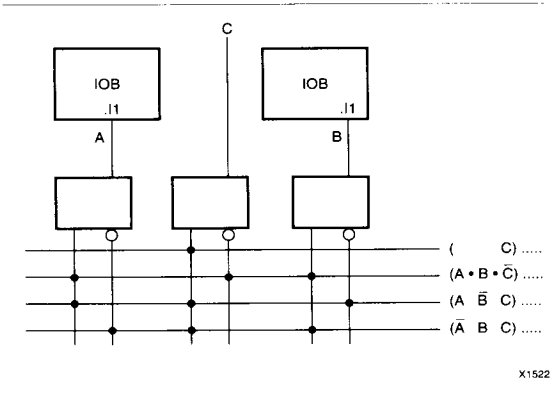


Figure 12. Example of Edge Decoding.
Each row or column of CLBs provide up to three variables (or their complements)

Configurable Logic Blocks

Configurable Logic Blocks implement most of the logic in an LCA device. Two 4-input function generators (F and G) offer unrestricted versatility. A third function generator (H) can combine the outputs of F and G with a ninth input variable, thus implementing certain functions of up to nine variables, like parity check or expandable-identity comparison of two sets of four inputs.

The four control inputs C1 through C4 can each generate any one of four logic signals, used in the CLB.

- Enable Clock, Asynchronous Preset/Reset, DIN, and H1, when the memory function is disabled, or
- Enable Clock, Write Enable, D0, and D1, when the memory function is enabled.

Since the function-generator outputs are brought out independently of the flip-flop outputs, and DIN and H1 can be used as direct inputs to the two flip-flops, the two combinatorial and the two sequential functions in the CLB can be used independently. This versatility increases logic density and simplifies routing.

The asynchronous flip-flop input can be configured as either set or reset. This configuration option also determines the state in which the flip-flops become operational after configuration, as well as the effect of an externally or internally applied Set/Reset during normal operation.

Fast Carry Logic

The CLBs can generate the arithmetic-carry output for incoming operands, and can pass this extra output on to the next CLB function generator above or below. This connection is independent of normal routing resources and it is, presently, only supported by Hard Macros. A later software release will accomodate Soft Macros and will permit graphic editing of the fast logic circuitry. This fast carry logic is one of the most significant improvements in the XC4000 family, speeding up arithmetic and counting into the 50-MHz range.

Using Function Generators as RAMs

Using XC4000 devices, the designer can write into the latches that hold the configuration content of the function generators. Each function generator can thus be used as a small Read/Write memory, or RAM. The function generators in any CLB can be configured in three ways.

- Two 16 x 1 RAMs with two data inputs and two data outputs – identical or, if preferred, different addressing for each RAM
- One 32 x 1 RAM with on data input and one data output
- One 16 x 1 RAM plus one 5-input function generator

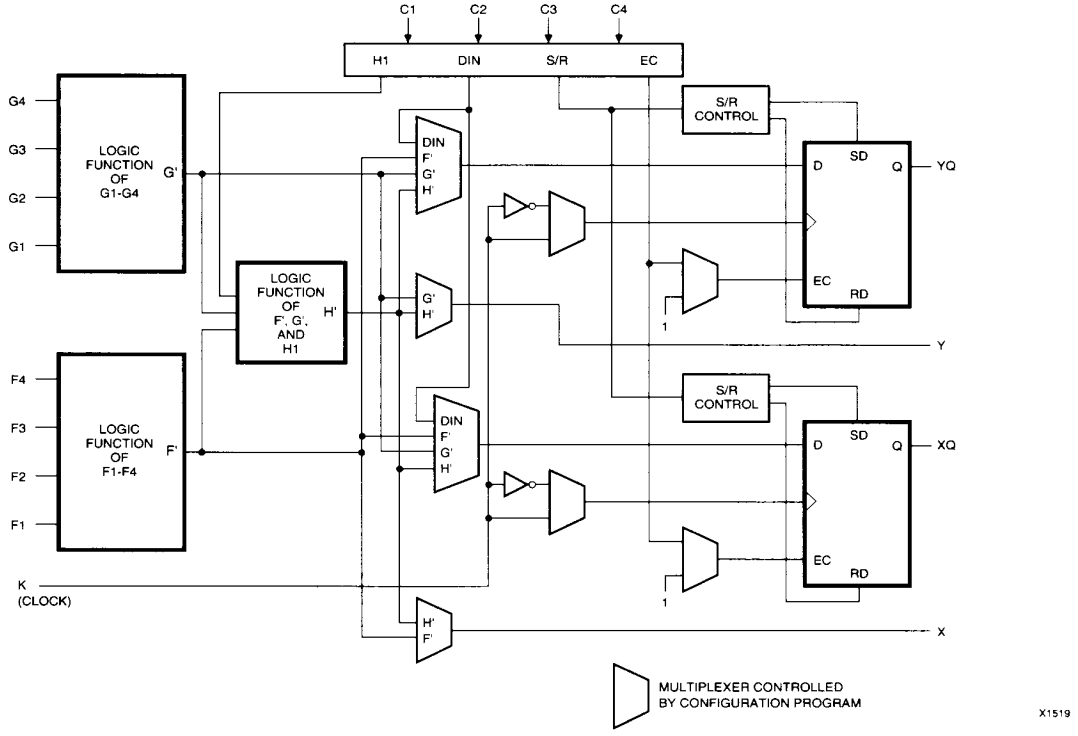


Figure 13. Simplified Block Diagram of XC4000 Configurable Logic Block

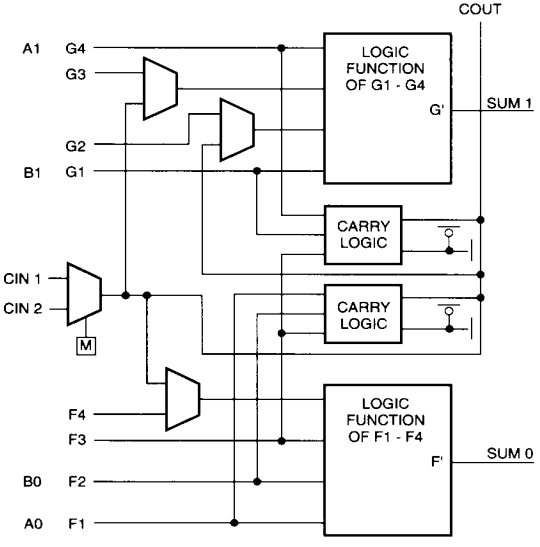


Figure 14. Fast Carry Logic in Each CLB

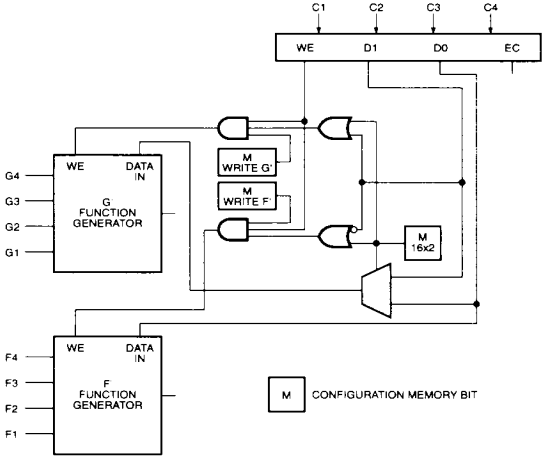


Figure 15. CLB Function Generators Can Be Used as Read/Write Memory Cells

Boundary Scan

Boundary Scan is becoming an attractive feature that helps sophisticated systems manufacturers test their PC boards more safely and more efficiently. The XC4000 family implements IEEE 1149.1 Boundary-Scan BYPASS, SAMPLE, and EXTEST. When the Boundary Scan configuration option is selected, three normal user I/O pins become dedicated inputs for these functions.

The "bed of nails" has been the traditional method of testing electronic assemblies. This approach has become less appropriate, due to closer pin spacing and more sophisticated assembly methods like surface-mount technology and multi-layer boards. The IEEE Boundary Scan standard 1149.1 was developed to facilitate board-level testing of electronic assemblies. Design and test engineers can imbed a standard test logic structure in their electronic design. This structure is easily implemented with the serial and/or parallel connections of a four-pin interface on any Boundary-Scan-compatible IC. By exercising these signals, the user can serially load commands and data into these devices to control the driving of their outputs and to examine their inputs. This is an improvement over bed-of-nails testing. It avoids the need to overdrive device outputs, and it reduces the user interface to four pins. An optional fifth pin, a reset for the control logic, is described in the standard but is not implemented in the Xilinx part.

The dedicated on-chip logic implementing the IEEE 1149.1 functions includes a 4-bit state machine, an instruction register and a number of data registers. Six machine states are used for Boundary-Scan instruction-register control and six for data-register control. A register operation begins with a *capture* where a set of data is parallel loaded into the designated register for shifting out. The next state is *shift*, where captured data are shifted out while the desired data are shifted in. A number of states are provided for Wait operations. The last state of a register sequence is the *update* where the shifted content of the register is loaded into the appropriate instruction- or data-holding register, either for instruction-register decode or for data-register pin control.

The primary data register is the Boundary-Scan register. For each IOB pin in the LCA, it includes three bits of shift register and three *update* latches for: in, out and 3-state control. Non-IOB pins have appropriate partial bit population for in or out only. Each "Extest Capture" captures all available input pins.

The other standard data register is the single flip-flop *bypass* register. It resynchronizes data being passed through a device that need not be involved in the current scan operation. The LCA provides two user nets (BSCAN.SEL1 and BSCAN.SEL2) which are the decodes of two user instructions. For these instructions, two corresponding nets (BSCAN.TDO1 and BSCAN.TDO2) allow user scan data to be shifted out on TDO. The data register clock (BSCAN.DRCK) is available for control of test logic which the user may wish to implement with CLBs. The NAND of TCK and Run-test-idle is also provided (BSCAN.IDLE).

Instruction	Code
EXTEST	000
SAMPLE	001
USER 1	010
USER 2	011
reserved	100
reserved	101
reserved	110
BYPASS	111

(LSB shifted in first)

Bit Sequence

The bit sequence within each IOB is: in, out, 3-state. From a cavity-up (XDE) view of the chip, starting in the upper right chip corner, the Boundary-Scan data-register bits have the following order:

BSCANT.UPD net*,

right-edge IOBs,

(lower right chip corner)

bottom edge IOBs, MD2.I net,

(lower left chip corner)

MD0.I net, MD1.I net, MD1.O net, MD1.T net,

left edge IOBs,

(upper left chip corner,)

top-edge IOBs,

TDO.O net*, TDO.T net*

(upper right chip corner,)

TDO

PROGRAM, CCLK and DONE are not included in the Boundary-Scan register.

* These three Boundary-Scan bits are special-purpose Xilinx test signals

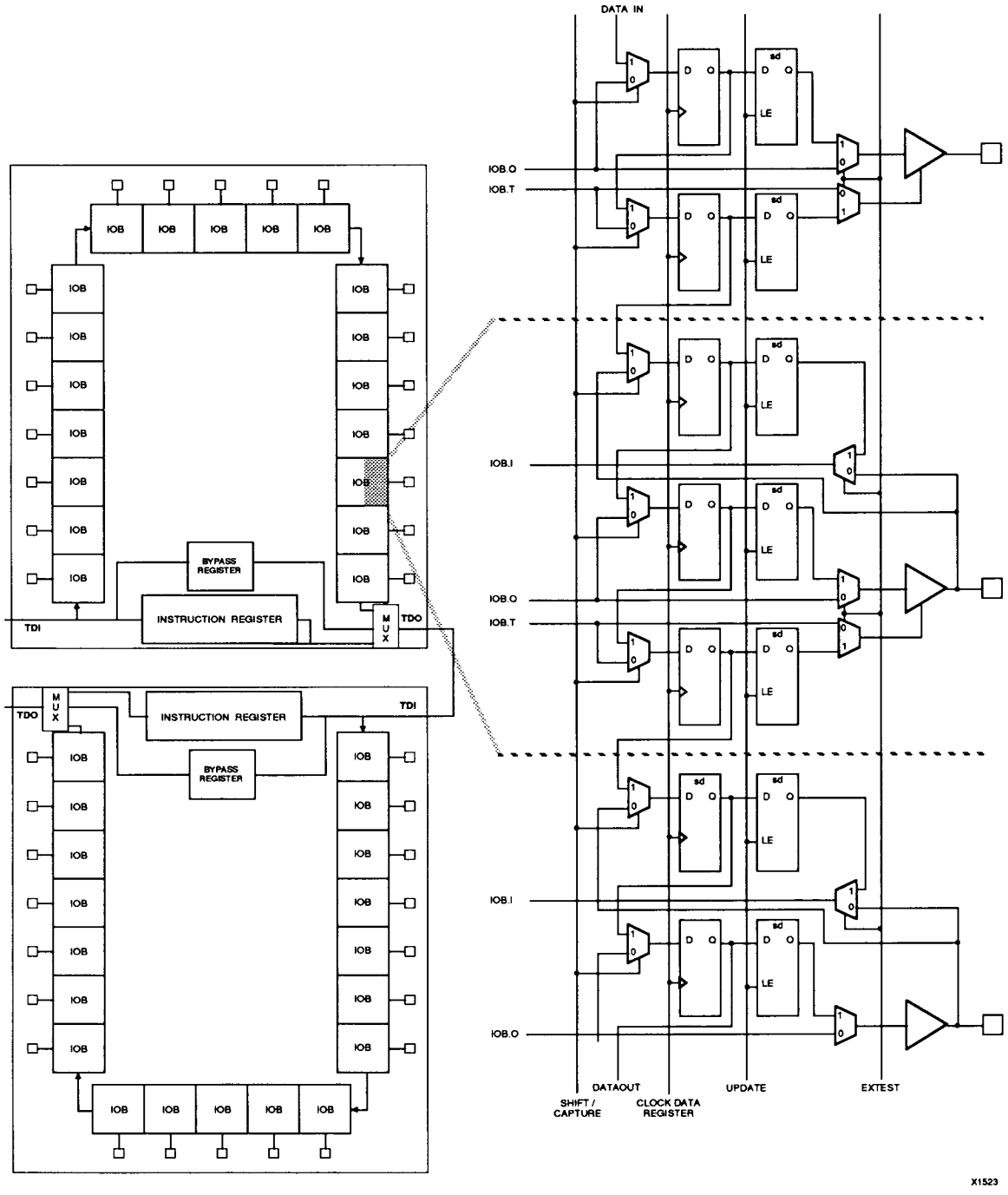


Figure 16. XC4000 Boundary Scan Logic.
Includes three bits of Data Register per IOB, the IEEE 1149.1 Test Access Port controller, and the Instruction Register with decodes.

Interconnects

The XC4000 family uses a hierarchy of interconnect resources.

- General purpose single-length and double-length lines offer fast routing between adjacent blocks, and highest flexibility for complex routes, but they incur a delay every time they pass through a switch matrix.
- Longlines run the width or height of the chip with negligible delay variations. They are used for signal distribution over long distances. Some Horizontal Longlines can be driven by 3-state or open-drain drivers, and can thus implement bidirectional buses or wired-AND decoding.
- Global Nets are optimized for the distribution of clock and time-critical or high-fan-out control signal. Four pad-driven Primary Global Nets offer shortest delay and negligible skew. Four pad-driven Secondary Global Nets have slightly longer delay and more skew due to heavier loading.

Each CLB column has four dedicated Vertical Longlines, each of these lines has access to a particular Primary Global Net, or to any one of the Secondary Global Nets. The Global Nets avoid clock skew and potential hold-time problems. The user must specify these Global Nets for all timing-sensitive global signal distribution.

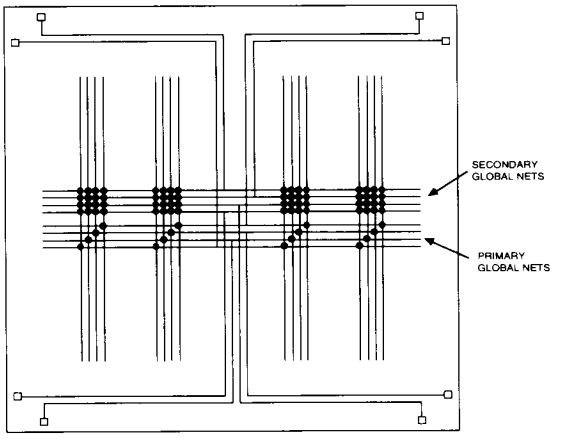
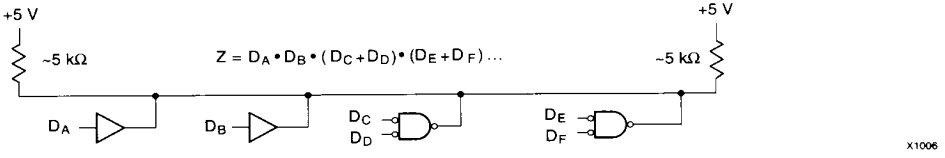
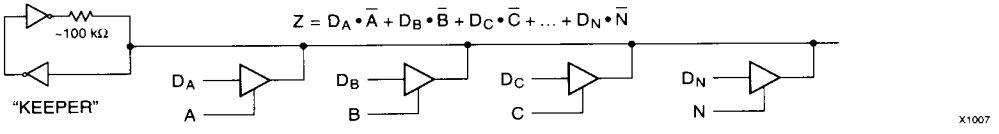


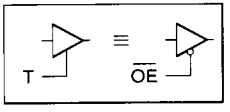
Figure 17. XC4000 Global Net Distribution.
Four Lines per Column; Eight Inputs in the Four Chip Corners.



Open Drain Buffers Implement a Wired-AND Function. When all the buffer inputs are High the pull-up resistor(s) provide the High output.



3-State Buffers Implement a Multiplexer. The selection is accomplished by the buffer 3-state signal.



Active High T is Identical to Active Low Output Enable.

Figure 18. TBUFs Driving Horizontal Long Lines.

Oscillator

An internal oscillator is used for clocking of the power-on time-out, configuration memory clearing, and as the source of CCLK in Master modes. This oscillator signal runs at a nominal 8 MHz and varies with process, Vcc and temperature. This signal is available on an output control net (OSCO) in the upper right corner of the chip, if the oscillator-run control bit is enabled in the configuration memory. Two of four resynchronized taps of the power-on time-out divider are also available on OSC1 and OSC2. These taps are at the fourth, ninth, fourteenth and nineteenth bits of the ripple divider. This can provide output signals of approximately 500 kHz, 16 kHz, 490 Hz and 15 Hz.

Special Purpose Pins

The mode pins are sampled prior to configuration to determine the configuration mode and timing options. After configuration, these pins can be used as auxiliary connections: Mode 0 (MD0.I) and Mode 2 (MD2.I) as inputs and Mode 1 (MD1.O and MD1.T) as an output. The XACT development system will not use these resources unless they are explicitly specified in the design entry. These dedicated nets are located in the lower left chip corner and are near the readback nets. This allows convenient routing if compatibility with the XC2000 and XC3000 family conventions of M0/RT, M1/RD is desired.

Configuration Modes

Mode	M2	M1	M0	CCLK	Data
Master Serial	0	0	0	output	Bit-Serial
Slave Serial	1	1	1	input	Bit-Serial
Master Parallel up	1	0	0	output	Byte-Wide, 00000 ↑
Master Parallel down	1	1	0	output	Byte-Wide, 3FFFF↓
Peripheral Synchr.	0	1	1	input	Byte-Wide
Peripheral Asynchr.	1	0	1	output	Byte-Wide
Reserved	0	1	0	—	—
Reserved	0	0	1	—	—

"Peripheral Synchronous" can be considered "Slave Parallel"

CONFIGURATION

Configuration is the process of loading design-specific programming data into one or more LCA devices to define the functional operation of the internal blocks and their interconnections. This is somewhat like loading the command registers of a programmable peripheral chip. The XC4000 family uses about 350 bits of configuration data per CLB and its associated interconnects. Each configuration bit defines the state of a static memory cell that controls either a function look-up table bit, a multiplexer input, or an interconnect pass transistor. The XACT development system translates the design into a netlist file. It automatically partitions, places and routes the logic and generates the configuration data in PROM format.

Modes

The XC4000 family has six configuration modes selected by a 3- bit input code applied to the M0, M1, and M2 inputs. There are three self-loading Master modes, two Peripheral modes and the Serial Slave mode used primarily for daisy-chained devices. During configuration, some of the I/O pins are used temporarily for the configuration process.

Master

The Master modes use an internal oscillator to generate CCLK for driving potential slave devices, and to generate address and timing for external PROM(s) containing the configuration data. Master Parallel (up or down) modes generate the CCLK signal and PROM addresses and receive byte parallel data, which is internally serialized into the LCA data-frame format. The up and down selection generates starting addresses at either zero or 3FFFF, to be compatible with different microprocessor addressing conventions. The Master Serial mode generates CCLK and receives the configuration data in serial form from a Xilinx serial-configuration PROM.

Peripheral

The two Peripheral modes accept byte-wide data from a bus. A READY/BUSY status is available as a handshake signal. In the asynchronous mode, the internal oscillator generates a CCLK burst signal that serializes the byte-wide data. In the synchronous mode, an externally supplied clock input to CCLK serializes the data.

Serial Slave

In the Serial Slave mode, the LCA device receives serial-configuration data on the rising edge of CCLK and, after loading its configuration, passes additional data out, resynchronized on the next falling edge of CCLK. Multiple slave devices with identical configurations can be wired with parallel DIN inputs so that the devices can be configured simultaneously.

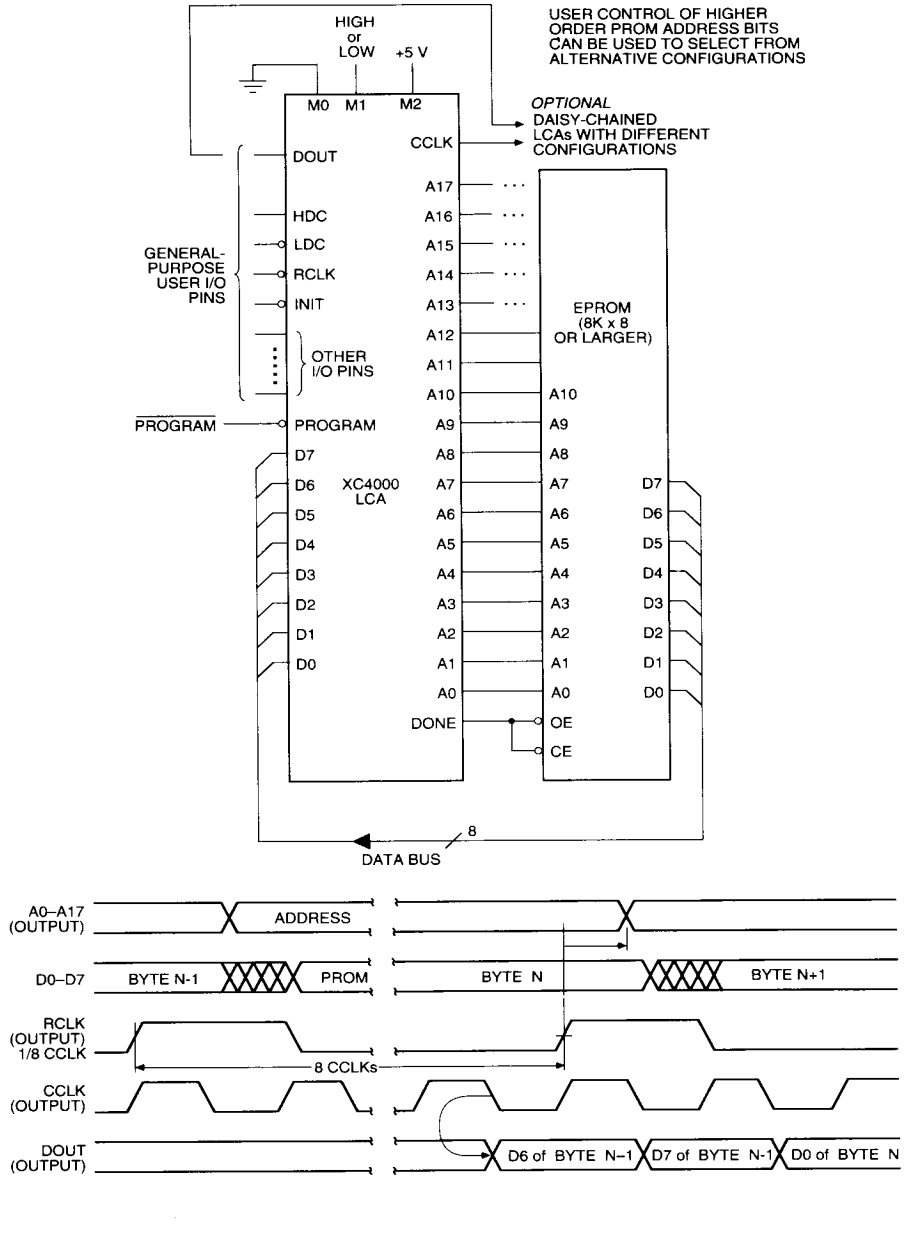


Figure 19. Master Parallel Mode.

Configuration data are loaded automatically from an external byte wide PROM.
An early DONE inhibits the PROM outputs a CCLK cycle before the LCA I/Os become active.

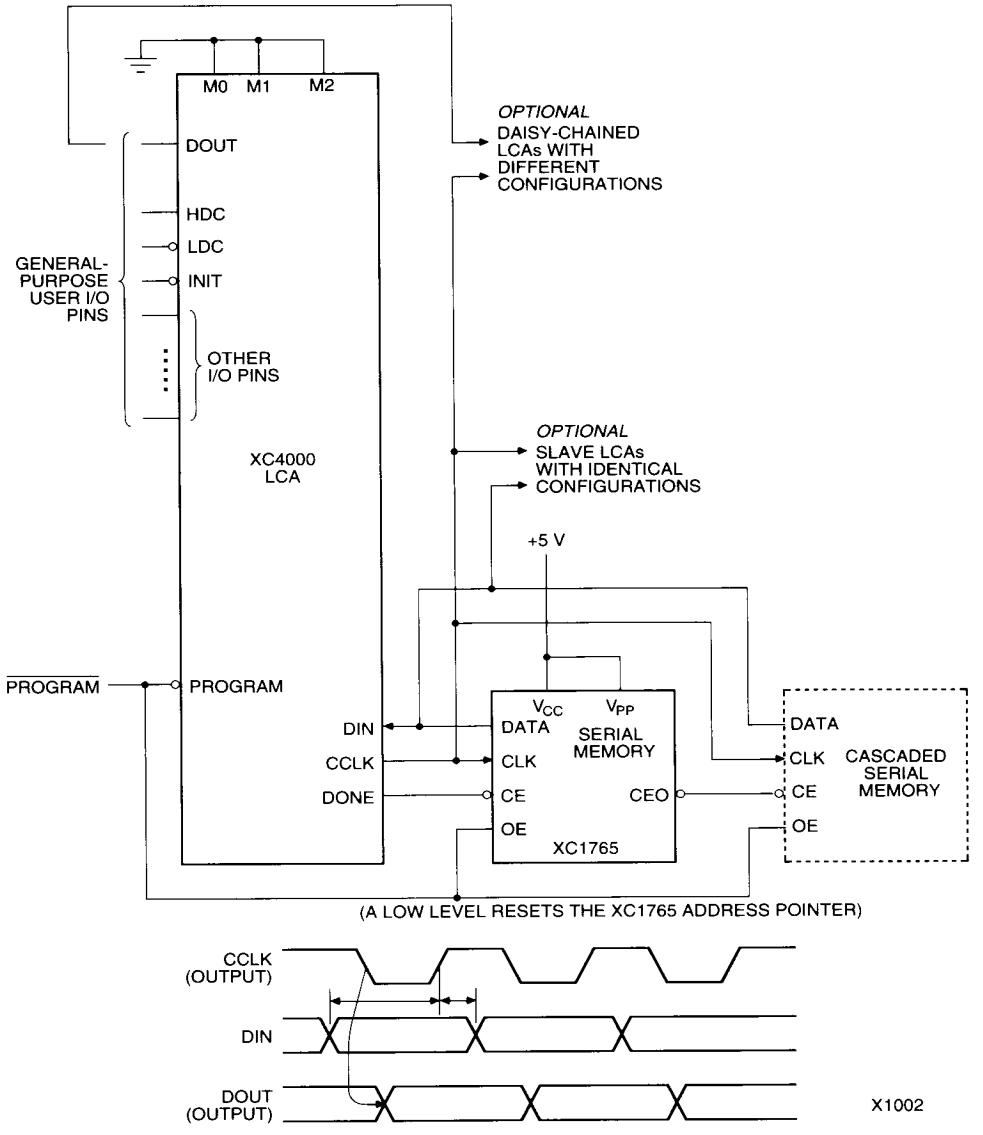


Figure 20. Master Serial Mode.

The one-time-programmable XC1765 Serial Configuration PROM supports automatic loading of configuration programs up to 65K bits. Multiple PROMs can be cascaded to support additional LCAs. An early DONE inhibits the PROM data output a CCLK cycle before the LCA I/Os become active, thus avoiding contention if DIN is used as a user output

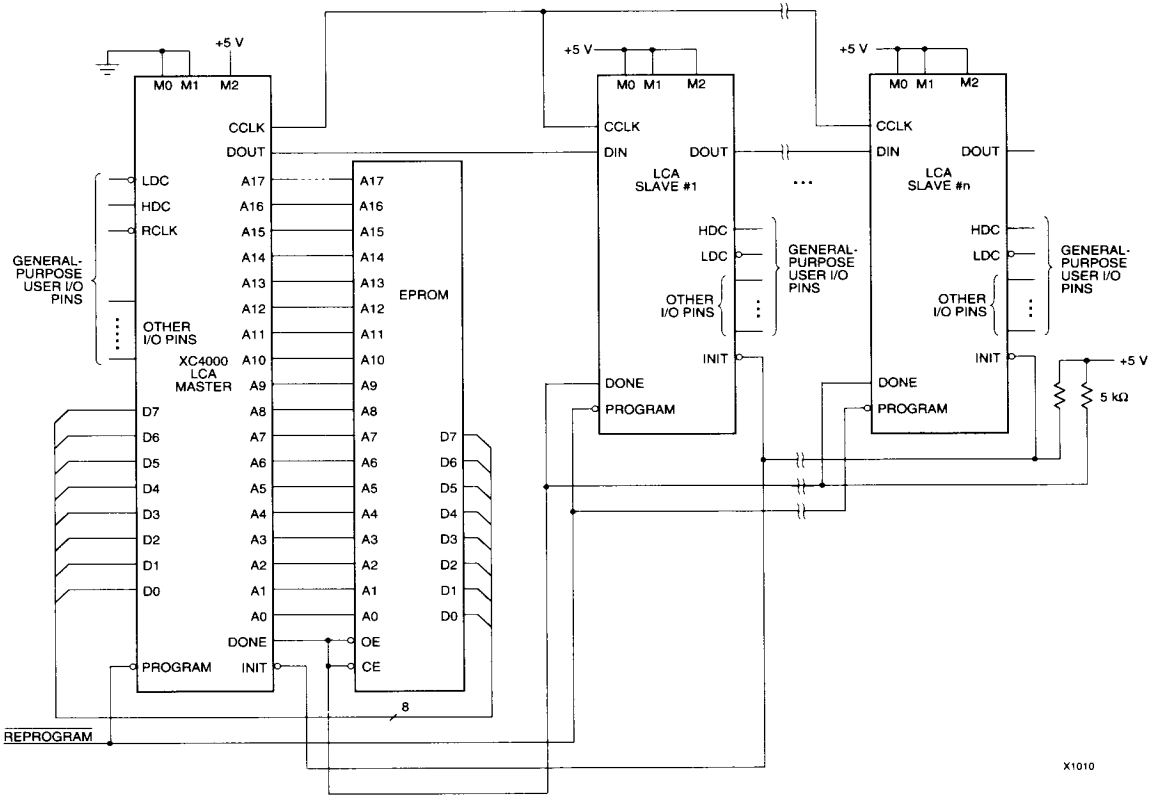


Figure 21. Master-Mode Configuration with Daisy-Chained Slave-Mode Devices.
All are configured from the common EPROM source. The Slave mode device INIT signals are wire-ANDed to delay the XC4000 Master device configuration until all slaves are initialized.
For XC2000 or XC3000 slave devices it is necessary to cycle their D/$\overline{P}$ and $\overline{RESET}$ to reprogram.
Since XC2000 devices do not have an $\overline{INIT}$ output to hold off the master device, the equivalent function must be performed by an external timing device.

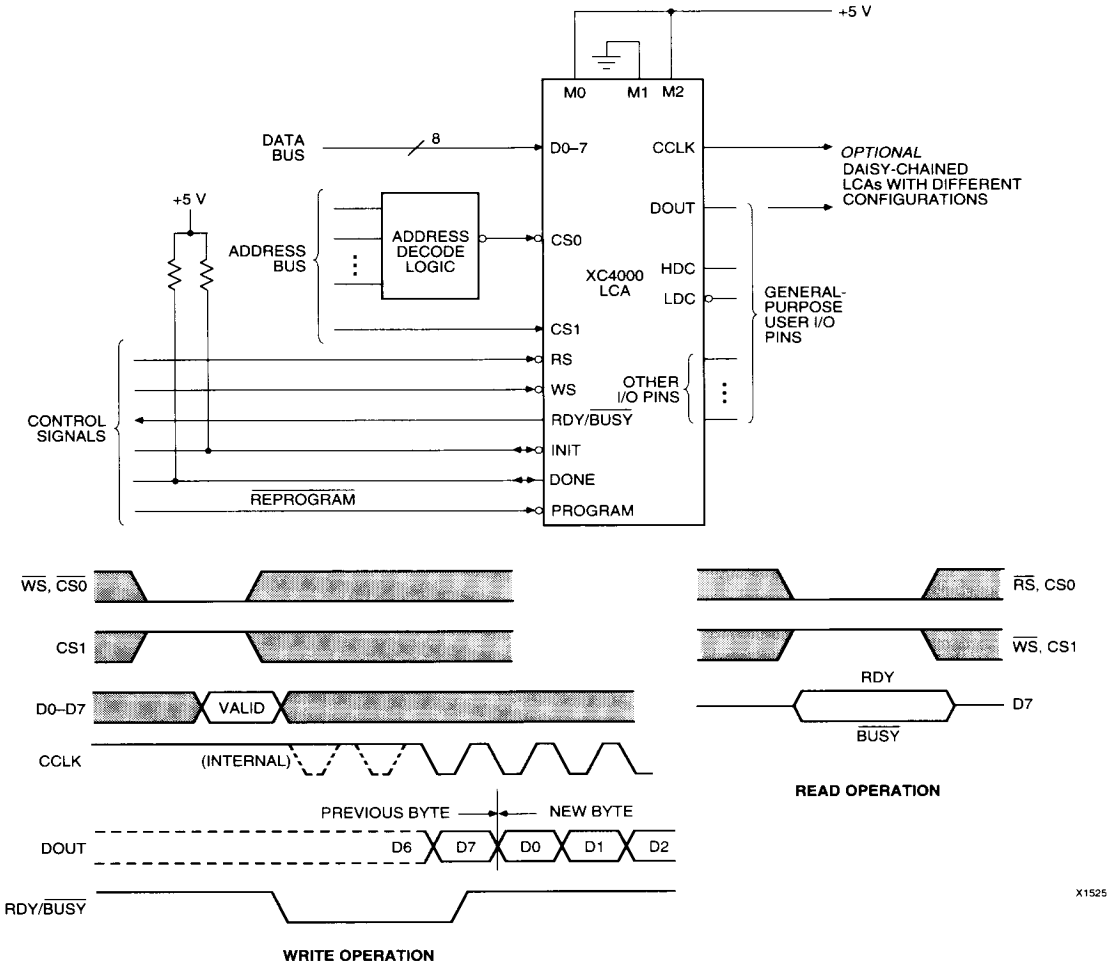


Figure 22. Peripheral Asynchronous Mode.

The trailing edge of the Write Strobe (WS and CS0 Low, CS1 High) loads a configuration byte into the D0-D7 inputs, and acknowledges this with a Low level on RDY/BUSY.

The parallel byte is serialized internally and shifted into the internal configuration latches.

It can also appear in serial form on the DOUT output.

RDY/BUSY goes High when the byte has been transferred into the internal shift register.

This may take as little as two or as many as nine CCLK cycles, depending on the state of the double-buffered parallel-to-serial converter.

When RS is active instead of WS, D7 becomes a READY/BUSY status output, convenient for a byte-wide microprocessor interface.

For timing parameters see page 50.

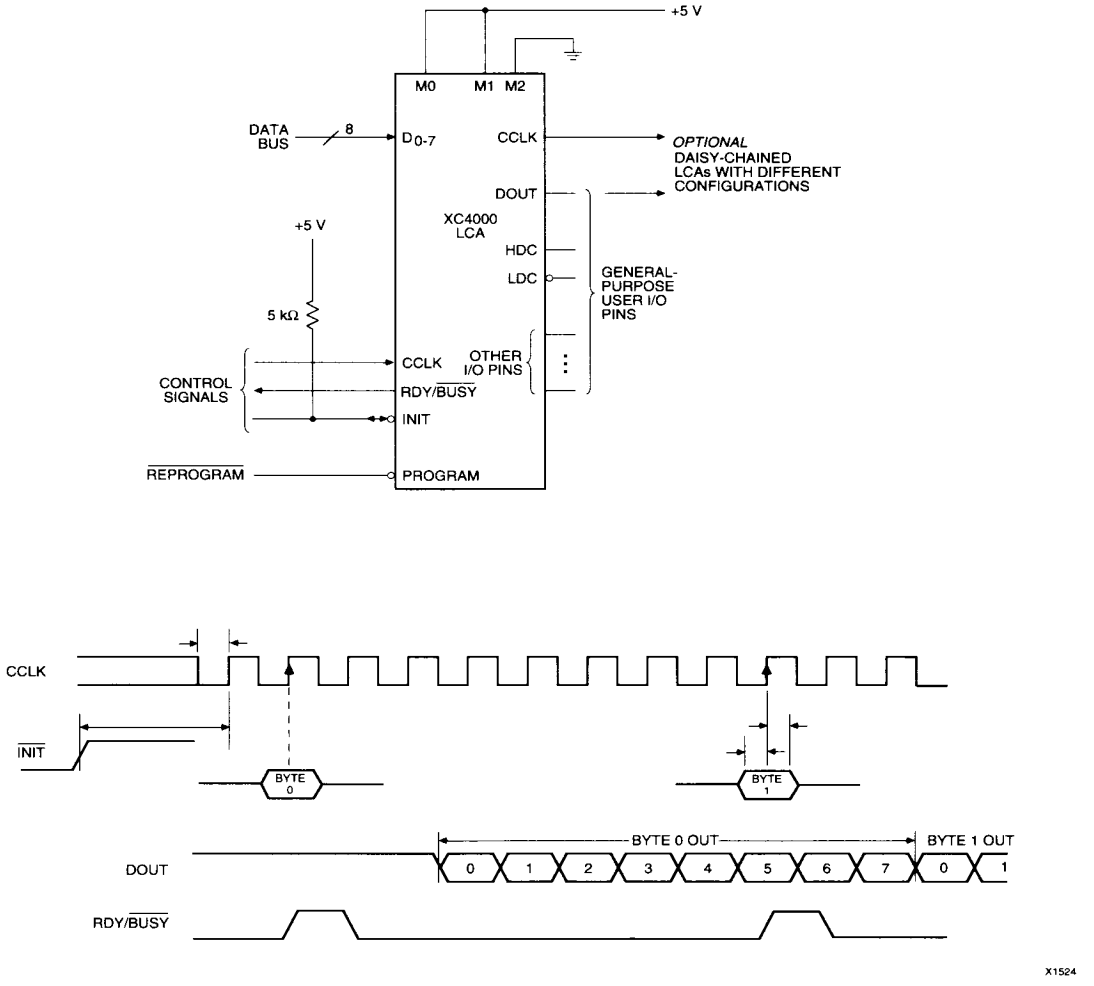


Figure 23. Peripheral Synchronous Mode

It can be considered Slave Parallel mode.
An external CCLK provides timing, clocking in the **first** data byte on the **second** rising edge of CCLK after $\overline{INIT}$ goes High.
Subsequent data bytes are clocked in on every eighth consecutive rising edge of CCLK.
The RDY/$\overline{BUSY}$ line goes High for one CCLK period after data has been clocked in, although synchronous operation does not require such a response.
The pin name RDY/$\overline{BUSY}$ is a misnomer; in Synchronous Peripheral mode this is really an ACKNOWLEDGE signal.

Note that data starts to shift out serially on the DOUT pin 2.5 CLK periods after it was loaded in parallel.
This obviously requires additional CCLK pulses after the last byte has been loaded.

For timing parameters see page 51.

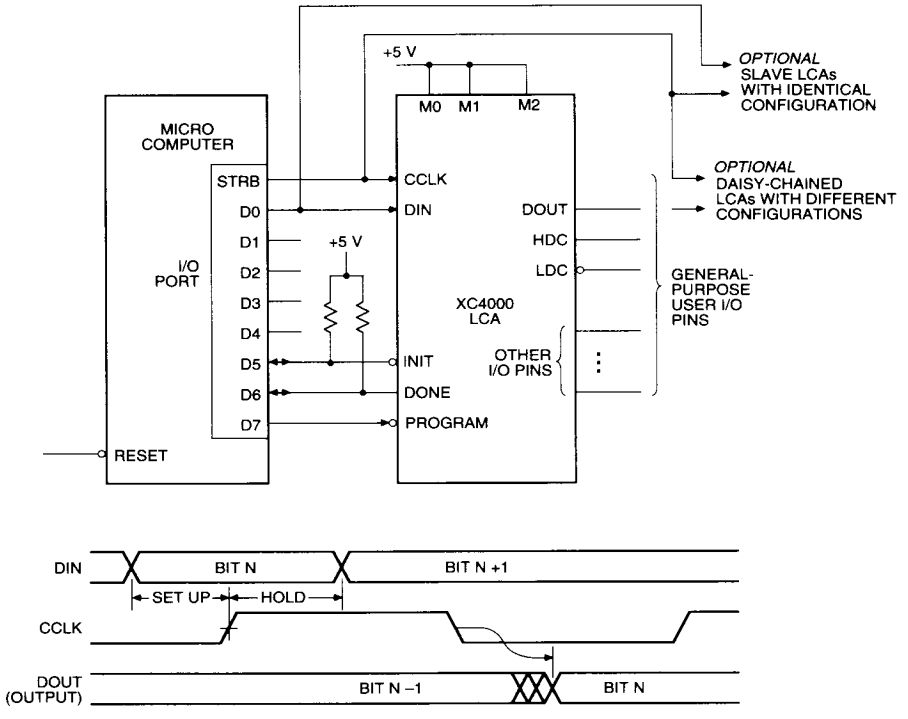
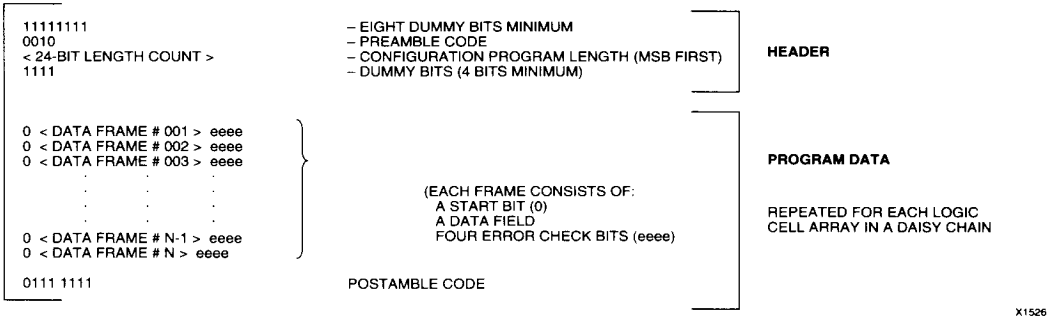


Figure 24. Slave Mode.
Bit-serial configuration data are read at rising edge of the CCLK.
Data on DOUT are provided on the falling edge of CCLK.



Device	XC4002	XC4003	XC4004	XC4005	XC4006	XC4008	XC4010
Gates	2,000	3,000	4,000	5,000	6,000	8,000	10,000
CLBs (Row x Col)	64 (8 x 8)	100 (10 x 10)	144 (12 x 12)	196 (14 x 14)	256 (16 x 16)	324 (18 x 18)	400 (20 x 20)
IOBs	64	80	96	112	128	144	160
Flip-flops	256	360	480	616	768	936	1120
Horizontal TBUF Long Lines	16	20	24	28	32	36	40
TBUFs per Long Line	10	12	14	16	18	20	22
Bits per Frame	106	126	146	166	186	206	226
Frames	356	428	500	572	644	716	788
Program Data	37,744	53,936	73,008	94,960	119,792	147,504	178,096
PROM size (bits)	37,784	53,976	73,048	95,000	119,832	147,544	178,136

Bits per Frame = (10 x number of Rows) + 7 for the top + 13 for the bottom + 1 + 1 start bit + 4 error check bits
Number of Frames = (36 x number of Columns) + 26 for the left edge + 41 for the right edge + 1
Program Data = (Bits per Frame x Number of Frames) + 8 postamble bits
PROM Size = Program Data + 40
The user can add more "one" bits as leading dummy bits in the header, or as trailing dummy bits at the end of any frame, following the four error check bits, but the Length Count value **must** be adjusted for all such extra "one" bits, even for leading extra ones at the beginning of the header.

Figure 25. Internal Configuration Data Structure.

Format

The configuration-data stream begins with a string of ones, a 0010 preamble code, a 24-bit length count, and a 4-bit separator field of ones. This is followed by the actual configuration data in frames, each starting with a zero bit and ending with a 4-bit Cyclic Redundancy Check (CRC). The length and number of data frames depend on the LCA device type. Multiple LCA devices can be connected in a daisy chain by wiring their CCLK pins in parallel and connecting the DOUT of each to the DIN of the next. The lead-master LCA device and following slaves each passes resynchronized configuration data coming from a single source. The Header data, including the length count, is passed through and is captured by each LCA device when it recognizes the 0010 preamble. Following the length-count data, any LCA device outputs a High on DOUT until it has received its required number of data frames.

After an LCA device has received its configuration data, it passes on any additional frame start bits and configuration data on DOUT. When the total number of configuration clocks applied after memory initialization equals the value of the 24-bit length count, the LCA device(s) begin the start-up sequence and become operational together.

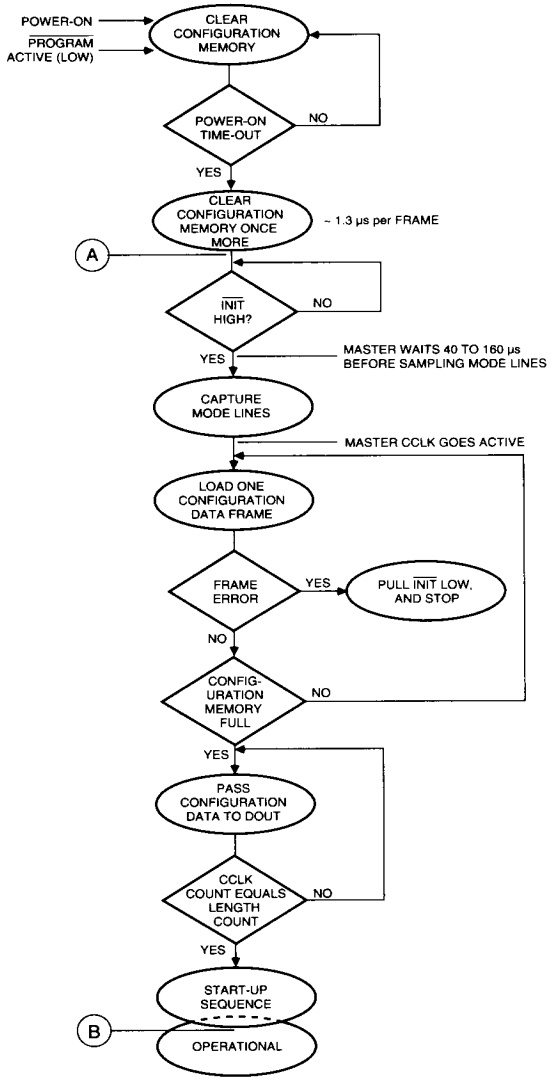


Figure 26. Flow Chart

Boundary Scan	at A	Between A-B	After B
Extest	✓	no	If Selected
Sample Bypass	✓	✓	If Selected
User	no	no	If Selected
Readback	no	no	✓

Opportunities for Boundary Scan and Readback Operations

Configuration Sequence

Configuration Memory Clear

When power is first applied or re-applied to an LCA device, an internal circuit forces initialization of the configuration logic. When Vcc reaches an operational level, and the circuit passes the write and read test of a sample pair of configuration bits, a nominal 22-ms time delay is started (four times longer when M0 is Low, i.e., in Master mode). During this time delay, or as long as the PROGRAM input is asserted, the configuration logic is held in a Configuration Memory Clear state. The configuration-memory frames are consecutively initialized, using the internal oscillator. At the end of each complete pass through the frame addressing, the power-on time-out delay circuitry and the level of the PROGRAM pin are tested. If neither is asserted, the logic initiates one additional clearing of the configuration frames and then tests the INIT input.

Initialization

During initialization and configuration, user pins HDC, LDC and INIT provide status outputs for system interface. The outputs, LDC, INIT and DONE are held Low and HDC is held High starting at the initial application of power. The open drain INIT pin is released after the final initialization pass through the frame addresses. There is a deliberate delay of 40 to 160 µs before a Master-mode device recognizes an inactive INIT. Two internal clocks after the INIT pin is recognized as High, the LCA device samples the three mode lines to determine the configuration mode. The appropriate interface lines become active and the configuration preamble and data can be loaded.

Configuration

The 0010 preamble code indicates that the following 24 bits represent the length count, i.e., the total number of configuration clocks needed to load the total configuration data. After the preamble and the length count have been passed through to all devices in the daisy chain, DOUT is held High to prevent frame start bits from reaching any daisy-chained devices. A specific configuration bit, early in the first frame of a master device, controls the configuration-clock rate and can increase it by a factor of eight. Each frame has a Low start bit followed by the frame-configuration data bits and a 4-bit frame error field. If a frame data error is detected, the LCA device halts loading, and signals the error by pulling the open-drain INIT pin Low.

After all configuration frames have been loaded into an LCA device, DOUT again follows the input data so that the remaining data is passed on to the next device.

START-UP

Start-up is the transition from the configuration process to the intended user operation. This means a change from one clock source to another, and a change from interfacing parallel or serial configuration data where most outputs are 3-stated, to normal operation with I/O pins active in the user-system. Start-up must make sure that the user-logic "wakes up" gracefully, that the outputs become active without causing contention with the configuration signals, and that the internal flip-flops are released from the global Reset or Set at the right time.

Figure 27 describes Start-up timing for the three Xilinx families in detail.

The **XC2000** family goes through a fixed sequence:
DONE goes High and the internal global Reset is de-activated one CCLK period after the I/O become active.

The **XC3000** family offers some flexibility:
DONE can be programmed to go High one CCLK period before or after the I/O become active. Independent of DONE, the internal global Reset is de-activated one CCLK period before or after the I/O become active.

The **XC4000** family offers additional flexibility:
The three events, DONE going High, the internal Reset/Set being de-activated, and the user I/O going active, can all occur in any arbitrary sequence, each of them one CCLK period before or after, or simultaneous with, any of the other.

The default option, and the most practical one, is for DONE to go High first, disconnecting the configuration data source and avoiding any contention when the I/Os become active one clock later. Reset/Set is then released another clock period later to make sure that user-operation starts from stable internal conditions. This is the most common sequence, shown with heavy lines in Figure 27, but the designer can modify it to meet particular requirements.

The XC4000 family offers another start-up clocking option:
The three events described above don't have to be triggered by CCLK, they can, as a configuration option, be triggered by a user clock. This means that the device can wake up in synchronism with the user system.

The XC4000 family introduces an additional option:
When this option is enabled, the user can externally hold the open-drain DONE output Low, and thus stall all further progress in the Start-up sequence, until DONE is released and has gone High. This option can be used to force synchronization of several LCA devices to a common user clock, or to guarantee that all devices are successfully configured before any I/Os go active.

Start-up Sequence

The Start-up sequence begins when the configuration memory is full, and the total number of configuration clocks received since INIT went High equals the loaded value of the length count. The next rising clock edge sets a flip-flop Q0 (see Figure 28), the leading bit of a 5-bit shift register. The outputs of this register can be programmed to control three events.

- The release of the open-drain DONE output,
- The change of configuration-related pins to the user function, activating all IOBs.
- The termination of the global Set/Reset initialization of all CLB and IOB storage elements.

The DONE pin can also be wire-ANDed with DONE pins of other LCA devices or with other external signals, and can then be used as input to bit Q3 of the start-up register. This is called "Start-up Timing Synchronous to Done In" and labeled: CCLK_SYNC or UCLK_SYNC. When DONE is not used as an input, the operation is called "Start-up Timing Not Synchronous to DONE In", and is labeled CCLK_NOSYNC or UCLK_NOSYNC. These labels are not intuitively obvious.

As a configuration option, the start-up control register beyond Q0 can be clocked either by subsequent CCLK pulses or from an on-chip user net called STARTUP.CLK.

Start-up from CCLK

If CCLK is used to drive the start-up, Q0 through Q3 provide the timing. Heavy lines in Figure 27 show the default timing which is compatible with XC2000 and XC3000 devices using early DONE and late Reset.The thin lines indicate all other possible timing options.

Start-up from a User Clock (STARTUP.CLK)

When, instead of CCLK, a user-supplied start-up clock is selected, Q1 is used to bridge the unknown phase relationship between CCLK and the user clock. This arbitration causes an unavoidable one-cycle uncertainty in the timing of the rest of the start-up sequence.

Using Global Set/Reset and Global 3-State Nets:

The global Set/Reset (STARTUP.GSR) net can be driven by the user at any time to re-initialize all CLBs and IOBs to the same state they had at the end of configuration. For CLBs that is the same state as the one driven by the individually programmable asynchronous Set/Reset inputs. The global 3-state net (STARTUP.GTS), whenever activated after configuration is completed, forces all LCA outputs to the high-impedance state, unless Boundary Scan is enabled and is executing an Extest instruction.

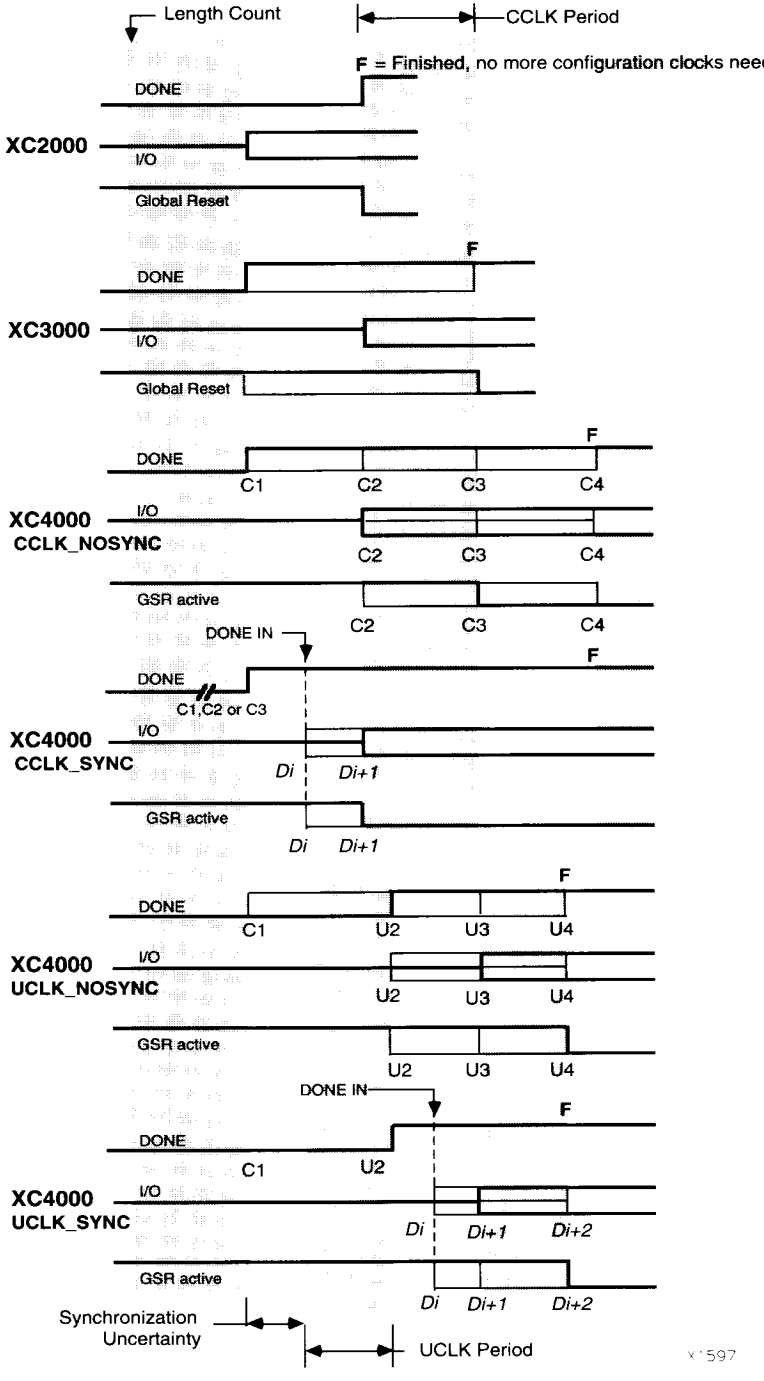


Figure 27 Start-up Timing

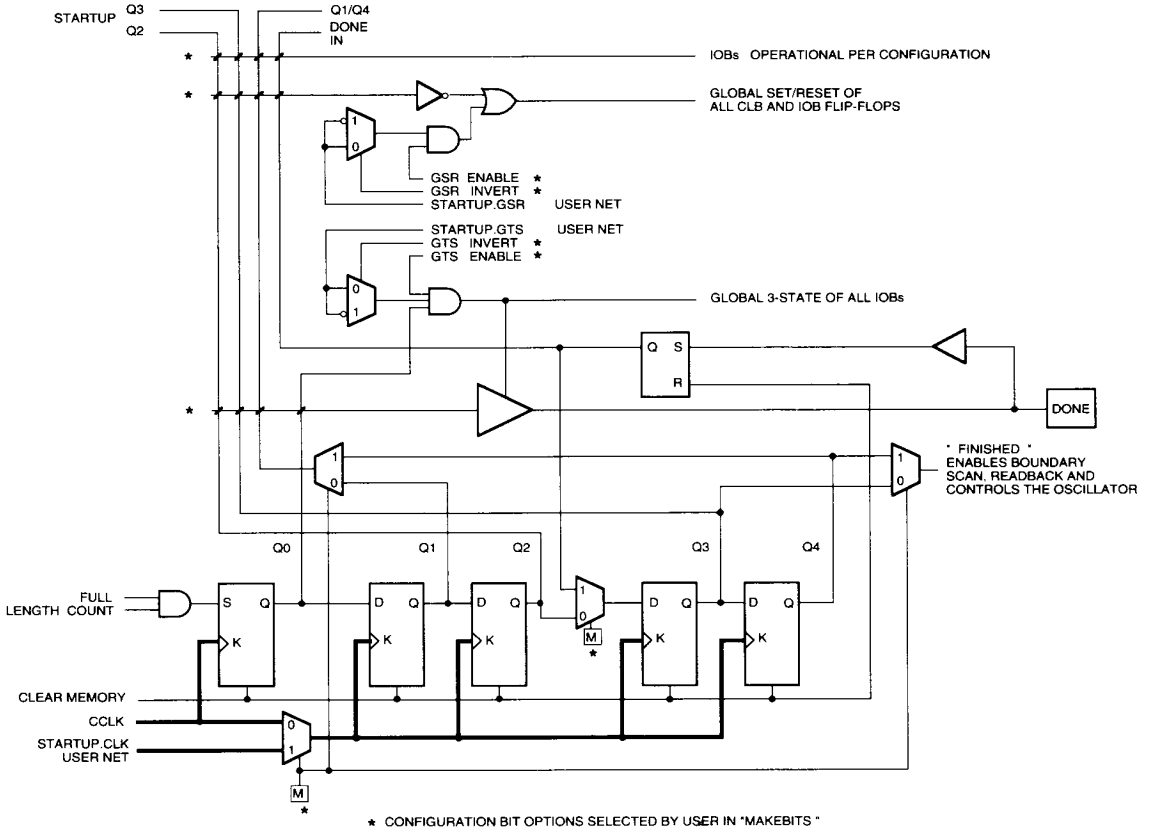


Figure 28. Start-up Logic

READBACK

The user can read back the content of configuration memory and the level of certain internal nodes without interfering with the normal operation of the device.

Readback reports not only the downloaded configuration bits, but can also include the present state of the device represented by the content of all used flip-flops and latches in CLBs and IOBs, as well as the content of function generators used as RAMs.

XC4000 Readback does not use any dedicated pins, but uses four internal nets (RDBK.TRIG, RDBK.DATA, RDBK.RIP and RDBK.CLK) that can be routed to any IOB.

After Readback has been initiated by a Low-to-High transition on RDBK.TRIG, the RDBK.RIP (Read In Progress) output goes High on the next rising edge of RDBK.CLK. Subsequent rising edges of this clock shift out Readback data on the RDBK.DATA net. Readback data does not include the preamble, but starts with five dummy bits (all High) followed by the Start bit (Low) of the first frame. The first two data bits of the first frame are always High.

Note that, in the XC4000, data is not inverted with respect to configuration the way it is in XC2000 and XC3000.

Each frame ends with four error check bits. They are read back as High. The last seven bits of the last frame are also read back as High. An additional Start bit (Low) and an 11-bit Cyclic Redundancy Check (CRC) signature follow, before RIP returns Low.

Readback options are: Read Capture, Read Abort, and Clock Select.

Read Capture

When the Readback Capture option is selected, the readback data stream includes sampled values of CLB and IOB signals imbedded in the data stream. The rising edge of RDBK.TRIG located in the lower-left chip corner, captures, in latches, the inverted values of the four CLB outputs and the IOB output flip-flops and the input signals I1, I2. When the capture option is not selected, the values of the capture bits reflect the configuration data originally written to those memory locations. If the RAM capability of the CLBs is used, RAM data are available in readback, since they directly overwrite the F and G function-table configuration of the CLB.

Read Abort

When the Readback Abort option is selected, a High-to-Low transition on RDBK.TRIG terminates the readback operation and prepares the logic to accept another trigger. After an aborted readback, additional clocks (up-to-one readback clock per configuration frame) may be required to re-initialize the control logic. The status of readback is indicated by the output control net (RDBK.RIP).

Clock Select

Readback control and data are clocked on rising edges of RDBK.CLK located in the lower left chip corner. CCLK is an optional clock. If Readback must be inhibited for security reasons, the readback control nets are simply not connected.

XChecker

The XChecker Universal Download/Readback Cable and Logic Probe uses the Readback feature for bitstream verification and for display of selected internal signals on the PC or workstation screen, effectively as a low-cost in-circuit emulator.

APPLICATIONS

The following application examples highlight the two most important innovative features of the XC4000 family: fast carry and distributed RAM. The XC4000 family can also implement any other logic designs, including those with internal 3-state buses, or designs with wide address decoders. Since the logic capabilities in the XC4000 are a superset of the XC3000, any existing XC3000 design can easily be converted to the XC4000 family. Note, however, that the XC4000 family has no crystal oscillator circuit and no power-down.

16-bit Adder/Subtractor

When the Add/Subtract input is High, this design accepts two 16-bit two complement operands, A and B, and generates their sum. When the Add/Subtract input is Low, the circuit generates A minus B, also in 2's complement notation. The overflow/underflow output indicates when the result falls outside the possible range of $+(2^{15}-1)$ to -2^{15}.

As an accumulator, the circuit has only one 16-bit 2's complement operand input, A, that is synchronously added to or subtracted from the content of the accumulator register with outputs Q.

This design is available as a Hard Macro, i.e., as a design file with fixed lay-out, fixed signal routing, and guaranteed performance (9 CLBs, 38-MHz clock rate).

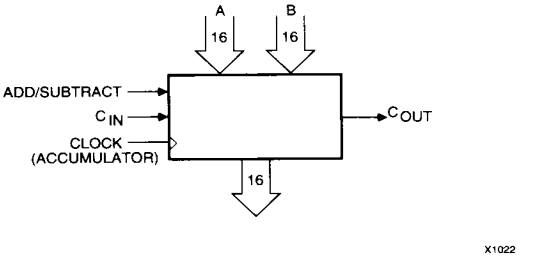


Figure 29. 16-Bit Adder/Subtractor Accumulator

32-Deep, 8-Wide Shift Register

This circuit emulates a shift register by using a RAM and an address counter. The rising clock edge transfers the content of the addressed RAM location into the lower CLB flip-flop. The same clock edge transfers the incoming data into the upper CLB flip-flop, from where it is written into the RAM while the Clock line, serving as a Write Enable, is High.

This design is available as a Hard Macro, i.e., as a design file with fixed lay-out, fixed signal routing, and guaranteed performance (11 CLBs, 30-MHz clock rate).

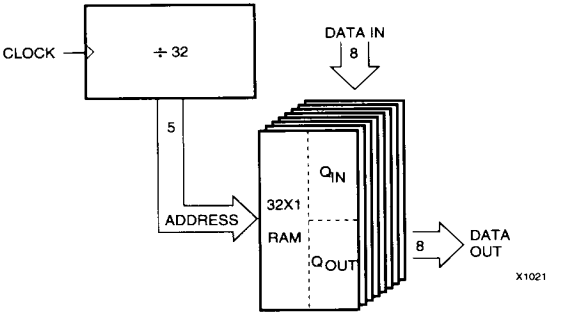


Figure 30. 32-Deep, 8-Wide Shift Register

16-Deep, 8-Bit Wide Register Stack

This register stack consists of a 16 x 8 RAM with an 8-bit wide register at the Read port. Input data available a few nanoseconds before the rising (trailing) edge of Write Enable = Clock is written into the memory location addressed by A0–3. The same rising clock edge transfers the content of the addressed memory location into the output register. This design is available as a hard macro, i.e., as a design file with fixed layout, fixed signal routing, and guaranteed performance (4 CLBs).

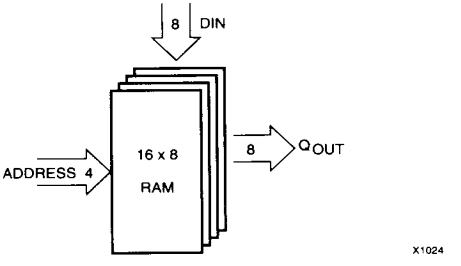


Figure 31. 16-Deep, 8-Wide Register Stack

16-bit Loadable Up/Down Counter

The operation of this 16-bit counter is determined by three control inputs, Count Enable (CE), Up/Down (U/D), and Parallel Enable (PE). PE overrides CE, and is unaffected by U/D.

PE	U/D	CE	
0	X	0	no change
0	0	1	count down
0	1	1	count up
1	X	X	load D into Q

AND is in the Terminal Count position appropriate for the count direction, i.e., when PE is Low, CE is High, and all Qs have the same level as U/D.

This design is available as a Hard Macro, i.e., as a design file with fixed lay-out, fixed signal routing, and guaranteed performance (16 CLBs, 30 MHz clock rate).

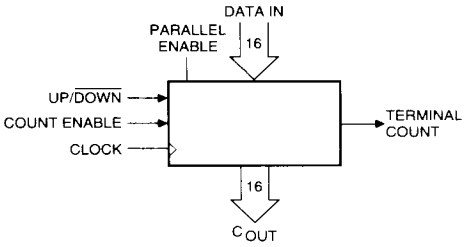


Figure 32. 16-Bit Up/Down Counter

A non-loadable version of this counter uses only eight CLBs and runs at up to 42 MHz. (See Table 3 on page 5.)

100 MHz, 24-Bit Programmable Frequency Divider

This frequency divider is a 24-bit down-counter that reloads a programmable value whenever it reaches the all-zero state (TC). To operate at the highest possible clock frequency, it employs a dual modulus ÷7/÷8 prescaler inside the LCA. This reduces the maximum clock frequency for most of the circuitry by a factor of 7.

With a simple ÷8 prescaler, the preset value would have to be an exact multiple of eight, and this would reduce the effective resolution of the counter to 21 bits. However, a ÷7/÷8 prescaler may be controlled to give the full 24-bit resolution, with some isolated exceptions.

There are 21 divide ratios which cannot be achieved with a ÷7/÷8 prescaler. These are:

1,	2,	3,	4,	5,	6,
9,	10,	11,	12,	13,	
17,	18,	19,	20,		
25,	26,	27,			
33,	34,				
41.					

Except for these values, the counter can divide by any integer up to 16,777,216.

This frequency divider can be used in a phase-locked loop frequency synthesizer. It could also generate programmable delays with 10 ns resolution. Any delay could be generated in the range 0.42 µs, 0.43 µs... 167,772.16 µs.

This circuit uses 16 CLBs. For a more detailed description see the macro library.

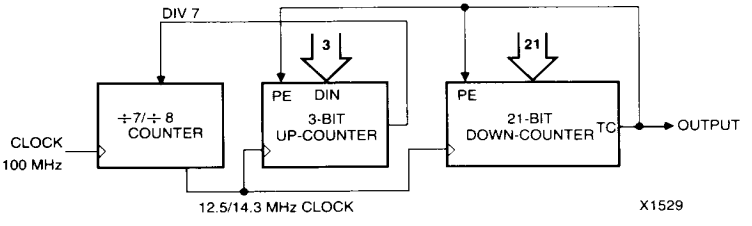


Figure 33. 24-Bit Frequency Division with State-Skipping Prescaler

16-Deep, 8-bit Wide First-In-First-Out Memory

Internally, this is a synchronous design, but it works with an external handshake interface. A Read Request is clocked in on the rising clock edge, and is answered with a Read Acknowledge starting on the first rising clock edge after any potential conflict has been eliminated.

A Write Request is clocked in and acknowledged in a similar manner. Simultaneous Read/Write requests while the RAM is not empty are executed as Read first, Write next. Simultaneous Read/Write requests while the RAM is empty are executed as Write first, Read next. A Read Request from an empty memory, or a Write Request to a full memory will not be acknowledged.

This design is available as a Hard Macro, i.e. as a design file with fixed lay-out, fixed signal routing, and guaranteed performance.

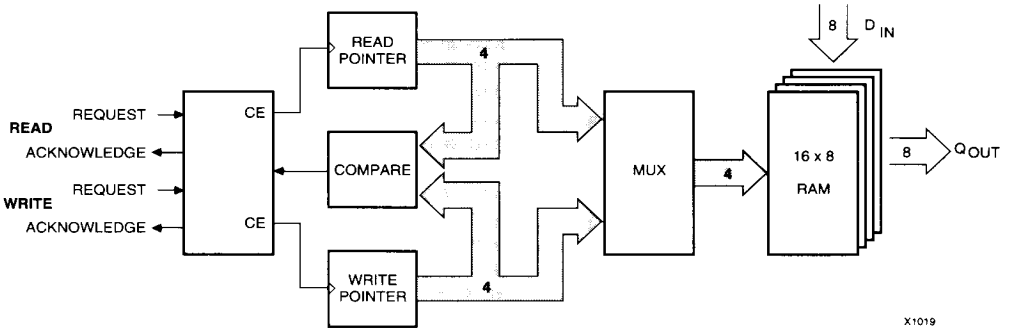


Figure 34. 16-Deep, 8-Wide FIFO

Waveform Generator

This circuit generates a programmable repetitive waveform, e.g., a sine wave, specified with eight bits of amplitude resolution and six bits of timing resolution per output period. The output frequency can be programmed in 1-Hz increments, covering a range from 1 Hz to >1 MHz, using a 20-bit binary input.

The 20-bit accumulator runs at 2^{26} Hz, that is, 67.108864 MHz. Whenever it overflows, it increments a 6-bit counter that addresses a 6-bit to 8-bit table-look-up code converter. The table stores 64 samples of the desired waveform, expressed as an 8-bit digital word, to be converted in an external Digital-to-Analog converter. When the output waveform is symmetrical, the look-up table can be simplified, down to 32 or only 16 samples per period.

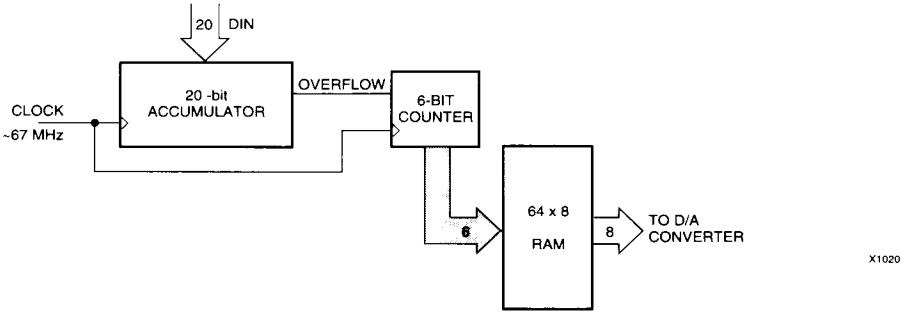


Figure 35. 1 MHz Waveform Generator

XC4000 Family Configuration Pin Assignments

CONFIGURATION MODE: <M2:M1:M0>						
SLAVE <1:1:1>	MASTER-SER <0:0:0>	PERIPH.SYN <0:1:1>	PERIPH.ASYN <1:0:1>	MASTER-HIGH <1:1:0>	MASTER-LOW <1:0:0>	USER OPERATION
				A16	A16	PGI-I/O
				A17	A17	I/O
TDI	TDI	TDI	TDI	TDI	TDI	TDI-I/O
TCK	TCK	TCK	TCK	TCK	TCK	TCK-I/O
TMS	TMS	TMS	TMS	TMS	TMS	TMS-I/O
						SGI-I/O
M1 (HIGH) (I)	M1 (LOW) (I)	M1 (HIGH) (I)	M1 (LOW) (I)	M1 (HIGH) (I)	M1 (LOW) (I)	(O)
M0 (HIGH) (I)	M0 (LOW) (I)	M0 (HIGH) (I)	M0 (HIGH) (I)	M0 (LOW) (I)	M0 (LOW) (I)	(I)
M2 (HIGH) (I)	M2 (LOW) (I)	M2 (LOW) (I)	M2 (HIGH) (I)	M2 (HIGH) (I)	M2 (HIGH) (I)	(I)
						PGI-I/O
HDC (HIGH)	HDC (HIGH)	HDC (HIGH)	HDC (HIGH)	HDC (HIGH)	HDC (HIGH)	I/O
LDC (LOW)	LDC (LOW)	LDC (LOW)	LDC (LOW)	LDC (LOW)	LDC (LOW)	I/O
$\overline{\text{INIT-ERROR}}$	$\overline{\text{INIT-ERROR}}$	$\overline{\text{INIT-ERROR}}$	$\overline{\text{INIT-ERROR}}$	$\overline{\text{INIT-ERROR}}$	$\overline{\text{INIT-ERROR}}$	I/O
						SGI-I/O
DONE	DONE	DONE	DONE	DONE	DONE	DONE
$\overline{\text{PROGRAM}}$ (I)	$\overline{\text{PROGRAM}}$ (I)	$\overline{\text{PROGRAM}}$ (I)	$\overline{\text{PROGRAM}}$ (I)	$\overline{\text{PROGRAM}}$ (I)	$\overline{\text{PROGRAM}}$ (I)	$\overline{\text{PROGRAM}}$
		DATA 7 (I)	DATA 7 (I)	DATA 7 (I)	DATA 7 (I)	I/O
						PGI-I/O
		DATA 6 (I)	DATA 6 (I)	DATA 6 (I)	DATA 6 (I)	I/O
		DATA 5 (I)	DATA 5 (I)	DATA 5 (I)	DATA 5 (I)	I/O
			$\overline{\text{CS0}}$ (I)			I/O
		DATA 4 (I)	DATA 4 (I)	DATA 4 (I)	DATA 4 (I)	I/O
		DATA 3 (I)	DATA 3 (I)	DATA 3 (I)	DATA 3 (I)	I/O
			$\overline{\text{RS}}$ (1)			I/O
		DATA 2 (I)	DATA 2 (I)	DATA 2 (I)	DATA 2 (I)	I/O
		$\overline{\text{DATA 1}}$ (I)	$\overline{\text{DATA 1}}$ (I)	$\overline{\text{DATA 1}}$ (I)	$\overline{\text{DATA 1}}$ (I)	I/O
		RDY/$\overline{\text{BUSY}}$	RDY/$\overline{\text{BUSY}}$	$\overline{\text{RCLK}}$	$\overline{\text{RCLK}}$	I/O
DIN (I)	DIN (I)	DATA 0 (I)	DATA 0 (I)	DATA 0 (I)	DATA 0 (I)	I/O
DOUT	DOUT	DOUT	DOUT	DOUT	DOUT	SGI-I/O
CCLK (I)	CCLK (I)	CCLK (O)	CCLK (I)	CCLK	CCLK	CCLK (I)
TDO	TDO	TDO	TDO	TDO	TDO	TDO-(O)
			$\overline{\text{WS}}$ (I)	A0	A0	I/O
				A1	A1	PGI-I/O
			CS1 (I)	A2	A2	I/O
				A3	A3	I/O
				A4	A4	I/O
				A5	A5	I/O
				A6	A6	I/O
				A7	A7	I/O
				A8	A8	I/O
				A9	A9	I/O
				A10	A10	I/O
				A11	A11	I/O
				A12	A12	I/O
				A13	A13	I/O
				A14	A14	I/O
				A15	A15	SGI-I/O

REPRESENTS A 50 kΩ TO 100 kΩ PULL-UP

* INIT IS AN OPEN-DRAIN OUTPUT DURING CONFIGURATION

(I)REPRESENTS AN INPUT

X1530.1

PIN DESCRIPTIONS

Permanently Dedicated Pins

V_{CC}

Eight or more (depending on package type) connections to the nominal +5 V supply voltage. All must be connected.

GND

Eight or more (depending on package type) connections to ground. All must be connected.

CCLK

During configuration, Configuration Clock is an output of the LCA in Master modes or asynchronous Peripheral mode, but is an input to the LCA in Slave mode and Synchronous Peripheral mode.

After configuration, CCLK has a weak pull-up resistor and can be selected as Readback Clock.

DONE

This is a bidirectional signal with optional pull-up resistor.

As an output, it indicates the completion of the configuration process. The configuration program determines the exact timing, the clock source for the Low-to-High transition, and enable of the pull-up resistor.

As an input, a Low level on DONE can be configured to delay the global logic initialization or the enabling of outputs

PROGRAM

This is an active Low input that forces the LCA to clear its configuration memory.

When PROGRAM goes High, the LCA finishes the current clear cycle and executes another complete clear cycle, before it goes into a WAIT state and releases INIT.

User I/O Pins that can have Special Functions

RDY/BUSY

During peripheral modes, this pin indicates when it is appropriate to write another byte of data into the LCA device. The same status is also available on D7 in asynchronous peripheral mode, if a read operation is performed when the device is selected. After configuration, this is a user-programmable I/O pin.

RCLK

During Master parallel configuration, this output indicates a read operation of an external dynamic memory device. This output is normally not used. After configuration, this is a user-programmable I/O pin.

M0, M1, M2

As Mode inputs, these pins are sampled before the start of configuration to determine the configuration mode to be used.

After configuration, M0 and M2 can be used as inputs, and M1 can be used as a 3-state output. These three pins have no associated input or output registers.

These pins can be user inputs or outputs only when called out by special schematic definitions.

TDO

If boundary scan is used, this is the Test Data Output.

If boundary scan is not used, this pin is a 3-state output without a register, after configuration is completed.

This pin can be user output only when called out by special schematic definitions.

TDI,TCK, TMS

If boundary scan is used, these pins are Test Data In, Test Clock, and Test Mode Select inputs respectively coming directly from the pads, bypassing theIOBs. These pins can also be used as inputs to the CLB logic after configuration is completed.

If the boundary scan option is not selected, all boundary scan functions are inhibited once configuration is completed, and these pins become user-programmable I/O.

Note:
The XC4000 has no Powerdown control input; use the global 3-state net instead.
The XC4000 has no dedicated Reset input. Any user I/O can be configured to drive the global Set/Reset net.

HDC

High During Configuration is driven High until configuration is completed. It is available as a control output indicating that configuration is not yet completed. After configuration, this is a user-programmable I/O pin.

LDC

Low During Configuration is driven Low until configuration. It is available as a control output indicating that configuration is not yet completed. After configuration, this is a user-programmable I/O pin.

$\overline{\text{INIT}}$

Before and during configuration, this is a bidirectional signal. An external pull-up resistor is recommended.

As an active-Low open-drain output, $\overline{\text{INIT}}$ is held Low during the power stabilization and internal clearing of the configuration memory. As an active-Low input, it can be used to hold the LCA device in the internal WAIT state before the start of configuration. Master mode devices stay in a WAIT state an additional 30 to 300 µs after INIT has gone High.

During configuration, a Low on this output indicates that a configuration data error has occurred. After configuration, this is a user-programmable I/O pin.

PGCK1 - PGCK4

Four Primary Global Inputs each drive a dedicated internal global net with short delay and minimal skew. If not used for this purpose, any of these pins is a user-programmable I/O.

SGCK1 - SGCK4

Four Secondary Global Inputs can each drive a dedicated internal global net, that alternatively can also be driven from internal logic. If not used for this purpose, any of these pins is a user-programmable I/O pin.

$\overline{\text{CS0}}$, CS1, WS, RS

These four inputs are used in Peripheral mode. The chip is selected when $\overline{\text{CS0}}$ is Low and CS1 is High. While the chip is selected, a Low on Write Strobe (WS) loads the data present on the D0 - D7 inputs into the internal data buffer; a Low on Read Strobe (RS) changes D7 into a status output: High if Ready, Low if Busy. WS and RS should be mutually exclusive, but if both are Low simultaneously, the Write Strobe overrides. After configuration, these are user-programmable I/O pins.

A0 - A17

During Master Parallel mode, these 18 output pins address the configuration EPROM. After configuration, these are user-programmable I/O pins.

D0 - D7

During Master Parallel and Peripheral configuration modes, these eight input pins receive configuration data. After configuration, they are user-programmable I/O pins.

DIN

During Slave Serial or Master Serial configuration modes, this is the serial configuration data input receiving data on the rising edge of CCLK.

During parallel configuration modes, this is the D0 input. After configuration, DIN is a user-programmable I/O pin.

DOUT

During configuration in any mode, this is the serial configuration data output that can drive the DIN of daisy-chained slave LCA devices. DOUT data changes on the falling edge of CCLK, one-and-a-half CCLK periods after it was received at the DIN input. After configuration, DOUT is a user-programmable I/O pin.

Unrestricted User-Programmable I/O Pins

I/O

A pin that can be configured to be input and/or output after configuration is completed. Before configuration is completed, these pins have an internal high-value pull-up resistor that defines the logic level as High.

XC4003 Pinouts

Pin Description	PC84	PQ100	PG120
VCC	2	92	G3
I/O (A8)	3	93	G1
I/O (A9)	4	94	F1
I/O	–	95	E1
I/O	–	96	F2
I/O (A10)	5	97	F3
I/O (A11)	6	98	D1
I/O (A12)	7	99	C1
I/O (A13)	8	100	D2
I/O (A14)	9	1	C2
SGCK1 (A15,I/O)	10	2	D3
VCC	11	3	C3
GND	12	4	C4
PGCK1 (A16,I/O)	13	5	B2
I/O (A17)	14	6	B3
I/O (TDI)	15	7	C5
I/O (TCK)	16	8	B4
I/O (TMS)	17	9	B5
I/O	18	10	A4
I/O	–	–	C6
I/O	–	11	A5
I/O	19	12	B6
I/O	20	13	A6
GND	21	14	B7
VCC	22	15	C7
I/O	23	16	A7
I/O	24	17	A8
I/O	–	18	A9
I/O	–	–	B8
I/O	25	19	C8
I/O	26	20	A10
I/O	27	21	B9
I/O	–	22	A11
I/O	28	23	C9
SGCK2 (I/O)	29	24	A12

Pin Description	PC84	PQ100	PG120
M1	30	25	B11
GND	31	26	C10
M0	32	27	C11
VCC	33	28	D11
M2	34	29	B12
PGCK2 (I/O)	35	30	C12
I/O (HDC)	36	31	A13
I/O	–	32	D12
I/O (LDC)	37	33	C13
I/O	38	34	E12
I/O	39	35	D13
I/O	–	36	F11
I/O	–	37	E13
I/O	40	38	F12
I/O ($\overline{ERR}$, $\overline{INIT}$)	41	39	F13
VCC	42	40	G12
GND	43	41	G11
I/O	44	42	G13
I/O	45	43	H13
I/O	–	44	J13
I/O	–	45	H12
I/O	46	46	H11
I/O	47	47	K13
I/O	48	48	J12
I/O	49	49	L13
I/O	50	50	M13
SGCK3 (I/O)	51	51	L12
GND	52	52	K11
DONE	53	53	L11
VCC	54	54	L10
$\overline{PROG}$	55	55	M12
I/O (D7)	56	56	M11
PGCK3 (I/O)	57	57	N13
I/O (D6)	58	58	M10
I/O	–	59	N11

Pin Description	PC84	PQ100	PG120
I/O (D5)	59	60	M9
I/O ($\overline{CS0}$)	60	61	N10
I/O	–	62	L8
I/O	–	63	N9
I/O (D4)	61	64	M8
I/O	62	65	N8
VCC	63	66	M7
GND	64	67	L7
I/O (D3)	65	68	N7
I/O ($\overline{RS}$)	66	69	N6
I/O	–	70	N5
I/O	–	–	M6
I/O (D2)	67	71	L6
I/O	68	72	N4
I/O (D1)	69	73	M5
I/O ($\overline{RCLK}$-$\overline{BUSY}$/RDY)	70	74	N3
I/O (D0, DIN)	71	75	N2
SGCK4 (DOUT,I/O)	72	76	M3
CCLK	73	77	L4
VCC	74	78	L3
TD0	75	79	M2
GND	76	80	K3
I/O (A0, $\overline{WS}$)	77	81	L2
PGCK4 (A1,I/O)	78	82	N1
I/O (CS1, A2)	79	83	K2
I/O (A3)	80	84	L1
I/O (A4)	81	85	J2
I/O (A5)	82	86	K1
I/O	–	87	H3
I/O	–	88	J1
I/O (A6)	83	89	H2
I/O (A7)	84	90	H1
GND	1	91	G2

XC4005 Pinouts

Pin Description	PC84	PQ160	PG156
VCC	2	142	H3
I/O (A8)	3	143	H1
I/O (A9)	4	144	G1
I/O	–	145	G2
I/O	–	146	G3
I/O (A10)	5	147	F1
I/O (A11)	6	148	F2
I/O	–	149	E1
I/O	–	150	E2
GND	–	151	F3
–	–	152*	D1*
–	–	153*	D2*
I/O (A12)	7	154	E3
I/O (A13)	8	155	C1
I/O	–	156	C2
I/O	–	157	D3
I/O (A14)	9	158	B1
SGCK1 (A15,I/O)	10	159	B2
VCC	11	160	C3
GND	12	1	C4
PGCK1 (A16,I/O)	13	2	B3
I/O (A17)	14	3	A1
I/O	–	4	A2
I/O	–	5	C5
I/O (TDI)	15	6	B4
I/O (TCK)	16	7	A3
–	–	8*	A4*
–	–	9*	–
GND	–	10	C6
I/O	–	11	B5
I/O	–	12	B6
I/O (TMS)	17	13	A5
I/O	18	14	C7
I/O	–	15	B7
I/O	–	16	A6
I/O	19	17	A7
I/O	20	18	A8
GND	21	19	C8
VCC	22	20	B8
I/O	23	21	C9
I/O	24	22	B9
I/O	–	23	A9
I/O	–	24	B10
I/O	25	25	C10
I/O	26	26	A10
I/O	–	27	A11
I/O	–	28	B11
GND	–	29	C11
–	–	30*	A12*
–	–	31*	–
I/O	27	32	B12
I/O	–	33	A13
I/O	–	34	A14
I/O	–	35	C12

Pin Description	PC84	PQ160	PG156
I/O	28	36	B13
SGCK2 (I/O)	29	37	B14
M1	30	38	A15
GND	31	39	C13
M0	32	40	A16
VCC	33	41	C14
M2	34	42	B15
PGCK2 (I/O)	35	43	B16
I/O (HDC)	36	44	D14
I/O	–	45	C15
I/O	–	46	D15
I/O	–	47	E14
I/O (LDC)	37	48	C16
–	–	49*	E15*
–	–	50*	D16*
GND	–	51	F14
I/O	–	52	F15
I/O	–	53	E16
I/O	38	54	F16
I/O	39	55	G14
I/O	–	56	G15
I/O	–	57	G16
I/O	40	58	H16
I/O (ERR, INIT)	41	59	H15
VCC	42	60	H14
GND	43	61	J14
I/O	44	62	J15
I/O	45	63	J16
I/O	–	64	K16
I/O	–	65	K15
I/O	46	66	K14
I/O	47	67	L16
I/O	–	68	M16
I/O	–	69	L15
GND	–	70	L14
–	–	71*	N16*
–	–	72*	M15*
I/O	48	73	P16
I/O	49	74	M14
I/O	–	75	N15
I/O	–	76	P15
I/O	50	77	N14
SGCK3 (I/O)	51	78	R16
GND	52	79	P14
DONE	53	80	R15
VCC	54	81	P13
PROG	55	82	R14
I/O (D7)	56	83	T16
PGCK3 (I/O)	57	84	T15
I/O	–	85	R13
I/O	–	86	P12
I/O (D6)	58	87	T14
I/O	–	88	T13
–	–	89*	R12*

Pin Description	PC84	PQ160	PG156
–	–	90*	T12*
GND	–	91	P11
I/O	–	92	R11
I/O	–	93	T11
I/O (D5)	59	94	T10
I/O (CS0)	60	95	P10
I/O	–	96	R10
I/O	–	97	T9
I/O (D4)	61	98	R9
I/O	62	99	P9
VCC	63	100	R8
GND	64	101	P8
I/O (D3)	65	102	T8
I/O ($\overline{RS}$)	66	103	T7
I/O	–	104	T6
I/O	–	105	R7
I/O (D2)	67	106	P7
I/O	68	107	T5
I/O	–	108	R6
I/O	–	109	T4
GND	–	110	P6
–	–	111*	R5*
–	–	112*	–
I/O (D1)	69	113	T3
I/O ($\overline{RCLK}$-BUSY/RDY)	70	114	P5
I/O	–	115	R4
I/O	–	116	R3
I/O (D0, DIN)	71	117	P4
SGCK4 (DOUT,I/O)	72	118	T2
CCLK	73	119	R2
VCC	74	120	P3
TDO	75	121	T1
GND	76	122	N3
I/O (A0, $\overline{WS}$)	77	123	R1
PGCK4 (A1,I/O)	78	124	P2
I/O	–	125	N2
I/O	–	126	M3
I/O (CS1, A2)	79	127	P1
I/O (A3)	80	128	N1
–	–	129*	M2*
–	–	130*	M1*
GND	–	131	L3
I/O	–	132	L2
I/O	–	133	L1
I/O (A4)	81	134	K3
I/O (A5)	82	135	K2
–	–	136*	–
I/O	–	137	K1
I/O	–	138	J1
I/O (A6)	83	139	J2
I/O (A7)	84	140	J3
GND	1	141	H2

* Indicates unconnected package pins.

XC4008 Pinouts

Pin Description	PG191
VCC	J4
I/O (A8)	J3
I/O (A9)	J2
I/O	J1
I/O	H1
I/O	H2
I/O	H3
I/O (A10)	G1
I/O (A11)	G2
I/O	F1
I/O	E1
GND	G3
*	F2
*	D1
I/O	C1
I/O	E2
I/O (A12)	F3
I/O (A13)	D2
I/O	B1
I/O	E3
I/O (A14)	C2
SGCK1 (A15, I/O)	B2
VCC	D3
GND	D4
PGCK1 (A16, I/O)	C3
I/O (A17)	C4
I/O	B3
I/O	C5
I/O (TDI)	A2
I/O (TCK)	B4
I/O	C6
I/O	A3
*	B5
*	B6
GND	C7
I/O	A4
I/O	A5
I/O (TMS)	B7
I/O	A6
I/O	C8
I/O	A7
I/O	B8
I/O	A8
I/O	B9
I/O	C9
GND	D9
VCC	D10
I/O	C10

Pin Description	PG191
I/O	B10
I/O	A9
I/O	A10
I/O	A11
I/O	C11
I/O	B11
I/O	A12
I/O	B12
I/O	A13
GND	C12
*	B13
*	A14
I/O	A15
I/O	C13
I/O	B14
I/O	A16
I/O	B15
I/O	C14
I/O	A17
SGCK2 (I/O)	B16
M1	C15
GND	D15
M0	A18
VCC	D16
M2	C16
PGCK2 (I/O)	B17
I/O (HDC)	E16
I/O	C17
I/O	D17
I/O	B18
I/O (LDC)	E17
I/O	F16
I/O	C18
*	D18
*	F17
GND	G16
I/O	E18
I/O	F18
I/O	G17
I/O	G18
I/O	H16
I/O	H17
I/O	H18
I/O	J18
I/O	J17
I/O (ERR, INIT)	J16
VCC	J15
GND	K15

Pin Description	PG191
I/O	K16
I/O	K17
I/O	K18
I/O	L18
I/O	L17
I/O	L16
I/O	M18
I/O	M17
I/O	N18
I/O	P18
GND	M16
*	N17
*	R18
I/O	T18
I/O	P17
I/O	N16
I/O	T17
I/O	R17
I/O	P16
I/O	U18
SGCK3 (I/O)	T16
GND	R16
DONE	U17
VCC	R15
PROG	V18
I/O (D7)	T15
PGCK3 (I/O)	U16
I/O	T14
I/O	U15
I/O (D6)	V17
I/O	V16
I/O	T13
I/O	U14
*	V15
*	V14
GND	T12
I/O	U13
I/O	V13
I/O (D5)	U12
I/O (CSO)	V12
I/O	T11
I/O	U11
I/O	V11
I/O	V10
I/O (D4)	U10
I/O	T10
VCC	R10
GND	R9

Pin Description	PG191
I/O (D3)	T9
I/O (RS)	U9
I/O	V9
I/O	V8
I/O	U8
I/O	T8
I/O (D2)	V7
I/O	U7
I/O	V6
I/O	U6
GND	T7
*	V5
*	V4
I/O	U5
I/O	T6
I/O (D1)	V3
I/O (RCLK-BUSY/RDY)	V2
I/O	U4
I/O	T5
I/O (D0, DIN)	U3
SGCK4 (I/O)	T4
CCLK	V1
VCC	R4
TDO	U2
GND	R3
I/O (A0, WS)	T3
PGCK4 (I/O, A1)	U1
I/O	P3
I/O	R2
I/O (CS1, A2)	T2
I/O (A3)	N3
I/O	P2
I/O	T1
*	R1
*	N2
GND	M3
I/O	P1
I/O	N1
I/O (A4)	M2
I/O (A5)	M1
I/O	L3
I/O	L2
I/O	L1
I/O	K1
I/O (A6)	K2
I/O (A7)	K3
GND	K4

* Indicates unconnected package pins.

XC4010 Pinouts

Pin Description	PG191
VCC	J4
I/O (A8)	J3
I/O (A9)	J2
I/O	J1
I/O	H1
I/O	H2
I/O	H3
I/O (A10)	G1
I/O (A11)	G2
I/O	F1
I/O	E1
GND	G3
I/O	F2
I/O	D1
I/O	C1
I/O	E2
I/O (A12)	F3
I/O (A13)	D2
I/O	B1
I/O	E3
I/O (A14)	C2
SGCK1 (A15, I/O)	B2
VCC	D3
GND	D4
PGCK1 (A16, I/O)	C3
I/O (A17)	C4
I/O	B3
I/O	C5
I/O (TDI)	A2
I/O (TCK)	B4
I/O	C6
I/O	A3
I/O	B5
I/O	B6
GND	C7
I/O	A4
I/O	A5
I/O (TMS)	B7
I/O	A6
I/O	C8
I/O	A7
I/O	B8
I/O	A8
I/O	B9
I/O	C9
GND	D9
VCC	D10
I/O	C10

Pin Description	PG191
I/O	B10
I/O	A9
I/O	A10
I/O	A11
I/O	C11
I/O	B11
I/O	A12
I/O	B12
I/O	A13
GND	C12
I/O	B13
I/O	A14
I/O	A15
I/O	C13
I/O	B14
I/O	A16
I/O	B15
I/O	C14
I/O	A17
SGCK2 (I/O)	B16
M1	C15
GND	D15
M0	A18
VCC	D16
M2	C16
PGCK2 (I/O)	B17
I/O (HDC)	E16
I/O	C17
I/O	D17
I/O	B18
I/O (LDC)	E17
I/O	F16
I/O	C18
I/O	D18
I/O	F17
GND	G16
I/O	E18
I/O	F18
I/O	G17
I/O	G18
I/O	H16
I/O	H17
I/O	H18
I/O	J18
I/O	J17
I/O ($\overline{ERR}$, $\overline{INIT}$)	J16
VCC	J15
GND	K15

Pin Description	PG191
I/O	K16
I/O	K17
I/O	K18
I/O	L18
I/O	L17
I/O	L16
I/O	M18
I/O	M17
I/O	N18
I/O	P18
GND	M16
I/O	N17
I/O	R18
I/O	T18
I/O	P17
I/O	N16
I/O	T17
I/O	R17
I/O	P16
I/O	U18
SGCK3 (I/O)	T16
GND	R16
DONE	U17
VCC	R15
PROG	V18
I/O (D7)	T15
PGCK3 (I/O)	U16
I/O	T14
I/O	U15
I/O (D6)	V17
I/O	V16
I/O	T13
I/O	U14
I/O	V15
I/O	V14
GND	T12
I/O	U13
I/O	V13
I/O (D5)	U12
I/O (CSO)	V12
I/O	T11
I/O	U11
I/O	V11
I/O	V10
I/O (D4)	U10
I/O	T10
VCC	R10
GND	R9

Pin Description	PG191
I/O (D3)	T9
I/O (RS)	U9
I/O	V9
I/O	V8
I/O	U8
I/O	T8
I/O (D2)	V7
I/O	U7
I/O	V6
I/O	U6
GND	T7
I/O	V5
I/O	V4
I/O	U5
I/O	T6
I/O (D1)	V3
RCLK-BUSY/RDY	V2
I/O	U4
I/O	T5
I/O (D0, DIN)	U3
SGCK4 (DOUT, I/O)	T4
CCLK	V1
VCC	R4
TDO	U2
GND	R3
I/O (A0, WS)	T3
PGCK4 (A1, I/O)	U1
I/O	P3
I/O	R2
I/O (CS1, A2)	T2
I/O (A3)	N3
I/O	P2
I/O	T1
I/O	R1
I/O	N2
GND	M3
I/O	P1
I/O	N1
I/O (A4)	M2
I/O (A5)	M1
I/O	L3
I/O	L2
I/O	L1
I/O	K1
I/O (A6)	K2
I/O (A7)	K3
GND	K4

ABSOLUTE MAXIMUM RATINGS

			Units
V_{CC}	Supply voltage relative to GND	–0.5 to 7.0	V
V_{IN}	Input voltage with respect to GND	–0.5 to 7	V
V_{TS}	Voltage applied to 3-state output	–0.5 to 7	V
T_{STG}	Storage temperature (ambient)	–65 to + 150	°C
T_{SOL}	Maximum soldering temperature (10 s @ 1/16 in. = 1.5 mm)	+ 260	°C
T_J	Junction temperature	+ 150	°C

Note: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those listed under Recommended Operating Conditions is not implied. Exposure to Absolute Maximum Ratings conditions for extended periods of time may affect device reliability.

OPERATING CONDITIONS

				Min	Max	Units
V_{CC}	Supply voltage relative to GND	Commercial	0°C to 70°C	4.75	5.25	V
	Supply voltage relative to GND	Industrial	–40°C to 85°C	4.5	5.5	V
	Supply voltage relative to GND	Military	–55°C to 125°C	4.5	5.5	V
V_{IH}	High-level input voltage (XC4000 has TTL-like input thresholds)			2.0	V_{CC}	V
V_{IL}	Low-level input voltage (XC4000 has TTL-like input thresholds)			0	0.8	V
T_{IN}	Input signal transition time				250	ns

DC CHARACTERISTICS OVER OPERATING CONDITIONS

		Min	Max	Units
V_{OH}	High-level output voltage @ I_{OH} = –4.0 mA, V_{CC} min	2.4		V
V_{OL}	Low-level output voltage @ I_{OL} = 12.0 mA, V_{CC} max (Note 1)		0.4	V
I_{CCO}	Quiescent LCA supply current (Note 2)		10	mA
I_{IL}	Leakage current	–10	+10	µA
C_{IN}	Input capacitance (sample tested)		15	pF
I_{RIN}	Pad pull-up (when selected) @ V_{IN} = 0V (sample tested)	0.02	0.17	mA
I_{RLL}	Horizontal Long Line pull-up (when selected) @ logic Low	0.2	2.5	mA

Note: 1. With 50% of the outputs simultaneously sinking 12 mA.
2. With no output current loads, no active input or long line pull-resistors, all package pins at V_{CC} or GND, and the LCA configured with a MakeBits "tie" option.

WIDE DECODER SWITCHING CHARACTERISTIC GUIDELINES

These switching parameters are advance information. They are intended to represent worst-case values over temperature and supply voltage variations. Following more extensive characterization, Xilinx may change these values without prior notice.

		Speed Grade	-6	-5	Units
Description	Symbol	Device	Max	Max	Max
Full length, both pull-ups, inputs from IOB i-pins	TWAF	XC4003	3.6	3.0	ns
		XC4005	3.9	3.3	ns
		XC4010	4.5	3.8	ns
Full length, both pull-ups inputs from internal logic	TWAFL	XC4003	4.2	3.5	ns
		XC4005	4.8	4.0	ns
		XC4010	6.0	5.0	ns
Half length, one pull-up inputs from IOB i-pins	TWAO	XC4003	3.3	2.8	ns
		XC4005	3.9	3.3	ns
		XC4010	5.1	4.3	ns
Half length, one pull-up inputs from internal logic	TWAOL	XC4003	4.8	4.0	ns
		XC4005	5.4	4.5	ns
		XC4010	6.6	5.5	ns

Note: These delays are specified from the decoder input to the decoder output. For pad-to-pad delays, add the input delay (TPID) and output delay (TOPF or TOPS), as listed on page 46.

BUFFER (Internal) SWITCHING CHARACTERISTIC GUIDELINES

Testing of the switching parameters is modeled after testing methods specified by MIL-M-38510/605. All devices are 100% functionally tested. Since many internal timing parameters cannot be measured directly, they are derived from benchmark timing patterns. The following guidelines reflect worst-case values over the recommended operating conditions. For more detailed, more precise, and more up-to-date timing information, use the values provided by the XACT timing calculator and used in the simulator.

	Speed Grade	-6	-5	Units
Description	Symbol	Max	Max	Max
Global Signal Distribution				
From pad through **primary** buffer, to any clock k		6.1	4.8	ns
From pad through **secondary** buffer, to any clock k		6.5	5.2	ns
TBUF driving a Horizontal Longline (L.L.)				
I to L.L. while T is Low (buffer active)	TIO	4.4	3.6	ns
I↓ (open drain) to LL		4.4	3.6	ns
T↓ to L.L. active and valid	TON	7.7	6.3	ns
T↑ to L.L. (inactive) with single pull-up resistor	TPUS	12.1	9.9	ns
with pair of pull-up resistors	TPUF	5.5	4.5	ns

CLB SWITCHING CHARACTERISTIC GUIDELINES (Continued)

Testing of the switching parameters is modeled after testing methods specified by MIL-M-38510/605. All devices are 100% functionally tested. Since many internal timing parameters cannot be measured directly, they are derived from benchmark timing patterns. The following guidelines reflect worst-case values over the recommended operating conditions. For more detailed, more precise, and more up-to-date timing information, use the values provided by the XACT timing calculator and used in the simulator.

	Speed Grade	-6		-5		Units
Description	Symbol	Min	Max	Min	Max	
Combinatorial Delays						
F/G inputs to X/Y outputs	T_{ILO}		6		4.5	ns
F/G inputs via H' to X/Y outputs	T_{IHO}		8		6	ns
C inputs via H' to X/Y outputs	T_{HHO}		7		5	ns
CLB FAST CARRY LOGIC						
Operand inputs (F1,F2,G1,G4) to COUT	T_{OPCY}		7		5.5	ns
Add/Subtract input (F3) to COUT	T_{ASCY}		8		6	ns
Initialization inputs (F1,F3) to COUT	T_{INCY}		6		4	ns
C_{IN} through function generators to X/Y outputs	T_{SUM}		8		6	ns
C_{IN} to C_{OUT}, bypass function generators.	T_{BYP}		2		1.5	ns
Sequential Delays						
Clock K to outputs Q	T_{CKO}		5		3	ns
Set-up Time before Clock K						
F/G inputs	T_{ICK}	6		4.5		ns
F/G inputs via H'	T_{IHCK}	8		6		ns
C inputs via H1	T_{HHCK}	7		5		ns
C inputs via DIN	T_{DICK}	4		3		ns
C inputs via EC	T_{ECCK}	7		4		ns
C inputs via S/R, going Low (inactive)	T_{RCK}	4.5		3.5		ns
C_{IN} input via F'/G'		8		6		ns
C_{IN} input via F'/G' and H'		10		7.5		ns
Hold Time after Clock K						
F/G inputs	T_{CKI}	0		0		ns
F/G inputs via H'	T_{CKIH}	0		0		ns
C inputs via H1	T_{CKHH}	0		0		ns
C inputs via DIN	T_{CKDI}	0		0		ns
C inputs via EC	T_{CKEC}	0		0		ns
C inputs via S/R, going Low (inactive)	T_{CKR}	0		0		ns
Clock						
Clock Hightime	T_{CH}	5		4		ns
Clock Low time	T_{CL}	5		4		ns
Set/Reset Direct						
Width (High)	T_{RPW}	5		4		ns
Delay from C to Q	T_{RIO}		9		8	ns
Master Set/Reset						
Width (High or Low)	T_{MRW}	12		10		ns
Delay from Global Set/Reset net to Q	T_{MRQ}		24		23	ns

CLB SWITCHING CHARACTERISTIC GUIDELINES (Continued)

Testing of the switching parameters is modeled after testing methods specified by MIL-M-38510/605. All devices are 100% functionally tested. Since many internal timing parameters cannot be measured directly, they are derived from benchmark timing patterns. The following guidelines reflect worst-case values over the recommended operating conditions. For more detailed, more precise, and more up-to-date timing information, use the values provided by the XACT timing calculator and used in the simulator.

CLB RAM OPTION	Speed Grade		-6		-5		Units
Description	Symbol		Min	Max	Min	Max	Min Max
Read Operation							
Address read cycle time	16 x 2	T_{RC}	7		5.5		ns
	32 x 1	T_{RCT}	10		7.5		ns
Data valid after address change	16 x 2	T_{ILO}		6		4.5	ns
(no Write Enable)	32 x 1	T_{IHO}		8		6	ns
Read During Write, Clocking Data into Flip-Flop							
Address setup time before clock K	16 x 2	T_{ICK}	6		4.5		ns
	32 x 1	T_{IHCK}	8		6		ns
Read During Write							
Data valid after WE going active	16 x 2	T_{WO}		12		10	ns
(DIN stable before WE)	32 x 1	T_{WOT}		15		12	ns
Data valid after DIN	16 x 2	T_{DO}		11		9	ns
(DIN change during WE)	32 x 1	T_{DOT}		14		11	ns
Read During Write, Clocking Data into Flip-Flop							
WE setup time before clock K	16 x 2			12		10	ns
	32 x 1			15		12	ns
Data setup time before clock K	16 x 2			11		9	ns
	32 x 1			14		11	ns
Write Operation							
Address write cycle time	16 x 2	T_{WC}	7		5.5		ns
	32 x 1	T_{WCT}	7		5.5		ns
Write Enable pulse width (High)	16 x 2	T_{WP}	5		4		ns
	32 x 1	T_{WPT}	5		4		ns
Address set-up time before beginning of WE	16 x 2	T_{AS}	0		0		ns
	32 x 1	T_{AST}	0		0		ns
Address hold time after end of WE	16 x 2	T_{AH}		2		2	ns
	32 x 1	T_{AHT}		2		2	ns
DIN set-up time before end of WE	16 x 2	T_{DS}	4		4		ns
	32 x 1	T_{DST}	5		5		ns
DIN hold time after end of WE		T_{DHT}		0		0	ns

Note: Timing for the 16 x 1 RAM option is identical to 16 x 2 RAM timing

IOB SWITCHING CHARACTERISTIC GUIDELINES (Continued)

Testing of the switching parameters is modeled after testing methods specified by MIL-M-38510/605. All devices are 100% functionally tested. Since many internal timing parameters cannot be measured directly, they are derived from benchmark timing patterns. The following guidelines reflect worst-case values over the recommended operating conditions. For more detailed, more precise, and more up-to-date timing information, use the values provided by the XACT timing calculator and used in the simulator.

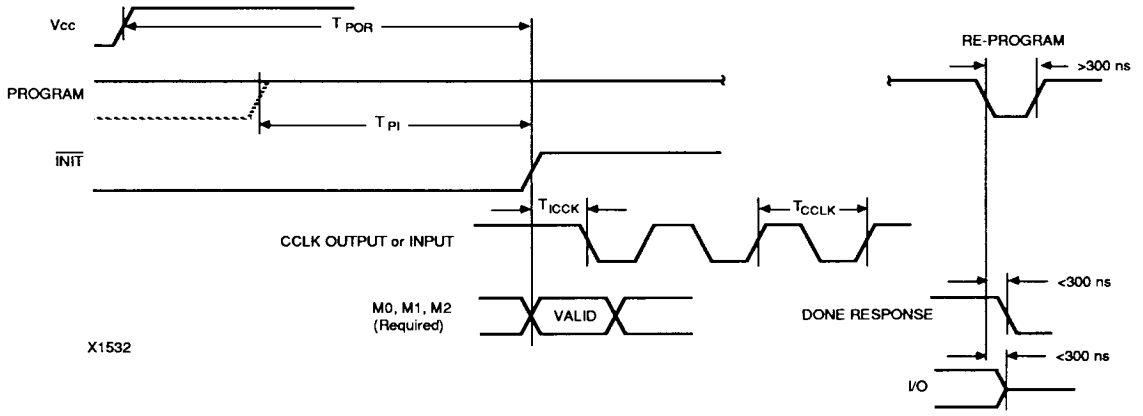
		-6		-5			Units
Description	Symbol	Min	Max	Min	Max	Min Max	
INPUT							
Propagation Delays							
Pad to I1, I2	T_{PID}		4		3		ns
Pad to I1, I2, via transparent latch (fast)	T_{PLI}		8.5		7		ns
Pad to I1, I2, via transparent latch (with delay)	T_{PDLI}		23		19		ns
Clock (IK) toI1, I2, (flip-flop)	T_{IKRI}		6		5		ns
Clock (IK) to I1, I2 (latch enable)	T_{IKLI}		8		7		ns
Set-up Time (Note 3)							
Pad to Clock (IK), fast	T_{PICK}	4		3			ns
Pad to Clock (IK) with delay	T_{PICKD}	16		13			ns
Hold Time (Note 3)							
Pad to Clock (IK), fast	T_{IKPI}		1		1		ns
Pad to Clock (IK) with delay	T_{IKPID}		negative		negative		
OUTPUT							
Propagation Delays							
Clock (OK) to Pad (fast)	T_{OKPOF}		7.5		7		ns
same (slew rate limited)	T_{OKPOS}		11.5		10		ns
Output (O) to Pad (fast)	T_{OPF}		9		7		ns
same (slew-rate limited)	T_{OPS}		13		10		ns
3-state to Pad begin hi-Z (fast)	T_{TSHZF}		9		7		ns
same (slew-rate limited)	T_{TSHZS}		13		10		ns
3-state to Pad active and valid (fast)	T_{TSONF}		13		10		ns
same (slew -rate limited)	T_{TSONS}		17		12		ns
Set-up and Hold Times							
Output (O) to clock (OK) set-up time	T_{OOK}	7		5			ns
Output (O) to clock (OK) hold time	T_{OKO}		0		0		ns
Clock							
Clock High or Low time	T_{CH}/T_{CL}	5		4			ns
Global Set/Reset							
Delay from GSR net through Q to I1, I2	T_{RRI}		13		12		ns
Delay from GSR net to Pad	T_{RPO}		15		13		ns
GSR width	T_{MRW}	12		10			ns

Notes: 1. Timing is measured at pin threshold, with 50 pF external capacitive loads (incl. test fixture).
Slew rate limited output rise/fall times are approximately two times longer than **fast** output rise/fall times.
A maximum total external capacitive load for simultaneous fast mode switching in the same direction is 200 pF per power/ground pin pair. For slew-rate limited outputs this total is two times larger. Exceeding this maximum capacitive load can result in ground bounce of >1.5 V amplitude, <5 ns duration, which might cause problems when the LCA drives clocks and other asynchronous signals.

2. Voltage levels of unused (bonded and unbonded) pads must be valid logic levels. Each can be configured with the internal pull-up or pull-down resistor or alternatively configured as a driven output or be driven from an external source.

3. Input pad setup times and hold times are specified with respect to the internal clock (IK). To calculate system setup time, subtract clock delay (clock pad to IK) from the specified input pad setup time value, but do not subtract below zero. "Negative" hold time means that the delay in the input data is adequate for the **external system hold time** to be zero, provided the input clock uses the Global signal distribution from pad to IK.

GENERAL LCA SWITCHING CHARACTERISTICS



Master Modes

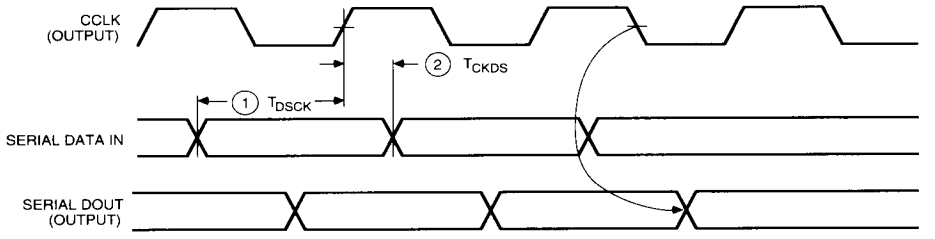
	Symbol	Min	Max	Units
Power-On-Reset M0 = High M0 = Low	T_{POR} T_{POR}	10 40	40 130	ms ms
Program Latency	T_{PI}	3	20	µs per CLB column
CCLK (output) Delay period (slow) period (fast)	T_{ICCK} T_{CCLK} T_{CCLK}	40 640 100	250 2000 250	µs ns ns

Slave and Peripheral Modes

	Symbol	Min	Max	Units
Power-On-Reset	T_{POR}	10	33	ms
Program Latency	T_{PI}	3	20	µs per CLB column
CCLK (input) Delay (required) period (required)	T_{ICCK} T_{CCLK}	4 125		µs ns

Note: At power-up, Vcc must rise from 2.0 V to Vcc min in less than 25 ms, otherwise delay configuration using $\overline{INIT}$ until Vcc is valid.

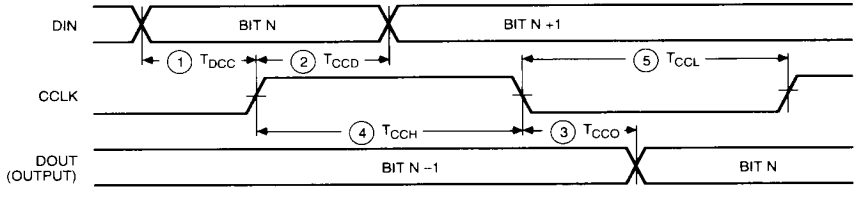
MASTER SERIAL MODE PROGRAMMING SWITCHING CHARACTERISTICS



	Speed Grade			-6		-5				Units
	Description		Symbol	Min	Max	Min	Max	Min	Max	
CCLK	Data In setup	1	TDSCK	60		60				ns
	Data In hold	2	TCKDS	0		0				ns

Notes: 1. At power-up, Vcc must rise from 2.0 V to Vcc min in less than 25 ms, otherwise delay configuration using INIT until Vcc is valid.
2. Configuration can be controlled by holding INIT Low with or until after the INIT of all daisy-chain slave mode devices is High.
3. Master-serial-mode timing is based on testing in slave-mode.

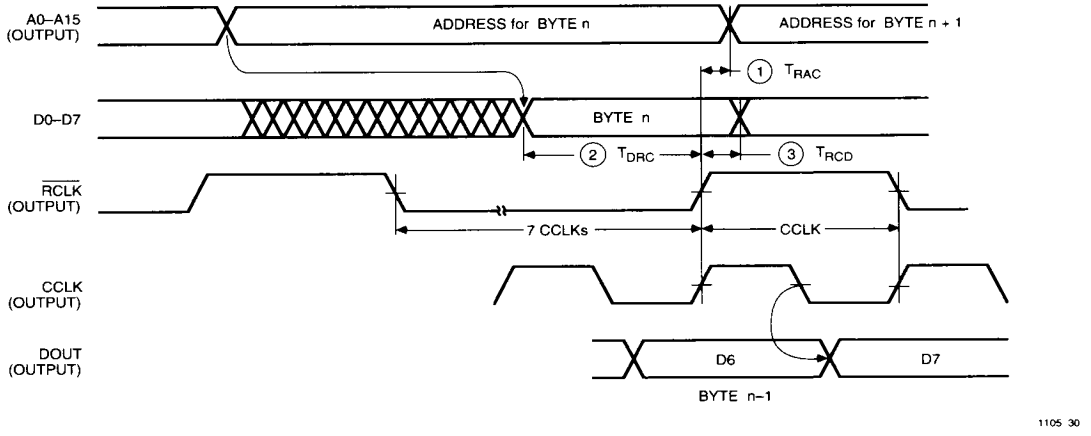
SLAVE SERIAL MODE PROGRAMMING SWITCHING CHARACTERISTICS



				-6		-5				Units
	Description		Symbol	Min	Max	Min	Max	Min	Max	
CCLK	To DOUT	3	TCCO		30		30			ns
	DIN setup	1	TDCC	20		20				ns
	DIN hold	2	TCCD	0		0				ns
	High time	4	TCCH	50		50				ns
	Low time	5	TCCL	60		60				ns
	Frequency		FCC		8		8			MHz

Note: Configuration must be delayed until the INIT of all daisy-chained LCA devices is High.

MASTER PARALLEL MODE PROGRAMMING SWITCHING CHARACTERISTICS

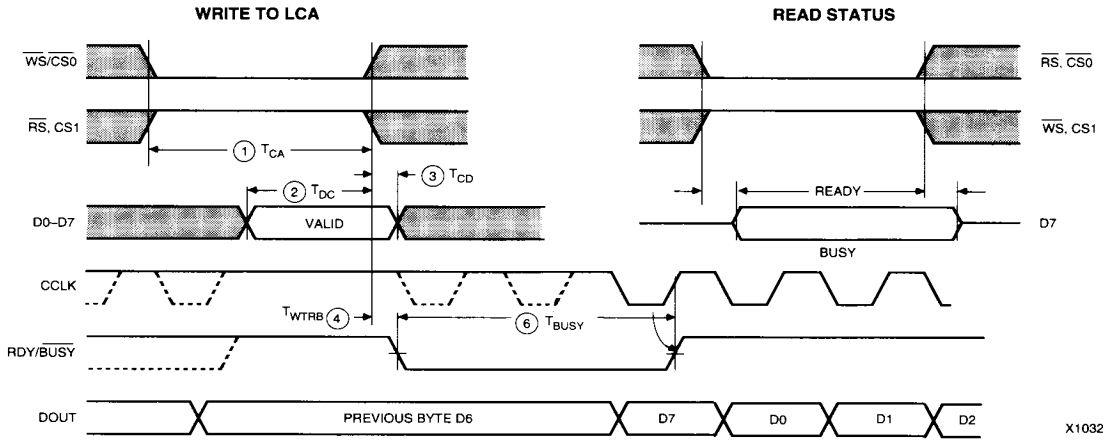


				-6		-5				Units
	Description	Symbol		Min	Max	Min	Max	Min	Max	
RCLK	Delay to Address valid	1	T_{RAC}	0	200	0	200			ns
	Data setup time	2	T_{DRC}	60		60				ns
	Data setup time	3	T_{RCD}	0		0				ns

Notes: 1. At power-up, Vcc must rise from 2.0 V to Vcc min in less than 25 ms, otherwise delay configuration using $\overline{INIT}$ until Vcc is valid.
2. Configuration can be delayed by holding INIT Low with or until after the $\overline{INIT}$ of all daisy-chain slave mode devices is High.
3. The first Data byte is loaded and CCLK starts at the end of the first RCLK active cycle (rising edge).

This timing diagram shows that the EPROM requirements are extremely relaxed: EPROM access time can be longer than 500 ns. EPROM data output has no hold-time requirements.

ASYNCHRONOUS PERIPHERAL MODE PROGRAMMING SWITCHING CHARACTERISTICS

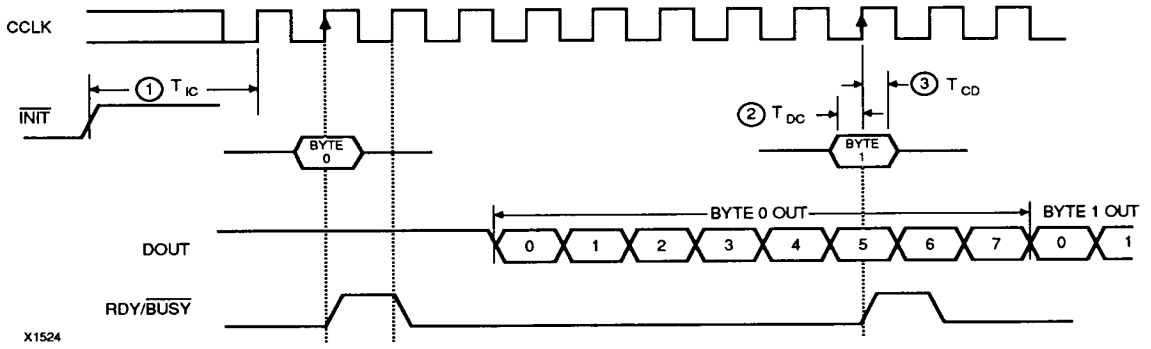


				-6		-5				Units
	Description		Symbol	Min	Max	Min	Max	Min	Max	
Write	Effective Write time required ($\overline{CS0} \bullet CS1 \bullet \overline{RS} \bullet \overline{WS}$)	1	T_{CA}	100		100				ns
	DIN Setup time required	2	T_{DC}	60		60				ns
	DIN Hold time required	3	T_{CD}	0		0				ns
RDY	RDY/BUSY delay after end of WS	4	T_{WTRB}		60		60			ns
	Earliest next $\overline{WS}$ after end of BUSY	5	T_{RBWT}	0		0				ns
	BUSY Low output (Note 4)	6	T_{BUSY}	2	9	2	9			CCLK Periods

Notes:
1. Configuration must be delayed until the INIT of all LCAs is High.
2. Time from end of WS to CCLK cycle for the new byte of data depends on completion of previous byte processing and the phase of the internal timing generator for CCLK.
3. CCLK and DOUT timing is tested in slave mode.
4. T_{BUSY} indicates that the double-buffered parallel-to-serial converter is not yet ready to receive new data. The shortest T_{BUSY} occurs when a byte is loaded into an empty parallel-to-serial converter. The longest T_{BUSY} occurs when a new word is loaded into the input register before the second-level buffer has started shifting out data.

This timing diagram shows very relaxed requirements:
Data need not be held beyond the rising edge of $\overline{WS}$. BUSY will go active within 60 ns after the end of $\overline{WS}$.
$\overline{WS}$ may be asserted immediately after the end of BUSY.

SYNCHRONOUS PERIPHERAL MODE PROGRAMMING SWITCHING CHARACTERISTICS



SYNCHRONOUS PERIPHERAL MODE PROGRAMMING SWITCHING CHARACTERISTICS

				-6		-5				Units
	Description	Symbol		Min	Max	Min	Max	Min	Max	
CCLK	INIT (High) Setup time required	1	TIC	60		60				ns
	DIN Setup time required	2	TDC	60		60				ns
	DIN Hold time required	3	TCD	0		0				ns
	CCLK High time		TCCH	50		50				ns
	CCLK Low time		TCCL	60		60				ns
	CCLK Frequency		FCC		8		8			MHz

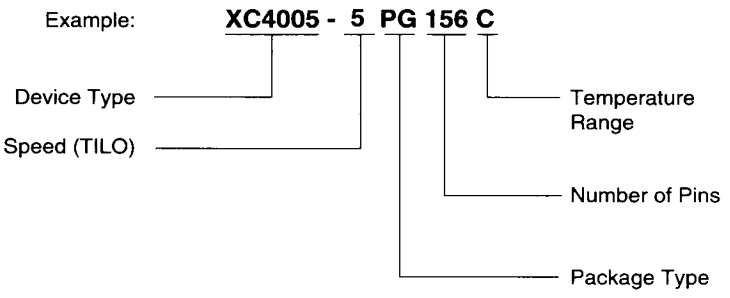
Notes: Peripheral Synchronous mode can be considered Slave Parallel mode. An external CCLK provides timing, clocking in the **first** data byte on the **second** rising edge of CCLK after INIT goes High. Subsequent data bytes are clocked in on every eighth consecutive rising edge of CCLK.

The RDY/BUSY line goes High for one CCLK period after data has been clocked in, although synchronous operation does not require such a response.

The pin name RDY/BUSY is a misnomer; in Synchronous Peripheral mode this is really an ACKNOWLEDGE signal.

Note that data starts to shift out serially on the DOUT pin 2.5 CLK periods after it was loaded in parallel. This obviously requires additional CCLK pulses after the last byte has been loaded.

ORDERING INFORMATION



X1535

COMPONENT AVAILABILITY (11/91)

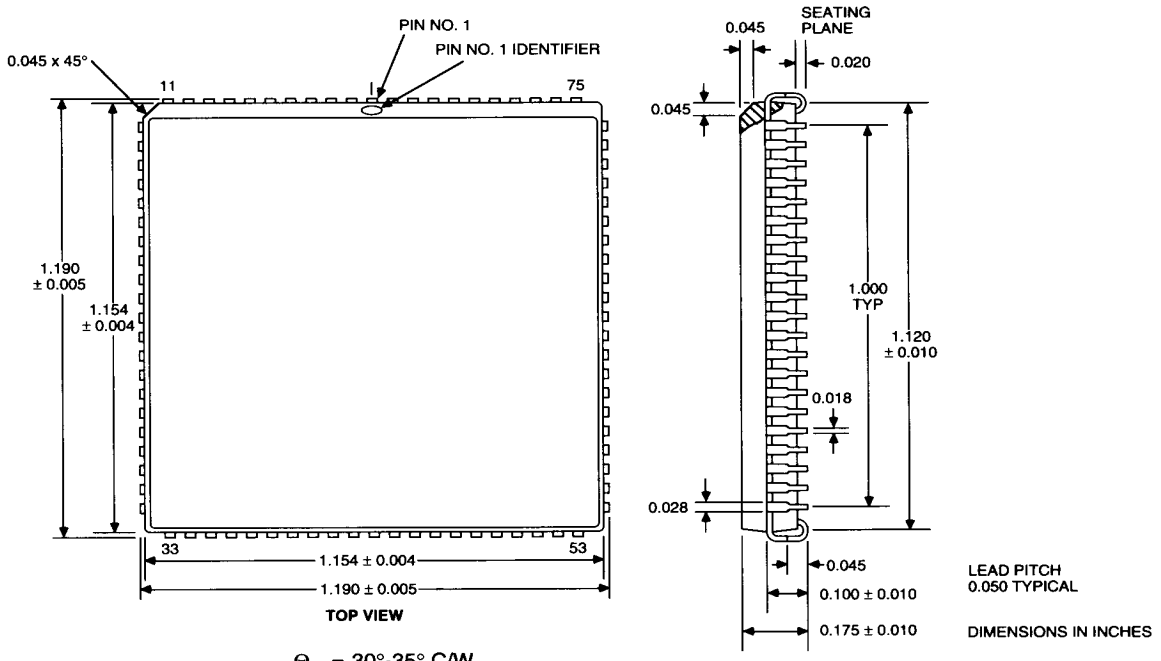
		84 PIN PLASTIC PLCC	100 PIN PLASTIC PQFP	120 PIN CERAMIC PGA	156 PIN CERAMIC PGA	160 PIN PLASTIC PQFP	191 PIN CERAMIC PGA	196 PIN CERAMIC CQFP	208 PIN PLASTIC PQFP
		PC84	**PQ100**	**PG120**	**PG156**	**PQ160**	**PG191**	**CQ196**	**PQ208**
XC4003	-6	NOW		NOW					
	-5	NOW		NOW					
XC4005	-6	NOW			NOW	NOW			
	-5	NOW			NOW	NOW			
XC4006	-6								
	-5								
XC4008	-6								
	-5								
XC4010	-6								
	-5								

White boxes indicate planned products

X1104C

Shaded boxes indicate device-package combinations that are not planned

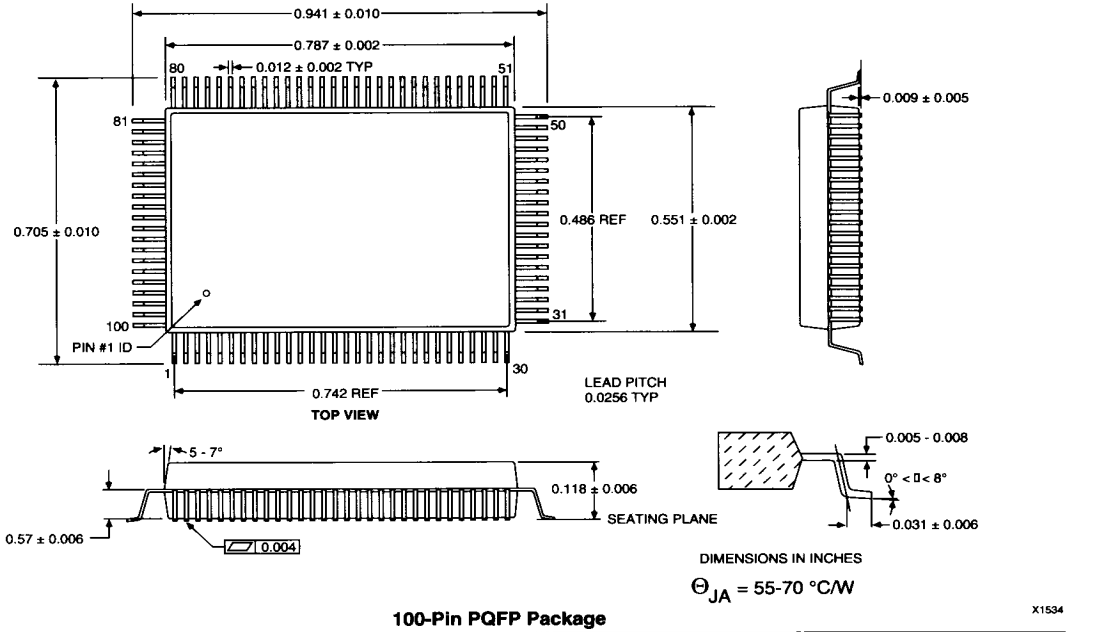
PACKAGE OUTLINES



Θ_{JA} = 30°-35° C/W

Θ_{JC} = 3°-7° C/W

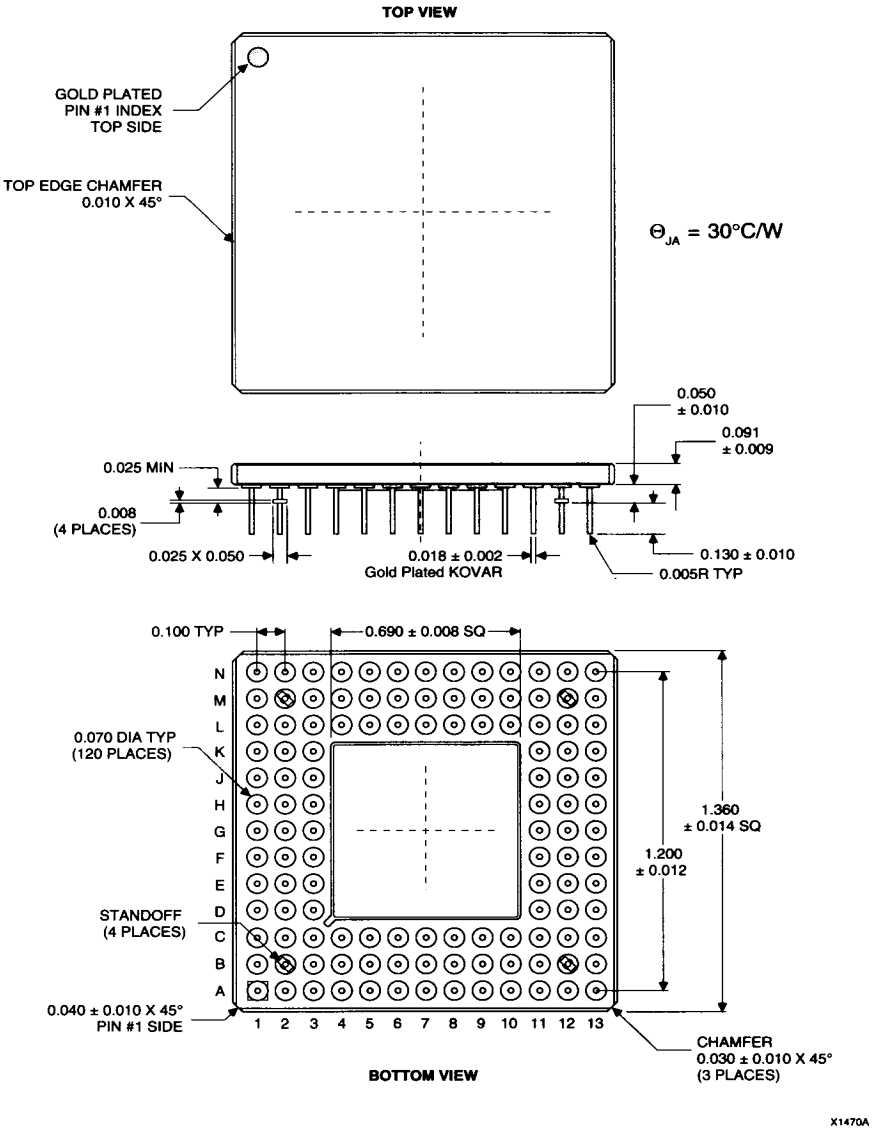
84-Pin PLCC Package



Θ_{JA} = 55-70 °C/W

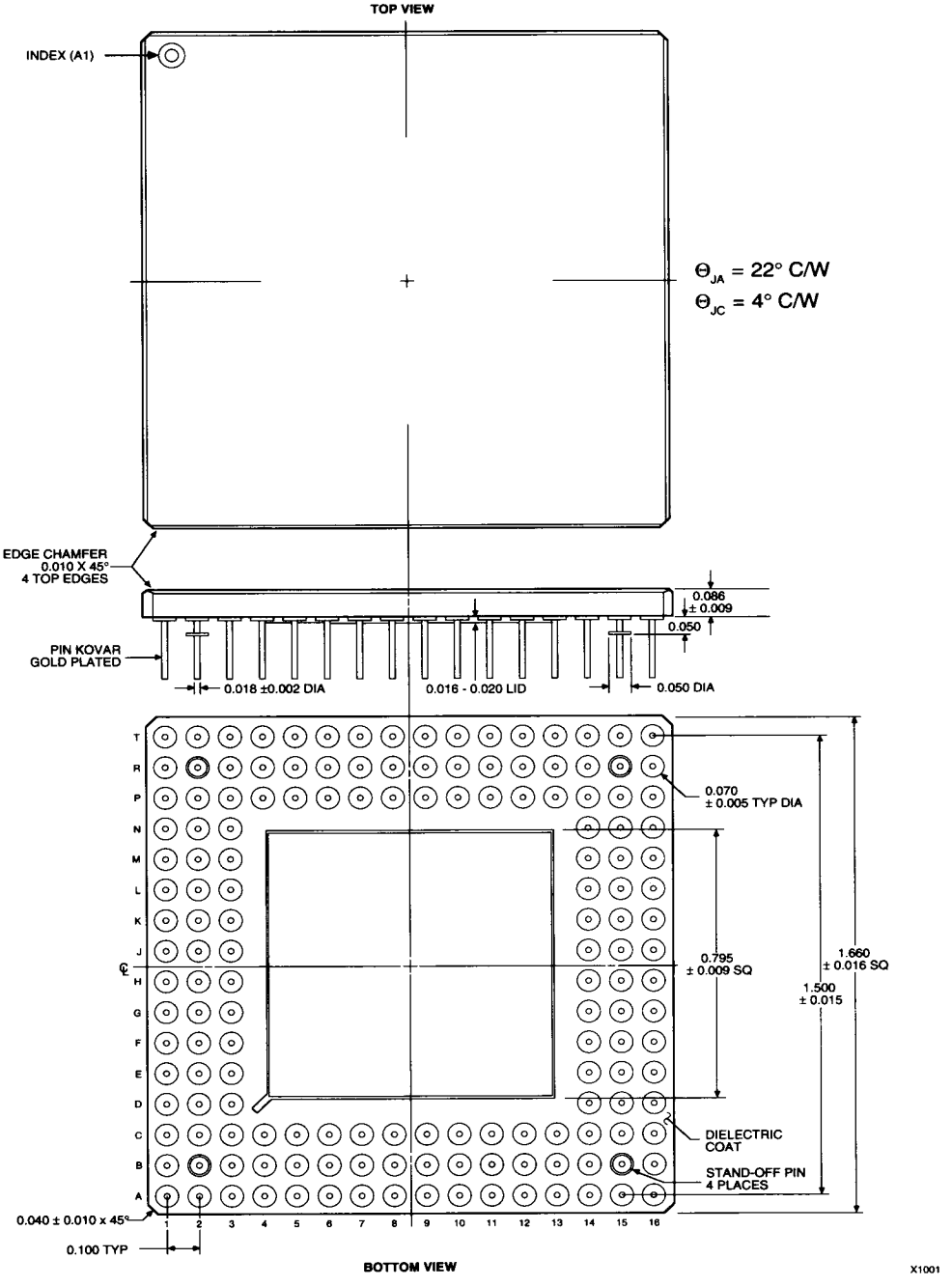
100-Pin PQFP Package

PACKAGE OUTLINES



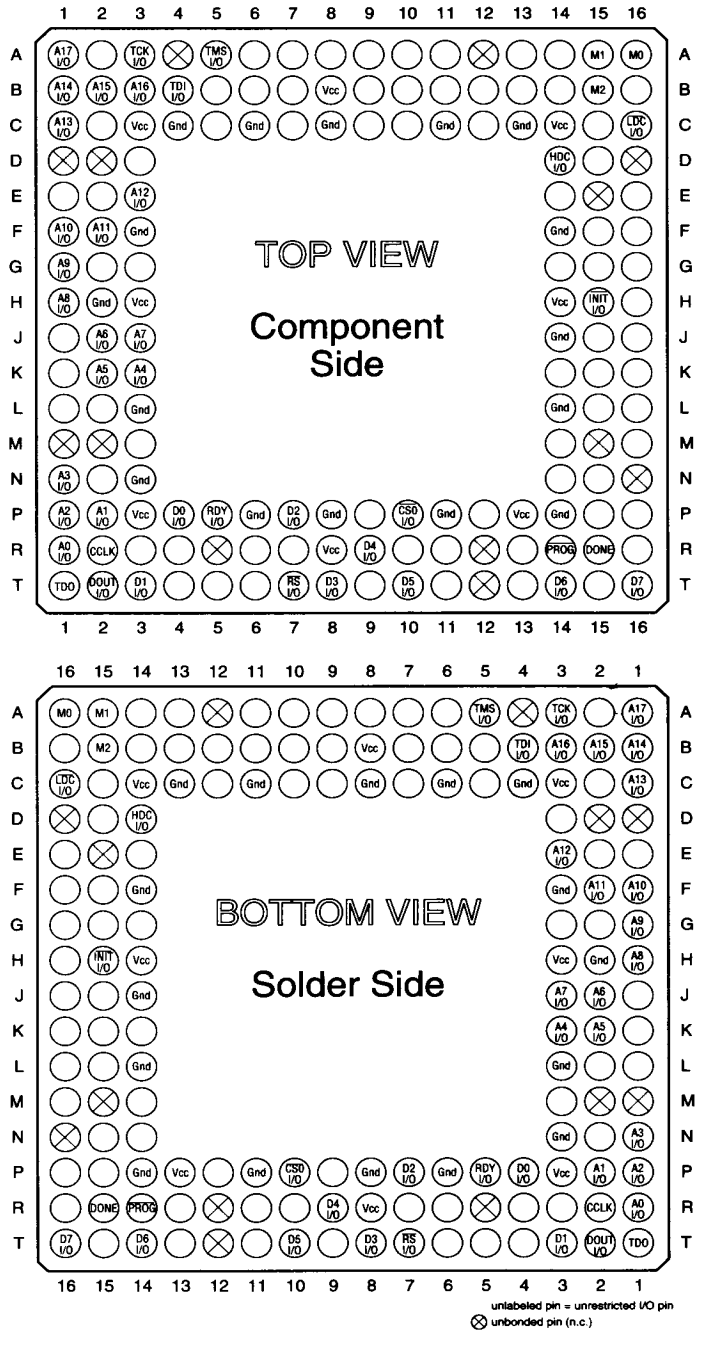
120-Pin PGA Package

PACKAGE OUTLINES

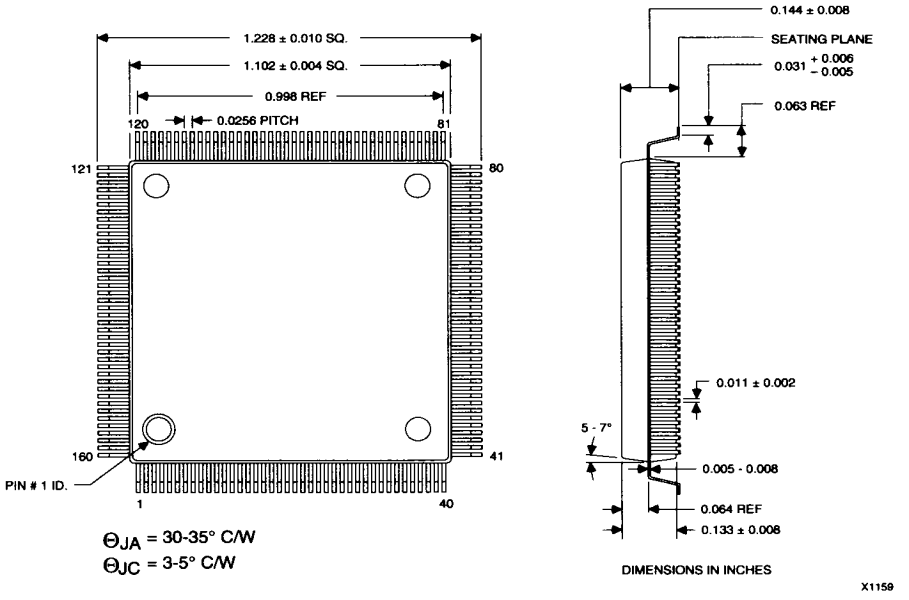


156-Pin PGA Package

XC4005-PG156, -PP156

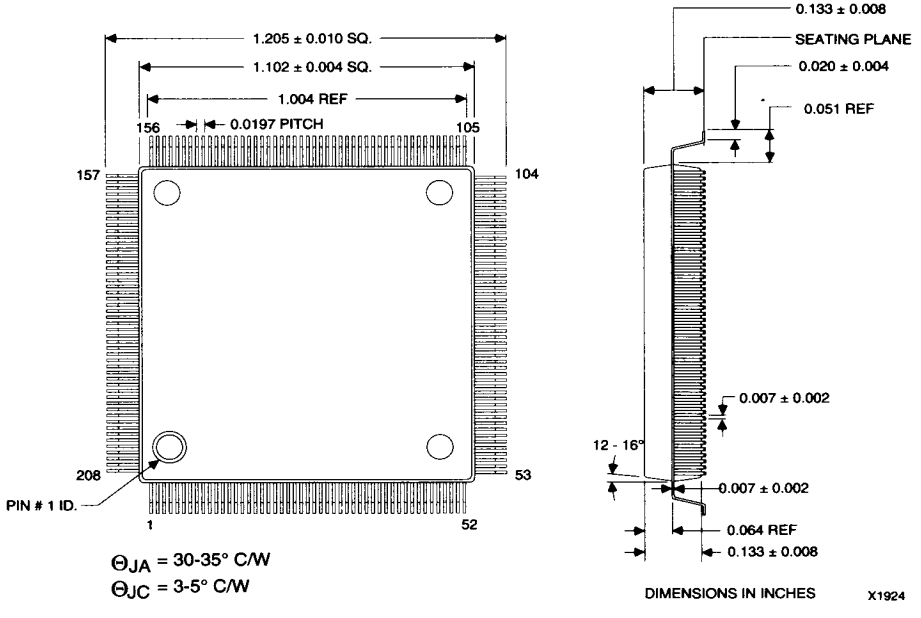


PACKAGE OUTLINES



Θ_{JA} = 30-35° C/W
Θ_{JC} = 3-5° C/W

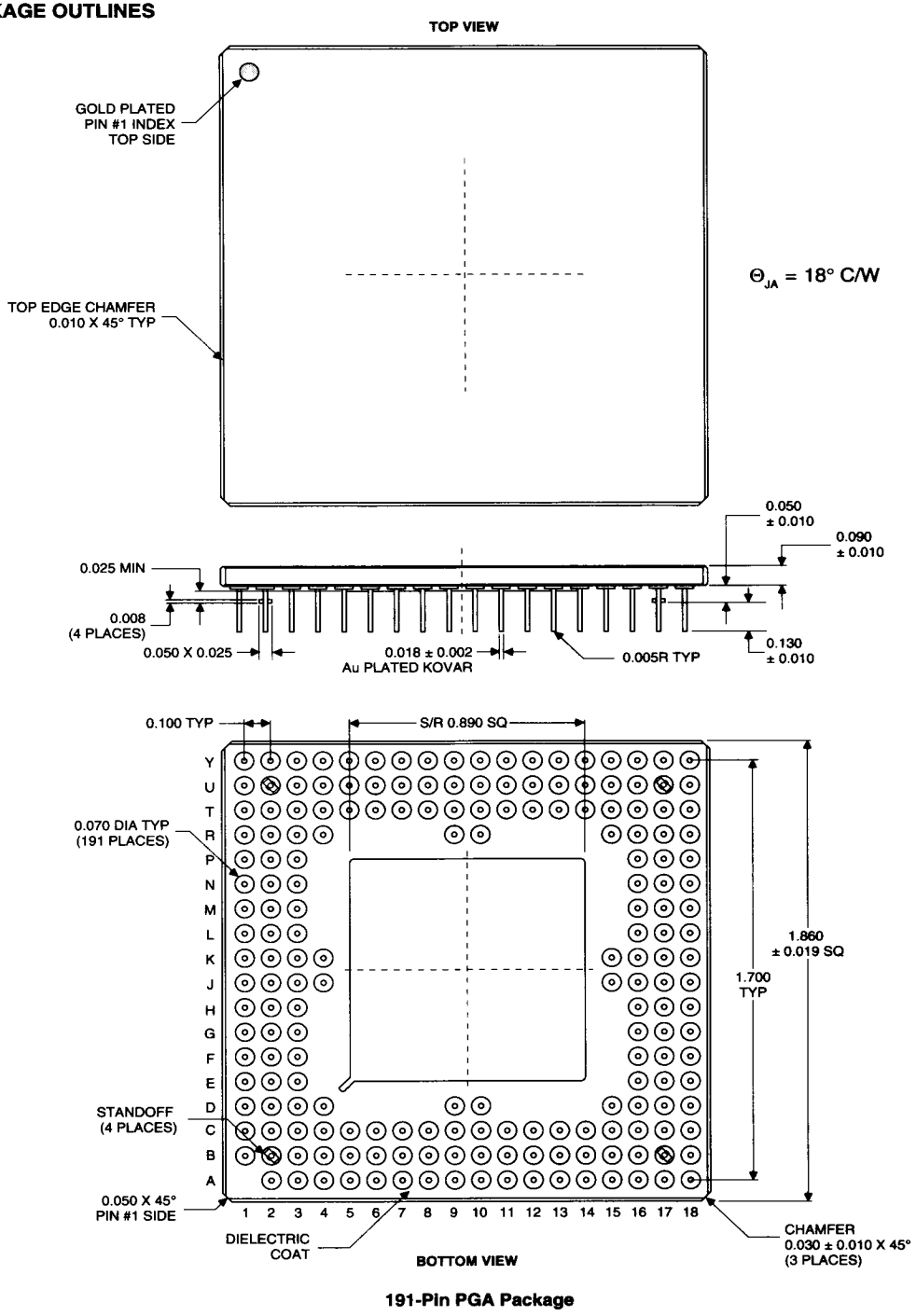
160-Pin PQFP Package (0.65 mm Lead Pitch)



Θ_{JA} = 30-35° C/W
Θ_{JC} = 3-5° C/W

208-Pin PQFP Package (0.50 mm Lead Pitch)

PACKAGE OUTLINES



191-Pin PGA Package

X1304A

XACT DEVELOPMENT SYSTEM HARDWARE REQUIREMENTS

Xilinx provides an integrated development system for design and implementation of LCA devices. The XACT Development System operates on any 386-based or 486-based IBM or IBM-compatible PC with 8 Mbytes of extended memory (RAM), 80 Mbytes of hard-disk space, and a VGA display.

Minimum Requirements

- 386 or 486-based IBM-PC or compatible
- One high-density floppy disk drive, 5.25" or 3.5"
- 80 Mbyte hard disk drive
- VGA display
- Two RS-232-C serial ports and one parallel port
- Mouse
- MS-DOS version 3.3 or higher

PC I/O Ports

The XACT Development System requires several I/O ports. A parallel port is needed for the software execution protection key. The key must be in place to allow Xilinx software to execute but is virtually transparent, and the port can be used simultaneously for a parallel printer or the Xilinx download cable. Several printer types are supported for text or graphic hard copy. Serial COM ports are used for a mouse and for the Configuration PROM Programmer.

PC Mouse

The Xilinx Development System programs are compatible with several varieties of mice offered for the PC. These include Mouse Systems PC Mouse (no device driver required), Microsoft (serial or parallel), LogiTech C7 and the FutureNet mouse. The Xilinx software supports any mouse directly that emulates the PC mouse or has a device driver that provides Microsoft compatibility and defines the PC COM port.

Please note however, only the Mouse System M4 and the LogiTech C7 will work with the VIEWLogic software, VIEWdraw-LCA and VIEWsim.

Apollo Workstation System Requirements

The Apollo system configuration needed to run the XACT Development System consists of:

- Apollo DN4000 Series or 400 Series
- Apollo Operating System SR10.3
- Mentor Graphics Version 7.0
- 60 Mbytes allocated for Xilinx design software
- 16 Mbytes of RAM
- Color Monitor
- X-Apollo Display Manager or MOTIF

Sun-3 Workstation System Requirements

The Sun-3 system configuration needed to run the XACT Development System consists of:

- Series 60 or better
- Sun Operating System OS4.1
- 60 Mbytes allocated for Xilinx design software
- 16 Mbytes of RAM
- Color Monitor
- X-Windows
- Openlook or MOTIF

Sun-4 Workstation System Requirements

The Sun-4 system configuration needed to run the XACT Development System consists of:

- Sun-4 and SparcStation Series
- Sun Operating System OS4.1
- 60 Mbytes allocated for Xilinx design software
- 16 MBytes of RAM
- Color Monitor
- X-Windows
- Openlook or MOTIF

DECstation System Requirements

The DECstation system configuration needed to run the XACT Development System consists of:

- DECstation 3100 Series
- Worksystem V2.2
- 60 Mbytes allocated for Xilinx design software
- Color Monitor
- 16 MBytes of RAM
- X-Windows
- DEC Windows or MOTIF