



High Speed CMOS Multilevel Pipeline Registers

QS29FCT520T
QS29FCT521T

QS29FCT2520T
QS29FCT2521T

FEATURES/BENEFITS

- Pin and function compatible to the Am29520
- Ground bounce controlled outputs
- Reduced output swing of 0-3.5V
- Available in DIP, ZIP, SOIC, QSOP, HQSOP
- TTL-compatible input and output levels
- CMOS power levels: <7.5 mW static
- Undershoot clamp diodes on all inputs
- Military product compliant to MIL-STD-883

FCT-T520T/1T

- JEDEC-FCT spec compatible
- Fastest CMOS logic family available
- A, B, and C speed grades with 6 ns t_{PD} for C
- I_{OL} = 48 mA Com., 32 mA Mil.

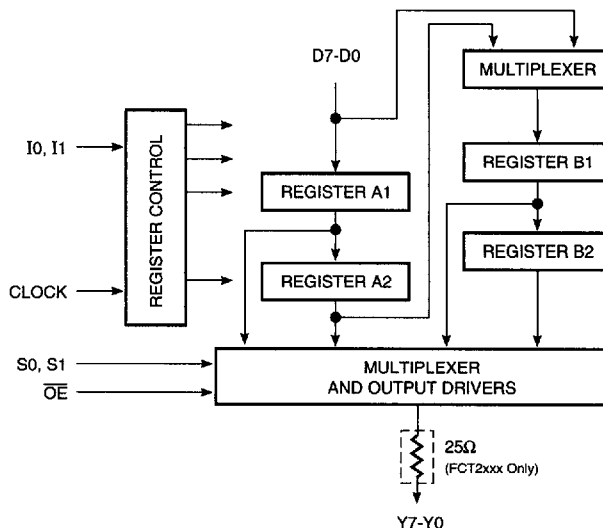
FCT-T 2520T/1T

- Built-in 25Ω series resistor outputs reduce reflection and other system noise
- A, B, and C speed grades with 6 ns t_{PD} for C
- I_{OL} = 12 mA Com.

DESCRIPTION

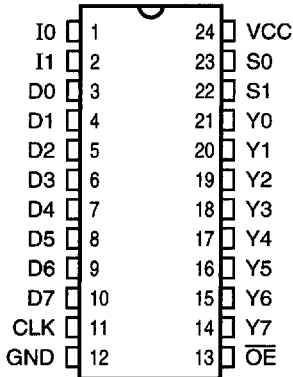
The QS29FCT520AT/BT and QS29FCT521AT/BT provide four 8-bit registers useful for temporary storage and for stage delays in pipelined systems. The four registers may be configured as a dual 2-level or single 4-level shift register pipeline. A single 8-bit input is provided, and any of the four registers may be selected for gating to the single 8-bit output. The 520 and 521 differ only in how the registers are loaded in the dual 2-rank mode, as shown in the function tables. The QS29FCT520/1 are pin and function compatible with the Am29520/1 bipolar parts, except for higher speed and significantly lower power.

FUNCTIONAL BLOCK DIAGRAM

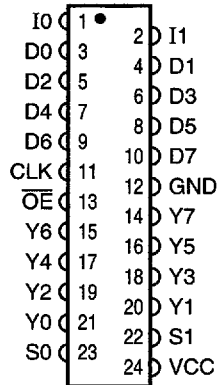


PIN CONFIGURATIONS (All Pins Top View)

PDIP, SOIC, QSOP, HQSOP



ZIP



PIN DESCRIPTION

Name	I/O	Description
D7-D0	I	Data Inputs
Y7-Y0	O	Data Outputs - Three State
I0, I1	I	Register Load Control
S0, S1	I	Register Output Select
CLK	I	Clock Pulse
OE	I	Output Enable

FUNCTION TABLES

REGISTER LOAD CONTROL

PART NO	Register Control Code			
	I1,0 = LL = 0	I1,0 = LH = 1	I1,0 = HL = 2	I1,0 = HH = 3
FCT520				Hold Data
FCT521				Hold Data

REGISTER OUTPUT SELECTION

S1	S0	OE	Y1	Register to Y7-Y0
L	L	L	Data	B2
L	H	L	Data	B1
H	L	L	Data	A2
H	H	L	Data	A1
X	X	H	Hi-Z	Outputs Disabled

ABSOLUTE MAXIMUM RATINGS

Supply Voltage to Ground	-0.5V to +7.0V
DC Output Voltage V_{OUT}	-0.5V to +7.0V
DC Input Voltage V_{IN}	-0.5V to +7.0V
AC Input Voltage (for a pulse width ≤ 20 ns)	-3.0V
DC Input Diode Current with $V_{IN} < 0$	-20 mA
DC Output Diode Current with $V_{OUT} < 0$	-50 mA
DC Output Current Max. Sink Current/ P_{IN}	120 mA
Maximum Power Dissipation	0.5 watts
T_{STG} Storage Temperature	-65° to +150°C

Note: Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to this device resulting in functional or reliability type failures.

CAPACITANCE

$T_A = 25^\circ\text{C}$, $f = 1$ MHz, $V_{IN} = 0\text{V}$, $V_{OUT} = 0\text{V}$

Pins	SOIC	QSOP	PDIP	ZIP	Unit
1-11, 13, 22, 23	4	4	5	7	pF
14-21	6	6	7	9	pF
—	8	8	9	10	pF

Note: Capacitance is characterized but not tested.

POWER SUPPLY CHARACTERISTICS

Symbol	Parameter	Test Conditions ⁽¹⁾	Min	Max	Unit
I_{CC}	Quiescent Power Supply Current	$V_{CC} = \text{Max.}$, $\text{freq} = 0$ $0\text{V} \leq V_{IN} \leq 0.2\text{V}$ or $V_{CC} - 0.2\text{V} \leq V_{IN} \leq V_{CC}$	—	1.5	mA
ΔI_{CC}	Supply Current per Input @ TTL HIGH	$V_{CC} = \text{Max.}$, $V_{IN} = 3.4\text{V}$, $\text{freq} = 0$ ⁽²⁾	—	2.0	mA
Q_{CCD}	Supply Current per Input per MHz	$V_{CC} = \text{Max.}$, Outputs Open and Enabled One Bit Toggling @ 50% Duty Cycle Other Inputs at GND or V_{CC} ^(3,4)	—	0.25	mA/MHz

Notes:

- For conditions shown as Min. or Max., use the appropriate values specified under DC specifications.
- Per TTL driven input ($V_{IN} = 3.4\text{V}$).
- For flip-flops, Q_{CCD} is measured by switching one of the data input pins so that the output changes every clock cycle. This is a measurement of device power consumption only and does not include power to drive load capacitance or tester capacitance. This parameter is guaranteed by design but not tested.
- I_C can be computed using the above parameters as explained in the Technical Overview section.

DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE

Commercial $T_A = 0^{\circ}\text{C}$ to 70°C , $V_{CC} = 5.0\text{V} \pm 5\%$

Military $T_A = -55^{\circ}\text{C}$ to 125°C , $V_{CC} = 5.0\text{V} \pm 10\%$

Symbol	Parameter	Test Conditions	Min	Typ ⁽¹⁾	Max	Unit
V_{IH}	Input HIGH Voltage	Logic HIGH for All Inputs	2.0	—	—	V
V_{IL}	Input LOW Voltage	Logic LOW for All Inputs	—	—	0.8	V
ΔV_T	Input Hysteresis	$V_{TLH} - V_{THL}$ for All Inputs	—	0.2	—	V
$ I_{IH} $ $ I_{IL} $	Input Current Input HIGH or LOW	$V_{CC} = \text{Max.}, 0 \leq V_{IN} < V_{CC}$	—	—	5	μA
$ I_{OZ} $	Off-State Output Current (Hi-Z)	$V_{CC} = \text{Max.}, 0 \leq V_{IN} \leq V_{CC}$	—	—	5	μA
I_{OS}	Short Circuit Current (FCTXXX)	$V_{CC} = \text{Max.}, V_{OUT} = \text{GND}^{(2,3)}$	-60	—	—	mA
I_{OR}	Current Drive (FCT2XXX)	$V_{CC} = \text{Min.}, V_{OUT} = 2.0\text{V}^{(3)}$	50	—	—	mA
V_{IC}	Input Clamp Voltage	$V_{CC} = \text{Min.}, I_{IN} = -18\text{ mA}, T_A = 25^{\circ}\text{C}^{(3)}$	—	-0.7	-1.2	V
V_{OH}	Output HIGH Voltage	$V_{CC} = \text{Min.}, I_{OH} = -12\text{ mA (MIL)}$ $I_{OH} = -15\text{ mA (COM)}$	2.4 2.4	— —	— —	V
V_{OL}	Output LOW Voltage (FCTXXX)	$V_{CC} = \text{Min.}, I_{OL} = 32\text{ mA (MIL)}$ $I_{OL} = 48\text{ mA (COM)}$	— —	— —	0.50 0.50	V
V_{OL}	Output LOW Voltage (FCT2XXX - 25Ω)	$V_{CC} = \text{Min.}, I_{OL} = 12\text{ mA (MIL)}$ $I_{OL} = 12\text{ mA (COM)}$	— —	— —	0.50 0.50	V
R_{OUT}	Output Resistance (FCT2XXX - 25Ω)	$V_{CC} = \text{Min.}, I_{OL} = 12\text{ mA (MIL)}$ $I_{OL} = 12\text{ mA (COM)}$	— 20	25 28	— 40	Ω

Notes:

1. Typical values indicate $V_{CC} = 5.0\text{V}$ and $T_A = 25^{\circ}\text{C}$.
2. Not more than one output should be shorted and the duration is ≤ 1 second.
3. These parameters are guaranteed by design but not tested.

SWITCHING CHARACTERISTICS OVER OPERATING RANGE

Commercial T_A = 0°C to 70°C, V_{CC} = 5.0V ± 5%

Military T_A = -55°C to 125°C, V_{CC} = 5.0V ± 10%

C_{LOAD} = 50 pF, R_{LOAD} = 500Ω unless otherwise noted.

Symbol	Description		29FCT 520/1A 2520/1A		29FCT 520/1B 2520/1B		29FCT 520/1C 2520/1C		Unit
			Min	Max	Min	Max	Min	Max	
t _{CPD}	Clock to Y Delay ⁽¹⁾	Com Mil	2 2	14 16	2 2	7.5 8	2 2	6 7	ns
t _{DY}	S0, S1 to Y Delay ⁽¹⁾	Com Mil	5 6	13 15	2.5 2	7.5 8	2 2	6 7	ns
t _{DS}	Data to CLK Setup Time	Com Mil	5 6	— —	2.5 2.8	— —	2.5 2.8	— —	ns
t _{DH}	Data to CLK Hold Time	Com Mil	2 2	— —	2 2	— —	2 2	— —	ns
t _{IS}	I0, I1 to CLK Setup Time	Com Mil	5 6	— —	4 4.5	— —	4 4.5	— —	ns
t _{IH}	I0, I1 to CLK Hold Time	Com Mil	2 2	— —	2 2	— —	2 2	— —	ns
t _{OZ}	Output Disable Time ⁽²⁾ OE to Y	Com Mil	1.5 1.5	12 13	1.5 1.5	7 7.5	1.5 1.5	6 6	ns
t _{OE}	Output Enable Time ⁽¹⁾ OE to Y	Com Mil	1.5 1.5	15 16	1.5 1.5	7.5 8	1.5 1.5	6 7	ns
t _{OW}	CLK Pulse Width, ⁽²⁾ HIGH or LOW	Com Mil	7 8	— —	5.5 6	— —	5.5 6	— —	ns

Notes:

1. Minimums guaranteed but not tested.
2. This parameter is guaranteed by design but not tested.
3. See Test Circuit and Waveforms.