QUALITY SEMICONDUCTOR, INC.

QuickSwitch® Products
High-Speed CMOS QuickSwitch 16-Bit Widebus™ Compatible Bus Switches

FEATURES/BENEFITS

- Enhanced N channel FET with no inherent diode to V_{CC}
- 5Ω bidirectional switches connect inputs to outputs
- Pin compatible with FCT16245
- Flowthrough pinout for easy layout
- Zero propagation delay, zero ground bounce
- Undershoot clamp diodes on all switch and control inputs
- TTL-compatible control inputs
- Available in 48-pin SSOP (PV)

APPLICATIONS

- Hot-docking, hot-swapping (Application Note AN-13)
- Voltage translation (5V to 3.3V; Application Note AN-11)
- Bus switching, isolation
- Power conservation, clock gating
- Logic replacement

DESCRIPTION

The QS316245 provides a set of 16 high-speed CMOS TTL-compatible bus switches (two banks of 8 switches each) in a flow-thru pinout. The low ON resistance of the QS316245 allows inputs to be connected to outputs without adding propagation delay and without generating additional ground bounce noise. The Output Enable ($\overline{OEn}$) signal turns the switches on similar to the $\overline{OEn}$ signal of the 74'245. The QS316245 is ideally suited for 5V to 3.3V translation, bus switching and isolation, and hot insertion.

QuickSwitch devices provide an order of magnitude faster speed than conventional logic devices.

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Figure 1. Functional Block Diagram

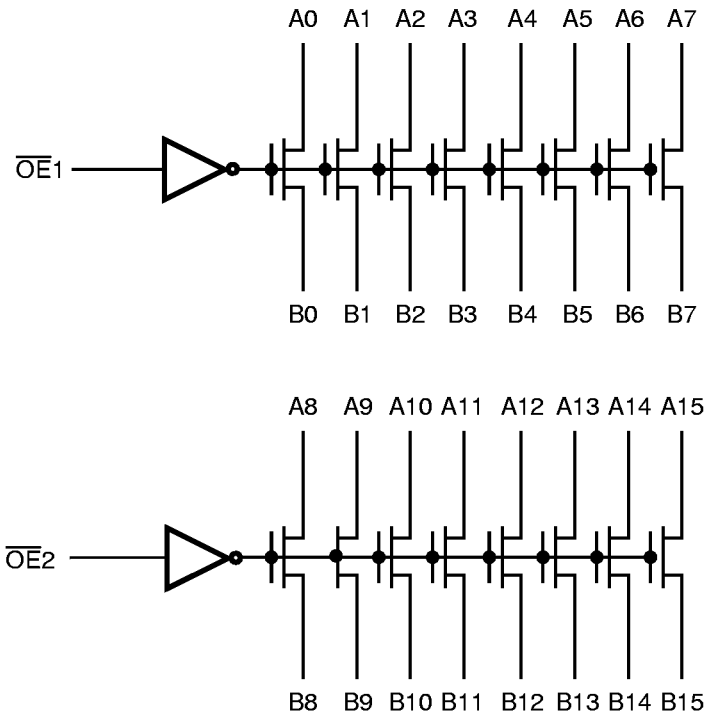

Table 1. Pin Description

Name	I/O	Function
An	I/O	Bus A
Bn	I/O	Bus B
$\overline{OEn}$	I	Bus Enable

Table 2. Function Table

$\overline{OEn}$	An	Function
L	Bn	Connect
H	Z	Disconnect

Figure 2. Pin Configuration (All Pins Top View)

SSOP(PV)

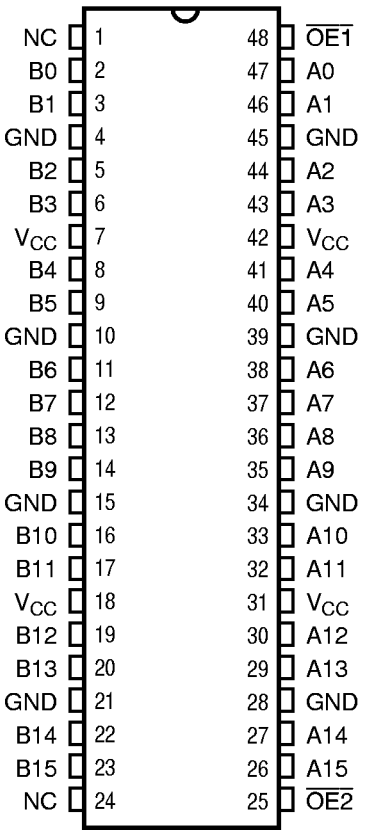

Table 3. Absolute Maximum Rating

Supply Voltage to Ground	–0.5V to +7.0V
DC Switch Voltage to Ground	–0.5V to +7.0V
DC Input Voltage V_{IN}	–0.5V to +7.0V
AC Input Voltage (for a pulse width ≤ 20ns)	-3.0V
DC Output Current Max. Sink Current/Pin	120mA
Maximum Power Dissipation	0.5 watts
T_{STG} Storage Temperature	–65° to +150°C

Note: ABSOLUTE MAXIMUM CONTINUOUS RATINGS are those values beyond which damage to the device may occur. Exposure to these conditions or conditions beyond those indicated may adversely affect device reliability. Functional operation under absolute-maximum conditions is not implied.

Table 4. Capacitance

T_A = 25°C, f = 1MHz, V_{IN} = 0V, V_{OUT} = 0V

Pins	SSOP Typ	SSOP Max	Unit
Control Inputs	3	5	pF
QuickSwitch Channels (Switch OFF)	5	7	pF

Note: Capacitance is guaranteed but not tested. For total capacitance while the switch is ON, please see Section 1 under "Input and Switch Capacitance."

Table 5. DC Electrical Characteristics Over Operating Range

T_A = –40°C to 85°C, V_{CC} = 5.0V ± 10%

Symbol	Parameter	Test Conditions	Min	Typ(1)	Max	Unit
V_{IH}	Input HIGH Voltage	Guaranteed Logic HIGH for Control Inputs	2.0	—	—	V
V_{IL}	Input LOW Voltage	Guaranteed Logic LOW for Control Inputs	—	—	0.8	V
$\| I_{IN} \|$	Input Leakage Current (Control Inputs)	$0 \le V_{IN} \le V_{CC}$	—	—	1	µA
$\| I_{OZ} \|$	Off-State Current (Hi-Z)	$0 \le V_{OUT} \le V_{CC}$, Switches OFF	—	—	1	µA
R_{ON}	Switch ON Resistance(2)	V_{CC} = Min., V_{IN} = 0.0V I_{ON} = 30mA	—	5	7	Ω
R_{ON}	Switch ON Resistance(2)	V_{CC} = Min., V_{IN} = 2.4V I_{ON} = 15mA	—	10	15	Ω
V_P	Pass Voltage(3)	$V_{IN} = V_{CC}$ = 5V, I_{OUT} = –5µA	3.7	4	4.2	V

Notes:
1. Typical values indicate V_{CC} = 5.0V and T_A = 25°C.
2. For a diagram explaining the procedure for R_{ON} measurement, please see Section 1 under "DC Electrical Characteristics." Max. value of R_{ON} guaranteed but not production tested.
3. Pass Voltage is guaranteed, but not production tested.

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Figure 3. Typical ON Resistance vs V_{IN} at V_{CC} = 5.0V

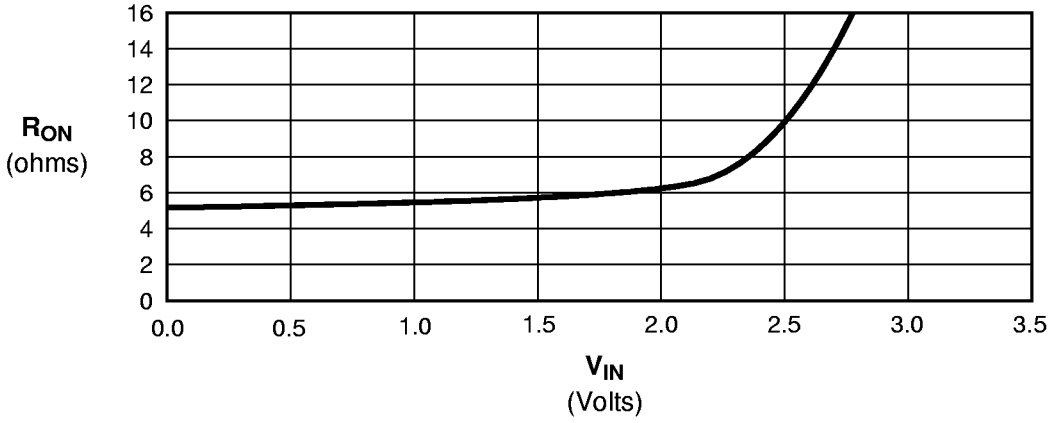


Table 6. Power Supply Characteristics Over Operating Range

T_A = –40°C to 85°C, V_{CC} = 5.0V ± 10%

Symbol	Parameter	Test Conditions[1]	Max	Unit
I_{CCQ}	Quiescent Power Supply Current	V_{CC} = Max., V_{IN} = GND or V_{CC}, f = 0	3.0	µA
ΔI_{CC}	Power Supply Current per Input HIGH[2]	V_{CC} = Max., V_{IN} = 3.4V, f = 0 per Control Input	1.5	mA
Q_{CCD}	Dynamic Power Supply Current per MHz[3]	V_{CC} = Max., A and B Pins Open, Per Control Input Toggling @ 50% Duty Cycle	0.25	mA/ MHz

Notes:
1. For conditions shown as Min. or Max., use the appropriate values specified under DC specifications.
2. Per TTL driven input (V_{IN} = 3.4V, control inputs only). A and B pins do not contribute to I_{CC}.
3. This current applies to the control inputs only and represents the current required to switch internal capacitance at the specified frequency. The A and B inputs generate no significant AC or DC currents as they transition. This parameter is guaranteed, but not production tested.

Table 7. Switching Characteristics Over Operating Range

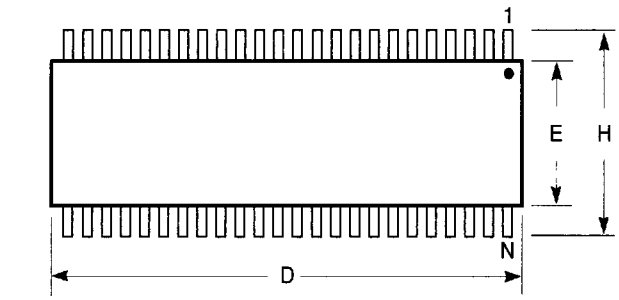
T_A = –40°C to 85°C, V_{CC} = 5.0V ± 10%
C_{LOAD} = 50pF, R_{LOAD} = 500Ω unless otherwise noted.

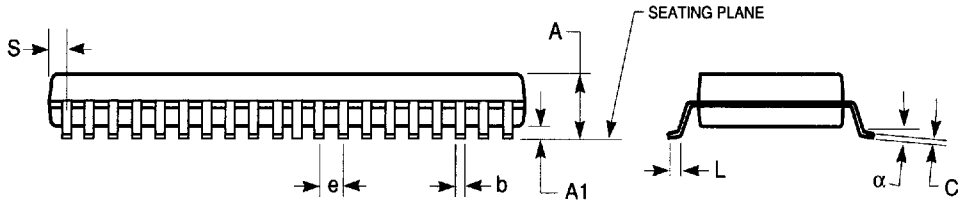
Symbol	Description[1]	Min	Typ	Max	Unit
t_{PLH} t_{PHL}	Data Propagation Delay[2,4] An to Bn, Bn to An	—	—	0.25[3]	ns
t_{PZL} t_{PZH}	Switch Turn-on Delay $\overline{OE}$n to An/Bn	1.5	—	6.5	ns
t_{PLZ} t_{PHZ}	Switch Turn-off Delay[2] $\overline{OE}$n to An/Bn	1.5	—	5.5	ns

Notes:
1. See Test Circuit and Waveforms.
2. This parameter is guaranteed, but not tested.
3. The time constant for the switch alone is of the order of 0.25ns for C_L = 50pF.
4. The bus switch contributes no propagation delay other than the RC delay of the ON resistance of the switch and the load capacitance. Since this time constant is much smaller than the rise/fall times of typical driving signals, it adds very little propagation delay to the system. Propagation delay of the bus switch when used in a system is determined by the driving circuit on the driving side of the switch and its interaction with the load on the driven side.

300-MIL SSOP - Package Code PV

Shrink Small Outline Package
Plastic Small Outline Gull-Wing





Notes:
1. Refer to applicable symbol list.
2. All dimensions are in inches.
3. N is the number of lead positions.
4. Dimensions D and E are to be measured at maximum material condition but do not include mold flash. Allowable mold flash is 0.006in. per side.
5. Lead coplanarity is 0.004in. maximum.

JEDEC#	MO-118AA			MO-118AB		
DWG#	PSS-48B			PSS-56B		
Symbol	Min	Nom	Max	Min	Nom	Max
A	0.095	0.102	0.110	0.095	0.102	0.110
A1	0.008	0.012	0.016	0.008	0.012	0.016
b	0.008	0.010	0.0135	0.008	0.010	0.0135
C	0.005	0.008	0.010	0.005	0.008	0.010
D	0.620	0.625	0.630	0.720	0.725	0.730
E	0.291	0.295	0.299	0.291	0.295	0.299
e	0.025 BSC			0.025 BSC		
H	0.395	0.410	0.420	0.395	0.410	0.420
L	0.020	0.030	0.040	0.020	0.030	0.040
N	48			56		
α	0°	5°	8°	0°	5°	8°
S	0.022	0.025	0.028	0.022	0.025	0.028