QUALITY SEMICONDUCTOR, INC.

# QuickSwitch® Products
# QuickScan™
# 9-Bit Universal JTAG Access Port With Output Enable

## FEATURES/BENEFITS

- IEEE 1149.1a-1993 (JTAG) compliant
- JTAG access to data, control and address lines
- Capture and observe the embedded node
- QuickSwitch® fast switch technology
- TTL-compatible I/O
- Direct bus connection when switches on
- Balanced ±8mA drive in JTAG Mode
- Low power QCMOS™ technology
- Zero added signal skew in non-JTAG mode
- Zero propagation delay in non-JTAG mode
- Includes CLAMP and HIGH-Z instructions
- Bidirectional data paths in non-scan mode
- Available in 28-pin QSOP

## DESCRIPTION

The QS3J309 JTAG QuickScan device is designed to provide JTAG access to data, address, and control lines (or internal signals), while being transparent to the system during normal (non-JTAG) operation. This is achieved by combining the "like-a-wire" characteristics of QSI's QuickSwitch devices with a JTAG boundary scan access port. The QS3J309 can provide scan coverage of system functional blocks without the cost overhead and performance penalties of individual scan components. When not in boundary scan mode, the QS3J309 QuickSwitch pass gates are turned on, allowing transparent, bidirectional data propagation. When in boundary scan mode, scan data can be captured from or loaded onto the data bus. The serial access port also can be used to monitor bus data while the device remains electrically transparent. This feature is useful for debugging or bus monitoring. The QS3J309 is IEEE1149.1a-1993 compliant, with complete instruction register functionality, bypass and 32-bit device ID register.

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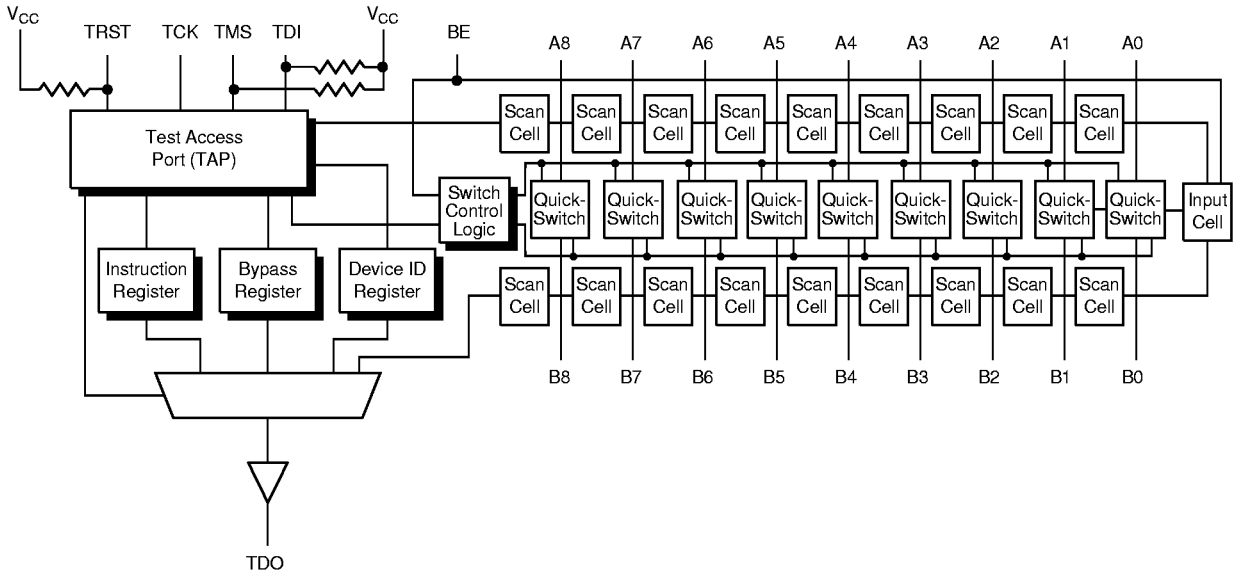
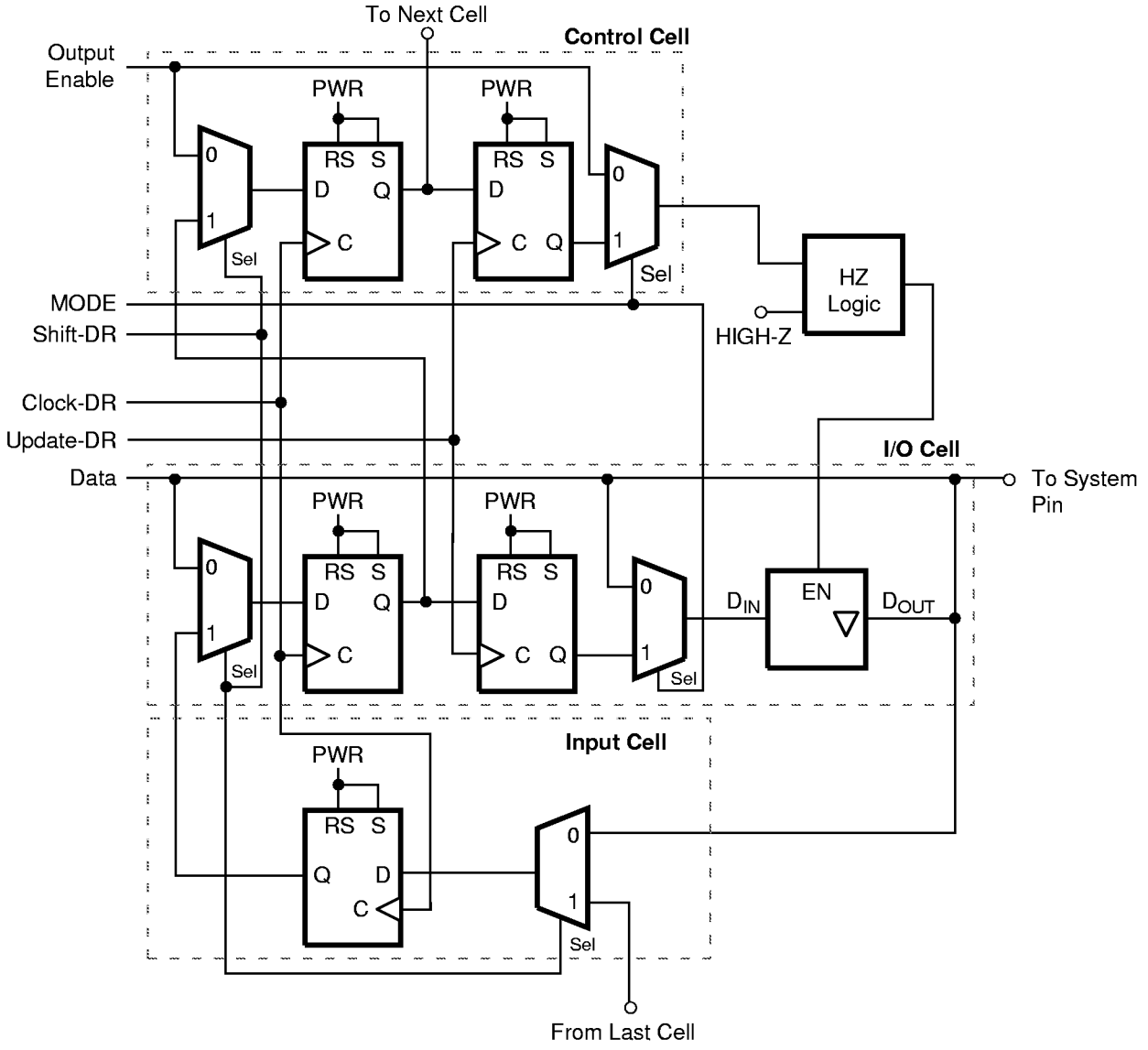
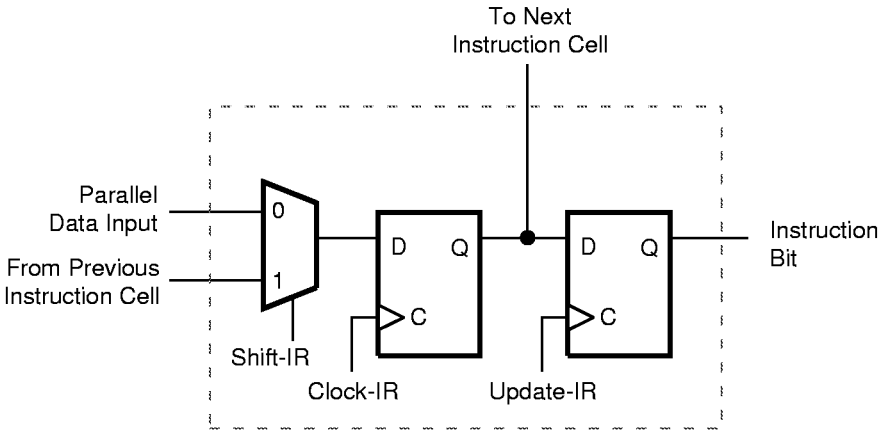
## Figure 1. Functional Block Diagram



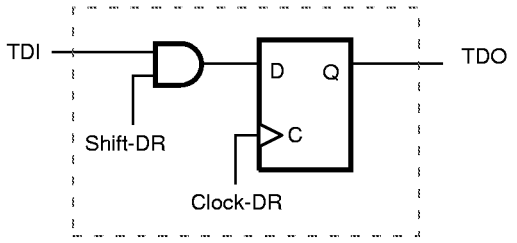
## Figure 2. Scan Cell



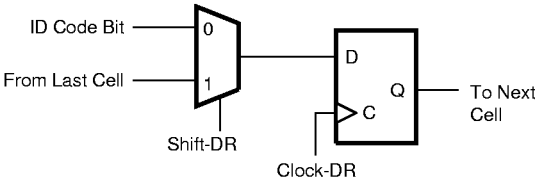

## Figure 3. Instruction Register Cell



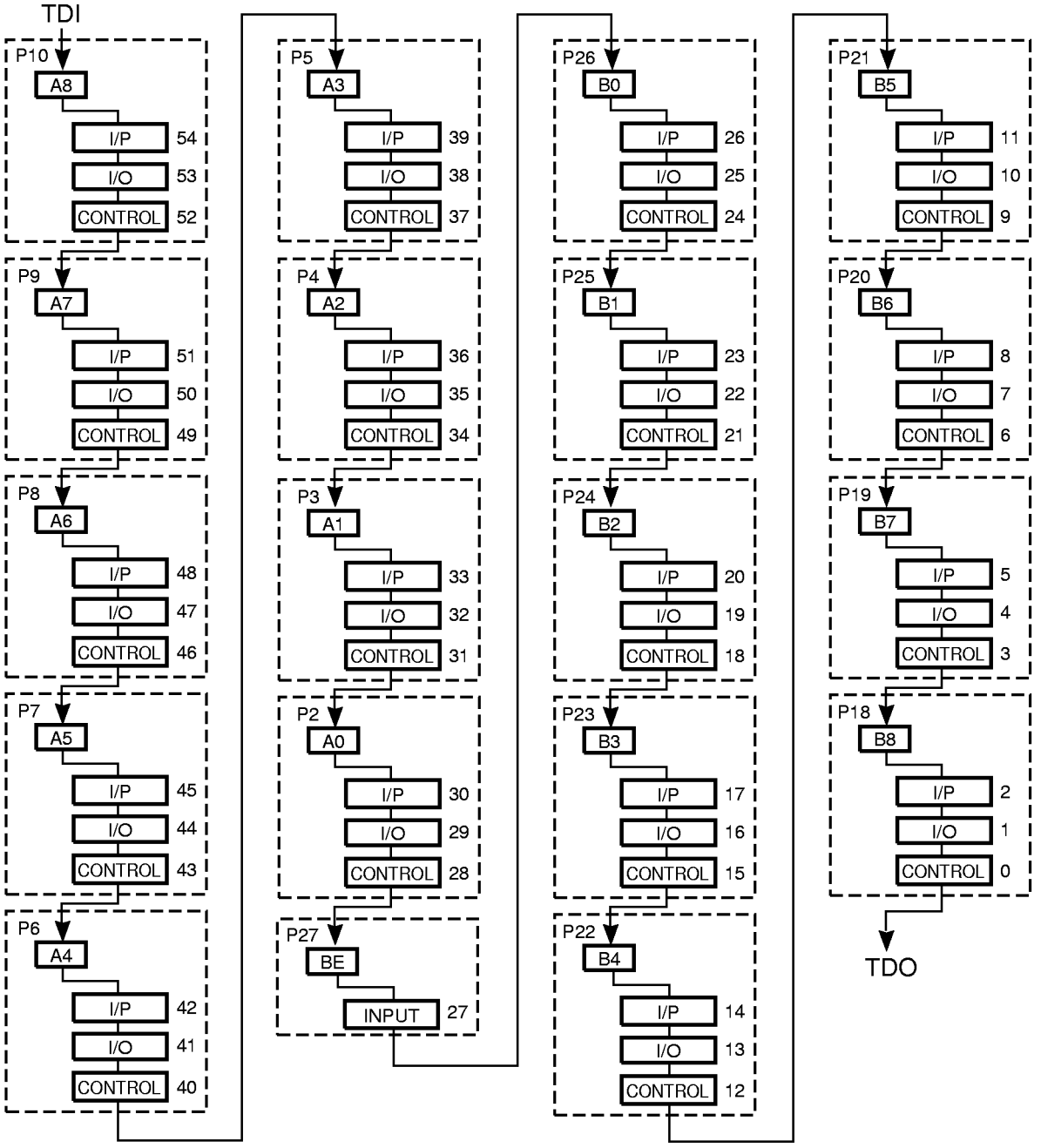
## Figure 4. Bypass Register




## Figure 5. Device ID Register




## Figure 6. Scan Chain Definition

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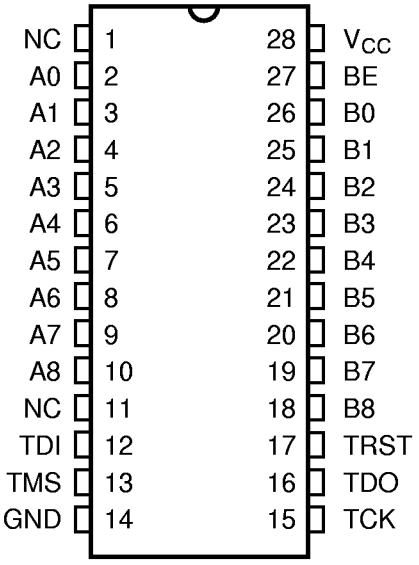
## Figure 7. Pin Configuration

(All Pins Top View)

QSOP




## Table 1. Function Table

(Non-scan Mode: TAP Controller in RESET mode)

| Inputs | | Output |
|---|---|---|
| BE | A | B |
| H | X | Z |
| L | L | L |
| L | H | H |

## Table 2. Instruction Register Definitions

| Instruction Code | Instruction | Switch State | BE |
|---|---|---|---|
| 00000000 | EXTEST | OFF | X |
| All others | BYPASS | ON | L |
| 00000001 | SAMPLE/PRELOAD | ON | L |
| 00000010 | IDCODE | ON | L |
| 00000100 | HIGH-Z | OFF | X |
| 00000101 | CLAMP | OFF | X |
| 00000110 | BOUNDARY READ | ON | L |

## Table 3. Pin Definitions

| Name | I/O | Description |
|---|---|---|
| A8-A0 | I/O | Normal function data inputs or outputs. |
| B8-B0 | I/O | Normal function data inputs or outputs. |
| TRST | I | Asynchronously resets the TAP controller. |
| BE | I | Normal function bus enable input. See Table 1 Function Table for normal function. |
| TCK | I | Test Clock. One of four terminals required by IEEE Standard 1149.1a-1993. Test operations of the device are synchronous to TCK. |
| TMS | O | Test Mode Select. One of four terminals required by IEEE Standard 1149.1a-1993. The signal received at TMS is decoded by the TAP controller to control the test operations. |
| TDI | I | Test Data Input. One of four terminals required by IEEE Standard 1149.1a-1993. Serial test instructions and data are received by the test logic at TDI. |
| TDO | O | Test Data Output. One of four terminals required by IEEE Standard 1149.1a-1993. TDO is the serial output for test instructions and data from the test logic. |

## Table 4. Absolute Maximum Ratings

| | |
|---|---|
| Supply Voltage to Ground | –0.5V to +7.0V |
| DC Switch Voltage $V_S$ | –0.5V to $V_{CC}$ + 0.5V |
| DC Input Voltage $V_{IN}$ | –0.5V to +7.0V |
| AC Input Voltage (for a pulse width ≤ 20ns) | –3.0V |
| DC Input Diode Current with $V_{IN}$ < 0 | –20mA |
| DC Output Current Max. Sink Current/Pin | 120mA |
| Maximum Power Dissipation | 0.9 watts |
| $T_{STG}$ Storage Temperature | –50° to +125°C |

**Note:** Absolute Maximum Ratings are those conditions beyond which damage to the device may occur. Exposure to these conditions or beyond those indicated may adversely affect device reliability. Functional operation under absolute maximum rating conditions is not implied.

## Table 5. DC Electrical Characteristics Over Operating Range

Industrial: $T_A$ = –40°C to 85°C, $V_{CC}$ = 5.0V ± 10%

| Symbol | Parameter | Test Conditions | Min | Typ(1) | Max | Unit |
|---|---|---|---|---|---|---|
| $V_{IH}$ | Input HIGH Voltage | Guaranteed Logic HIGH for Inputs | 2.0 | — | — | V |
| $V_{IL}$ | Input LOW Voltage | Guaranteed Logic LOW for Inputs | — | — | 0.8 | V |
| $V_{OH}$ | Output HIGH Voltage | $V_{CC}$ = Min, $I_{OH}$ = –8mA | 2.4 | — | — | V |
| | (Scan mode) | $V_{CC}$ = 4.5V, $I_{OH}$ = –100µA | 4.3 | — | — | |
| $V_{OL}$ | Output LOW Voltage | $V_{CC}$ = Min, $I_{OL}$ = 8mA | — | — | 0.4 | V |
| | (Scan mode) | $V_{CC}$ = 4.5V, $I_{OL}$ = 100µA | — | — | 0.2 | |
| $\|I_{IN}\|$ | Input Leakage Current | $V_{IN}$ = $V_{CC}$ | — | — | 20 | µA |
| | | $V_{IN}$ = GND | — | — | 500 | |
| $\|I_{OZ}\|$ | Off-State Current (Hi-Z) | 0 ≤ A ≤ $V_{CC}$, 0 ≤ B ≤ $V_{CC}$ | — | — | 10 | µA |
| $R_{ON}$ | Switch ON Resistance(2) | $V_{CC}$ = Min., $V_{IN}$ = 0.0V, $I_{ON}$ = 30mA | — | 5 | 7 | Ω |
| $R_{ON}$ | Switch ON Resistance(2) | $V_{CC}$ = Min., $V_{IN}$ = 2.4V, $I_{ON}$ = 15mA | — | 10 | 15 | Ω |
| $R_{ON}$ | Switch ON Resistance(2) | $V_{CC}$ = Min., $V_{IN}$ = 4.0V, $I_{ON}$ = 15mA | — | 17 | 20 | Ω |

**Notes:**

1. Typical values indicate $V_{CC}$ = 5.0V and $T_A$ = 25°C. For a diagram explaining the procedure for $R_{ON}$ measurement, please see Section 1 under "DC Electrical Characteristics."

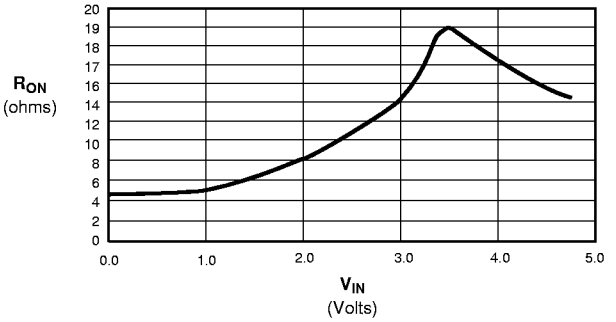
## Table 6. Capacitance

$T_A$ = 25°C, f = 1MHz, $V_{IN}$ = 0V, $V_{OUT}$ = 0V

| Pins | Typ | Unit |
|---|---|---|
| Control/JTAG Pins | 8 | pF |
| QuickSwitch Channels (OFF) | 16 | pF |

**Note:** Capacitance is characterized but not production tested. For total capacitance while the switch is ON, please see Section1 under "Input and Switch Capacitance."

## Figure 8. Typical Switch ON Resistance Characteristics vs $V_{IN}$ at 4.75 $V_{CC}$



## Table 7. Power Supply Characteristics Over Operating Range

Industrial: $T_A = -40°C$ to $85°C$, $V_{CC} = 5.0V \pm 10\%$

| Symbol | Parameter | Test Conditions[1] | Max | Unit |
|---|---|---|---|---|
| $I_{CCQ}$ | Quiescent Power Supply Current | $V_{CC}$ = Max., f = 0<br>TMS = TDI = TRST = $V_{CC}$ | 0.25 | mA |
| | | $V_{CC}$ = Max., f = 0[4]<br>TMS = TDI = TRST = GND, TCK = $V_{CC}$ | 1.5 | |
| | | $V_{CC}$ = Max., f = 0[4]<br>TCK = TMS = TDI = TRST = GND | 5.0 | |
| $\Delta I_{CC}$ | Power Supply Current per Input HIGH[2] | $V_{CC}$ = Max., $V_{IN}$ = 3.4V, f = 0 | 2.5 | mA |
| $Q_{CCD}$ | Dynamic Power Supply Current per MHz[3] | $V_{CC}$ = Max., A & B Pins Open, Controls Toggling @ 50% Duty Cycle | 0.5 | mA/ MHz |

**Notes:**

1. For conditions shown as Min. or Max., use the appropriate values specified under DC specifications.
2. Per TTL driven input ($V_{IN}$ = 3.4V, control inputs only). A and B pins do not contribute to $\Delta I_{CC}$.
3. This current applies to the control inputs only and represents the current required to switch internal capacitance at the specified frequency. The A and B inputs generate no significant AC or DC currents as they transition. This parameter is guaranteed by design, but not tested.
4. TRST, TMS, and TDI have resistor pull-up to $V_{CC}$.

## Table 8. Switching Characteristics for Non-scan (Normal) Operation

$C_{LOAD}$ = 50pF, $R_{LOAD}$ = 500Ω unless otherwise noted.

| | | QS3J309 | | | |
|---|---|---|---|---|---|
| Symbol | Description | Min | Typ | Max | Unit |
| $t_{PLH}$<br>$t_{PHL}$ | Data Propagation Delay[2,3]<br>A ↔ B, Switch On | — | 0.25 | — | ns |
| $t_{PZL}$<br>$t_{PZH}$ | Switch Turn-on Delay[1]<br>BE = L → Switch On | 1.5 | — | 12 | ns |
| $t_{PLZ}$<br>$t_{PHZ}$ | Switch Turn-off Delay[1,2]<br>BE = H → Switch HIGH-Z | 1.5 | — | 12 | ns |
| $\lvert Q_{CI} \rvert$ | Charge Injection, Typical[4,5] | — | 1.5 | — | pC |

**Notes:**

1. See Test Circuit and Waveforms. Minimums guaranteed but not tested.
2. This parameter is guaranteed, but not tested.
3. The bus switch contributes no propagation delay other than the RC time constant delay of the switch resistance and the load capacitance. The propagation delay specified assumes a standard 50pF external load. Since this time constant is much smaller than the rise/fall times of typical driving signals, it adds negligible propagation circuit on the driving side of the switch and its interaction with the load on the driven side.
4. Measured at switch turn off, A to B, load = 50pF in parallel with 10Ω scope probe, $V_{IN}$ at A = 0.0V.
5. Guaranteed parameter but not production tested.

## Table 9. Switching Characteristics for Scan Mode

Industrial: $T_A$ = –40°C to 85°C, $V_{CC}$ = 5.0V ± 10%
$C_{LOAD}$ = 50pF, $R_{LOAD}$ = 500Ω unless otherwise noted.

| Symbol | Description[1] | State | Industrial Min | Industrial Max | Unit |
|---|---|---|---|---|---|
| $t_{PLH}$ $t_{PHL}$ | Data Propagation Delay TCK to TDO | | 3.5 | 13 | ns |
| $t_{PLZ}$ $t_{PHZ}$ | Disable Time[2] TCK to TDO | | 2.5 | 12 | ns |
| $t_{PZL}$ $t_{PZH}$ | Enable Time TCK to TDO | | 3 | 15 | ns |
| $t_{PLH}$ $t_{PHL}$ | Data Propagation Delay TCK to Data Out | Update-DR | 5 | 21 | ns |
| $t_{PLZ}$ $t_{PHZ}$ | Disable Delay[2] TCK to Data Out | Update-DR | 4 | 13 | ns |
| | | Update-IR | — | 22 | |
| | | Test Reset | — | 20 | |
| $t_{PZL}$ $t_{PZH}$ | Enable Delay TCK to Data Out | Update-DR | 5 | 23 | ns |
| | | Update-IR | — | 32 | |
| $t_S$ | Setup Time, TDI to TCK | | 4 | — | ns |
| $t_H$ | Hold Time, TDI to TCK | | 4.5 | — | ns |
| $t_S$ | Setup Time, TMS to TCK | | 9 | — | ns |
| $t_H$ | Hold Time, TMS to TCK | | 2 | — | ns |
| $t_S$ | Setup Time, Data to TCK | | 4 | — | ns |
| $t_H$ | Hold Time, Data to TCK | | 6 | — | ns |
| $t_W$ | Pulse Width, TCK | HIGH | 9 | — | ns |
| | | LOW | 9 | — | ns |
| $f_{MAX}$ | Maximum Frequency TCK | | 25 | — | MHz |
| $t_{PU}$ | Power-Up to TCK | | 100 | — | ns |
| $t_{PD}$ | Power-Down Time | | 100 | — | ns |

**Note:**
1. All propagation delays measured from the falling edge of TCK.
2. This parameter is guaranteed by characterization but not production tested.

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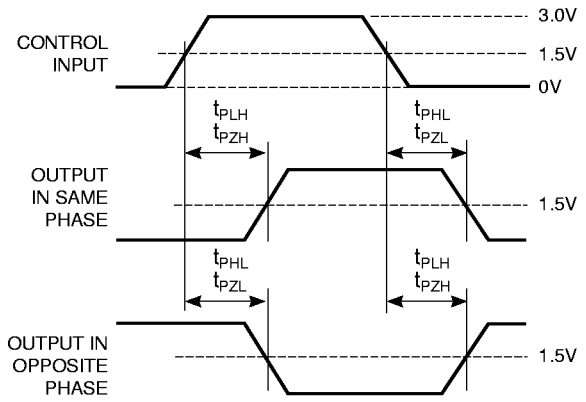
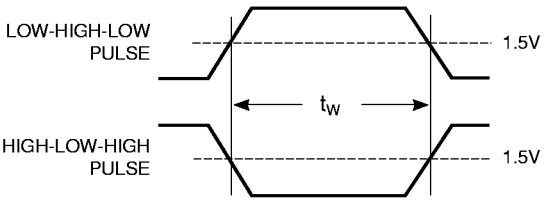
## WAVEFORMS

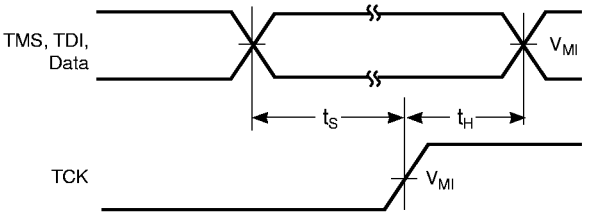
### Figure 9. Propagation Delay in Non-scan Operation



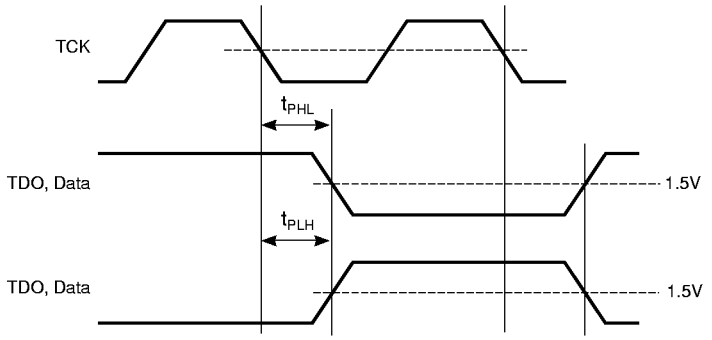

### Figure 10. Pulse Width



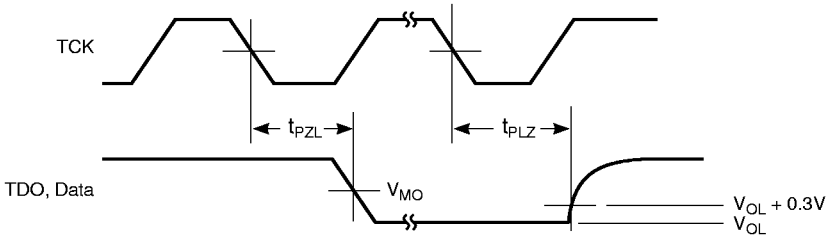

### Figure 11. Setup Time, Hold Time



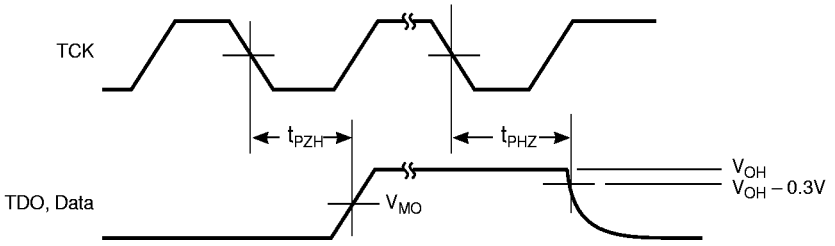

### Figure 12. Propagation Delay in Scan Test Operation




### Figure 13. Tri-state Output Low, Enable and Disable Times




### Figure 14. Tri-state Output High, Enable and Disable Times

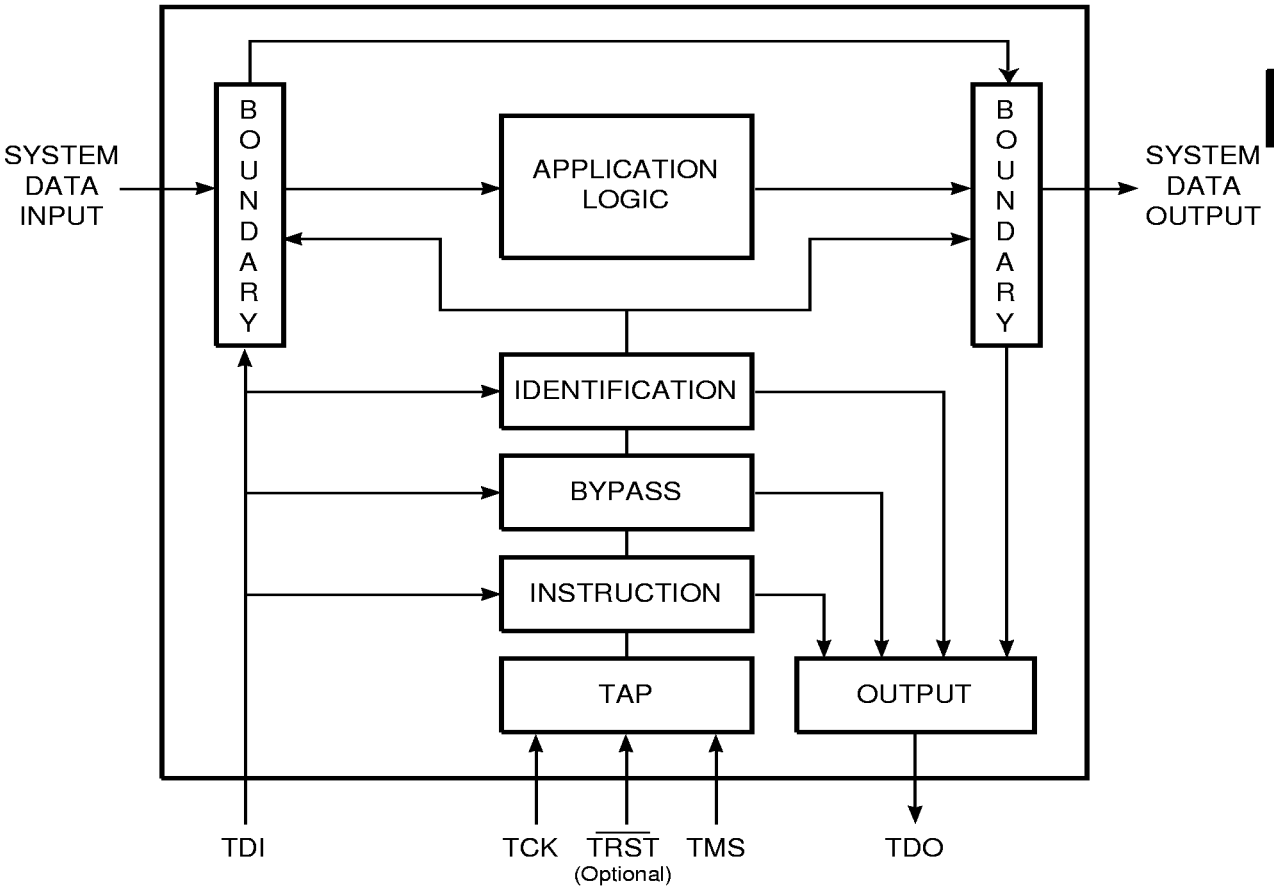


## DESCRIPTION OF BOUNDARY-SCAN ARCHITECTURE

Serial test information is conveyed by means of a test access port (TAP) that conforms to IEEE Standard 1149.1a-1993. Test instructions, data, and control signals are passed along this 4-wire serial test bus.

The test architecture consists of a test access port (TAP), serial output circuit, instruction register, bypass register, boundary-scan register, and an optional identification register. The TAP is a state machine that responds to test clock (TCK) and test mode select (TMS) inputs to shift data from the test data input (TDI) through either the instruction register or a selected data register to the test data output (TDO). The output circuit multiplexes the serial bit stream from the instruction or selected data register to TDO. The instruction register holds the current test command. The boundary-scan register refers to the IC's inputs and outputs and provides the test circuitry required for testing the internal functionality of the device as well as wiring interconnects between ICs on a board (a boundary scan cell refers to one individual IC input or output). The bypass register provides a single bit scan path through the IC when boundary-scan testing is not being performed. The optional identification register provides information about the IC (i.e., manufacturer, device type and version codes). Although there is reset capability in the TAP, a hardware reset can be performed via the optional test reset pin (TRST). Figure 10 shows the boundary-scan architecture.

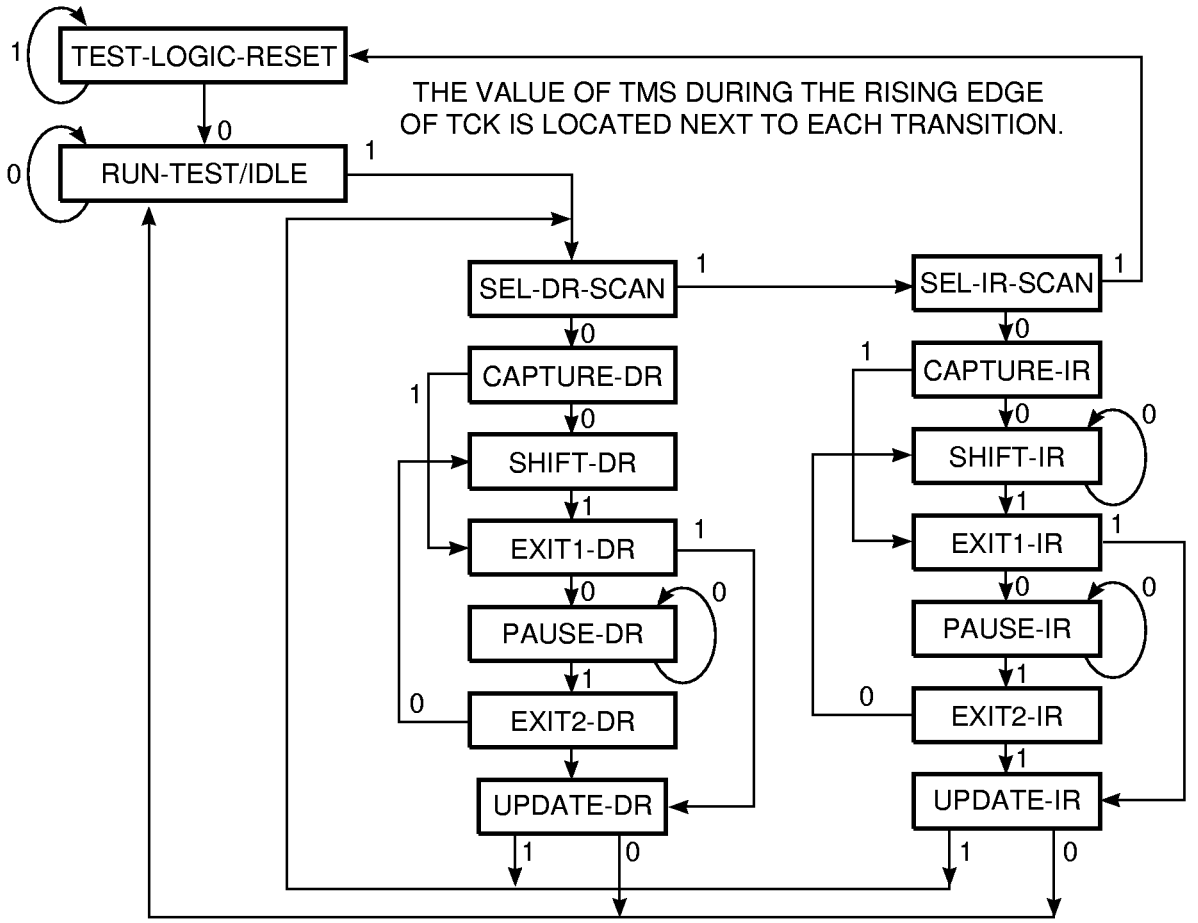
**Figure 15. Boundary-Scan Architecture**



The TAP state machine controls the boundary-scan activity via five modes of operation: Reset, Run/Test, Idle, Data scan, and Instruction scan modes. A diagram of the TAP can be shown in Figure 11. The diagram illustrates how the polarity of the TMS signal (with TCK) dictates the control and direction through the operation modes. The instruction register can be loaded during the instruction scan mode, and the data registers (i.e., I/O pins) can be loaded/retrieved during the data scan mode. A guaranteed reset can be performed by holding TMS HIGH for five clock cycles.

There are three required instructions as indicated in the boundary-scan standard. These are EXTEST, SAMPLE/PRELOAD, and BYPASS. The EXTEST instruction will drive the device external pin according to the data contained in each boundary scan cell. This instruction is commonly used to stimulate signal nets during board interconnection testing. The SAMPLE/PRELOAD instruction is used to read data from the device boundary register. This instruction is also used to load data into the boundary register prior to selection of another test instruction. The BYPASS instruction automatically selects the one bit bypass register to provide a minimum-length serial scan path. This instruction is used when a device is not being tested.

## Figure 16. TAP Controller State Diagram




The function block diagram illustrates the IEEE Standard 1149.1a-1993 4-wire test bus and boundary-scan architecture and the relationship between the test bus, test registers, and the TAP controller. The QS3J309 QuickScan device provides JTAG access to a databus, while being transparent to the system during normal (non-scan) operation. This is achieved by combining the "like-a-wire" characteristics of QSI's QuickSwitch® devices with a JTAG boundary-scan access port. This device consists of an 8-bit instruction register, a 32-bit ID register, a 1-bit bypass register, and 18 boundary-scan registers.

**TEST ACCESS PORT (TAP) DESCRIPTION**
The Test Access Port (TAP) consists of four pins dedicated solely to the operation of the test logic. The four pins include TMS (Test Mode Select), TDI (Test Data In), TDO (Test Data Out), and TCK (Test Clock). These pins are required by IEEE1149.1a.

**TCK**: **(TEST CLOCK)** This input provides the test clock for the test circuits. Data (TDI and TMS) is captured on the rising edge of TCK and outputs change on the falling edge.

**TMS: (TEST MODE SELECT)** This input controls test logic operation modes by directing the device through TAP controller states. This input has a pull-up resistor which guarantees that an undriven TMS input can put the TAP controller into the Test Logic Reset state. The requirement that an unforced TMS input produce a logic high ensures that the normal operation of the design can continue without interference from the test logic.

**TDI: (TEST DATA IN)** This input is for serial data input of instructions and data to the test logic. Test data will arrive at TDO without inversion after the appropriate number of clock cycles as determined by the length of the register currently connected between TDI and TDO. This input has a pull-up resistor to implement a logic high for an undriven input. The requirement that an unforced TDI input produce a logic high is to assist in the determination of manufacturing defects in the test scan chain interconnect. A repeating field of 1's can indicate where a break in the scan chain interconnect occurred.

**TDO: (TEST DATA OUT)** This output provides the serial data output of test instructions and data from the test logic. Changes in the logic state and drive activity for this output occur upon the falling edge of TCK. This is to avoid a race condition when TDO is connected to TDI of the next chip in the scan chain which is sampled on the rising edge. This output shall remain inactive except when the scanning of data is in progress. This is to permit the ability to multiplex scan chains on the board without causing signal contention between multiple TDO outputs connected together to form parallel scan chains.

**TRST**: **(RESET)** This pin resets the tap controller asynchronously to the clock and is not dependent upon any other signal.

BE: **(Bus Enable)** This is an overriding bus enable signal that when HIGH will disable all the switches in the non-scan mode.

## TAP STATE DESCRIPTION

The main feature of the TAP controller is a state machine which is defined by the IEEE 1149.1a JTAG specification. These states change in response to the value of TMS (upon the rising edge of TCK), or upon power-up. In any given state, actions of the test logic occur on the falling or rising edge of TCK following the rising edge of TCK which caused the TAP controller to enter the state initially.

**NOTE:** It may happen that actions to occur in one state happen on the same rising edge of TCK that causes the TAP controller to enter the next state.

**TEST LOGIC RESET**: The test logic is disabled during this state so that normal operation of the system logic may proceed uninhibited. Following entry into the Test Logic Reset state, the IDCODE instruction is latched onto the instruction register output on the falling edge of TCK.

Two features of the state diagram are realized in this state. First it can be noted that independent of what state the TAP controller is currently in, the QS3J309 will enter the Test Logic Reset state after, at most, five cycles of TCK with the TMS input high. Secondly, if a temporary glitch should occur on the TMS input during a rising edge of TCK, the TAP Controller will enter the Run-Test/Idle state then return to the Test Logic Reset state via the Select-DR state and Select-IR state provided that TMS returns to its logic high value for rising edge clocks following the glitch. The QS3J309 TAP controller will also be forced into the Test Logic Reset state upon power-up.

**RUN-TEST/IDLE**: The TAP controller must pass through the Run-Test/Idle state before executing any test operations. Once entered, the controller will remain in this state as long as TMS is held low. When TMS is high and a rising edge is applied at TCK, the controller moves to the Select-DR-Scan state. The instruction does not change while the TAP controller is in this state.

**SELECT-DR SCAN**: This is a temporary state in which all test data registers retain their previous values.

**CAPTURE-DR**: In this controller state, data may be parallel loaded into the data register selected by the current instruction; otherwise, it retains its previous values.

**SHIFT-DR**: In this state the test data register selected between TDI and TDO by the current instruction will shift one stage at each rising edge of TCK. TDO is active during this state. Test data registers not selected by the current instruction maintain their previous values.

**PAUSE-DR**: This is a temporary state in which all data registers retain their previous values. This state is intended to temporarily halt the shifting of test data into the data register selected while retaining the ability to keep TCK running; TCK may be a free-running clock.

**EXIT1-DR**: This is a temporary state in which all test data registers retain their previous values.

**EXIT2-DR**: This is a temporary state in which all test data registers retain their previous values.

**UPDATE-DR**: The parallel output register of the selected test data register may be updated on the falling edge of TCK in this state, provided the test data register has such a parallel output register. The intent of the parallel output register is to provide the ability to apply the contents of the test data.

**SELECT-IR SCAN**: This is a temporary state in which the instruction register retains its previous value.

**CAPTURE-IR**: In this controller state data may be parallel loaded into the instruction register. The only restriction on what data may be is that its least significant bit must be a logic high, or 1, and its second least significant bit must be a logic low, or 0. These opposite state bits can be used to check the correct operation of the scan chain on the board by forcing a bit toggle when the instructions are shifted.

**SHIFT-IR**: In this state the instruction register selected between TDI and TDO will shift one stage at each rising edge of TCK. TDO is active during this state.

**EXIT1-IR**: This is a temporary state in which the instruction registers retains its previous values.

**PAUSE-IR**: This is a temporary state in which the instruction register retains its previous value. This state is intended to temporarily halt the shifting of test data into the instruction register while retaining the ability to keep TCK running.

**EXIT2-IR**: This is a temporary state in which the instruction register retains its previous value.

**UPDATE-IR**: The current instruction is updated on the falling edge of TCK following entry into the Update-IR state.

## FEATURES OF THE TAP CONTROLLER

The TAP controller will not be initialized by the operation of any system pin such as a system reset. The TAP controller will be initialized into the Test Logic Reset state upon power-up or by grounding the TRST pin. This requirement is intended to avoid bus signal contention upon power-up by disabling the test logic which allows the system logic to operate normally and hence be controlled to avoid any contention. (The TAP controller will return to the Test Logic Reset state after, at most, five clock cycles of TCK with TMS high; but the time required to enact that operation may not be sufficient to avoid contention).

Note that the TAP controller has been defined such that six of the sixteen states have the ability to maintain their state provided that TMS remains at the same value it had when entering the state: **Test Logic Reset** to hold off the test logic during normal system operation, **Run Test/Idle** to undertake multi-cycle self tests, **Shift-DR** and **Shift-IR** to maintain the data shifting process for an extended period, and the **Pause-DR** and **Pause-IR** to halt the shifting process while some other activity is performed such as retrieving test data from additional memory. This feature is available in any/all states where multiple clock cycles may be required to achieve the desired outcome or where activity is to be halted but still provide the ability to make TCK a free-running clock.

## REGISTER OVERVIEW

With the exception of the Bypass register, any test register may be thought of as a serial shift register with a parallel latch on each bit. The bypass register only contains a single bit shift register. As detailed above, there are three main instructions for controlling these registers:

**Capture:** causes the shift register to be parallel loaded from a specific source.

**Shift:** causes shift register contents to shift from TDI to TDO.

**Update:** causes shift register data to latch into the parallel register on the falling edge of TCK.

## INSTRUCTION REGISTER

The ***Instruction*** register permits 8-bit instructions to be serially loaded which select a particular test data register and/or a specific test function. Each instruction will identify a particular test data register to be connected between TDI and TDO when in the Shift-DR state along with defining any particular test actions to occur to that test data register and/or any others. The order of scan through the instruction register must be least-to-most; that is, the least significant bit is closest to TDO for a loaded instruction. During the Shift-IR state the instruction shifts one bit between TDI and TDO upon each rising edge of TCK and appears without inversion at TDO.

During Capture-IR, the ***Instruction*** registers two LSB's are set to "01". The bit value "01" in the least significant locations can be used to check the connectivity of the scan chain by forcing a bit toggle at each instruction during a scan of the instruction registers. The technique not only assists in determining the correct connectivity of the scan chain about the board, but also assists in pinpointing the location of any break in the scan chain. During Update-IR, the value data that has been shifted into the ***Instruction*** register is loaded into the parallel latches. At this time, the current instruction is updated and relevant mode changes are initiated.

## INSTRUCTION DEFINITIONS

The instructions required by IEEE1149.1a include the BYPASS, EXTEST and SAMPLE/PRELOAD instructions. The additional IDCODE, CLAMP, HIGH-Z, and BOUNDARY READ has also been incorporated into this QuickScan device. In the following descriptions, each instruction will identify the test data register to be connected between TDI and TDO during the Shift-DR state, any restrictions on the binary codes used to implement the instruction, and what test data registers are used in undertaking the actions of the instruction.

**1. EXTEST**. This instruction allows circuitry external to the component package, typically the board interconnect, to be tested. ***Boundary Scan*** register cells at the QuickSwitch I/O pins are used to apply test and capture stimuli. When this instruction is selected, the states of all signals on the system input pins will be loaded into the ***Boundary Scan*** register upon the rising edge of TCK in the Capture-DR state and the contents of the ***Boundary Scan*** register will solely define the state of the system outputs upon the falling edge of TCK in the Update-DR state. The 00000000 instruction binary code invokes the EXTEST instruction. During this instruction the ***Boundary Scan*** register is connected between TDI and TDO in the Shift-DR state. Additional binary codes for this instruction are permitted. The EXTEST instruction shall select only the boundary-scan register to be connected for serial access between TDI and TDO in the Shift-DR controller state (i.e., no other test data register may be connected in series with the boundary-scan register).

**2. SAMPLE/PRELOAD**. This instruction allows a "snapshot" of the normal operation of the component to be taken and examined. It also allows data values to be loaded onto the latched parallel outputs of the ***Boundary Scan*** shift register prior to selection of another boundary scan test instruction. During this instruction the ***Boundary Scan*** register is connected between TDI and TDO in the Shift-DR state. When this instruction is selected, the states of all signals on the system pins will be loaded into the ***Boundary Scan*** register upon the rising edge of TCK in the Capture-DR state and the contents of the ***Boundary Scan*** register will be loaded into the parallel output register included with the ***Boundary Scan*** register bits upon the falling edge of TCK in the Update-DR state.

Note that by interfacing these two actions through the Exit1-DR state, the current state of the system pins can be captured into the ***Boundary Scan*** register and stored into its parallel output registers for later application back onto those same pins.

When the SAMPLE/PRELOAD instruction is selected, the test logic shall have no impact upon the system logic in performing its system function. The binary code may be device specific.

**3. BYPASS**. This instruction allows rapid movement of test data to and from other components on a board that are required to perform test operations by selecting the ***Bypass*** register, a single-bit shift-register stage, between TDI and TDO in the Shift-DR state to provide a minimum-length serial scan path. The "all others" opcode, along with the requirement that an undriven TDI input produce a logic high value, loads the BYPASS instruction if the scan chain is broken. In such a case all instructions following the break in the scan chain will be loaded with the BYPASS instruction and hence have no impact upon the system's normal functional operation. During Capture-DR, the bypass register captures a logic 0.

**4. IDCODE.** The IDCODE instruction instructs the device to output an internal ID code from the device ***Identification*** register. This code is locked into the device ***Identification*** register on the rising edge of TCK following entry into the capture-DR state. The device ***Identification*** register contains an encoded part number, as well as Quality Semiconductor's manufacturer identity as defined by JEDEC. The full ID code for the QS3J309 is listed below. Note that the LSB is fixed at "1". This allows differentiation from the ***Bypass*** register output that would begin with logic 0.

Each of the defined instructions in Table 9 fully indicate which data registers may operate or interact with the system logic while the instruction is current. Test data registers that are not selected by the current instruction do not interfere with the system logic or the operation of the test data registers currently selected.

**5. HIGH-Z.** This instruction places all I/O cells (A8-A0 and B8-B0) in a high-impedance state and selects the bypass register to be connected for serial access between TDI and TDO in the ***Shift-DR*** state. When leaving the HIGH-Z instruction and selecting the EXTEST instruction for example , the data held in the boundary scan register prior to the selection of the HIGH-Z instruction will be applied to the device output pins.

**6. CLAMP.** This instruction allows the state of the signals driven from the component pins to be determined from the boundary scan register while the bypass register is selected as the serial path between TDI and TDO. The signals driven from the device pins will not change while the CLAMP instruction is selected.

**7. BOUNDARY READ.** The boundary scan register is selected in the scan path. The value in the boundary scan register remains unchanged during Capture-DR. When a boundary read instruction is input to the device, the contents of the boundary register can be shifted out. This instruction differs from the EXTEST or SAMPLE instruction in that the capture operation that normally occurs in the TAP Capture-DR state is replaced with a data register hold operation.

## BOUNDARY-SCAN REGISTER

The ***Boundary Scan*** register permits testing of printed circuit board interconnects such as opens and shorts while also providing access to the components inputs and outputs when testing or monitoring its system logic. In the QS3J309, the ***Boundary Scan*** register is 18 bits long, with one boundary scan cell for each QuickSwitch I/O. The Boundary-Scan cells facilitate both observation and control of the QuickSwitch gate I/Os'.

***Each boundary scan cell can be configured to be an input, output or tri-state depending on the input data at TDI.***

### Table 10. IDCODE Instructions

| Version (bits 31-28) | Part Number (27-12) | QSI I.D. (11-1) | LSB(0) |
|---|---|---|---|
| 0000 | 1011111010101101 ($BEAD_H$) | 00011101001 (E9h) | 1 |

Data applied to the TDI input appears without inversion at TDO during the Shift-DR state following 55 TCK cycles. In the Capture-DR state, data will be parallel loaded into the ***Boundary Scan*** register upon the rising edge of TCK. Contents of the ***Boundary Scan*** register will be latched into its shadow register upon the falling edge of TCK in the Update-DR state provided that it is selected by the current instruction.

## BYPASS REGISTER

The ***Bypass*** register provides a minimum length serial path for the movement of test data between TDI and TDO. Use of this register speeds access to test data registers in other components on the board-level test data path. The ***Bypass*** register consists of a single shift register.

The ***Bypass*** register must set to a logic low value upon the rising edge of TCK in the Shift-DR state provided that it is selected by the current instruction. Upon an initial scan of the data registers connected across the board, all devices will connect the device ***Identification*** register while in the Shift-DR state. This condition is a result of power-up (or assertion of optional instruction) to initialize each JTAG device on board. The first logic high will be the framing bit of a device ***Identification*** register which would then indicate that the following 31 bits are identifiers to the specific device at that location of the scan chain.

## TIMING DESCRIPTION

All the operations of the QS3J309 device are synchronous to TCK. The TAP controller changes state only in response to the rising edge of TCK or a transition to logic 0 at the TRST input or power-up. All state transitions of the TAP controller (as shown in Figure 16) occur based on the value of TMS on the rising edge of TCK. Data on the TDI, TMS, and normal function inputs is captured on the falling edge of TCK. Data appears on the TDO and normal function output pins on the falling edge of TCK.

A simple timing example in the Bypass mode is shown in Figure 17. The TAP controller starts in the Test-Logic-Reset state and is advanced through its states as necessary to perform one IR-Scan and one DR-Scan. In the Shift-IR and Shift-DR states, TDI is used to input serial data, and TDO is used to output serial data. Table 11 describes the operation of the device during each TCK cycle.

Another simple timing example in the Scan mode is shown in Figure 18. It is very similar to the previous example, except the data is available on the TDO after 55 cycles. Table 12 describes the operation of the device during each TCK cycle.

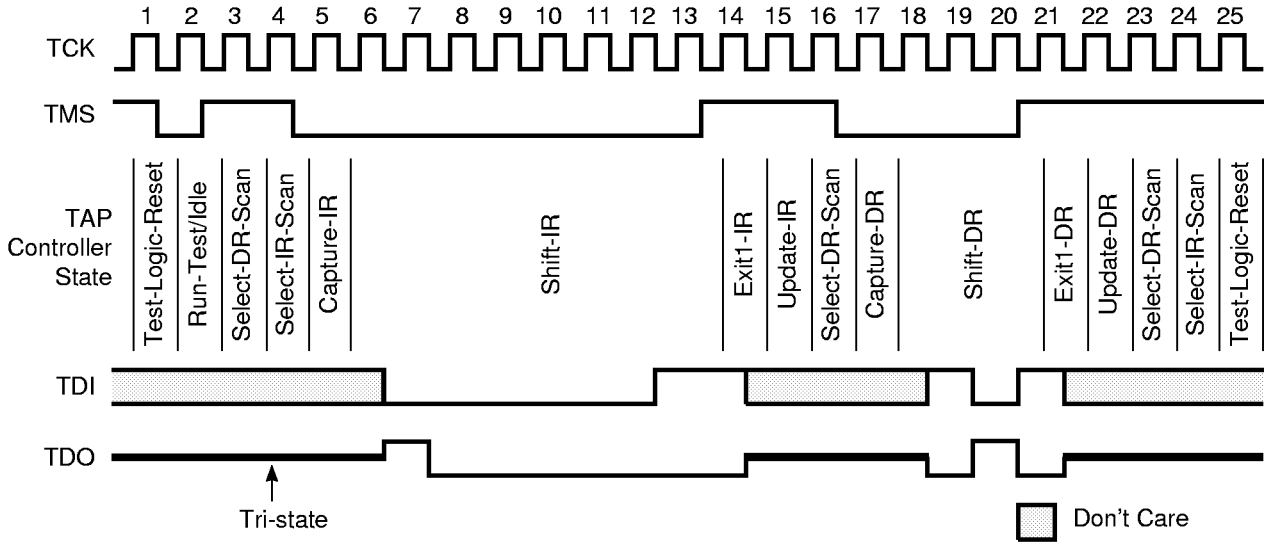
**Table 11. Explanation of Timing Example in Bypass Mode.** (See Figure 17)

| TCK Cycle(s) | TAP State After TCK | Description |
|---|---|---|
| 1 | Test-Logic-Reset | TMS is changed to a logic 0 value on the falling edge of TCK to begin advancing the TAP controller toward the desired state. |
| 2 | Run-Test/Idle | |
| 3 | Select-DR-Scan | |
| 4 | Select-IR-Scan | |
| 5 | Capture-IR | The IR captures the 8-bit binary value 00000001 on the rising edge of TCK as the TAP controller exits the Capture-IR state. |
| 6 | Shift-IR | TDO becomes active and TDI is made valid on the falling edge of TCK. The first bit is shifted into the TAP on the rising edge of TCK as the TAP controller advances to the next state. |
| 7–13 | Shift-IR | One bit is shifted into the IR on each TCK rising edge. With TDI held at logic 1 value, the 8-bit binary value 00000011 is serially scanned into the IR. At the same time, the 8-bit binary value 00000001 is serially scanned out of the IR via TDO. In TCK cycle 13, TMS is changed to a logic 1 value to end the IR scan on the next TCK cycle. The last bit of the instruction is shifted as the TAP controller advances from the Shift-IR to Exit1-IR. |
| 14 | Exit1-IR | TDO becomes inactive (goes to the high-impedance state) on the falling edge of TCK. |
| 15 | Update-IR | The IR is updated with the new instruction (Bypass) on the falling edge of TCK. |
| 16 | Select-DR-Scan | |
| 17 | Capture-DR | The Bypass register captures a logic 0 value on the rising edge of TCK as the TAP controller exits the Capture-DR state. |
| 18 | Shift-DR | TDO becomes active and TDI is made valid on the falling edge of TCK. The first bit is shifted into the TAP on the rising edge of TCK as the TAP controller advances to the next state. |
| 19–20 | Shift-DR | The binary value 101 is shifted in via TDI, while the binary value 010 is shifted out via TDO. |
| 21 | Exit1-DR | TDO becomes inactive (goes to the high-impedance state) on the falling edge of TCK. |
| 22 | Update-DR | In general, the selected data register is updated with the new data on the falling edge of TCK. |
| 23 | Select-DR-Scan | |
| 24 | Select-IR-Scan | |
| 25 | Test-Logic-Reset | Test operation completed. |

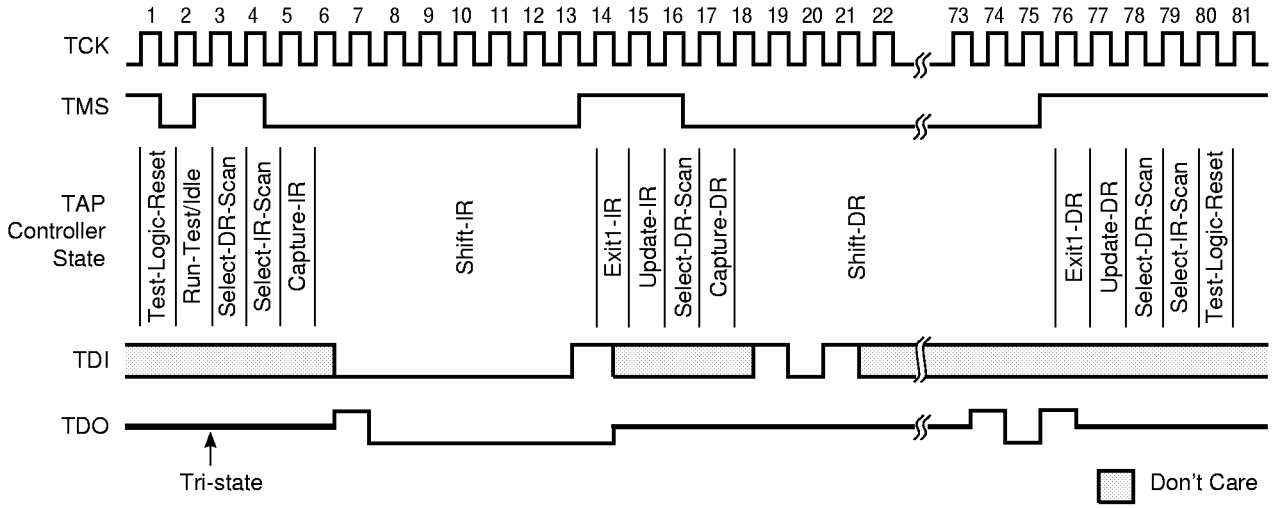
**Table 12. Explanation of Timing Example in Scan Mode.** (See Figure 18)

| TCK Cycle(s) | TAP State After TCK | Description |
|---|---|---|
| 1 | Test-Logic-Reset | TMS is changed to a logic 0 value on the falling edge of TCK to begin advancing the TAP controller toward the desired state. |
| 2 | Run-Test/Idle | |
| 3 | Select-DR-Scan | |
| 4 | Select-IR-Scan | |
| 5 | Capture-IR | The IR captures the 8-bit binary value 00000001 on the rising edge of TCK as the TAP controller exits the Capture-IR state. |
| 6 | Shift-IR | TDO becomes active and TDI is made valid on the falling edge of TCK. The first bit is shifted into the TAP on the rising edge of TCK as the TAP controller advances to the next state. |
| 7–13 | Shift-IR | One bit is shifted into the IR on each TCK rising edge. With TDI held at logic 1 value, the 8-bit binary value 00000001 is serially scanned into the IR. At the same time, the 8-bit binary value 00000001 is serially scanned out of the IR via TDO. In TCK cycle 13, TMS is changed to a logic 1 value to end the IR scan on the next TCK cycle. The last bit of the instruction is shifted as the TAP controller advances from the Shift-IR to Exit1-IR. |
| 14 | Exit1-IR | TDO becomes inactive (goes to the high-impedance state) on the falling edge of TCK. |
| 15 | Update-IR | The IR is updated with the new instruction (Sample/Preload) on the falling edge of TCK. |
| 16 | Select-DR-Scan | |
| 17 | Capture-DR | The Scan register captures TDI on the rising edge of TCK as the TAP controller exits the Capture-DR state. |
| 18 | Shift-DR | TDO becomes active and TDI is made valid on the falling edge of TCK. The first bit is shifted into the TAP on the rising edge of TCK as the TAP controller advances to the next state. |
| 19–72 | Shift-DR | The binary value 101 is shifted in via TDI and is available to TDO after 55 TCK cycles. |
| 73-75 | Shift-DR | TDO has the valid data 101. |
| 76 | Exit1-DR | TDO becomes inactive (goes to the high-impedance state) on the falling edge of TCK. |
| 77 | Update-DR | In general, the selected data register is updated with the new data on the falling edge of TCK. |
| 78 | Select-DR-Scan | |
| 79 | Select-IR-Scan | |
| 80 | Test-Logic-Reset | Test operation completed. |

## Figure 17. Timing Example in Bypass Mode

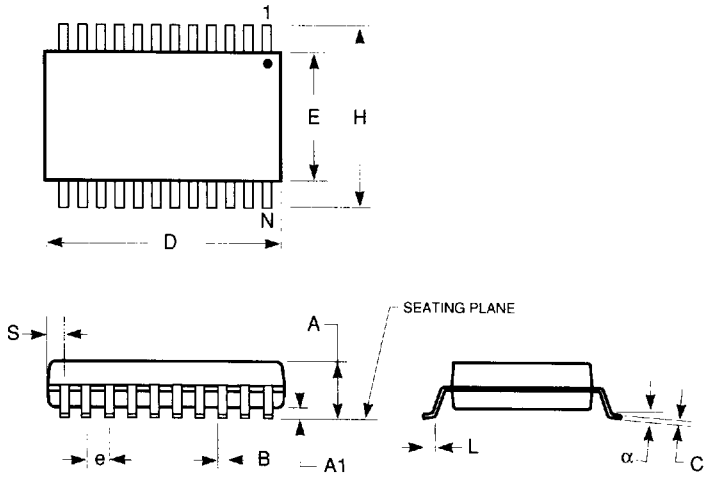



## Figure 18. Timing Example in Scan Mode



# 150-MIL HQSOP - Package Code H

**Hermetic Quarter-Size Outline Package**
**Ceramic Small Outline Gull-Wing**




| JEDEC# | TBD | | | TBD | | |
|---|---|---|---|---|---|---|
| DWG# | HSS-20A | | | HSS-24A | | |
| Symbol | Min | Nom | Max | Min | Nom | Max |
| A | 0.070 | 0.074 | 0.078 | 0.070 | 0.074 | 0.078 |
| A1 | 0.008 | 0.012 | 0.016 | 0.008 | 0.012 | 0.016 |
| B | 0.009 | 0.010 | 0.012 | 0.009 | 0.010 | 0.012 |
| C | 0.007 | 0.008 | 0.010 | 0.007 | 0.008 | 0.010 |
| D | 0.337 | 0.342 | 0.350 | 0.337 | 0.342 | 0.350 |
| E | 0.150 | 0.155 | 0.158 | 0.150 | 0.155 | 0.158 |
| e | 0.025 BSC | | | 0.025 BSC | | |
| H | 0.230 | 0.236 | 0.244 | 0.230 | 0.236 | 0.244 |
| L | 0.016 | 0.025 | 0.035 | 0.016 | 0.025 | 0.035 |
| N | 20 | | | 24 | | |
| α | 0° | 5° | 8° | 0° | 5° | 8° |
| S | 0.056 | 0.058 | 0.062 | 0.031 | 0.033 | 0.037 |

**Notes:**
1. Refer to applicable symbol list.
2. All dimensions are in inches.
3. N is the number of lead positions.
4. Dimensions D and E are to be measured at maximum material condition.
5. Lead coplanarity is 0.004in. maximum.