

FEATURES/BENEFITS

- Enhanced N channel FET with no inherent diode to V_{CC}
- 2.5Ω bidirectional switches connect inputs to outputs
- Zero propagation delay, zero ground bounce
- Undershoot clamp diodes on all switch and control pins
- Two enables control five bits each
- Available in 24-pin SOIC and QSOP

APPLICATIONS

- Hot-swapping and hot-docking (Application Note AN-13)
 - Low resistance for PCI and Compact PCI applications
- Voltage translation (5V to 3.3V; Application Note AN-11)
- Power conservation
- Capacitance reduction and isolation
- Bus isolation
- Clock gating

DESCRIPTION

The QS3R384 provides a set of ten high-speed CMOS TTL-compatible bus switches. Two banks of 5 switches are controlled by independent Bus Enable (\overline{BE}) signals. The very low R_{ON} resistance (2.5Ω) of the QS3R384 allows inputs to be connected without adding propagation delay and without generating additional ground bounce noise.

The low ON resistance of QS3R384 makes it ideal for PCI hot-plugging or hot-swapping applications.

Figure 1. Functional Block Diagram

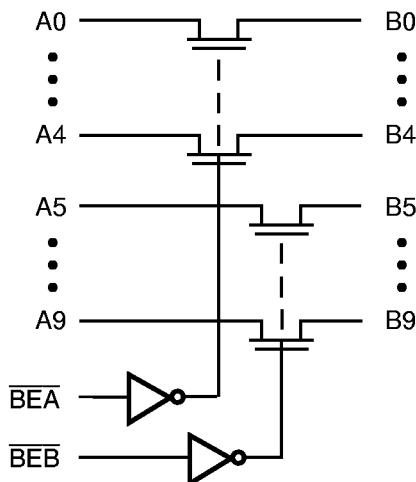


Table 1. Pin Description

Name	I/O	Function
A0-A9	I/O	Bus A
B0-B9	I/O	Bus B
$\overline{\text{BEA}}$, $\overline{\text{BEB}}$	I	Bus Switch Enable

Figure 2. Pin Configuration
(All Pins Top View)

SOIC, QSOP

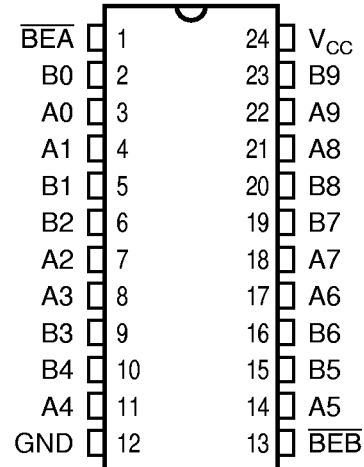


Table 2. Function Table

$\overline{\text{BEA}}$	$\overline{\text{BEB}}$	B0-B4	B5-B9	Function
H	H	Hi-Z	Hi-Z	Disconnect
L	H	A0-A4	Hi-Z	Connect
H	L	Hi-Z	A5-A9	Connect
L	L	A0-A4	A5-A9	Connect

Table 3. Absolute Maximum Ratings

Supply Voltage to Ground	-0.5V to 7.0V
DC Switch Voltage V_S	-0.5V to 7.0V
DC Input Voltage V_{IN}	-0.5V to 7.0V
AC Input Voltage (for a pulse width $\leq 20\text{ns}$)	-3.0V
DC Output Current Max. Sink Current/Pin	120mA
Maximum Power Dissipation	0.5 watts
T_{STG} Storage Temperature	-65° to 150°C

Note: ABSOLUTE MAXIMUM CONTINUOUS RATINGS are those values beyond which damage to the device may occur. Exposure to these conditions or conditions beyond those indicated may adversely affect device reliability. Functional operation under absolute-maximum conditions is not implied.

Table 4. Capacitance

$T_A = 25^\circ\text{C}$, $f = 1\text{MHz}$, $V_{IN} = 0\text{V}$, $V_{OUT} = 0\text{V}$

Pins	SOIC, QSOP		Unit
	Typ	Max	
Control Inputs	3	4	pF
QuickSwitch Channels (Switch OFF)	5	6	pF

Note: Capacitance is guaranteed but not production tested. For total capacitance while the switch is ON, please see Section 1 under "Input and Switch Capacitance."

Table 5. DC Electrical Characteristics Over Operating Range

Commercial: $T_A = -40^{\circ}\text{C}$ to 85°C , $V_{CC} = 5.0\text{V} \pm 10\%$

Symbol	Parameter	Test Conditions	Min	Typ ⁽¹⁾	Max	Unit
V_{IH}	Input HIGH Voltage	Guaranteed Logic HIGH for Control Inputs	2.0	—	—	V
V_{IL}	Input LOW Voltage	Guaranteed Logic LOW for Control Inputs	—	—	0.8	V
$ I_{IN} $	Input Leakage Current (Control Inputs)	$0 \leq V_{IN} \leq V_{CC}$	—	0.01	1	μA
$ I_{OZ} $	Off-State Current (Hi-Z)	$0 \leq V_{OUT} \leq V_{CC}$, Switches OFF	—	0.01	1	μA
R_{ON}	Switch ON Resistance ⁽²⁾	$V_{CC} = \text{Min.}$, $V_{IN} = 0.0\text{V}$, $I_{ON} = 30\text{mA}$	—	2.5	4	Ω
R_{ON}	Switch ON Resistance ⁽²⁾	$V_{CC} = \text{Min.}$, $V_{IN} = 2.4\text{V}$, $I_{ON} = 15\text{mA}$	—	4	5.5	Ω
V_P	Pass Voltage ⁽³⁾	$V_{IN} = V_{CC} = 5\text{V}$, $I_{OUT} = -5\mu\text{A}$	3.7	4	4.3	V

Notes:

1. Typical values indicate $V_{CC} = 5.0\text{V}$ and $T_A = 25^{\circ}\text{C}$.
2. For a diagram explaining the procedure for R_{ON} measurement, please see Section 1 under "DC Electrical Characteristics." Max. value of R_{ON} guaranteed, but not production tested.
3. Pass Voltage is guaranteed but not production tested.

Figure 3. Typical ON Resistance vs V_{IN} at $V_{CC} = 5.0\text{V}$

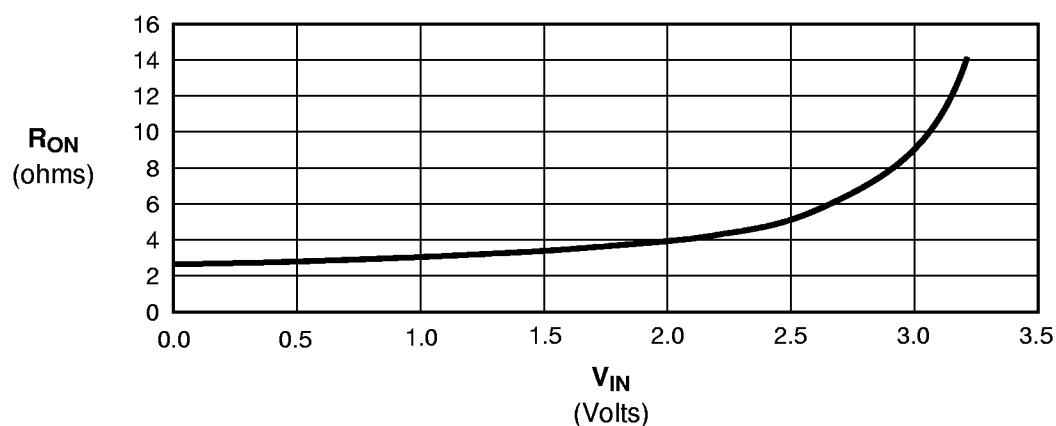


Table 6. Power Supply Characteristics Over Operating Range

Commercial: $T_A = -40^{\circ}\text{C}$ to 85°C , $V_{CC} = 5.0\text{V} \pm 10\%$

Symbol	Parameter	Test Conditions ⁽¹⁾	Max	Unit
I_{CCQ}	Quiescent Power Supply Current	$V_{CC} = \text{Max.}$, $V_{IN} = \text{GND}$ or V_{CC} , $f = 0$	1.5	mA
ΔI_{CC}	Power Supply Current per Input HIGH ⁽²⁾	$V_{CC} = \text{Max.}$, $V_{IN} = 3.4\text{V}$, $f = 0$	2.5	mA
Q_{CCD}	Dynamic Power Supply Current per MHz ⁽³⁾	$V_{CC} = \text{Max.}$, A and B Pins Open, Control Inputs Toggling @ 50% Duty Cycle	0.25	mA/MHz

Notes:

1. For conditions shown as Min. or Max., use the appropriate values specified under DC specifications.
2. Per TTL driven input ($V_{IN} = 3.4\text{V}$, control inputs only). A and B pins do not contribute to ΔI_{CC} .
3. This current applies to the control inputs only and represents the current required to switch internal capacitance at the specified frequency. The A and B inputs generate no significant AC or DC currents as they transition. This parameter is guaranteed by characterization, but not production tested.

Table 7. Switching Characteristics Over Operating Range

Commercial: $T_A = -40^{\circ}\text{C}$ to 85°C , $V_{CC} = 5.0\text{V} \pm 5\%$

$C_{LOAD} = 50\text{pF}$, $R_{LOAD} = 500\Omega$ unless otherwise noted.

Symbol	Description ⁽¹⁾	Min	Typ	Max	Unit
t_{PLH} t_{PHL}	Data Propagation Delay ^(2,4) Ai to Bi, Bi to Ai	—	—	0.12 ⁽³⁾	ns
t_{PZL} t_{PZH}	Switch Turn-on Delay \overline{BEA} , \overline{BEB} to Ai, Bi	1.5	—	6.0	ns
t_{PLZ} t_{PHZ}	Switch Turn-off Delay ⁽²⁾ \overline{BEA} , \overline{BEB} to Ai, Bi	1.5	—	4.0	ns

Notes:

1. See Test Circuit and Waveforms. Minimums guaranteed but not production tested.
2. This parameter is guaranteed by but not production tested.
3. The time constant for the switch alone is of the order of 0.12ns for QS3R384 for $C_L = 50\text{pF}$.
4. The bus switch contributes no propagation delay other than the RC delay of the ON resistance of the switch and the load capacitance. Since this time constant is much smaller than the rise/fall times of typical driving signals, it adds very little propagation delay to the system. Propagation delay of the bus switch when used in a system is determined by the driving circuit on the driving side of the switch and its interaction with the load on the driven side.