

FEATURES/BENEFITS

- 10 output, low skew clock signal buffer
- Guaranteed low skew
- 25Ω on-chip resistors available for low noise
 - 0.3ns same bank
 - 0.5ns opposite transition
 - 1.0ns different devices
- Reduced swing TTL outputs for low noise
- Input hysteresis for better noise margin
- Monitor output
- Undershoot clamp diodes on all inputs
- Military product compliant to MIL-STD-883
- Available in QSOP (Q) and SOIC (SO)

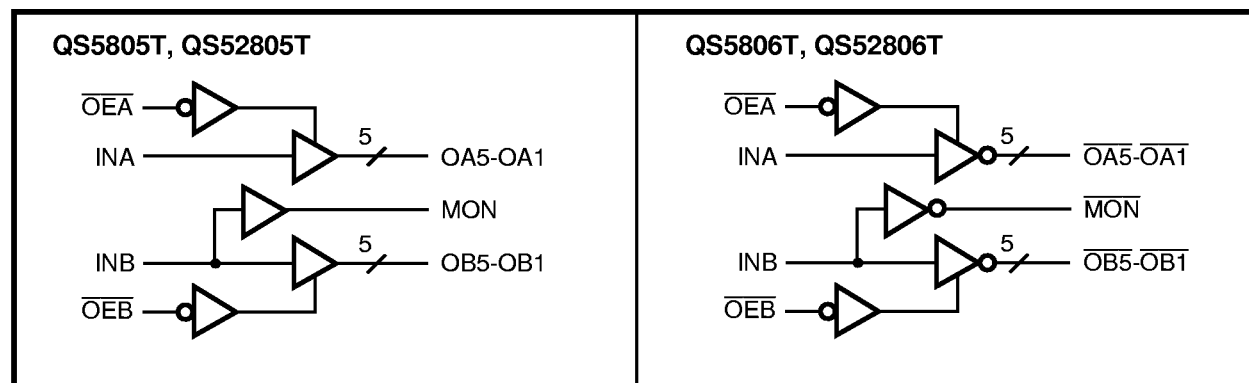
DESCRIPTION

The QS5805T and QS5806T clock driver/buffer circuits can be used for clock buffering schemes where low skew is a key parameter. The QS5805T offers two banks of five non-inverting outputs and the QS5806T provides inverting outputs. Designed in QSI's proprietary QCMOS process, these devices provide low propagation delay buffering with on-chip skew of 0.3ns for same-transition, same-bank signals.

The QS52805T and QS52806T have on-chip series termination resistors for lower noise clock signals. The QS52805T and QS52806T series resistor versions are recommended for driving unterminated lines with capacitive loading and other noise sensitive clock distribution circuits. These clock buffer products are designed for use in high-performance workstations, embedded and personal computing systems. Several devices can be used in parallel or scattered throughout a system for guaranteed low skew, system-wide clock distribution networks.

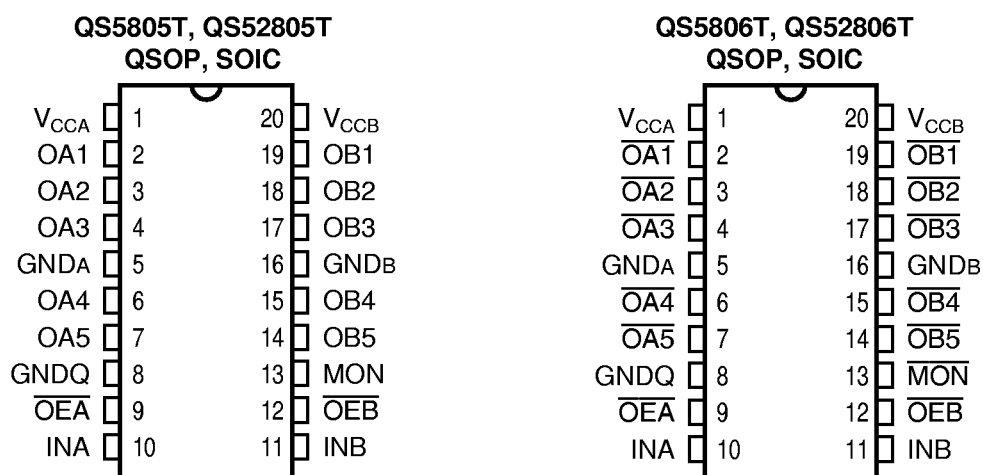
See Application Note AN-21A for more information on low-skew clock buffers.

Figure 1. Functional Block Diagram



Note: QS52805T and QS52806T devices have 25Ω series termination resistors on each clock output including monitor.

Figure 2. Pin Configurations (All Pins Top View)



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Table 1. Pin Descriptions

Name	I/O	Description
$\overline{OE}A, \overline{OE}B$	I	Output Enable Inputs
INA, INB	I	Clock Inputs
OA _n , OB _n , $\overline{OA}n, \overline{OB}n$	O	Clock Outputs
MON, $\overline{MON}$	O	Unbuffered Monitor Output

Table 2. Absolute Maximum Ratings

Supply Voltage to Ground	-0.5V to +7.0V
DC Output Voltage V _{OUT}	-0.5V to +7.0V
DC Input Voltage V _{IN}	-0.5V to +7.0V
AC Input Voltage (for a pulse width ≤ 20ns)	-3.0V
DC Input Diode Current with V _{IN} < 0	-20mA
DC Output Current Max. Sink Current/Pin	120mA
Maximum Power Dissipation	1.0 watts
T _{STG} Storage Temperature	-65° to +150°C

Note: Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to QSI devices that result in functional or reliability type failures.

Table 3. Capacitance

T_A = 25°C, f = 1MHz, V_{IN} = 0V, V_{OUT} = 0V

Pins	QSOP		SOIC		Unit
	Typ	Max	Typ	Max	
C _{IN}	4	6	4	6	pF
C _{OUT}	7	9	7	9	pF

Note: Capacitance is characterized but not tested.

Table 4. DC Electrical Characteristics Over Operating Range

Industrial: $T_A = -40^{\circ}\text{C}$ to 85°C , $V_{CC} = 5.0\text{V} \pm 10\%$

Military: $T_A = -55^{\circ}\text{C}$ to 125°C , $V_{CC} = 5.0\text{V} \pm 10\%$

Symbol	Parameter	Test Conditions	Min	Typ ⁽¹⁾	Max	Unit
V_{IH}	Input HIGH Voltage	Guaranteed Logic HIGH for All Inputs	2.0	—	—	V
V_{IL}	Input LOW Voltage	Guaranteed Logic LOW for All Inputs	—	—	0.8	V
V_{IC}	Clamp Diode Voltage ⁽³⁾	$V_{CC} = \text{Min.}$, $I_{IN} = -18\text{mA}$	—	-0.7	-1.2	V
V_{OH}	Output HIGH Voltage QS5805T/5806T	$V_{CC} = \text{Min.}$, $I_{OH} = -24\text{mA}$ (IND)	2.4	—	—	V
		$I_{OH} = -32\text{mA}$ (IND)	2.0	—	—	
		$I_{OH} = -12\text{mA}$ (MIL)	2.4	—	—	
V_{OH}	Output HIGH Voltage QS52805T/52806T	$V_{CC} = \text{Min.}$, $I_{OH} = -12\text{mA}$ (IND)	2.4	—	—	V
		$I_{OH} = -4\text{mA}$ (MIL)	2.4	—	—	
V_{OL}	Output LOW Voltage QS5805/5806T	$V_{CC} = \text{Min.}$, $I_{OL} = 64\text{mA}$ (IND)	—	—	0.55	V
		$I_{OL} = 48\text{mA}$ (MIL)	—	—	0.55	
V_{OL}	Output LOW Voltage QS52805/52806T	$V_{CC} = \text{Min.}$, $I_{OL} = 12\text{mA}$ (IND)	—	—	0.50	V
		$I_{OL} = 8\text{mA}$ (MIL)	—	—	0.50	
$ I_{IN} $	Input Leakage Current	$V_{CC} = \text{Max.}$, $V_{IN} = V_{CC}$, $V_{IN} = \text{GND}$	—	—	1	μA
$ I_{OZ} $	Output Leakage Current	$V_{CC} = \text{Max.}$, $V_{OUT} = V_{CC}$, $V_{OUT} = \text{GND}$	—	—	1	μA
I_{OS}	Short Circuit Current ^(2,3)	$V_{CC} = \text{Max.}$, $V_{OUT} = \text{GND}$	-60	—	-250	mA
ΔV_T	Input Hysteresis	$V_{TLH} - V_{THL}$ for All Inputs	—	0.2	—	V
R_{OUT}	Output Resistance QS52805/52806T	$V_{CC} = \text{Min.}$, $I_{OL} = 12\text{mA}$	—	28	—	Ω

Notes:

1. Typical values indicate $V_{CC} = 5.0\text{V}$ and $T_A = 25^{\circ}\text{C}$.
2. Not more than one output should be used to test this high power condition and the duration is ≤ 1 second.
3. Guaranteed by design but not tested.

Table 5. Power Supply Characteristics

Symbol	Parameter	Test Conditions ⁽¹⁾	Typ ⁽³⁾	Max	Unit
I_{CC}	Quiescent Power Supply Current	$V_{CC} = \text{Max.}, V_{IN} = \text{GND or } V_{CC}$	0.005	0.5	mA
ΔI_{CC}	Supply Current per Input HIGH	$V_{CC} = \text{Max.}, V_{IN} = 3.4\text{V}, f_I = 0\text{MHz}$	1.0	2.5	mA
I_{CCD}	Dynamic Power Supply ⁽²⁾ Current per Output	$V_{CC} = \text{Max.}, V_{IN} = V_{CC} \text{ or } V_{IN} = \text{GND}$ Outputs enabled, 50% duty cycle	0.08	0.18	mA/ MHz
I_C	Total Power Supply ^(2,4) Current Examples	$V_{CC} = \text{Max.},$ $\overline{OEA} = \overline{OEB} = \text{GND}$ 50% duty cycle, $f_I = 10\text{MHz}$ 5 outputs toggling, Unused inputs = GND or V_{CC}	$V_{IN} = V_{CC} \text{ or } V_{IN} = \text{GND}$	4.0	9.5
			$V_{IN} = 3.4\text{V or } V_{IN} = \text{GND}$	4.5	10.8
		$V_{CC} = \text{Max.},$ $\overline{OEA} = \overline{OEB} = \text{GND}$ 50% duty cycle, $f_I = 2.5\text{MHz}$ All outputs toggling	$V_{IN} = V_{CC} \text{ or } V_{IN} = \text{GND}$	2.2	5.5
			$V_{IN} = 3.4\text{V or } V_{IN} = \text{GND}$	3.2	8.0

Notes:

- For conditions shown as Min. or Max., use the appropriate values specified under DC specifications.
- Guaranteed by design but not tested. $C_L = 0\text{pF}$
- Typical values are for reference only. Conditions are $V_{CC} = 5.0\text{V}$ and $T_A = 25^\circ\text{C}$.
- $I_C = I_{CC} + (\Delta I_{CC})(D_H)(N_T) + I_{CCD}(f_O)(N_O)$
where:
 D_H = Input duty cycle
 N_T = Number of TTL HIGH inputs at D_H (one or two)
 f_O = Output frequency
 N_O = Number of outputs at f_O

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Table 6. Skew Characteristics Over Operating Range

Industrial: $T_A = -40^{\circ}\text{C}$ to 85°C , $V_{CC} = 5.0\text{V} \pm 10\%$ Military: $T_A = -55^{\circ}\text{C}$ to 125°C , $V_{CC} = 5.0\text{V} \pm 10\%$
 For QS5805T, QS5806T $C_{LOAD} = 50\text{pF}$, $R_{LOAD} = 500\Omega$.
 For QS52805T, QS52806T $C_{LOAD} = 50\text{pF}$ (no resistor).

Symbol	Description ^(1,2)		—		A		B		C		Unit
			Min	Max	Min	Max	Min	Max	Min	Max	
$t_{SK(O1)}$	Skew between two outputs same transition, same bank	IND	—	0.5	—	0.35	—	0.3	—	0.3	ns
		MIL	—	0.7	—	0.6					
$t_{SK(O2)}$	Skew between two outputs same transition, different banks	IND	—	0.7	—	0.5	—	0.4	—	0.4	ns
		MIL	—	0.9	—	0.8					
$t_{SK(p)}$	Pulse Skew: Opposite transition skew, same output ($t_{PHL}-t_{PLH}$) QS5805/52805	IND	—	1.0	—	0.7	—	0.6	—	0.5	ns
		MIL	—	1.2	—	1.0					
$t_{SK(p)}$	Pulse Skew: Opposite transition skew, same output ($t_{PHL}-t_{PLH}$) QS5806/52806	IND	—	1.0	—	0.7	—	0.6	—	0.5	ns
		MIL	—	1.2	—	1.2					
$t_{SK(t)}$	Part to part skew ⁽³⁾	IND	—	1.5	—	1.0	—	1.0	—	1.0	ns
		MIL	—	1.5	—	1.5					

Notes:

1. Skew parameters are guaranteed across temperature range, but not production tested. Skew parameters apply to propagation delays only.
2. See Test Circuit and Waveforms.
3. $t_{SK(t)}$ only applies to devices of the same transition, same part type, same temperature, power supply voltage, loading, package and speed grade.

Table 7. Switching Characteristics Over Operating Range

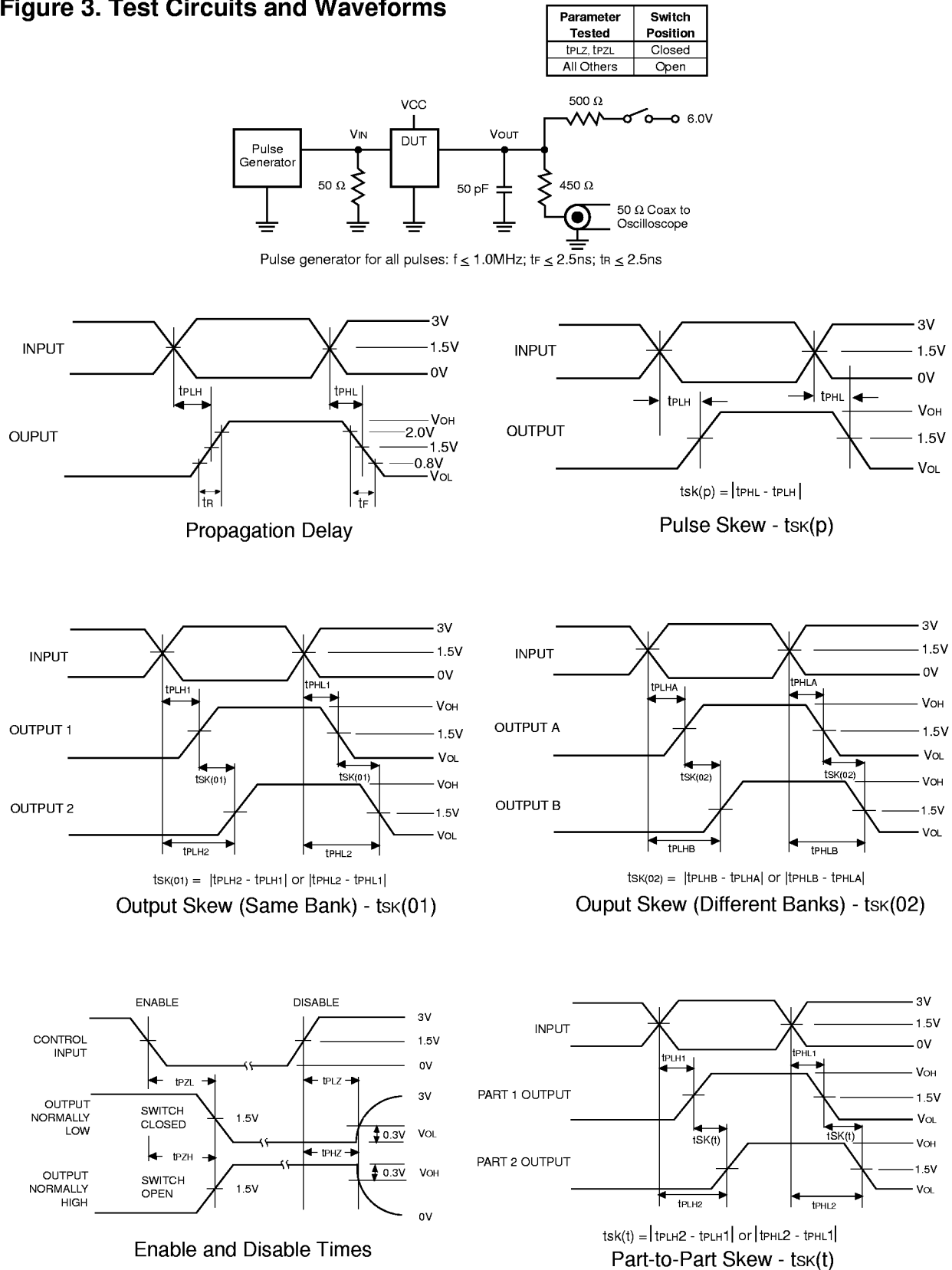
Industrial: $T_A = -40^{\circ}\text{C}$ to 85°C , $V_{CC} = 5.0\text{V} \pm 10\%$ Military: $T_A = -55^{\circ}\text{C}$ to 125°C , $V_{CC} = 5.0\text{V} \pm 10\%$
 For QS5805T, QS5806T $C_{LOAD} = 50\text{pF}$, $R_{LOAD} = 500\Omega$.
 For QS52805T, QS52806T $C_{LOAD} = 50\text{pF}$ (no resistor).

Symbol	Description ⁽¹⁾		—		A		B		C		Unit
			Min	Max	Min	Max	Min	Max	Min	Max	
t_{PLH} t_{PHL}	Propagation Delay ⁽²⁾	IND MIL	1.5 1.5	6.5 7.5	1.5 1.5	5.8 6.8	1.5	5.0	1.5	4.5	ns
t_{PZL} t_{PZH}	Output Enable Time	IND MIL	1.5 1.5	8.0 8.5	1.5 1.5	8.0 8.5	1.5	7.0	1.5	6.0	ns
t_{PLZ} t_{PZH}	Output Disable Time ⁽³⁾	IND MIL	1.5 1.5	7.0 7.5	1.5 1.5	7.0 7.5	1.5	6.0	1.5	5.0	ns
t_R, t_F	Output Rise/Fall Time ⁽³⁾ 0.8V-2.0V		—	1.5	—	1.5	—	1.5	—	1.5	ns

Notes:

1. See Test Circuit and Waveforms. Minimums guaranteed but not tested.
2. The propagation delay range indicated by Min. and Max. specifications results from process and environmental variables. These propagation delay limits do not imply skew.
3. Guaranteed but not tested.

Figure 3. Test Circuits and Waveforms

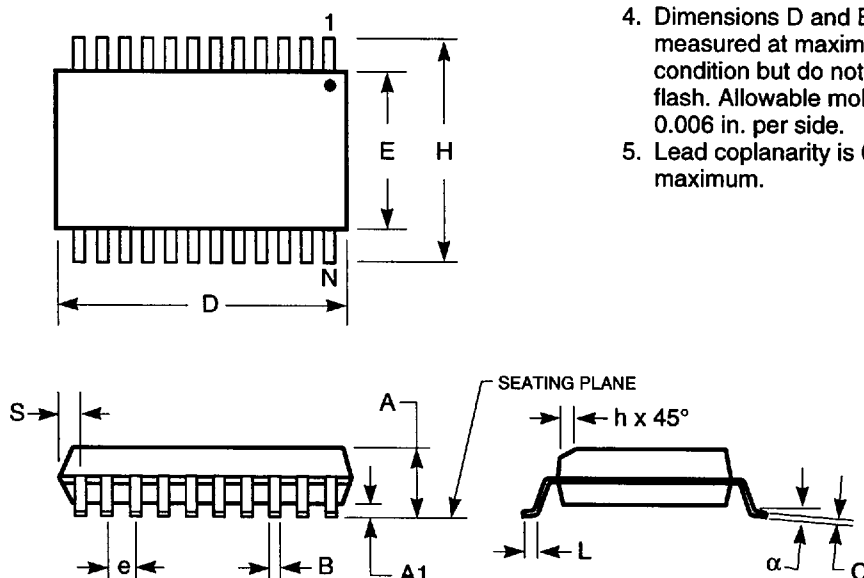


PACKAGING INFORMATION

150-MIL QSOP - Package Code Q

Quarter-Size Outline Package

Plastic Small Outline Gull-Wing



Notes:

1. Refer to applicable symbol list.
2. All dimensions are in inches.
3. N is the number of lead positions.
4. Dimensions D and E are to be measured at maximum material condition but do not include mold flash. Allowable mold flash is 0.006 in. per side.
5. Lead coplanarity is 0.004 in. maximum.

JEDEC#	MO-137AB			MO-137AD			MO-137AE			MO-137AF		
DWG#	PSS-16A			PSS-20A			PSS-24A			PSS-28A		
Symbol	Min	Nom	Max	Min	Nom	Max	Min	Nom	Max	Min	Nom	Max
A	0.060	0.064	0.068	0.060	0.064	0.068	0.060	0.064	0.068	0.060	0.064	0.068
A1	0.004	0.006	0.008	0.004	0.006	0.008	0.004	0.006	0.008	0.004	0.006	0.008
B	0.009	0.010	0.012	0.009	0.010	0.012	0.009	0.010	0.012	0.009	0.010	0.012
C	0.007	0.008	0.010	0.007	0.008	0.010	0.007	0.008	0.010	0.007	0.008	0.010
D	0.189	0.193	0.197	0.337	0.341	0.344	0.337	0.341	0.344	0.386	0.390	0.394
E	0.150	0.154	0.157	0.150	0.154	0.157	0.150	0.154	0.157	0.150	0.154	0.157
e	0.025 BSC			0.025 BSC			0.025 BSC			0.025 BSC		
H	0.230	0.236	0.244	0.230	0.236	0.244	0.230	0.236	0.244	0.230	0.236	0.244
h	0.010	0.013	0.016	0.010	0.013	0.016	0.010	0.013	0.016	0.010	0.013	0.016
L	0.016	0.025	0.035	0.016	0.025	0.035	0.016	0.025	0.035	0.016	0.025	0.035
N	16			20			24			28		
α	0°	5°	8°	0°	5°	8°	0°	5°	8°	0°	5°	8°
S	0.006	0.009	0.010	0.056	0.058	0.060	0.031	0.033	0.035	0.031	0.033	0.035

QUALITY SEMICONDUCTOR, INC.

APOP-00003-05

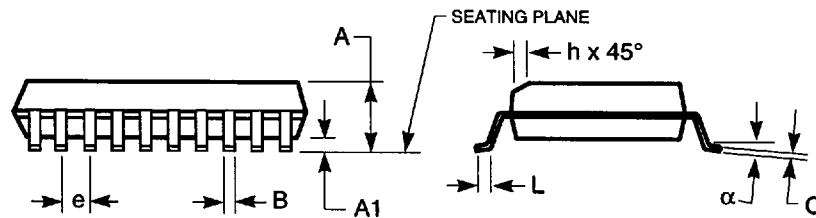
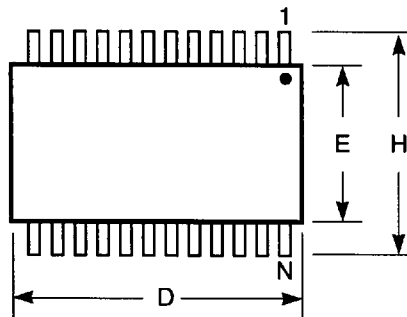
PACKAGING INFORMATION

300-MIL SOIC - Package Code SO

Plastic Small Outline Gull-Wing

Notes:

1. Refer to applicable symbol list.
2. All dimensions are in inches.
3. N is the number of lead positions.
4. Dimensions D and E are to be measured at maximum material condition but do not include mold flash. Allowable mold flash is 0.006 in. per side.
5. Lead coplanarity is 0.004 in. maximum.



JEDEC#	MS-013AA		MS-013AC		MS-013AD		MS-013AE	
DWG#	PS16A		PS20A		PS24A		PS28A	
Symbol	Min	Max	Min	Max	Min	Max	Min	Max
A	0.096	0.104	0.096	0.104	0.096	0.104	0.096	0.104
A1	0.005	0.011	0.005	0.011	0.005	0.011	0.005	0.011
B	0.014	0.019	0.014	0.019	0.014	0.019	0.014	0.019
C	0.009	0.012	0.009	0.012	0.009	0.012	0.009	0.012
D	0.402	0.412	0.500	0.510	0.602	0.612	0.701	0.711
E	0.292	0.299	0.292	0.299	0.292	0.299	0.292	0.299
e	0.044	0.056	0.044	0.056	0.044	0.056	0.044	0.056
H	0.396	0.416	0.396	0.416	0.396	0.416	0.396	0.416
h	0.010	0.016	0.010	0.016	0.010	0.016	0.010	0.016
L	0.020	0.040	0.020	0.040	0.020	0.040	0.020	0.040
N	16		20		24		28	
α	0°	8°	0°	8°	0°	8°	0°	8°