Creation Date: February 1994
Revision: June 6, 1996

Aptos SEMICONDUCTOR

AP32M256

256K x 32 Static RAM Module

Features

- High-density, 8-megabit, asynchronous Static RAM
- Low profile SIMM or ZIP package and 72-Pin Gold SIMM package
- High-speed, -15, -20 and -25 ns
- Single 5V 10% power supply
- TTL-compatible inputs and outputs
- JEDEC-compatible pinout

Functional Description

The Aptos AP32M256 is a high-speed SRAM memory module containing 262,144 words organized in a x32-bit configuration. The module consists of eight, 256K x 4 fast static RAMs mounted on either a 64-pin or 72-pin, double-sided, FR-4-printed circuit board.

The AP32M256 offers the optimum in packaging density and profile height. It is packaged on a 64-lead SIMM, a 64-lead ZIP, or a 72-pin Gold SIMM. The dual row configuration allows 64 pins to be placed on a package 3.65 inches long or 3.85 inches long, respectively. At only 0.58 and 0.61 inches high, these low-profile packages are ideal for systems with minimum board spacing. This module is designed to upgrade from 64-pin into a 72-pin socket.

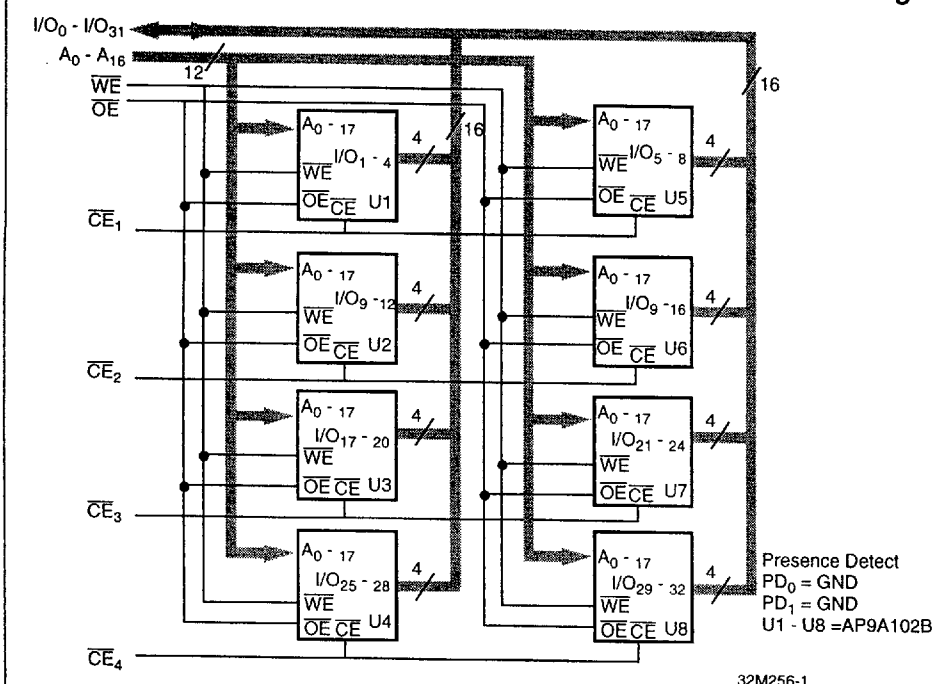
All inputs and outputs of the AP32M256 are TTL-compatible and operate from a single 5V supply. Full asynchronous circuitry requires no clocks or refresh for operation and provides equal access and cycle times for ease of use.

Reading the device is accomplished by taking the Chip Enable ($\overline{CE}$) LOW while Write Enable ($\overline{WE}$) remains HIGH. Under these conditions, the contents of the memory location specified on the address pins will appear on the data input/output pins (I/O).

Writing to each byte is accomplished when the appropriate chip select and write enable inputs are both LOW. Data on the input/output pin is written into the memory location specified on the address pins (A_0 through A_{17}).

PD_0 and PD_1 identify the module's density allowing interchangeable use of alternate density, industry-standard modules. Four chip enable inputs, $\overline{CE}_1$, $\overline{CE}_2$, $\overline{CE}_3$ and $\overline{CE}_4$, are used to enable the module's 4 bytes independently.

Block Diagram



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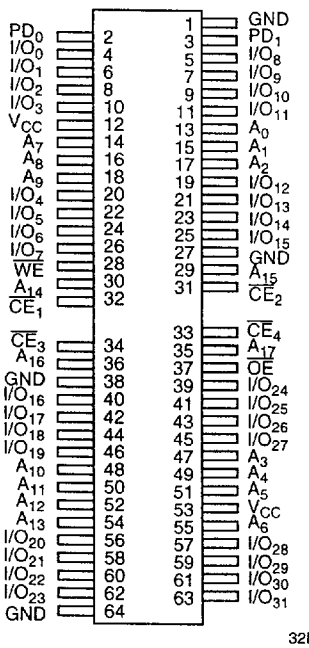
Pin Configuration

64-Pin SIMM/ZIP
Top View



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Selection Guide

	AP32M256-15	AP32M256-20	AP32M256-25
Maximum Access Time (ns)	15	20	25
Maximum Operating Current (mA)	1280	1120	960
Maximum Standby Current (mA)	40	40	40

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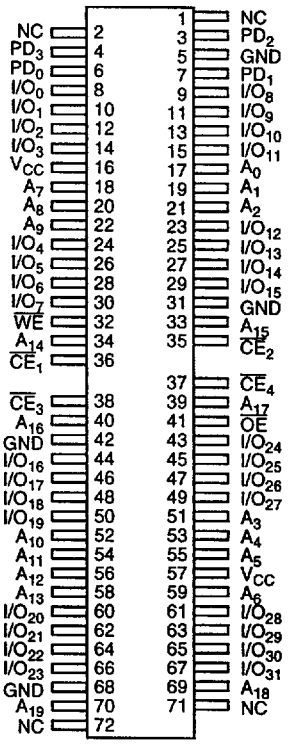
Pin Configurations (continued)

72-Pin SIMM
Top View



Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature..... -55°C to +125°C
Ambient Temperature
with Power Applied..... -0°C to +70°C
V_{CC} Supply Relative to GND ..... -0.5 V to +7.0 V
Voltage on Any Pin Relative to GND..... -0.5 V to V_{CC} +0.5 V
Short Circuit Output Current[1]..... 40 mA
Power Dissipation..... 8.0 W

Electrical Characteristics Over the Operating Range ($0°C \geq T_A \geq 70°C$, $V_{CC} = 5V \pm 10\%$)

Symbol	Parameter	Test Conditions	32M256-15		32M256-20		32M256-25		Unit
			Min.	Max.	Min.	Max.	Min.	Max.	
I_{CC}	Dynamic Operating Current [2]			1280		1120		960	mA
I_{SB1}	TTL Standby Current -TTL Inputs	$\overline{CE} \geq V_{IH}$, $I_{OUT} = 0$		360		280		240	mA
I_{SB2}	CMOS Standby Current -CMOS Inputs	$\overline{CE} \geq V_{CC}$ -0.2V, $I_{OUT} = 0$		40		40		40	mA
I_{LI}	Input Leakage Current	$V_{IN} = 0$ V to V_{CC}	-40	40	-40	40	-40	40	µA
I_{LO}	Output Leakage Current	$V_{IN} = 0$ V to V_{CC}	-5	5	-5	5	-5	5	µA
V_{OH}	Output High Voltage	V_{CC} = Min., I_{OH} = -4.0 mA	2.4		2.4		2.4		V
V_{OL}	Output Low Voltage	V_{CC} = Min., I_{OL} = 8.0 mA		0.4		0.4		0.4	V
V_{IH}	Input High Voltage		2.2	V_{CC} +0.5	2.2	V_{CC} +0.5	2.2	V_{CC} +0.5	V
V_{IL}	Input Low Voltage [3]		-0.5	0.8	-0.5	0.8	-0.5	0.8	V

Capacitance[2] (T_A = 25°C, f = 1MHz, V_{CC} = 5.0V)

Symbol	Description	Max.	Unit
C_{I1} (A_0 - A_{17}, $\overline{WE}$, $\overline{OE}$)	Input Capacitance	60	pF
C_{I2} ($\overline{CE}$)	Input Capacitance	15	pF
C_{I3} (I/O_0 - I/O_{31})	I/O Capacitance	10	pF

Notes:

1. Outputs should not be shorted for more than 30 seconds. No more than one output should be shorted at any time.
2. I_{CC} is dependent upon output loading and cycle rates. Specified values are with outputs open.
3. Negative undershoot of up to 3.0 V is permitted once per cycle.
4. Sample tested, only.

Switching Characteristics Over the Operating Range[5, 6]

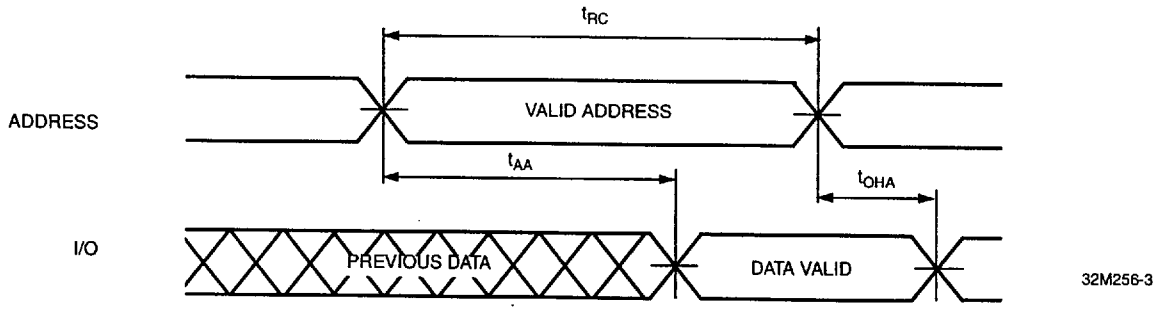
Parameter	Description	32M256-15		32M256-20		32M256-25		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
Read Cycle								
t_{RC}	Read Cycle Time	15		20		25		ns
t_{AA}	Address Access Time		15		20		25	ns
t_{OHA}	Output Hold Time	3		3		3		ns
t_{ACE}	$\overline{CE}$ LOW to Valid Data		15		20		25	ns
t_{LZCE}	$\overline{CE}$ LOW to Output Active	5		5		5		ns
t_{HZCE}	$\overline{CE}$ HIGH to Output High-Z		6		8		10	ns
t_{AOE}	$\overline{OE}$ LOW to Valid Data		5		7		8	ns
t_{LZOE}	$\overline{OE}$ LOW to Output Active	0		0		0		ns
t_{HZOE}	$\overline{OE}$ HIGH to Output High-Z		5		6		10	ns
t_{PU}	$\overline{CE}$ to Power Up	0		0		0		ns
t_{PD}	$\overline{CE}$ to Power Down		15		20		25	ns
Write Cycle								
t_{WC}	Write Cycle Time	15		20		25		ns
t_{SCE}	$\overline{CE}$ LOW to Write End	10		12		15		ns
t_{AW}	Address Valid to Write End	10		12		25		ns
t_{HA}	Address Hold to Write End	0		0		0		ns
t_{SA}	Address Set-up Time	0		0		0		ns
t_{PWE}	$\overline{WE}$ Pulse Width	12		12		15		ns
t_{SD}	Data Set-up to Write End	7		9		10		ns
t_{HD}	Data Hold from Write End	0		0		0		ns
t_{HZWE}	$\overline{WE}$ LOW to High-Z Output		7		8		10	ns
t_{LZWE}	$\overline{WE}$ HIGH to Output Active	3		3		3		ns

Notes:

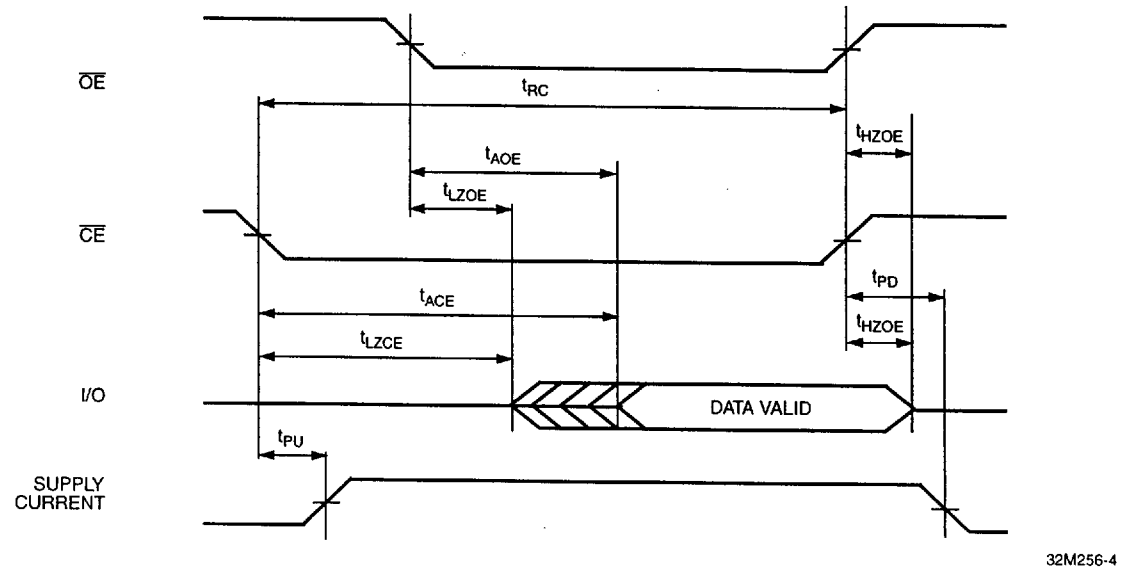
5. Active output to High-Z and High-Z to output active tests specified for a 500mV transition from steady state levels into the test load. C_{LOAD} = 5 pF.
6. Guaranteed, but not tested.

Switching Waveforms

Read Cycle No. 1 ($\overline{WE}$ and CE_2 are HIGH, $\overline{CE}_1$ and $\overline{OE}$ are LOW)[7]



Read Cycle No. 2 ($\overline{WE}$ is HIGH)[8]

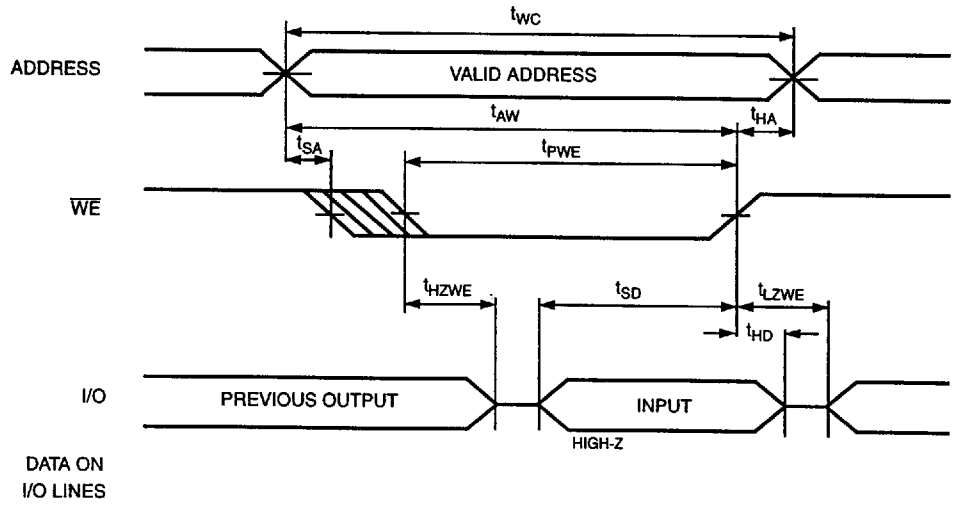


Notes:

7. Chip is in Read Mode: $\overline{WE}$ is HIGH, $\overline{CE}$ and $\overline{OE}$ are LOW. Read cycle timing is referenced from when all addresses are stable until the first address transition. Crosshatched portion of the I/O implies that data lines are in the Low-Z state and the data may not be valid.
8. $\overline{WE}$ is HIGH. I/O is not specified until t_{ACE}, but may become valid as soon as t_{LZCE}. Output will transition from High-Z to valid data out. Data out is valid after both t_{ACE} and t_{AOE} are met.

Switching Waveforms (continued)

Write Cycle No. 1 ($\overline{WE}$ controlled) [9, 10]



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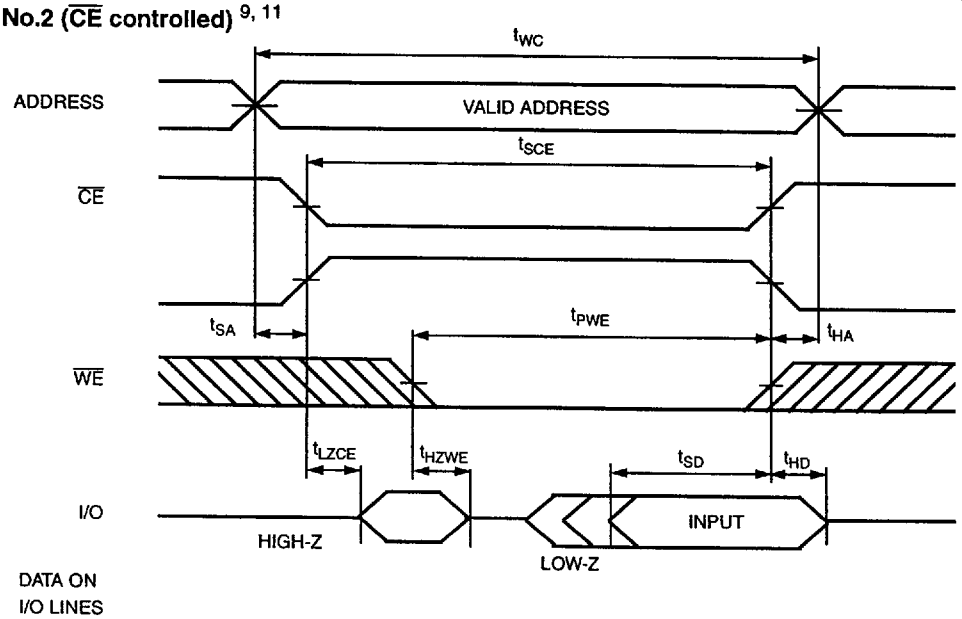
Write Cycle No.2 ($\overline{CE}$ controlled) [9, 11]



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Notes:

9. Addresses must be stable during Write cycles. $\overline{CE}$ or $\overline{WE}$ must be HIGH during address transitions. The outputs will remain in the High-Z state if $\overline{WE}$ is LOW when $\overline{CE}$ goes LOW. Care should be taken so that the output drivers are disabled prior to placing the Input Data on the I/O Lines. This will prevent bus contention, reducing system noise.

10. Chip is selected; $\overline{CE}$ and $\overline{OE}$ are LOW. Using only $\overline{WE}$ to control Write cycles may not offer the best device performance, since both t_{HZWE} and t_{SD} timing specifications must be met.

11. $\overline{OE}$ is LOW. I/O lines may transition to Low-Z if the falling edge of $\overline{WE}$ occurs after the falling edge of $\overline{CE}$.

Truth Table

Mode	$\overline{WE}$	$\overline{CE}$	$\overline{OE}$	I/O	V_{CC}
Standby	X	H	X	High-Z	Standby
Read	H	L	L	Output	Active
Read	H	L	H	High-Z	Active
Write	L	L	X	Input	Active

Ordering Information

Speed	Part Number	Package Name	Package Type
15	AP32M256M-15	M64.2	64-Pin SIMM, Double Sided
	AP32M256M7-15	M72.1	72-Pin Gold SIMM
	AP32M256Z-15	Z64.1	64-Pin ZIP
20	AP32M256M-20	M64.1	64-Pin SIMM, Double Sided
	AP32M256M7-20	M72.1	72-Pin Gold SIMM
	AP32M256Z-20	Z64.1	64-Pin ZIP
25	AP32M256M-25	M64.1	64-Pin SIMM, Double Sided
	AP32M256M7-25	M72.1	72-Pin Gold SIMM
	AP32M256Z-25	Z64.1	64-Pin ZIP

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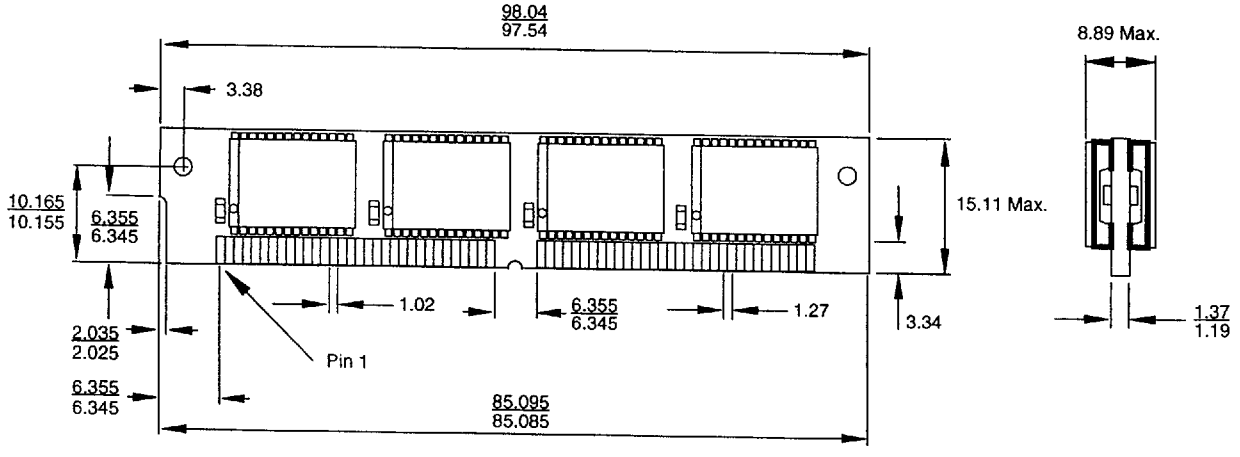
Package Diagrams

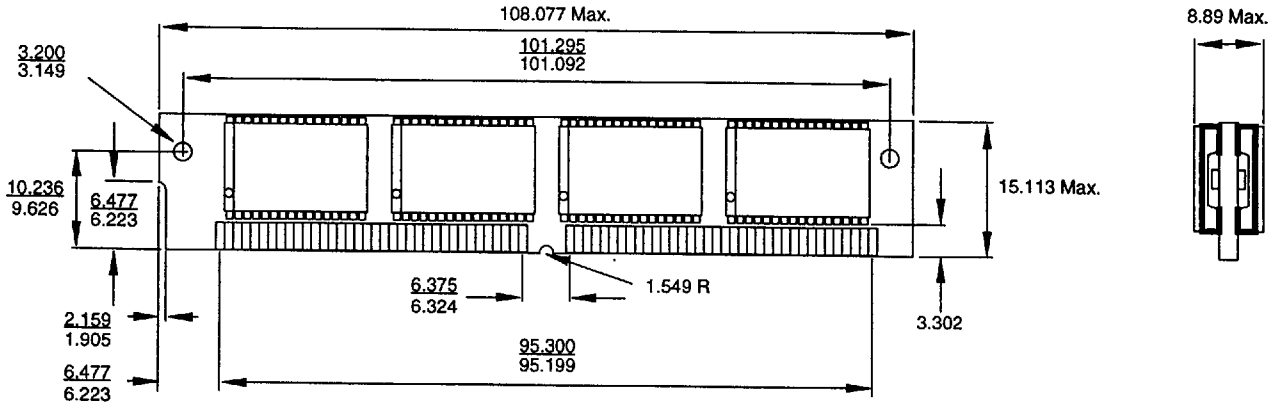
M64.2 - 64-Pin Single In-Line Memory Module (SIMM) - Double Sided



Measurements are in Millimeters unless otherwise specified $\left(\frac{MAX}{MIN}\right)$ or typical if not noted.

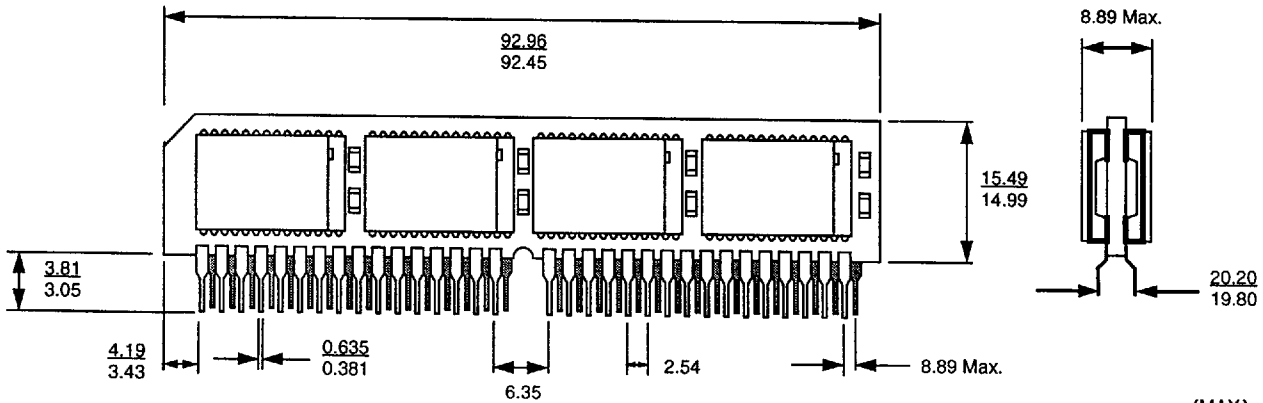
Package Diagrams (continued)

M72.1 - 72 -Pin Single In-Line Memory Module (SIMM) - Double Sided



Measurements are in Millimeters unless otherwise specified. (MAX / MIN)

Z64.1 - 64 -Pin Z In-Line Package (ZIP) - Double Sided



Measurements are in Millimeterss unless otherwise specified. (MAX / MIN)