

Q

High Speed CMOS Bus Interface 8-, 9-, and 10-Bit Registers

QS54/74FCT821T
QS54/74FCT823T
QS54/74FCT825T

QS54/74FCT2821T
QS54/74FCT2823T
QS54/74FCT2825T

FEATURES/BENEFITS

- Pin and function compatible to the 74F821/3/5 74FCT821/3/5 and 74FCT821T/3T/5T
- CMOS power levels: <7.5 mW static
- Available in DIP, SOIC, QSOP, ZIP, HQSOP
- Undershoot clamp diodes on all inputs
- TTL-compatible input and output levels
- Ground bounce controlled outputs
- Reduced output swing of 0-3.5V
- Military product compliant to MIL-STD-883

FCT 821T, 823T, 825T

- JEDEC-FCT spec compatible
- Fastest CMOS logic family available
- $I_{OL} = 48$ mA Com., 32 mA Mil.

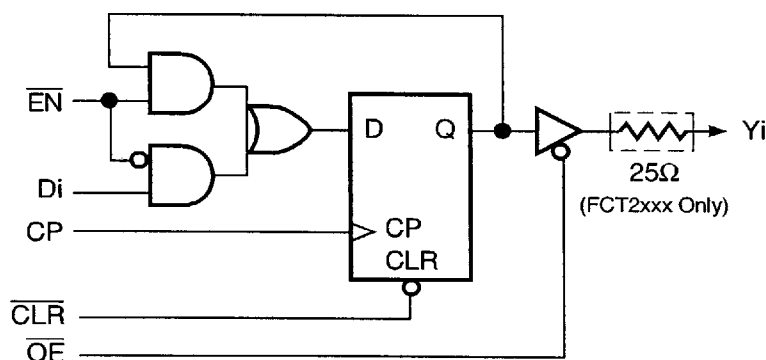
FCT 2821T, 2823T, 2825T

- Built-in 25Ω series resistor outputs reduce reflection and other system noise
- $I_{OL} = 12$ mA Com.

DESCRIPTION

The QSFCT821T/823T/825T and QSFCT2821T/2823T/2825T are 10-, 9-, and 8-bit high-speed CMOS TTL-compatible buffered registers with three-state outputs that are ideal for driving high capacitance loads such as memory and address buses. The 2821/3/5 devices are 25Ω resistor output versions useful for driving transmission lines and reducing system noise. The 2821 series parts can replace the 821 series to reduce noise in an existing design. All inputs have clamp diodes for undershoot noise suppression. All outputs have ground bounce suppression (see QSI Application Note AN-001), and outputs will not load an active bus when V_{CC} is removed from the device.

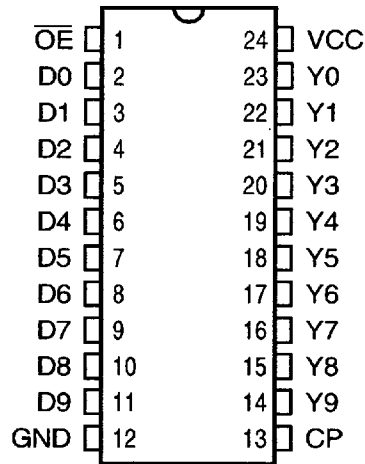
FUNCTIONAL BLOCK DIAGRAM



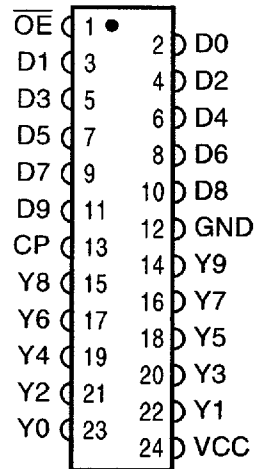
FCT821 - 10 BIT REGISTER

PIN CONFIGURATIONS (All Pins Top View)

PDIP, SOIC, QSOP, HQSOP



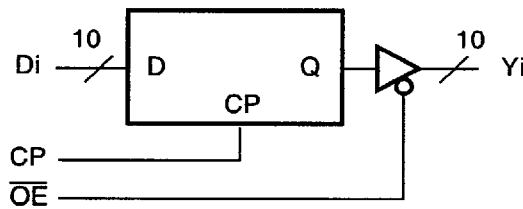
ZIP



PIN DESCRIPTION

Name	I/O	Description
Di	I	Data Inputs
Yi	O	Data Outputs-Three State
CP	I	Clock Pulse
$\overline{OE}$	I	Output Enable

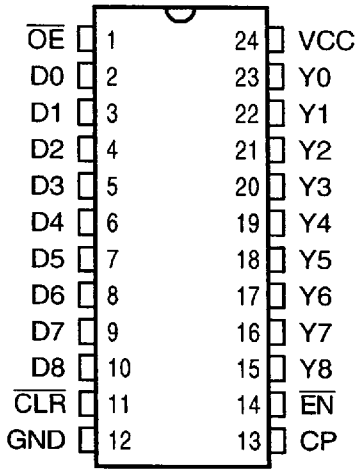
FCT821 LOGIC SYMBOL



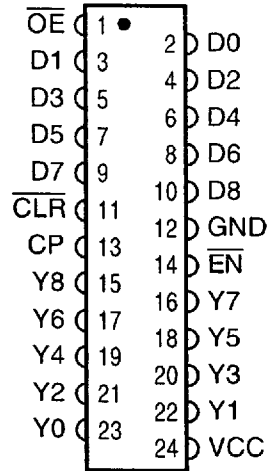
FCT823 - 9 BIT REGISTER

PIN CONFIGURATIONS (All Pins Top View)

PDIP, SOIC, QSOP, HQSOP



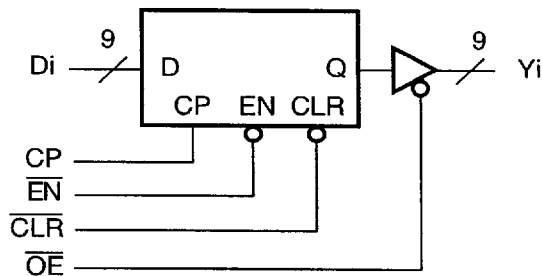
ZIP



PIN DESCRIPTION

Name	I/O	Description
Di	I	Data Inputs
Yi	O	Data Outputs-Three State
$\overline{OE}$	I	Output Enable
CP	I	Clock Pulse
$\overline{EN}$	I	Clock Enable
$\overline{CLR}$	I	Asynchronous Reset

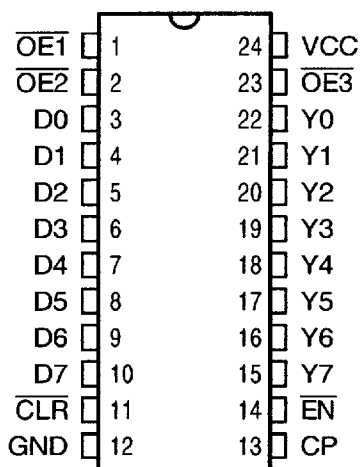
FCT823 LOGIC SYMBOL



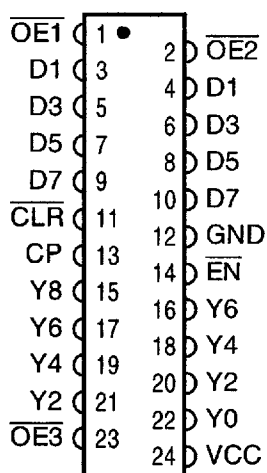
FCT825 - 8 BIT REGISTER

PIN CONFIGURATIONS (All Pins Top View)

PDIP, SOIC, QSOP, HQSOP



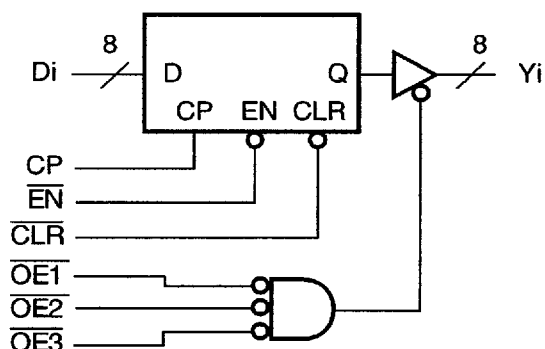
ZIP



PIN DESCRIPTION

Name	I/O	Description
Di	I	Data Inputs
Yi	O	Data Outputs-Three State
OE	I	Output Enable
CP	I	Clock Pulse
EN	I	Clock Enable
CLR	I	Asynchronous Reset

FCT825 LOGIC SYMBOL



FUNCTION TABLE

Inputs					Int.	O/P	Function
OE	CLR	EN	Di	CP	Qi	Yi	
H	X	L	L	↑	L	Hi-Z	High Z
H	X	L	H	↑	H	Hi-Z	High Z
H	L	X	X	X	L	Hi-Z	Clear
L	L	X	X	X	L	L	Clear
H	H	H	X	X	NC	Hi-Z	Hold
L	H	H	X	X	NC	NC	Hold
H	H	L	L	↑	L	Hi-Z	Load
H	H	L	H	↑	H	Hi-Z	Load
L	H	L	L	↑	L	L	Load
L	H	L	H	↑	H	H	Load

Note: For the 821, the HI-Z and Load functions only apply as the $\overline{EN}$ and $\overline{CLR}$ are not present in these devices. For the 825, there are three output enables, and the composite output enable is asserted on when all three are LOW. If any one of the three output enables are HIGH, the output is disabled.

ABSOLUTE MAXIMUM RATINGS

Supply Voltage to Ground	-0.5V to +7.0V
DC Output Voltage V_{OUT}	-0.5V to +7.0V
DC Input Voltage V_{IN}	-0.5V to +7.0V
AC Input Voltage (for a pulse width ≤ 20 ns)	-3.0V
DC Input Diode Current with $V_{IN} < 0$	-20 mA
DC Output Diode Current with $V_{OUT} < 0$	-50 mA
DC Output Current Max. Sink Current/Pin	120 mA
Maximum Power Dissipation	0.5 watts
T_{STG} Storage Temperature	-65° to +150°C

Note: Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to QSI devices that result in functional or reliability type failures.

CAPACITANCE

$T_A = 25^\circ\text{C}$, $f = 1$ MHz, $V_{IN} = 0\text{V}$, $V_{OUT} = 0\text{V}$

Pins	SOIC	QSOP	PDIP	ZIP	Unit
1, 3-11, 13	4	4	5	7	pF
15-22	6	6	7	9	pF
2, 14, 23	8	8	9	10	pF

Note: Capacitance is characterized but not tested.

POWER SUPPLY CHARACTERISTICS

Symbol	Parameter	Test Conditions ⁽¹⁾	Min	Max	Unit
I_{CC}	Quiescent Power Supply Current	$V_{CC} = \text{Max.}$, freq = 0 $0\text{V} \leq V_{IN} \leq 0.2\text{V}$ or $V_{CC}-0.2\text{V} \leq V_{IN} \leq V_{CC}$	—	1.5	mA
ΔI_{CC}	Supply Current per Input @ TTL HIGH	$V_{CC} = \text{Max.}$, $V_{IN} = 3.4\text{V}$, freq = 0 ⁽²⁾	—	2.0	mA
Q_{CCD}	Supply Current per Input per MHz	$V_{CC} = \text{Max.}$, Outputs open and enabled One bit toggling @ 50% duty cycle Other inputs at GND or V_{CC} ^(3,4)	—	0.25	mA/MHz

Notes:

- For conditions shown as Min. or Max., use the appropriate values specified under DC specifications.
- Per TTL driven input ($V_{IN} = 3.4\text{V}$).
- For flip-flops, Q_{CCD} is measured by switching one of the data input pins so that the output changes every clock cycle. This is a measurement of device power consumption only and does not include power to drive load capacitance or tester capacitance. This parameter is guaranteed by design but not tested.
- I_C can be computed using the above parameters as explained in the Technical Overview section.

DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE

Commercial $T_A = 0^\circ\text{C}$ to 70°C , $V_{CC} = 5.0\text{V} \pm 5\%$

Military $T_A = -55^\circ\text{C}$ to 125°C , $V_{CC} = 5.0\text{V} \pm 10\%$

Symbol	Parameter	Test Conditions	Min	Typ ⁽¹⁾	Max	Unit
V_{IH}	Input HIGH Voltage	Logic HIGH for All Inputs	2.0	—	—	V
V_{IL}	Input LOW Voltage	Logic LOW for All Inputs	—	—	0.8	V
ΔV_T	Input Hysteresis	$V_{TLH} - V_{THL}$ for All Inputs	—	0.2	—	V
$ I_{IH} $ $ I_{IL} $	Input Current Input HIGH or LOW	$V_{CC} = \text{Max.}, 0 \leq V_{IN} < V_{CC}$	—	—	5	μA
$ I_{OZ} $	Off-State Output Current (Hi-Z)	$V_{CC} = \text{Max.}, 0 \leq V_{IN} \leq V_{CC}$	—	—	5	μA
I_{OS}	Short Circuit Current (FCTXXX)	$V_{CC} = \text{Max.}, V_{OUT} = \text{GND}^{(2,3)}$	-60	—	—	mA
I_{OR}	Current Drive (FCT2XXX)	$V_{CC} = \text{Min.}, V_{OUT} = 2.0\text{V}^{(3)}$	50	—	—	mA
V_{IC}	Input Clamp Voltage	$V_{CC} = \text{Min.}, I_{IN} = -18\text{ mA}, T_A = 25^\circ\text{C}^{(3)}$	—	-0.7	-1.2	V
V_{OH}	Output HIGH Voltage	$V_{CC} = \text{Min.}$ $I_{OH} = -15\text{ mA (MIL)}$ $I_{OH} = -24\text{ mA (COM)}$	2.4 2.4	— —	— —	V
V_{OL}	Output LOW Voltage (FCTXXX)	$V_{CC} = \text{Min.}$ $I_{OL} = 32\text{ mA (MIL)}$ $I_{OL} = 48\text{ mA (COM)}$	— —	— —	0.50 0.50	V
V_{OL}	Output LOW Voltage (FCT2XXX- 25 Ω)	$V_{CC} = \text{Min.}$ $I_{OL} = 12\text{ mA (MIL)}$ $I_{OL} = 12\text{ mA (COM)}$	— —	— —	0.50 0.50	V
R_{OUT}	Output Resistance (FCT2XXX- 25 Ω)	$V_{CC} = \text{Min.}$ $I_{OL} = 12\text{ mA (MIL)}$ $I_{OL} = 12\text{ mA (COM)}$	— 20	25 28	— 40	Ω

Notes:

1. Typical values indicate $V_{CC} = 5.0\text{V}$ and $T_A = 25^\circ\text{C}$.
2. Not more than one output should be shorted and the duration is ≤ 1 second.
3. These parameters are guaranteed by design but not tested.

SWITCHING CHARACTERISTICS OVER OPERATING RANGE

Commercial $T_A = 0^\circ\text{C}$ to 70°C , $V_{CC} = 5.0\text{V} \pm 5\%$

Military $T_A = -55^\circ\text{C}$ to 125°C , $V_{CC} = 5.0\text{V} \pm 10\%$

$C_{LOAD} = 50\text{ pF}$, $R_{LOAD} = 500\Omega$ unless otherwise noted.

Symbol	Description ⁽¹⁾		821A 823A 825A 2821A 2823A 2825A		821B 823B 825B 2821B 2823B 2825B		821C 823C 825C 2821C 2823C		821D 823D 2821D 2823D		Unit
			Min	Max	Min	Max	Min	Max	Min	Max	
t _{PHL}	Clock to Y Delay	Com		10		7.5		6.0		5.3	ns
t _{PLH}	$\overline{OE} = \text{LOW}$, 821/3/5	Mil		11.5		8.5		7.0			
t _{PHL}	Clock to Y Delay ^(2,3)	Com		20		15		12.5		12.5	ns
t _{PLH}	$\overline{OE} = \text{LOW}$, 821/3/5	Mil		20		16		13.5			
t _{PHL}	Clock to Y Delay	Com		10		7.5		6.0		5.3	ns
t _{PLH}	$\overline{OE} = \text{LOW}$, 2821/3/5	Mil		11.5		8.5					
t _{PHL}	Clock to Y Delay ^(2,3)	Com		20		15		12.5		12.5	ns
t _{PLH}	$\overline{OE} = \text{LOW}$, 2821/3/5	Mil		20		16					
t _s	Data to CP Setup Time	Com	4.0		3.0		3.0		3.0		ns
		Mil	4.0		3.0		3.0				
t _h	Data to CP Hold Time	Com	2.0		1.5		1.5		1.5		ns
		Mil	2.0		1.5		1.5				
t _{ENS}	$\overline{EN}$ to CP Setup Time	Com	4.0		3.0		3.0		3.0		ns
		Mil	4.0		3.0		3.0				
t _{ENH}	$\overline{EN}$ to CP Hold Time	Com	2.0		0.0		0.0		0.0		ns
		Mil	2.0		0.0		0.0				

Notes:

1. See Test Circuit and Waveforms.
2. This parameter is guaranteed by design but not tested.
3. $C_{LOAD} = 300\text{ pF}$

TIMING REQUIREMENTS OVER OPERATING RANGE

Commercial TA = 0°C to 70°C, Vcc = 5.0V ± 5%

Military TA = -55°C to 125°C, Vcc = 5.0V ± 10%

CLOAD = 50 pF, RLOAD = 500Ω unless otherwise noted.

Symbol	Description(1)		821A 823A 825A 2821A 2823A 2825A		821B 823B 825B 2821B 2823B 2825B		821C 823C 825C 2821C 2823C		821D 823D 2821D 2823D		Unit
			Min	Max	Min	Max	Min	Max	Min	Max	
tCLR	CLR to Y Delay 823/5	Com Mil		11 12		9.0 9.5		8.0 8.5		7.0	ns
tCLR	CLR to Y Delay 2823/5	Com Mil		11 12		9.0 9.5		8.0		7.0	ns
tREC	CLR to CP Setup Time	Com Mil	6.0 7.0		6.0 6.0		6.0 6.0		6.0		ns
tpWH tpWL	Clock Pulse Width(2) HIGH or LOW	Com Mil	7.0 7.0		6.0 6.0		6.0 6.0		6.0		ns
tpZH tpZL	Output Enable Time OE to Yi, 821/3/5	Com Mil		12 13		8.0 9.0		7.0 8.0		6.5	ns
tpZH tpZL	Output Enable Time(2,3) OE to Yi, 821/3/5	Com Mil		23 25		15 16		12.5 13.5		12.5	ns
tpZH tpZL	Output Enable Time OE to Yi, 2821/3/5	Com Mil		12 13		8.0 9.0		7.0		6.5	ns
tpZH tpZL	Output Enable Time(2,3) OE to Yi, 2821/3/5	Com Mil		23 25							ns
tpHZ tplZ	Output Disable Time(2,4) OE to Yi	Com Mil		7.0 8.0		6.5 7.0		6.2 6.2		6.2	ns
tpHZ tplZ	Output Disable Time(2) OE to Yi	Com Mil		9.0 10		7.5 8.0		6.5 6.5		6.5	ns

Notes:

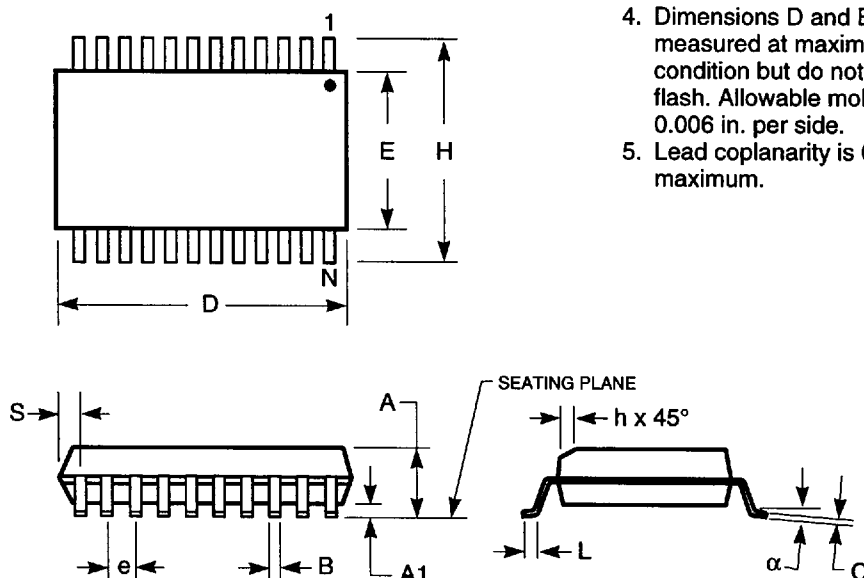
1. See Test Circuit and Waveforms.
2. This parameter is guaranteed by design but not tested.
3. CLOAD = 300 pF
4. CLOAD = 5 pF

PACKAGING INFORMATION

150-MIL QSOP - Package Code Q

Quarter-Size Outline Package

Plastic Small Outline Gull-Wing



Notes:

1. Refer to applicable symbol list.
2. All dimensions are in inches.
3. N is the number of lead positions.
4. Dimensions D and E are to be measured at maximum material condition but do not include mold flash. Allowable mold flash is 0.006 in. per side.
5. Lead coplanarity is 0.004 in. maximum.

JEDEC#	MO-137AB			MO-137AD			MO-137AE			MO-137AF		
DWG#	PSS-16A			PSS-20A			PSS-24A			PSS-28A		
Symbol	Min	Nom	Max	Min	Nom	Max	Min	Nom	Max	Min	Nom	Max
A	0.060	0.064	0.068	0.060	0.064	0.068	0.060	0.064	0.068	0.060	0.064	0.068
A1	0.004	0.006	0.008	0.004	0.006	0.008	0.004	0.006	0.008	0.004	0.006	0.008
B	0.009	0.010	0.012	0.009	0.010	0.012	0.009	0.010	0.012	0.009	0.010	0.012
C	0.007	0.008	0.010	0.007	0.008	0.010	0.007	0.008	0.010	0.007	0.008	0.010
D	0.189	0.193	0.197	0.337	0.341	0.344	0.337	0.341	0.344	0.386	0.390	0.394
E	0.150	0.154	0.157	0.150	0.154	0.157	0.150	0.154	0.157	0.150	0.154	0.157
e	0.025 BSC			0.025 BSC			0.025 BSC			0.025 BSC		
H	0.230	0.236	0.244	0.230	0.236	0.244	0.230	0.236	0.244	0.230	0.236	0.244
h	0.010	0.013	0.016	0.010	0.013	0.016	0.010	0.013	0.016	0.010	0.013	0.016
L	0.016	0.025	0.035	0.016	0.025	0.035	0.016	0.025	0.035	0.016	0.025	0.035
N	16			20			24			28		
α	0°	5°	8°	0°	5°	8°	0°	5°	8°	0°	5°	8°
S	0.006	0.009	0.010	0.056	0.058	0.060	0.031	0.033	0.035	0.031	0.033	0.035

QUALITY SEMICONDUCTOR, INC.

APOP-00003-05

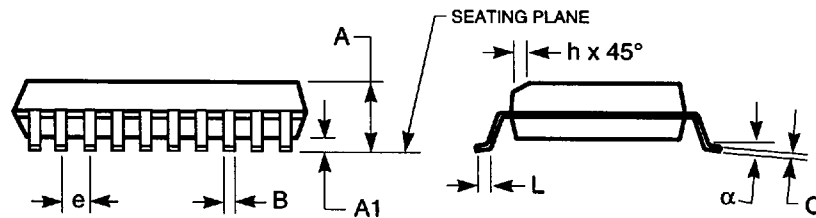
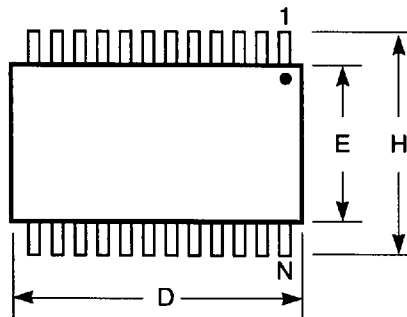
PACKAGING INFORMATION

300-MIL SOIC - Package Code SO

Plastic Small Outline Gull-Wing

Notes:

1. Refer to applicable symbol list.
2. All dimensions are in inches.
3. N is the number of lead positions.
4. Dimensions D and E are to be measured at maximum material condition but do not include mold flash. Allowable mold flash is 0.006 in. per side.
5. Lead coplanarity is 0.004 in. maximum.

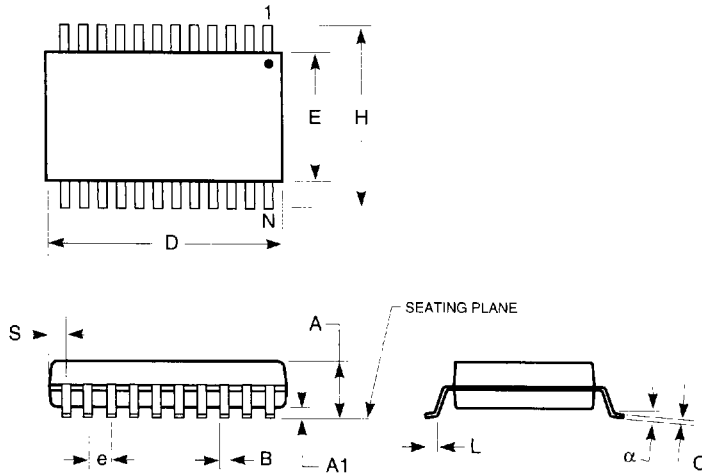


JEDEC#	MS-013AA		MS-013AC		MS-013AD		MS-013AE	
DWG#	PS16A		PS20A		PS24A		PS28A	
Symbol	Min	Max	Min	Max	Min	Max	Min	Max
A	0.096	0.104	0.096	0.104	0.096	0.104	0.096	0.104
A1	0.005	0.011	0.005	0.011	0.005	0.011	0.005	0.011
B	0.014	0.019	0.014	0.019	0.014	0.019	0.014	0.019
C	0.009	0.012	0.009	0.012	0.009	0.012	0.009	0.012
D	0.402	0.412	0.500	0.510	0.602	0.612	0.701	0.711
E	0.292	0.299	0.292	0.299	0.292	0.299	0.292	0.299
e	0.044	0.056	0.044	0.056	0.044	0.056	0.044	0.056
H	0.396	0.416	0.396	0.416	0.396	0.416	0.396	0.416
h	0.010	0.016	0.010	0.016	0.010	0.016	0.010	0.016
L	0.020	0.040	0.020	0.040	0.020	0.040	0.020	0.040
N	16		20		24		28	
α	0°	8°	0°	8°	0°	8°	0°	8°

PACKAGING INFORMATION

150-MIL HQSOP - Package Code H

Hermetic Quarter-Size Outline Package
Ceramic Small Outline Gull-Wing



Notes:

1. Refer to applicable symbol list.
2. All dimensions are in inches.
3. N is the number of lead positions.
4. Dimensions D and E are to be measured at maximum material condition.
5. Lead coplanarity is 0.004 in. maximum.

JEDEC#	TBD			TBD		
DWG#	HSS-20A			HSS-24A		
Symbol	Min	Nom	Max	Min	Nom	Max
A	0.070	0.074	0.078	0.070	0.074	0.078
A1	0.008	0.012	0.016	0.008	0.012	0.016
B	0.009	0.010	0.012	0.009	0.010	0.012
C	0.007	0.008	0.010	0.007	0.008	0.010
D	0.337	0.342	0.350	0.337	0.342	0.350
E	0.150	0.155	0.158	0.150	0.155	0.158
e	0.025 BSC			0.025 BSC		
H	0.230	0.236	0.244	0.230	0.236	0.244
L	0.016	0.025	0.035	0.016	0.025	0.035
N	20			24		
α	0°	5°	8°	0°	5°	8°
S	0.056	0.058	0.062	0.031	0.033	0.037

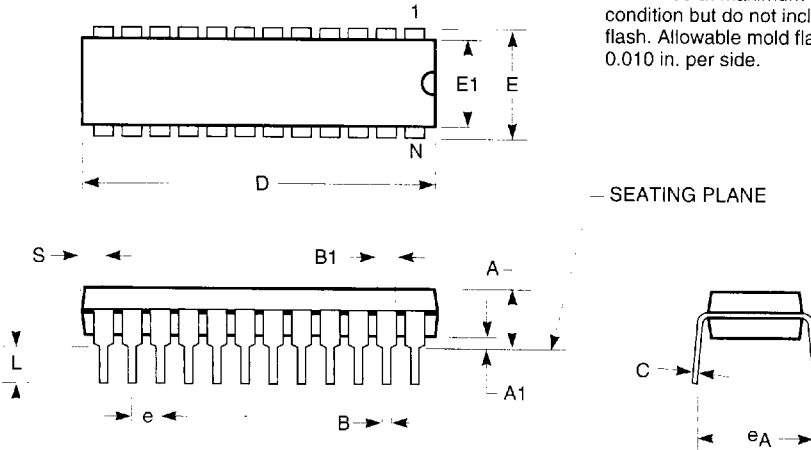
7466803 0003414 949

PACKAGING INFORMATION

300-MIL PDIP - Package Code P Plastic Dual In-line Package

Notes:

1. Refer to applicable symbol list.
2. All dimensions are in inches.
3. N is the number of lead positions.
4. Dimensions D and E1 are to be measured at maximum material condition but do not include mold flash. Allowable mold flash is 0.010 in. per side.



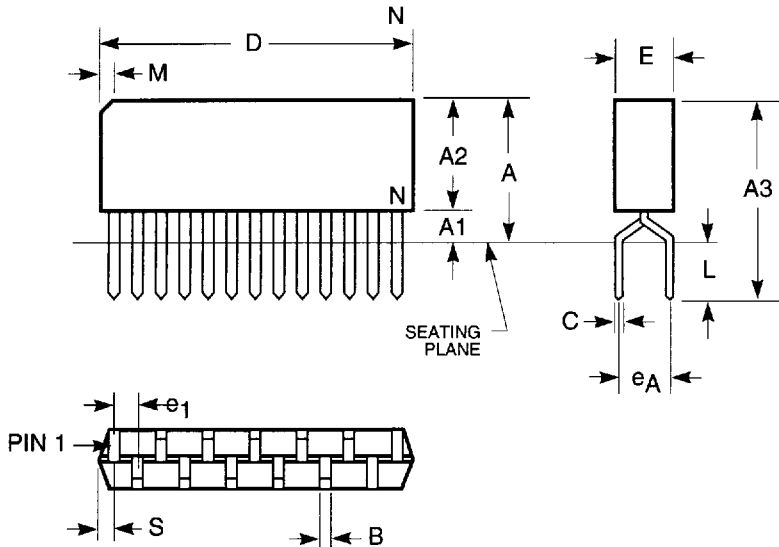
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DWG#	PD14A		PD16A		PD20A		PT22B		PT24A		PT28A	
Symbol	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max
A	0.130	0.170	0.130	0.170	0.130	0.170	0.130	0.170	0.130	0.170	0.130	0.180
A1	0.015	0.040	0.015	0.040	0.015	0.040	0.015	0.040	0.015	0.040	0.015	0.040
B	0.016	0.020	0.016	0.020	0.016	0.020	0.016	0.020	0.016	0.020	0.016	0.020
B1	0.045	0.070	0.045	0.070	0.045	0.070	0.045	0.070	0.045	0.070	0.045	0.060
C	0.009	0.012	0.009	0.012	0.009	0.012	0.009	0.012	0.009	0.012	0.009	0.012
D	0.745	0.765	0.745	0.765	1.020	1.040	1.020	1.040	1.150	1.260	1.345	1.385
E	0.300	0.325	0.300	0.325	0.300	0.325	0.300	0.325	0.300	0.325	0.300	0.325
E1	0.240	0.270	0.240	0.270	0.240	0.270	0.240	0.270	0.250	0.280	0.275	0.295
e	0.090	0.110	0.090	0.110	0.090	0.110	0.090	0.110	0.090	0.110	0.090	0.110
eA	0.310	0.380	0.310	0.380	0.310	0.380	0.310	0.380	0.310	0.380	0.310	0.380
L	0.120	0.140	0.120	0.140	0.120	0.140	0.120	0.140	0.120	0.140	0.120	0.140
S	0.070	0.080	0.020	0.035	0.060	0.070	0.010	0.020	0.025	0.080	0.020	0.040
N	14		16		20		22		24		28	

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PACKAGING INFORMATION

300-MIL ZIP - Package Code Z

Zig-zag In-line Packages



JEDEC#	MO-072AB		MO-072AC		MO-072AD	
DWG#	PZ20A		PZ24A		PZ28A	
Symbol	Min	Max	Min	Max	Min	Max
A	0.350	0.400	0.350	0.400	0.350	0.400
A1	0.030	0.070	0.030	0.070	0.032	0.055
A2	0.280	0.340	0.320	0.350	0.335	0.345
A3	0.450	0.550	0.450	0.550	0.460	0.550
B	0.015	0.024	0.015	0.024	0.015	0.024
C	0.008	0.012	0.008	0.012	0.008	0.012
D	1.008	1.030	1.200	1.250	1.409	1.424
E	0.100	0.120	0.100	0.120	0.110	0.120
e1	0.050 BSC		0.050 BSC		0.050 BSC	
eA	0.100 BSC		0.100 BSC		0.100 BSC	
L	0.100	0.150	0.100	0.150	0.110	0.150
M	0.035	0.085	0.035	0.085	0.035	0.085
N	20		24		28	
S	0.018	0.032	0.018	0.032	0.025	0.038

Notes:

1. Refer to applicable symbol list.
2. All dimensions are in inches.
3. N is the number of lead positions.
4. Dimensions D and E are to be measured at maximum material condition but do not include mold flash. Allowable mold flash is 0.010 in. per side.

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