



High Speed CMOS 32-Bit Transceivers in MillipaQ™

QS74FCT4X245ATQ3
QS74FCT4X245CTQ3
QS74FCT4X2245ATQ3

FEATURES/BENEFITS

- 32-bit Function compatible to the 74F245, 74ABT245, 74FCT245T and 74FCT2245T
- QS74FCT4X245T: $I_{OL} = 64 \text{ mA}$
- QS74FCT4X2245T: $I_{OL} = 12 \text{ mA}$
- Low CMOS power consumption
- Ground bounce controlled outputs
- A and C speed grades; 4.1 ns t_{PD} for C
- Smallest footprint 32-bit logic solution
- 80-pin, 150-mil MillipaQ package (Q3)
- Easy layout flow-through pinout
- Tube or tape-and-reel shipment
- TTL-compatible input and output levels
- Undershoot clamp diodes on all inputs

DESCRIPTION

The FCT4X245T and FCT4X2245T are 32-bit non-inverting transceivers with three-state outputs that are useful for bus-oriented applications. The Transmit/Receive (T/R) inputs determine the direction of data flow, whether from A-to-B or B-to-A, and the Output Enable (\bar{OE}) inputs enable the selected port for output. All inputs have clamp diodes for undershoot noise suppression. All outputs have ground bounce suppression (see QSI Application Note AN-01), and outputs will not load an active bus when V_{CC} is removed from the device. The MillipaQ 80-pin small outline package provides the smallest possible footprint while also offering an easy to layout flow-through, dual-in-line format.

Figure 1. Functional Block Diagram

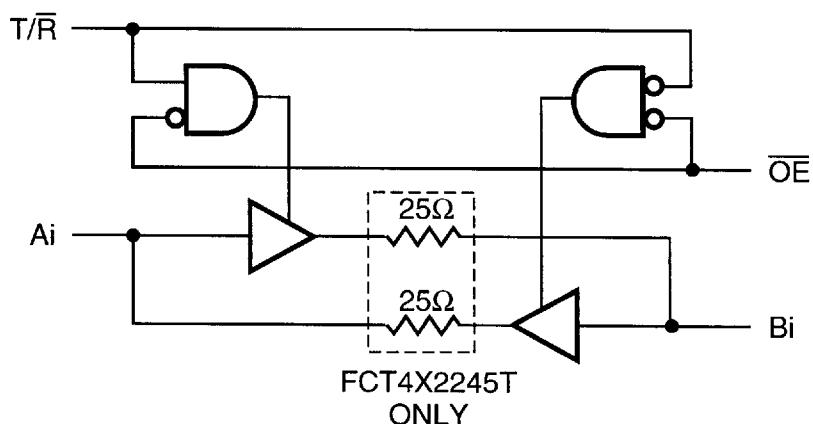


Figure 2. Pin Configuration
(All Pins Top View)

T/R0	1	80	Vcc
A0	2	79	OE0
A1	3	78	B0
A2	4	77	B1
A3	5	76	B2
A4	6	75	B3
A5	7	74	B4
A6	8	73	B5
A7	9	72	B6
GND	10	71	B7
T/R1	11	70	Vcc
A8	12	69	OE1
A9	13	68	B8
A10	14	67	B9
A11	15	66	B10
A12	16	65	B11
A13	17	64	B12
A14	18	63	B13
A15	19	62	B14
GND	20	61	B15
T/R2	21	60	Vcc
A16	22	59	OE2
A17	23	58	B16
A18	24	57	B17
A19	25	56	B18
A20	26	55	B19
A21	27	54	B20
A22	28	53	B21
A23	29	52	B22
GND	30	51	B23
T/R3	31	50	Vcc
A24	32	49	OE3
A25	33	48	B24
A26	34	47	B25
A27	35	46	B26
A28	36	45	B27
A29	37	44	B28
A30	38	43	B29
A31	39	42	B30
GND	40	41	B31

Table 1. Pin Description

Name	I/O	Description
AI	I/O	Data Bus A
BI	I/O	Data Bus B
T/R0	I	Direction for A/B7-A/B0
T/R1	I	Direction for A/B15-A/B8
T/R2	I	Direction for A/B23-A/B16
T/R3	I	Direction for A/B31-A/B24
OE0	I	Output Enables for A/B7-A/B0
OE1	I	Output Enables for A/B15-A/B8
OE2	I	Output Enables for A/B23-A/B16
OE3	I	Output Enables for A/B24-A/B31

Table 2. Function Table

OE _n	T/R _n	Bus A	Bus B	Function
H	X	Hi-Z	Hi-Z	Disable
L	L	Output	Input	Bus B to Bus A
L	H	Input	Output	Bus A to Bus B

Table 3. Absolute Maximum Ratings

Supply Voltage to Ground	-0.5V to +7.0V
DC Output Voltage V _{OUT}	-0.5V to +7.0V
DC Input Voltage V _{IN}	-0.5V to +7.0V
AC Input Voltage (for a pulse width \leq 20 ns)	-3.0V
DC Input Diode Current with V _{IN} < 0	-20 mA
DC Output Diode Current with V _{OUT} < 0	-50 mA
DC Output Current Max. Sink Current/Pin	120 mA
Maximum Power Dissipation	1.4 Watts (0 LFPM)
T _{STG} Storage Temperature.....	-65° to +150°C

Note: Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to this device resulting in functional or reliability type failures.

Table 4. Capacitance

T_A = 25°C, f = 1 MHz, V_{IN} = 0V, V_{OUT} = 0V

Pins	Typ	Unit
1, 11, 21, 31, 49, 59, 69, 79	4	pF
2-9, 12-19, 22-29, 32-39 41-48, 51-58, 61-68, 71-78	8	pF

Note: Capacitance is characterized but not production tested.

Table 5. DC Electrical Characteristics Over Operating Range

Commercial T_A = 0°C to 70°C, V_{CC} = 5.0V ± 5%

Symbol	Parameter	Test Conditions	Min	Typ ⁽¹⁾	Max	Unit
V _{IH}	Input HIGH Voltage	Logic HIGH for All Inputs	2.0	—	—	V
V _{IL}	Input LOW Voltage	Logic LOW for All Inputs	—	—	0.8	V
ΔV _T	Input Hysteresis	V _{TLH} – V _{THL} for All Inputs ⁽³⁾	—	0.2	—	V
I _{IIH} I _{IL}	Input Current Input HIGH or LOW	V _{CC} = Max., 0 ≤ V _{IN} < V _{CC}	—	—	5	μA
I _{OZ}	Off-State Output Current (Hi-Z)	V _{CC} = Max., 0 ≤ V _{IN} ≤ V _{CC}	—	—	5	μA
I _{OS}	Short Circuit Current QS74FCT4X245T	V _{CC} = Max., V _{OUT} = GND ^(2,3)	-60	—	—	mA
I _{OR}	Current Drive QS74FCT4X2245T (25Ω)	V _{CC} = Max., V _{OUT} = 2.0V	50	—	—	mA
V _{IC}	Input Clamp Voltage	V _{CC} = Min., I _{IN} = -18 mA ⁽³⁾	—	-0.7	-1.2	V
V _{OH}	Output HIGH Voltage	V _{CC} = Min., I _{OH} = -15 mA	2.4	—	—	V
V _{OL}	Output LOW Voltage QS74FCT4X245T	V _{CC} = Min., I _{OL} = 64 mA	—	—	0.55	V
V _{OL}	Output LOW Voltage QS74FCT4X2245T (25Ω)	V _{CC} = Min., I _{OL} = 12 mA	—	—	0.50	V
R _{OUT}	Output Resistance QS74FCT4X2245T (25Ω)	V _{CC} = Min., I _{OL} = 12 mA	20	28	40	Ω

Notes:

1. Typical values indicate V_{CC} = 5.0V and T_A = 25°C.
2. Not more than one output should be shorted and the duration is \leq 1 second.
3. These parameters are guaranteed by design but not production tested.

Table 6. Power Supply Characteristics

Symbol	Parameter	Test Conditions ⁽¹⁾	Typ	Max	Unit
I _{CC}	Quiescent Power Supply Current	V _{CC} = Max., Freq = 0 0V ≤ V _{IN} ≤ 0.2V or V _{CC} -0.2V ≤ V _{IN} ≤ V _{CC}	—	6.0	mA
ΔI _{CC}	Supply Current per Input @ TTL HIGH	V _{CC} = Max., V _{IN} = 3.4V, Freq = 0 ⁽²⁾	—	2.0	mA
Q _{CCD}	Supply Current per Output per MHz	V _{CC} = Max., Outputs Open and Enabled One Bit Toggling @ 50% Duty Cycle Other Inputs at GND or V _{CC} ^(3,4)	90	—	μA/MHz

Notes:

1. For conditions shown as Min. or Max., use the appropriate values specified under DC specifications.
2. Per TTL driven input (V_{IN} = 3.4V).
3. For flip-flops, Q_{CCD} is measured by switching one of the data input pins so that the output changes every clock cycle. This is a measurement of device power consumption only and does not include power to drive load capacitance or tester capacitance. This parameter is guaranteed by design but not production tested.
4. Total power supply current (I_C) can be computed using the above parameters as explained in *FCT-T Family Characteristics*.

Table 7. Switching Characteristics Over Operating RangeCommercial T_A = 0°C to 70°C, V_{CC} = 5.0V ± 5%C_{LOAD} = 50 pF, R_{LOAD} = 500Ω unless otherwise noted.

Symbol	Description ⁽¹⁾	4X245A/4X2245A		4X245C		Unit
		Min	Max	Min	Max	
t _{PHL}	Propagation Delay A _i to B _i	1.5	4.6	1.5	4.1	ns
t _{TPLH}						
t _{PZH}	Output Enable Time OE, T/R to A/B	1.5	6.2	1.5	5.8	ns
t _{TPZL}						
t _{PHZ}	Output Disable Time ⁽²⁾ OE, T/R to A/B	1.5	5.0	1.5	4.5	ns
t _{PLZ}						
t _{TSK0}	Rising Edge Skew ⁽²⁾	—	1.0	—	1.0	ns

Notes:

1. Minimums guaranteed but not production tested. See Test Circuit and Waveforms.
2. This parameter is guaranteed but not production tested.