# High Speed CMOS 32-Bit Register in MillipaQ™

**QS74FCT4X374ATQ3**
**QS74FCT4X374CTQ3**
**QS74FCT4X2374ATQ3**

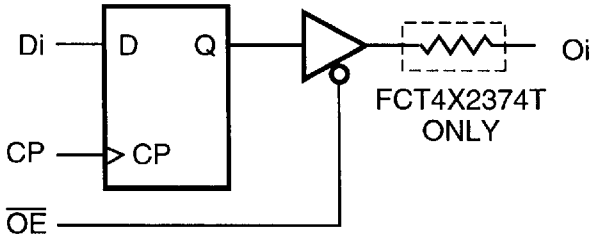
## FEATURES/BENEFITS

- 32-bit Function compatible to the 74F374 74ABT374, 74FCT374T and 74FCT2374T
- QS74FCT4X374T: $I_{OL}$ = 48 mA
- QS74FCT4X2374T: $I_{OL}$ = 12 mA
- Low CMOS power consumption
- Ground bounce controlled outputs
- A and C speed grades; 5.2 ns $t_{PD}$ for C
- Smallest footprint 32-bit logic solution
- 80-pin, 150-mil MillipaQ package (Q3)
- Easy layout flow-through pinout
- Tube or tape-and-reel shipment
- TTL-compatible input and output levels
- Undershoot clamp diodes on all inputs

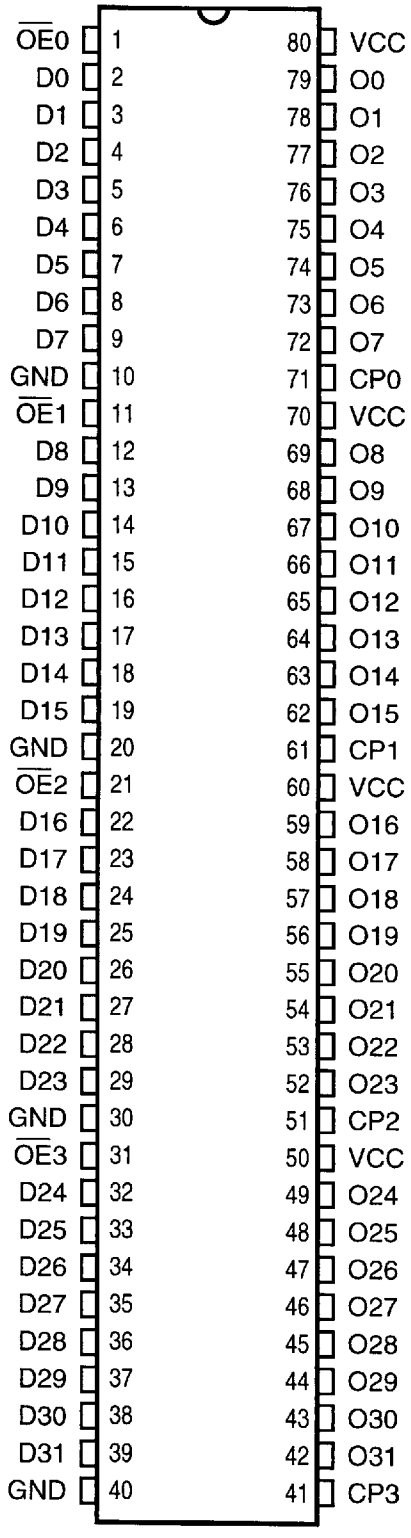
## DESCRIPTION

The FCT4X374T and FCT4X2374T are 32-bit registers with three-state outputs that are useful for bus-oriented applications. Output Enable ($\overline{OE}$) inputs enable the selected port for output. All inputs have clamp diodes for undershoot noise suppression. All outputs have ground bounce suppression (see QSI Application Note AN-01), and outputs will not load an active bus when Vcc is removed from the device. The MillipaQ 80-pin small outline package provides the smallest possible footprint while also offering an easy to layout flow-through, dual-in-line format.

## Figure 1. Functional Block Diagram



## Figure 2. Pin Configuration
(All pins top view)




## Table 1. Pin Description

| Name | I/O | Description |
|---|---|---|
| Di | I | Data Inputs |
| Oi | O | Data Outputs |
| CPi | I | Clock Inputs |
| $\overline{OE}$0 | I | Output Enable, O7-O0 |
| $\overline{OE}$1 | I | Output Enable, O15-O8 |
| $\overline{OE}$2 | I | Output Enable, O23-O16 |
| $\overline{OE}$3 | I | Output Enable, O31-O24 |

## Table 2. Function Table

| $\overline{OE}$n | CPn | Di | Internal Q Value | Outputs | Function |
|---|---|---|---|---|---|
| H | X | X | X | Hi-Z | Disable Outputs |
| L | ↑ | L | L | L | Load Input Data, Enable Outputs |
| L | ↑ | H | H | H | |
| H | ↑ | L | L | Hi-Z | Load Input Data, Disable Outputs |
| H | ↑ | H | H | Hi-Z | |

## Table 3. Absolute Maximum Ratings

| | |
|---|---|
| Supply Voltage to Ground | –0.5V to +7.0V |
| DC Output Voltage $V_{OUT}$ | –0.5V to +7.0V |
| DC Input Voltage $V_{IN}$ | –0.5V to +7.0V |
| AC Input Voltage (for a pulse width ≤ 20 ns) | –3.0V |
| DC Input Diode Current with $V_{IN} < 0$ | –20 mA |
| DC Output Diode Current with $V_{OUT} < 0$ | –50 mA |
| DC Output Current Max. Sink Current/Pin | 120 mA |
| Maximum Power Dissipation | 1.4 watts (0 LFPM) |
| $T_{STG}$ Storage Temperature | –65° to +150°C |

**Note:** Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to this device resulting in functional or reliability type failures.

## Table 4. Capacitance

$T_A$ = 25°C, f = 1 MHz, $V_{IN}$ = 0V, $V_{OUT}$ = 0V

| Pins | Typ | Unit |
|---|---|---|
| 1-9, 11-19, 21-29, 31-39, 41, 51, 61, 71 | 4 | pF |
| 42-49, 52-59, 62-69, 72-79 | 6 | pF |

**Note:** Capacitance is characterized but not production tested.

## Table 5. DC Elcetrical Characteristics Over Operating Range

Commercial $T_A$ = 0°C to 70°C, Vcc = 5.0V ± 5%

| Symbol | Parameter | Test Conditions | Min | Typ(1) | Max | Unit |
|---|---|---|---|---|---|---|
| $V_{IH}$ | Input HIGH Voltage | Logic HIGH for All Inputs | 2.0 | — | — | V |
| $V_{IL}$ | Input LOW Voltage | Logic LOW for All Inputs | — | — | 0.8 | V |
| $\Delta V_T$ | Input Hysteresis | $V_{TLH} - V_{THL}$ for All Inputs(3) | — | 0.2 | — | V |
| $\lvert I_{IH} \rvert$ $\lvert I_{IL} \rvert$ | Input Current Input HIGH or LOW | Vcc = Max., 0 ≤ $V_{IN}$ < Vcc | — | — | 5 | µA |
| $\lvert I_{OZ} \rvert$ | Off-State Output Current (Hi-Z) | Vcc = Max., 0 ≤ $V_{IN}$ ≤ Vcc | — | — | 5 | µA |
| $I_{OS}$ | Short Circuit Current QS74FCT4X374T | Vcc = Max., $V_{OUT}$ = GND(2,3) | –60 | — | — | mA |
| $I_{OR}$ | Current Drive QS74FCT4X2374T (25Ω) | Vcc = Max., $V_{OUT}$ = 2.0V | 50 | — | — | mA |
| $V_{IC}$ | Input Clamp Voltage | Vcc = Min., $I_{IN}$ = –18 mA(3) | — | –0.7 | –1.2 | V |
| $V_{OH}$ | Output HIGH Voltage | Vcc = Min., $I_{OH}$ = –15 mA | 2.4 | — | — | V |
| $V_{OL}$ | Output LOW Voltage QS74FCT4X374T | Vcc = Min., $I_{OL}$ = 48 mA | — | — | 0.50 | V |
| $V_{OL}$ | Output LOW Voltage QS74FCT4X2374T (25Ω) | Vcc = Min., $I_{OL}$ = 12 mA | — | — | 0.50 | V |
| $R_{OUT}$ | Output Resistance QS74FCT4X2374T (25Ω) | Vcc = Min., $I_{OL}$ = 12 mA | 20 | 28 | 40 | Ω |

**Notes:**
1. Typical values indicate Vcc = 5.0V and $T_A$ = 25°C.
2. Not more than one output should be shorted and the duration is ≤1 second.
3. These parameters are guaranteed by design but not production tested.

## Table 6. Power Supply Characteristics

| Symbol | Parameter | Test Conditions[1] | Typ | Max | Unit |
|---|---|---|---|---|---|
| $I_{CC}$ | Quiescent Power Supply Current | $V_{CC}$ = Max., Freq = 0<br>0V ≤ $V_{IN}$ ≤ 0.2V or $V_{CC}$-0.2V ≤ $V_{IN}$ ≤ $V_{CC}$ | — | 6.0 | mA |
| $\Delta I_{CC}$ | Supply Current per Input @ TTL HIGH | $V_{CC}$ = Max., $V_{IN}$ = 3.4V, Freq = 0[2] | — | 2.0 | mA |
| $Q_{CCD}$ | Supply Current per Output per MHz | $V_{CC}$ = Max., Outputs Open and Enabled<br>One Bit Toggling @ 50% Duty Cycle<br>Other Inputs at GND or $V_{CC}$[3,4] | 90 | — | µA/ MHz |

**Notes:**
1. For conditions shown as Min. or Max., use the appropriate values specified under DC specifications.
2. Per TTL driven input ($V_{IN}$ = 3.4V).
3. For flip-flops, $Q_{CCD}$ is measured by switching one of the data input pins so that the output changes every clock cycle. This is a measurement of device power consumption only and does not include power to drive load capacitance or tester capacitance. This parameter is guaranteed by design but not production tested.
4. Total power supply current (Ic) can be computed using the above parameters as explained in *FCT-T Family Characteristics.*

## Table 7. Switching Characteristics Over Operating Range

Commercial $T_A$ = 0°C to 70°C, $V_{CC}$ = 5.0V ± 5%
$C_{LOAD}$ = 50 pF, $R_{LOAD}$ = 500Ω unless otherwise noted.

| Symbol | Description | 4X374A/4X2374A Min | 4X374A/4X2374A Max | 4X374C Min | 4X374C Max | Unit |
|---|---|---|---|---|---|---|
| $t_{PHL}$<br>$t_{PLH}$ | Propagation Delay[1]<br>CP to Oi | 2.0 | 6.5 | 2.0 | 5.2 | ns |
| $t_{PZH}$<br>$t_{PZL}$ | Output Enable Time[1] | 1.5 | 6.5 | 1.5 | 5.5 | ns |
| $t_{PHZ}$<br>$t_{PLZ}$ | Output Disable Time[2] | 1.5 | 5.5 | 1.5 | 5.0 | ns |
| $t_S$ | Data Setup Time | 2.0 | — | 1.5 | — | ns |
| $t_H$ | Data Hold Time | 1.5 | — | 1.0 | — | ns |
| $t_W$ | Clock Pulse Width[2]<br>HIGH or LOW | 5.0 | — | 4.0 | — | ns |
| $t_{SKO}$ | Rising Edge Skew[2] | — | 1.0 | — | 1.0 | ns |

**Notes:**
1. Minimums guaranteed but not production tested. See Test Circuit and Waveforms.
2. This parameter is guaranteed but not production tested.