High-Speed 3.3V CMOS 8-Bit Transparent Latch with Output Resistor and Bus Hold

FEATURES/BENEFITS

- 5V tolerant inputs and outputs
- 25Ω series resistor for low switching noise
- Bus Hold feature holds last active state during 3-state operation
- 10µA I_{CCQ} quiescent power supply current
- Hot insertable
- 2.0V-3.6V V_{CC} supply operation
- ±12mA balanced output drive
- Power down high impedance inputs and outputs
- Meets or exceeds JEDEC 36 specifications
- C speed performance: t_{PD} = 5.4ns
- Input hysteresis for noise immunity
- Operating temperature range: –40°C to 85°C
- Latch-up performance exceeds 500mA
- Packages available:
  - 20-pin QSOP
  - 20-pin SOIC

DESCRIPTION

The LCX2H573 is an 8-bit buffered latch with three-state outputs that is ideal for driving high capacitance loads such as memory address and data buses. The QS74LCX2H573 with integrated output resistor is ideally suited for low noise environments where reduced output overshoot and undershoot are critical requirements. Bus Hold circuitry on the data inputs retains the last active state during 3-state operation, eliminating the need for external pull-up resistors. The 3.3V LCXPlus family features low power, low switching noise, and fast switching speeds for low power portable applications as well as high-end, advanced workstation applications. 5V tolerant inputs and outputs allow this LCXPlus product to be used in mixed 5V and 3.3V applications. To accomodate hot-plug or live insertion applications, this product is designed not to load an active bus when V_{CC} is removed.

Figure 1. Functional Block Diagram

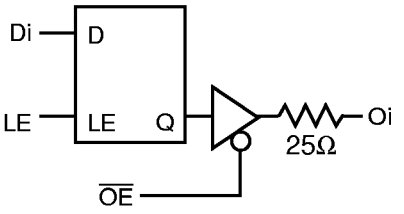

Figure 2. Pin Configurations
(All Pins Top View)

SOIC, QSOP

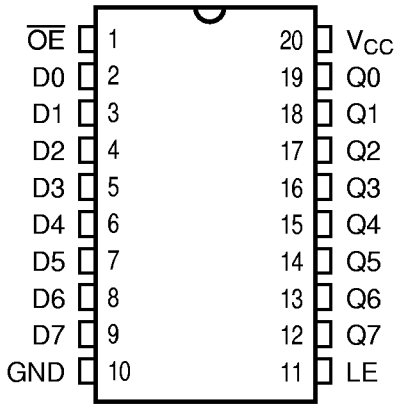

Table 1. Pin Description

Name	I/O	Description
Di	I	Data Inputs (Bus Hold Inputs)
Oi	O	Data Outputs
LE	I	Latch Enable
$\overline{OE}$	I	Output Enable

4

Table 2. Function Table

Inputs			Internal	Outputs	
$\overline{OE}$	LE	Di	Q Value	Oi	Function
H	X	X	X	Z	Disable Outputs
L	L	X	L	L	Enable Outputs
L	L	X	H	H	
X	H	L	L	L	Pass Input Data
X	H	H	H	H	
L	L	X	Q	Q	Hold Prior Data

Table 3. Capacitance

Symbol	Pins	Typ	Unit	Conditions
C_{IN}	Input Capacitance	7.0	pF	V_{IN} = 0V, V_{OUT} = 0V, f = 1MHz
$C_{I/O}$	I/O Capacitance	8.0	pF	V_{IN} = 0V, V_{OUT} = 0V, f = 1MHz
C_{PD}	Power Dissipation Capacitance	20	pF	V_{CC} = 3.3V, V_{IN} = 0V, or V_{CC} f = 10MHz

Note: Capacitance is characterized, but not production tested.

Table 4. Absolute Maximum Ratings

Supply Voltage to Ground ..... –0.5V to 7.0V
DC Output Voltage V_{OUT}
Outputs HIGH-Z ..... –0.5V to 7.0V
Outputs Active ..... –0.5V to V_{CC} + 0.5V
DC Input Voltage V_{IN} ..... –0.5V to 7.0V
DC Input Diode Current with V_{IN} < 0 ..... –50mA
DC Output Diode Current
V_O < 0 ..... –50mA
V_O > V_{CC} 50mA
DC Output Source/Sink Current (I_{OH}/I_{OL}) ..... ±50mA
DC Supply Current per Supply Pin ..... ±100mA
DC Ground Current per Ground Pin ..... ±100mA
T_{STG} Storage Temperature ..... –65° to 150°C

Note: Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to QSI devices that result in functional or reliability type failures.

Table 5. Recommended Operating Conditions

Symbol	Parameter		Min	Max	Unit
V_{CC}	Supply Voltage, Operating		2.0	3.6	V
	Suppply Voltage, Data Retention Only		1.5	3.6	
V_{IN}	Input Voltage		0	5.5	V
V_{OUT}	Output Voltage in Active State		0	V_{CC}	V
V_{OUT}	Output Voltage in "OFF" State		0	5.5	V
I_{OH}/I_{OL}	Output Current	V_{CC} = 3.0 – 3.6V	—	±12	mA
		V_{CC} = 2.7V	—	±6	
$\Delta t/\Delta v$	Input Transition Slew Rate		—	10	ns/V
T_A	Operating Free Air Temperature		–40	85	°C

Table 6. DC Electrical Characteristics Over Operating Range

Industrial Temperature Range, T_A = –40°C to 85°C.

Symbol	Parameter	Test Conditions[1]	Min	Typ[2]	Max	Unit
V_{IH}	Input HIGH Voltage	Logic HIGH for All Inputs	2.0	—	—	V
V_{IL}	Input LOW Voltage	Logic LOW for All Inputs	—	—	0.8	V
V_{OH}	Output HIGH Voltage	V_{CC} = 2.7V, I_{OH} = –100µA V_{CC} = 3.0V, I_{OH} = –12mA V_{CC} = 3.0V, I_{OH} = –18mA	V_{CC}– 0.2 2.4 2.2	— — —	— — —	V
V_{OL}	Output LOW Voltage	V_{CC} = 2.7V, I_{OL} = 100µA V_{CC} = 3.0V, I_{OL} = 12mA V_{CC} = 3.0V, I_{OL} = 18mA	— — —	— — —	0.2 0.55 0.8	V
R_{OUT}	Output Resistance	V_{CC} = 3.0V, I_{OL} = 12mA	—	28	—	Ω
ΔV_T	Input Hysteresis[3]	V_{TLH} – V_{THL} for All Inputs	—	150	—	mV
$\lvert I_{OZ} \rvert$	Off-State Output Current (Hi-Z)	V_{CC} = 3.6V, V_O = 0V, V_O = 5.5V	—	—	1.0	µA
I_{OS}	Short Circuit Current[3,4]	V_{CC} = 3.6V, V_{OUT} = GND	–60	—	–200	mA
I_{OR}	Current Drive[3]	V_{CC} = 3.6V, V_{OUT} = 2.0V	40	—	—	mA
V_{IK}	Input Clamp Voltage	V_{CC} = 2.7V, I_{IN} = –18mA	—	–0.7	–1.2	V
I_I	Input Leakage Current	V_I = 0V, V_I = 5.5V, V_{CC} = 3.6V	—	—	±1.0	µA
$\lvert I_{BH} \rvert$	Input Current Input HIGH or LOW Bus Hold Inputs[3,5]	V_{CC} = 3.6V, V_{IN} = 0V or V_{IN} = V_{CC}	—	—	50	µA
		V_{CC} = 3.6V, 0.8 < V_{IN} < 2.0V	—	—	500[6]	µA
I_{BHH}	Bus Hold Sustaining Current Bus Hold Inputs	V_{CC} = 3.0V, V_{IN} = 2.0V	–75	—	—	µA
I_{BHL}		V_{CC} = 3.0V, V_{IN} = 0.8V	75	—	—	µA
I_{OFF}	Power Off Leakage	V_{CC} = 0V, V_I or V_O = 5.5V	—	—	10	µA

Notes:
1. For conditions shown as Min. or Max. use appropriate value specified under Recommended Operating Conditions for the applicable device type.
2. Typical values are at V_{CC} = 3.3V and T_A = 25°C.
3. These parameters are guaranteed by characterization, but not production tested.
4. Not more than one output should be tested at one time. Duration of test should not exceed one second.
5. Pins with Bus Hold are identified in the Pin Description.
6. An external driver must provide at least $\lvert I_{BH} \rvert$ during transition to guarantee that the Bus Hold input will change state.

Table 7. Power Supply Characteristics

Symbol	Parameter	Test Conditions[1]		Typ[2]	Max	Unit
I_{CC}	Quiescent Power Supply Current	V_{CC} = 3.6V, Freq = 0 V_{IN} = GND or V_{CC}		0.1	10	µA
ΔI_{CC}	Supply Current per Input @ TTL HIGH[3]	V_{CC} = 3.6V V_{IN} = V_{CC}–0.6V, Freq = 0	Control Inputs	2.0	30	µA
			Bus Hold Inputs	—	500	µA
I_{CCD}	Supply Current per Input per MHz[4]	V_{CC} = 3.6V, Outputs Open One Bit Toggling @ 50% Duty Cycle $\overline{OE}$ = GND		50	75	µA/ MHz
I_C	Total Power Supply Current[6]	V_{CC} = 3.6V, Outputs Open One Bit Toggling @ 50% Duty Cycle $\overline{OE}$ = GND, f = 10MHz	V_{IN} = V_{CC}–0.6V V_{IN} = GND	0.5[5]	1.0[5]	mA
		V_{CC} = 3.6V, Outputs Open Eight Bits Toggling @ 50% Duty Cycle $\overline{OE}$ = GND, f = 2.5MHz	V_{IN} = V_{CC}–0.6V V_{IN} = GND	1.0[5]	3.5[5]	mA

Notes:
1. For conditions shown as Min. or Max., use the appropriate values specified under Recommended Operating Conditions for applicable device type.
2. Typical values are at V_{CC} = 3.3V, 25°C ambient.
3. Per TTL driven input. All other inputs at V_{CC} or GND.
4. This parameter is not directly testable, but is derived for use in total power supply calculations.
5. Values for these conditions are examples of the I_{CC} formula. These limits are guaranteed by design but not tested.
6. $I_C = I_{QUIESCENT} + I_{INPUTS} + I_{DYNAMIC}$.
   $I_C = I_{CCQ} + \Delta I_{CC} D_H N_T + I_{CCD} f N_O$.
   I_{CCQ} = Quiescent Current (I_{CCL}, I_{CCH}, and I_{CCZ}).
   ΔI_{CC} = Power Supply Current for a TTL-High Input (V_{IN} = V_{CC}-0.6V).
   D_H = Duty Cycle for TTL High Inputs.
   N_T = Number of TTL High Inputs.
   I_{CCD} = Dynamic Current Caused by an Input Transition Pair (HLH or LHL).
   f = Average Switching Frequency per Output.
   N_O = Number of Outputs Switching.

Table 8. Dynamic Switching Characteristics[1]

Symbol	Parameter	Conditions	V_{CC} (V)	T_A = 25°C Typical	Units
V_{OLP}	Quiet Output Dynamic Peak V_{OL}	C_L = 30pF, V_{IH} = 3.3V, V_{IL} = 0V	3.3	0.8	V
V_{OLV}	Quiet Output Dynamic Valley V_{OL}	C_L = 30pF, V_{IH} = 3.3V, V_{IL} = 0V	3.3	0.8	V

Note:
1. Characterized but not production tested.

Table 9. Switching Characteristics Over Operating Range

Industrial Temperature Range, T_A = –40°C to 85°C.
C_{LOAD} = 30pF, R_{LOAD} = 500Ω unless otherwise noted.

Symbol	Description[1]	2H573 V_{CC} = 3.3 ±0.3V Min	2H573 V_{CC} = 3.3 ±0.3V Max	2H573 V_{CC} = 2.7V[2] Min	2H573 V_{CC} = 2.7V[2] Max	2H573C V_{CC} = 3.3V ±0.3V Min	2H573C V_{CC} = 3.3V ±0.3V Max	Unit
t_{PHL} t_{PLH}	Propagation Delay Di to Oi	1.5	8.0	1.5	9.0	1.5	5.4	ns
t_{PHL} t_{PLH}	Propagation Delay LE to Oi	1.5	8.5	1.5	9.5	2.0	5.5	ns
t_{PZH} t_{PZL}	Output Enable Time $\overline{OE}$ to Oi	1.5	8.5	1.5	9.5	1.5	6.2	ns
t_{PHZ} t_{PLZ}	Output Disable Time $\overline{OE}$ to Oi [2]	1.5	6.5	1.5	7.0	1.5	6.0	ns
t_S	Data Setup Time Di to LE HIGH to LOW	2.5	—	2.5	—	2.0	—	ns
t_H	Data Hold Time Di to LE HIGH to LOW	1.5	—	1.5	—	1.5	—	ns
t_W	LE Pulse Width HIGH or LOW [2]	3.3	—	3.3	—	3.3	—	ns
$t_{SK(O)}$	Output Skew [3]	—	0.5	—	—	—	0.5	ns

Notes:
1. Minimums guaranteed but not production tested. See test circuit and waveforms.
2. Guaranteed by characterization.
3. Skew between any two outputs of the same package switching in the same direction. This parameter is guaranteed by characterization, but not production tested.

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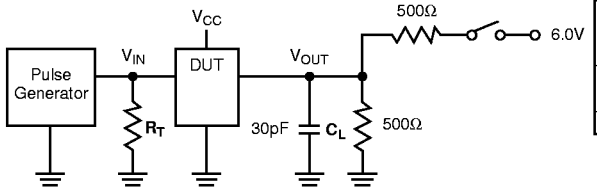
TEST CIRCUIT AND WAVEFORMS

Figure 3. Test Circuit



SWITCH POSITION

Test	Switch
Open Drain Disable LOW Enable LOW	6V
Disable HIGH Enable HIGH	GND
All Other Inputs	Open

DEFINITIONS:
C_L = Load capacitance: includes jig and probe capacitance.
R_T = Termination resistance: should be equal to Z_{OUT} of the Pulse Generator.

Figure 4. Setup, Hold, and Release Timing

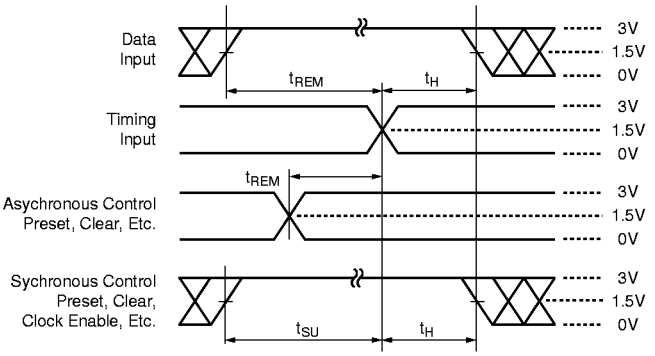


Figure 5. Enable and Disable Timing

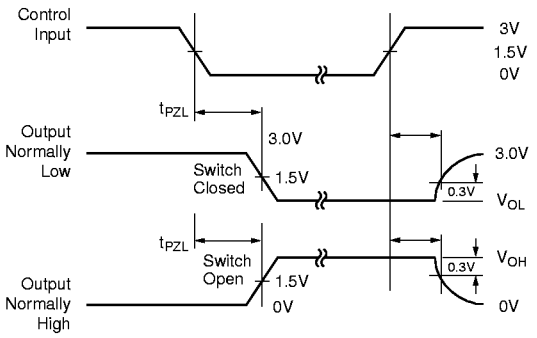


Figure 6. Pulse Width

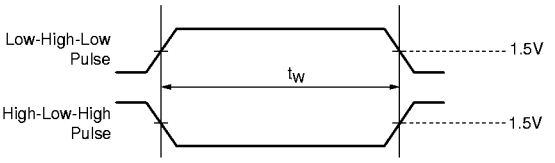
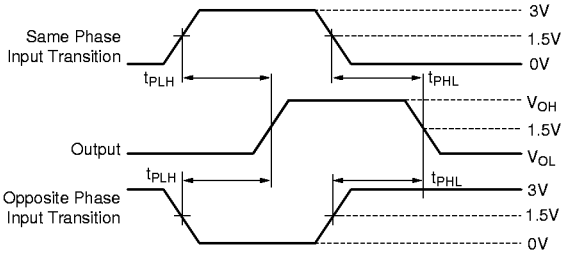


Figure 7. Propagation Delay

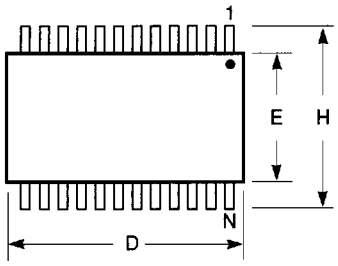


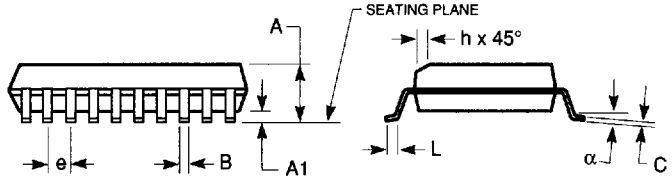
Notes:
1. Input Control Enable = LOW and Input Control Disable = HIGH.
2. Pulse Generator for All Pulses: Rate ≤ 1.0MHz; $Z_{OUT} \leq 50\Omega$; t_F, $t_R \leq 2.5$ns.

300-MIL SOIC - Package Code SO

Plastic Small Outline Gull-Wing

Notes:
1. Refer to applicable symbol list.
2. All dimensions are in inches.
3. N is the number of lead positions.
4. Dimensions D and E are to be measured at maximum material condition but do not include mold flash. Allowable mold flash is 0.006in. per side.
5. Lead coplanarity is 0.004in. maximum.

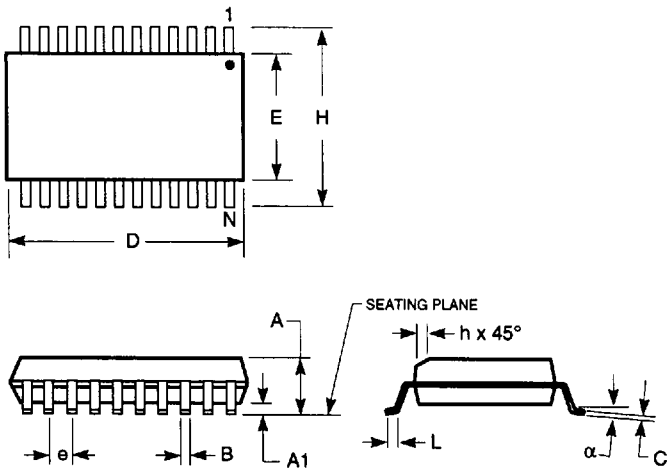




JEDEC#	MS-013AA		MS-013AC		MS-013AD		MS-013AE	
DWG#	PS16A		PS20A		PS24A		PS28A	
Symbol	Min	Max	Min	Max	Min	Max	Min	Max
A	0.096	0.104	0.096	0.104	0.096	0.104	0.096	0.104
A1	0.005	0.011	0.005	0.011	0.005	0.011	0.005	0.011
B	0.014	0.019	0.014	0.019	0.014	0.019	0.014	0.019
C	0.009	0.012	0.009	0.012	0.009	0.012	0.009	0.012
D	0.402	0.412	0.500	0.510	0.602	0.612	0.701	0.711
E	0.292	0.299	0.292	0.299	0.292	0.299	0.292	0.299
e	0.044	0.056	0.044	0.056	0.044	0.056	0.044	0.056
H	0.396	0.416	0.396	0.416	0.396	0.416	0.396	0.416
h	0.010	0.016	0.010	0.016	0.010	0.016	0.010	0.016
L	0.020	0.040	0.020	0.040	0.020	0.040	0.020	0.040
N	16		20		24		28	
α	0°	8°	0°	8°	0°	8°	0°	8°

150-MIL SOIC - Package Code S1

Plastic Small Outline Gull-Wing



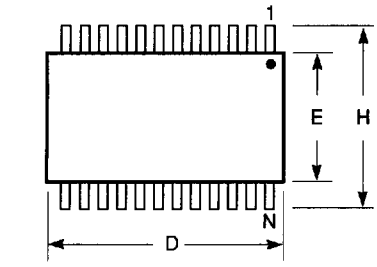
JEDEC#	MS-012AB			MS-012AC		
DWG#	PS-14B			PS-16B		
Symbol	Min	Nom	Max	Min	Nom	Max
A	0.060	0.064	0.068	0.060	0.064	0.068
A1	0.004	0.006	0.008	0.004	0.006	0.008
B	0.014	0.016	0.019	0.014	0.016	0.019
C	0.0075	0.008	0.0098	0.0075	0.008	0.0098
D	0.337	0.341	0.346	0.386	0.390	0.394
E	0.150	0.154	0.157	0.150	0.154	0.157
e	0.050 BSC			0.050 BSC		
H	0.230	0.236	0.244	0.230	0.236	0.244
h	0.010	0.013	0.016	0.010	0.013	0.016
L	0.016	0.025	0.035	0.016	0.025	0.035
N	14			16		
α	0°	5°	8°	0°	5°	8°

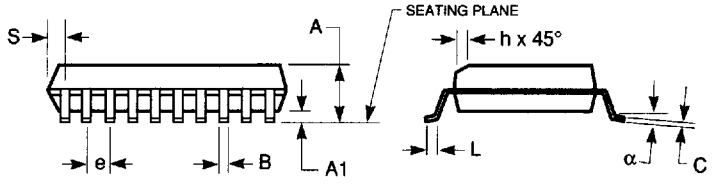
Notes:
1. Refer to applicable symbol list.
2. All dimensions are in inches.
3. N is the number of lead positions.
4. Dimensions D and E are to be measured at maximum material condition but do not include mold flash. Allowable mold flash is 0.006 in. per side.
5. Lead coplanarity is 0.004 in. maximum.

150-MIL QSOP - Package Code Q

Quarter-Size Outline Package
Plastic Small Outline Gull-Wing

Notes:
1. Refer to applicable symbol list.
2. All dimensions are in inches.
3. N is the number of lead positions.
4. Dimensions D and E are to be measured at maximum material condition but do not include mold flash. Allowable mold flash is 0.006in. per side.
5. Lead coplanarity is 0.004in. maximum.





JEDEC#	MO-137AB			MO-137AD			MO-137AE			MO-137AF		
DWG#	PSS-16A			PSS-20A			PSS-24A			PSS-28A		
Symbol	Min	Nom	Max	Min	Nom	Max	Min	Nom	Max	Min	Nom	Max
A	0.060	0.064	0.068	0.060	0.064	0.068	0.060	0.064	0.068	0.060	0.064	0.068
A1	0.004	0.006	0.008	0.004	0.006	0.008	0.004	0.006	0.008	0.004	0.006	0.008
B	0.009	0.010	0.012	0.009	0.010	0.012	0.009	0.010	0.012	0.009	0.010	0.012
C	0.007	0.008	0.010	0.007	0.008	0.010	0.007	0.008	0.010	0.007	0.008	0.010
D	0.189	0.193	0.197	0.337	0.341	0.344	0.337	0.341	0.344	0.386	0.390	0.394
E	0.150	0.154	0.157	0.150	0.154	0.157	0.150	0.154	0.157	0.150	0.154	0.157
e	0.025 BSC			0.025 BSC			0.025 BSC			0.025 BSC		
H	0.230	0.236	0.244	0.230	0.236	0.244	0.230	0.236	0.244	0.230	0.236	0.244
h	0.010	0.013	0.016	0.010	0.013	0.016	0.010	0.013	0.016	0.010	0.013	0.016
L	0.016	0.025	0.035	0.016	0.025	0.035	0.016	0.025	0.035	0.016	0.025	0.035
N	16			20			24			28		
α	0°	5°	8°	0°	5°	8°	0°	5°	8°	0°	5°	8°
S	0.006	0.009	0.010	0.056	0.058	0.060	0.031	0.033	0.035	0.031	0.033	0.035